Predictive Digital Current Programmed Control

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***Abstract*—This paper explores predictive digital current programmed control for valley, peak or average current. The control laws are derived for the three basic converters: buck, boost, and buck–boost. It is found that for each variable of interest (valley, peak or average current) there is a choice of the appropriate pulse-width modulation method to achieve predictive digital current control without oscillation problems. The proposed digital control techniques can be used in a range of power conversion applications, including rectifiers with power factor correction (PFC). Very low current distortion meeting strict avionics requirements (400–800 Hz line frequency) is experimentally demonstrated on a digitally controlled boost PFC employing predictive average current programmed control.**

***Index Terms*—Current-programmed control, digital control, switching power converters.**

I. Introduction

ANALOG current programmed control finds wide applications in dc–dc and power-factor-correction (PFC) applications [1]–[8]. Analog current programmed control can be classified as peak or valley current control, depending on whether the maximum or the minimum point of the sensed current is compared to a reference. The fact that the inductor current is tightly controlled results in simpler converter dynamics allowing simple and robust wide-bandwidth control in dc–dc applications. In addition, the peak current control offers fast over-current switch protection. In PFC applications, the peak or valley control results in some line current harmonic distortion, which can be reduced by biasing the current reference waveform [5], [6]. Another strategy is to operate the converter at the boundary of continuous and discontinuous conduction mode, such that the average inductor current follows one half of the peak current reference. However, the switching frequency is variable, and additional circuitry is needed to detect the zero crossing of the inductor current [7], [8]. Constant frequency operation and low harmonic distortion can be achieved using analog average current mode control [9].

Digital control offers potential advantages of lower sensitivity to parameter variations, programmability and possibilities to improve performance using more advanced control schemes. For example, it has been shown that digital control techniques can result in improved voltage loop dynamic responses in PFC systems [10]–[12]. Microprocessor and DSP based digital control is already widespread in motor control and high-power three-phase applications operating at relatively low switching frequencies. With recent advances in microprocessor/DSP technology, including increasing processing capabilities and decreasing cost, digital control becomes increasingly viable even for high-frequency low-to-medium power switching converters. The main purpose of this paper is to address algorithms and implementation of digital current mode control for high-frequency switching power converters.

In analog current mode control, the switch current or the inductor current is monitored continuously, and the switch control waveforms are generated by comparing a signal proportional to the sensed current to a reference. Given the fact that the switch (or the inductor) current is a fast-changing waveform, and that switching frequencies are in the hundreds of KHz to MHz range, a direct implementation of the analog current programmed control in digital hardware is not easy. The need for a very fast analog-to-digital (A/D) converter to produce multiple samples of the sensed current per switching period, and the corresponding need for large signal processing capabilities may require excessively complex hardware. Our objective is to investigate alternative digital current programmed control techniques that can match or exceed the performance of standard analog current programmed control while requiring relatively modest digital hardware resources for implementation.

As an example, Fig. 1 shows a completely digitally controlled low-harmonic rectifier (PFC) system employing an outer voltage and an inner current loop. A DSP system designed for motor drive or power conversion applications usually integrates analog/digital interfaces, PWM generators, and a processing unit. Sampling and processing result in a delay that can compromise control performance, especially in high-frequency applications. One way to improve the digital control performance is the predictive technique, which has been applied in three-phase systems [13], [14]. In one switching period, the duty cycle for the next switching cycle is calculated based on the sensed or observed state and input/output information, such that the error of the controlled variable is cancelled out or minimized in the next cycle or in the next several cycles. In addition to three-phase applications, predictive techniques have found applications in single-phase rectifiers and dc–dc converters. In particular, an approximate predictive technique using linear extrapolation has been proposed for a buck dc–dc converter in [15], and for a boost PFC application in [16]. In both cases, the predictive technique has only been applied to the control of the inductor valley current.

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In this paper, an accurate predictive digital control technique is proposed based on inductor current waveform predicted by sampled input and output voltage and inductor current information. In addition to the predictive valley control, we also consider realization of a predictive peak current and a predictive average current control technique in three basic converters, including the boost, the buck, and the buck–boost converters. The proposed digital control techniques can be used in a range of power conversion applications, including rectifiers with power factor correction and dc–dc applications with current mode control. It is found that the "period-doubling" oscillation issues, which are well known in analog current programmed control [1]–[4], also exist in digital predictive current controllers. We show how the oscillation problem can be eliminated by properly selecting the modulation method according to the control objective (valley, peak, or average current).

The paper is organized as follows. Predictive current control under the most commonly used trailing edge pulse-width modulation is first introduced for the boost converter in Section II, followed by an analysis of the oscillation problems in average and peak current control. The correlations between different pulse-width modulation methods and current control objectives are then identified in Section III. Robustness and design considerations are discussed in Section IV. Derivation of the predictive control law for other nonisolated converters is given in Section V. Finally, in Section VI, the predictive average current controller is implemented and experimentally verified in a boost PFC rectifier, and high performance is demonstrated under strict requirements for avionics applications.

II. Predictive Current Programmed Control Using Trailing Edge Modulation

In this section, three predictive current programmed control techniques are discussed: valley current control, peak current control, and average current control. The commonly used trailing-edge pulse-width modulation method illustrated in Fig. 2 is assumed. The pulsating switch control signal $g(t)$ is produced by comparing the control variable $v_c(t)$ with a trailing edge saw-tooth signal $v_{saw}(t)$. Under this modulation, the transistor switch is turned on at the beginning of each switching cycle, and turned off after time dT_S, where d is the switch duty ratio. The switch then stays off for the remainder of the switching cycle.

All three considered current control techniques are based on the same approach of using the sampled inductor current and (possibly) input and output voltages to compute the duty ratio in the next switching cycle so that the error between the current reference i_c and the target control variable (the valley, the peak, or the average current) is reduced to zero. The sampling of the current occurs at equally spaced intervals equal to the switching period T_s. Without loss of generality, we assume that the sample $i_s[n]$ is obtained by sampling the inductor current $i(t)$ at the beginning of the nth switching period.

In all derivations in this section, the boost converter is used as an example. The results and conclusions are extended to other basic converter configurations in Section V.

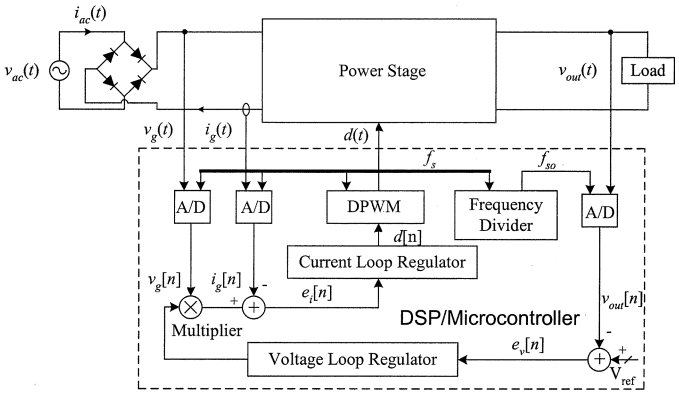

Fig. 1. Digitally controlled converter employing an outer voltage and an inner current loop.

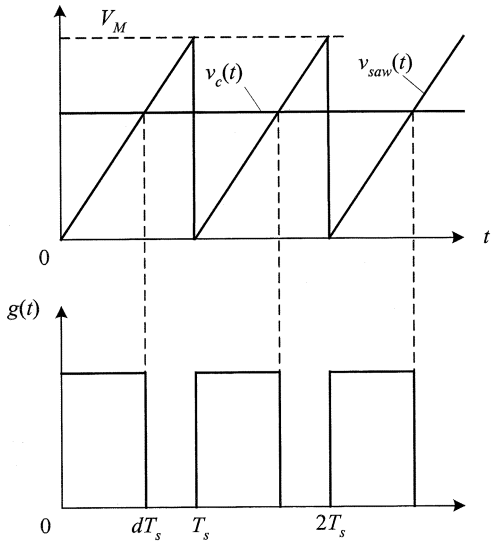

Fig. 2. Trailing edge modulation.

A. Predictive Valley Current Control

The goal of the proposed control method is to ensure that the valley inductor current follows the reference i_c. The required duty cycle for the next switching period is predicted based on the sampled current and possibly the input and the output voltage. The resulting inductor current waveform is shown in Fig. 3. Since the input and the output voltage are slowly varying signals, they can be considered constant during a switching period. The sampled inductor current $i(n)$ at time nT_s can be found as a function of the previous sampled value $i(n-1)$ and the applied duty ratio $d[n]$, provided that the input voltage, the output voltage, the inductance and the switching period are known

$$i(n) = i(n-1) + \frac{v_{in} d[n] T_s}{L} + \frac{(v_{in} - v_o) d'[n] T_s}{L}. \quad (1)$$

We use the notation $d' = 1 - d$. By collecting terms, (1) can be rewritten as

$$i(n) = i(n-1) + \frac{v_{in} T_s}{L} - \frac{v_o d'[n] T_s}{L}. \quad (2)$$

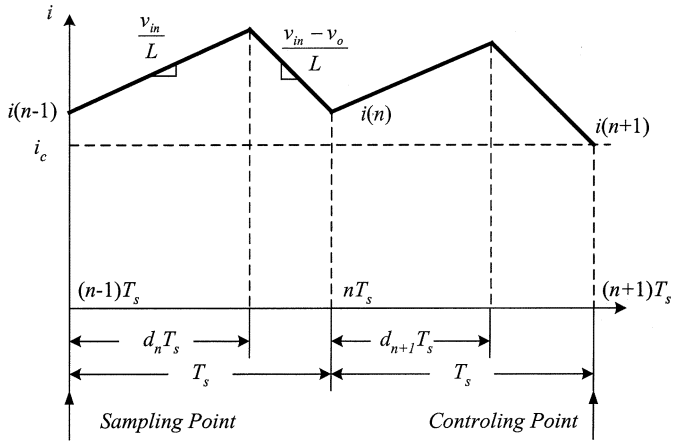

Fig. 3. Inductor current waveform in the boost converter under valley current control.

We can then extend (2) for another switching cycle to obtain

$$i(n+1) = i(n-1) + 2\frac{v_{in}T_s}{L} - \frac{v_o d'[n]T_s}{L} - \frac{v_o d'[n+1]T_s}{L}. \tag{3}$$

The prediction for the duty cycle $d[n+1]$ can now be obtained based on the values sampled in the previous switching period. Denoting the sampled current as $i_s[n]$, and substituting the control objective $i(n+1) = i_c$ in (3), we have

$$i_c = i_s[n] + 2\frac{v_{in}T_s}{L} - \frac{v_o d'[n]T_s}{L} - \frac{v_o d'[n+1]T_s}{L}. \tag{4}$$

Equation (4) can be solved for the predicted duty cycle

$$d[n+1] = 2 - d[n] - \frac{L}{v_o T_s}\left[i_s[n] - i_c\right] - 2\frac{v_{in}}{v_o}. \tag{5}$$

Equation (5) gives the basic control law for the predictive current programmed control.

Stability properties of the predictive valley current control under trailing edge modulation can be examined with reference to the waveforms of Fig. 4. The solid line shows the current waveform in steady state, while the dashed line shows the current with a perturbation Δi at the beginning of the switching period n. Since the effects of the predicted duty cycle $d[n+1]$ cannot be observed until the next switching period, this perturbation appears at the beginning of the $(n+1)$th cycle. With the next duty ratio $d[n+1]$ computed according to (5), the valley current reaches the reference i_c by the end of the $(n+1)$th switching period. The initially assumed perturbation disappears. As a result, for the predictive valley control under trailing edge modulation, the current controller is inherently stable for all operating points.

B. Predictive Peak Current Control

Peak current control, which among other advantages features instantaneous peak current protection, is the most popular current programmed control method in analog implementations for dc–dc applications. In this section, we examine properties of the predictive peak current control under trailing edge modulation.

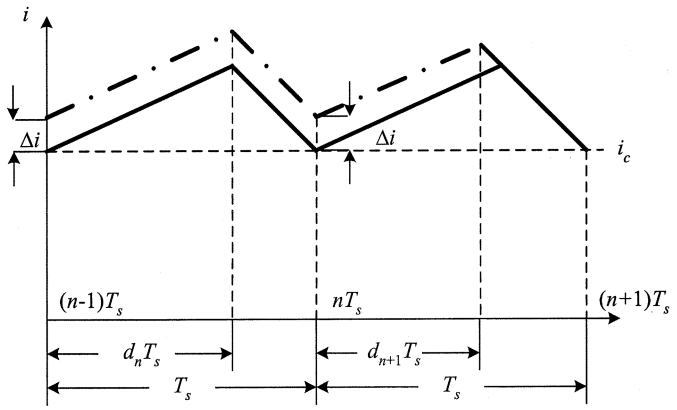

Fig. 4. Valley current control under trailing edge modulation.

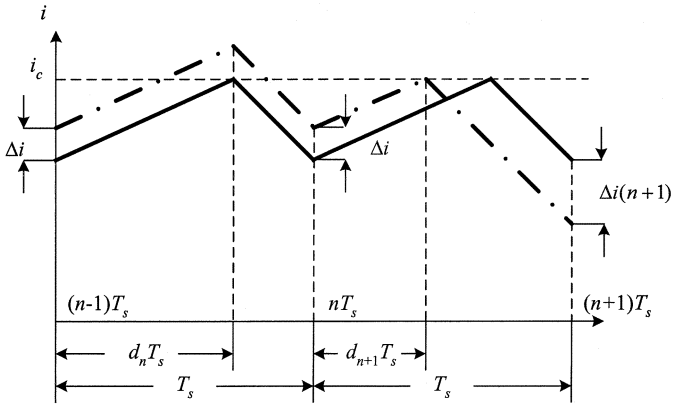

Fig. 5. Peak current control under trailing edge modulation.

Fig. 5 shows the inductor current waveforms where the solid line corresponds to the steady state operation, while the dashed line shows the current with a perturbation Δi at the beginning of the switching period n. In this case, the control objective is that the peak current follows the reference i_c. As shown in Fig. 5, the next duty ratio $d[n+1]$ is computed so that the peak current in the $(n+1)$th cycle equals the reference value i_c. Our objective is to find how the perturbation Δi propagates under this control law.

For the boost converter in continuous conduction mode (CCM), the steady-state duty cycle D and the steady-state peak current I_{peak} are given by

$$D = 1 - \frac{v_{in}}{V} \tag{6}$$

and

$$I_{peak} = I_0 + \frac{v_{in}DT_s}{L} \tag{7}$$

where I_0 is the steady-state valley current. As shown in Fig. 5, assume that the perturbation Δi in the inductor current has been detected by sampling the inductor current in the switching period n. Again, this perturbation will propagate to the beginning of the $(n+1)$th switching period. Taking into account this perturbation, the new duty cycle can be predicted using the following relationship:

$$i_{peak}[n+1] = i_c = I_0 + \Delta i + \frac{v_{in}d[n+1]T_s}{L}. \tag{8}$$

Using (6) and (7), the predicted duty cycle can be written as

$$d[n+1] = D - \frac{\Delta i L}{v_{in} T_s}. \tag{9}$$

Upon application of this duty cycle, the current at the end of the nth switching cycle becomes

$$\begin{aligned} i(n+1) &= I_0 + \Delta i + \frac{v_{in} T_s}{L} + \frac{V d[n+1] T_s}{L} - \frac{V T_s}{L} \\ &= I_0 + \Delta i - \Delta i \frac{V}{v_{in}} \\ &= I_0 - \frac{D}{1-D} \Delta i. \end{aligned} \tag{10}$$

Therefore, the current perturbation at the end of the $(n+1)$th period is given by

$$\Delta i(n+1) = i(n+1) - I_0 = -\frac{D}{1-D} \Delta i. \tag{11}$$

Equation (11) shows that oscillations occur under the operating conditions when the duty cycle is greater than 0.5. This is exactly the same as in analog current-programmed control, where the instability is usually suppressed by adding a slope-compensation ramp signal to the sensed current signal [2].

C. Predictive Average Current Control

In some applications, the average current control is preferred compared to valley or peak current control. In particular, in PFC applications, the analog average current control results in very low current distortion without the need for any additional compensation.

In predictive average current control, the new duty cycle is computed so that the average current $\langle i[n+1] \rangle$ in the next switching cycle equals the reference i_c. The average current in the $(n+1)$th switching cycle can be written in terms of the valley current and the applied duty cycle

$$\langle i[n+1] \rangle = i(n) + \frac{T_s v_{in}}{2L} - \frac{d'^2[n+1] T_s V}{2L}. \tag{12}$$

Based on (12), and assuming the steady-state and perturbed waveforms as shown in Fig. 6, the predicted duty cycle can be found from

$$i_c = I_0 + \Delta i + \frac{T_s v_{in}}{2L} - \frac{d'^2[n+1] T_s V}{2L}. \tag{13}$$

In steady state, we have

$$i_c = I_0 + \frac{T_s v_{in}}{2L} - \frac{D'^2 T_s V}{2L}. \tag{14}$$

Subtracting (14) from (13) yields

$$\Delta i = \left(d'^2[n+1] - D'^2 \right) \frac{T_s V}{2L}. \tag{15}$$

If we define $\Delta d = d'[n+1] - D'$, (15) can be simplified as

$$\Delta i = \left(\Delta d^2 + \Delta d \cdot 2D' \right) \frac{T_s V}{2L}. \tag{16}$$

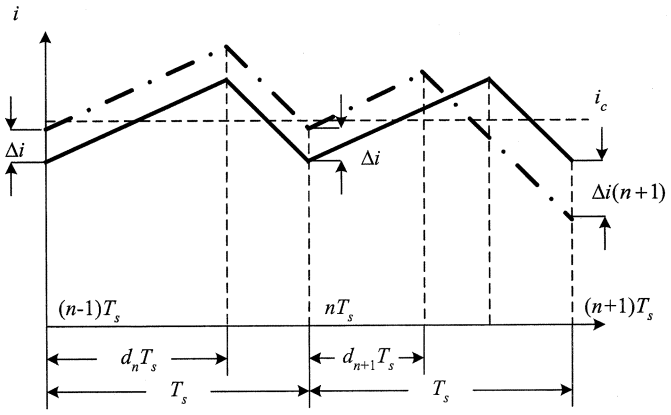

Fig. 6. Average current control under trailing edge modulation.

By neglecting the second order term, we obtain

$$\Delta i \approx \Delta d \cdot 2D' \frac{T_s V}{2L}. \tag{17}$$

Using (17), we can find the predicted duty cycle in terms of the perturbation and steady-state values

$$d'[n+1] = D' + \frac{\Delta i L}{D' T_s V}. \tag{18}$$

The inductor current at the end of the $(n+1)$th switching cycle is then found as

$$i(n+1) = I_0 + \Delta i - d'[n] \frac{V T_s}{L} = I_0 - \frac{D}{1-D} \Delta i. \tag{19}$$

Finally, the perturbed current at the end of the $(n+1)$th period is given by

$$\Delta i(n+1) = -\frac{D}{1-D} \Delta i. \tag{20}$$

We conclude that under trailing edge modulation the predictive average current control has the same instability problem under the operating conditions when the duty cycle is greater than 0.5.

III. Selection of the Modulation Method in Correlation With the Current Control Objective

In Section II, we found that under trailing edge modulation only the predictive valley current control can be achieved without "period-doubling" oscillations for all operating conditions. A distinction between the valley current control and the other two control objectives (peak or average current) is that in trailing edge modulation the targeted control variable (the valley current) can always be sampled at the beginning of the switching period, i.e., at *equally spaced intervals* equal to the switching period T_s. This is not the case for peak or average current control. For example, under trailing edge modulation, the peak current occurs at $d[n]T_s$, i.e., at variable time instants during a switching period. As a result, even though the controller may achieve the objective of forcing the peak current to follow the reference, a perturbation in the current waveform can grow in time, causing undesirable oscillations.

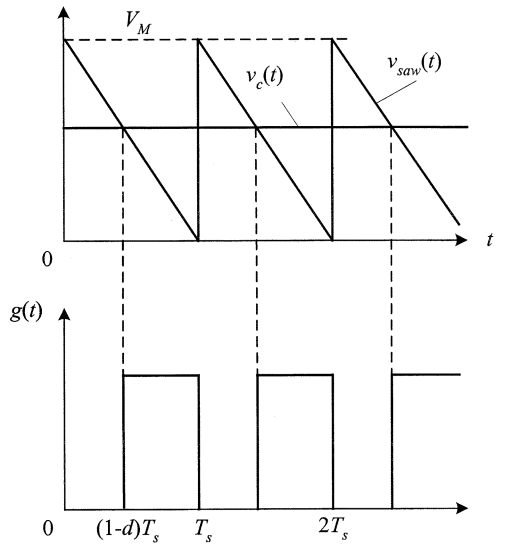

Fig. 7. Leading edge modulation.

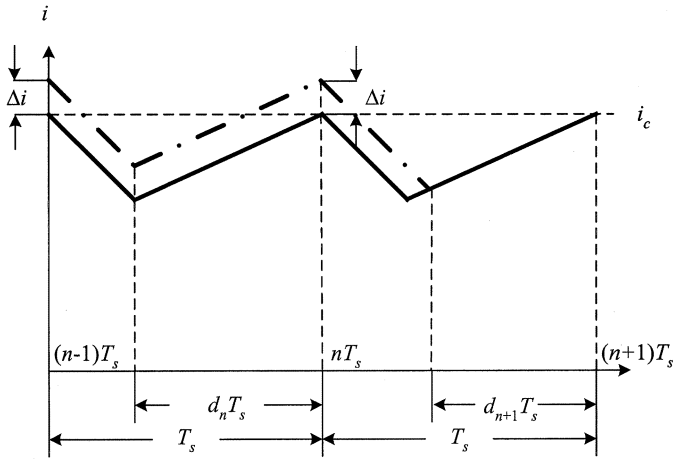

Fig. 8. Peak current control under leading edge modulation.

A key point in eliminating the stability problem is to enable sampling of the targeted variable of interest (valley, peak or average current) at equally spaced intervals equal to the switching period. In this section, we show how this can be accomplished by selecting the modulation method in correlation with the targeted control objective.

A. Predictive Peak Current Control Using Leading Edge Modulation

The leading edge modulation is illustrated by the waveforms of Fig. 7. The pulsating, switch control signal is generated by comparing the control variable with a leading saw-tooth signal. At the beginning of a switching period, the transistor switch is turned off, and then turned on at $(1-d)T_s$. The switch remains on until the end of the period. The peak current occurs at the beginning of each switching period, and can therefore be sampled at equally spaced intervals equal to T_s. Following the same steps as in Section II-A, one finds that the predictive peak current control under leading edge modulation follows the *same* law [given by (5)] as the valley current control under trailing edge modulation. The waveforms of Fig. 8 illustrate the point that a perturbation disappears within a switching period and therefore the predictive peak current control under leading edge modulation is inherently stable.

B. Predictive Average Current Control Using Dual Edge (Triangle) Modulation

The dual edge, or triangle modulation, is found to be suitable for achieving predictive average current control without oscillation problems. This modulation can be defined as trailing, illustrated by the waveforms of Fig. 9, or as leading, as shown in Fig. 10. In the case of the trailing triangle modulation, the transistor switch is on at the beginning of a switching cycle, it is turned off at $(d/2)T_s$ and then turned on again at $(1-d/2)T_s$. In the case of the leading triangle modulation, the transistor switch is off at the beginning of a switching cycle. Both triangle modulation methods are suitable for the predictive average current

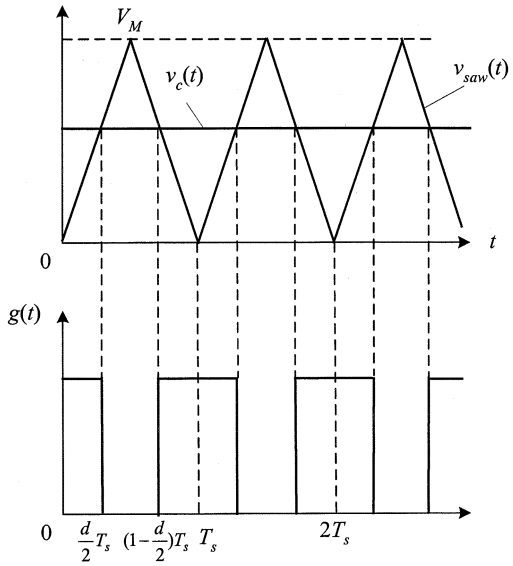

Fig. 9. Trailing triangle modulation.

control. We again find that the same control law given by (5) applies in this case. The inductor current waveform illustrating operation of the predictive average current control under trailing triangle modulation is shown in Fig. 11. This predictive average current control does not have oscillation problems.

C. Summary of Predictive Current Control and Modulation Methods

Table I summarizes the correlation between different modulation methods and the controlled variables of interest. It can be observed that for each variable of interest (valley, peak or average current) there is a choice of the appropriate modulation method to achieve predictive digital control without oscillation problems. Furthermore, the *same* predictive control law [given by (5)] applies to:

1) valley current control under trailing edge modulation;
2) peak current control under leading edge modulation;
3) average current control under triangle modulation.

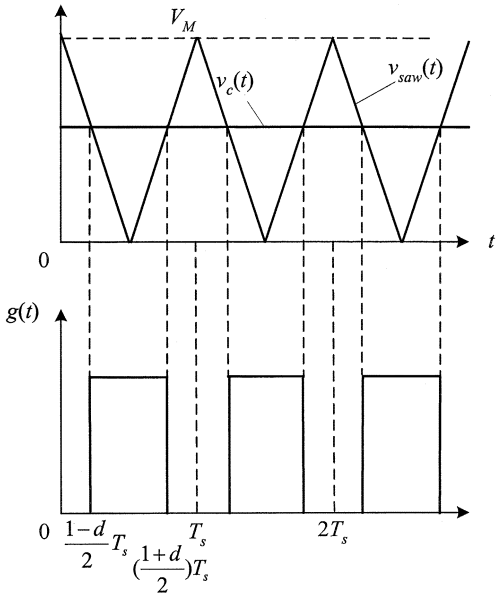

Fig. 10. Leading triangle modulation.

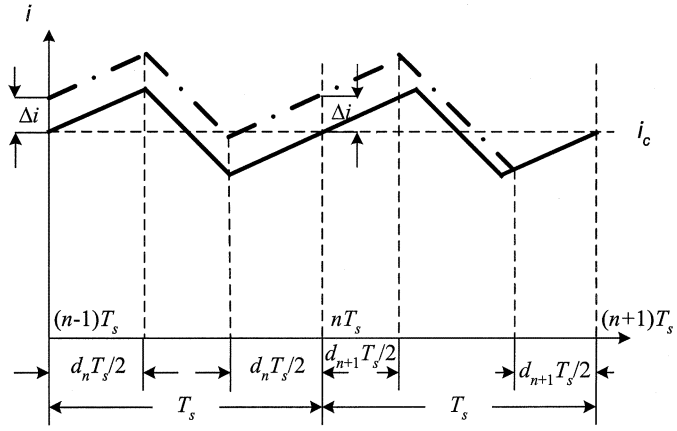

Fig. 11. Average current control under triangle modulation.

TABLE I
CORRELATION BETWEEN DIFFERENT PULSE-WIDTH MODULATION METHODS AND CURRENT CONTROL OBJECTIVES. "PERIOD-DOUBLING" OSCILLATIONS OCCUR FOR THE INDICATED RANGE OF DUTY RATIOS; * DENOTES NO OSCILLATION FOR THE WHOLE RANGE OF DUTY RATIO

	Valley	Peak	Average
Trailing	*	$D > 0.5$	$D > 0.5$
Leading	$D < 0.5$	*	$D < 0.5$
Trailing Triangle	*	$D > 0.5$	*
Leading Triangle	$D < 0.5$	*	*

IV. ROBUSTNESS AND DESIGN CONSIDERATIONS

It can be seen from the control law in (5) that the predictive control depends on the assumptions that the inductance, the switching period and the output voltage are known. In practice, the switching period T_s is usually determined by the DSP or microprocessor system's clock and its variations can be considered relatively insignificant. However, the value of the inductance may have significant initial tolerances and may further be affected by changes in temperature, operating conditions or aging. The output voltage value can be obtained by sampling, which is usually done for the purpose of closing a voltage feedback loop. However, the output voltage appears in the denominator, which complicates computation of the predicted duty cycle, especially in fixed-point DSP/microprocessor systems suitable for power control applications. In this section, we discuss how tolerances in the inductance (or period), and the approach of approximating the output voltage using a constant value affect the control performance.

Suppose that the converter is operating in steady state and that the controlled current has perturbation Δi at the beginning of the switching period n. Taking into account the difference ΔL between the real inductance value and the assumed value, the error $\Delta d[n+1]$ between the predicted duty cycle and the steady-state value can be found from (5)

$$\Delta d[n+1] = -\frac{\Delta L}{VT_s}\Delta i. \tag{21}$$

This error in the predicted duty cycle causes the error $\Delta i(n+1)$ of the current value at the end of the $(n+1)$th switching period

$$\Delta i(n+1) = \frac{\Delta L}{L}\Delta i. \tag{22}$$

As shown by (22), the error decreases and the control performance is not significantly affected by the inductance tolerances as long as $\Delta L < L$, which is not difficult to meet. A similar result is obtained for tolerances in the switching period.

Instead of using the real-time sampled output voltage value, we consider approximating the output voltage with the constant reference value V to avoid the division and to simplify the control law. Suppose that there is an error ΔV between the actual output voltage and the reference. From (5), the resulting error $\Delta d[n+1]$ in the duty cycle is given by

$$\Delta d[n+1] = -\frac{\Delta VL}{V^2T_s}\Delta i - \frac{2v_{in}\Delta V}{V^2}. \tag{23}$$

As a result, the controlled current will have an error $\Delta i(n+1)$ at the end of the next switching period

$$\Delta i(n+1) = \frac{\Delta V}{V}\Delta i + \frac{\Delta V}{V}\frac{2V_{in}T_s}{L}. \tag{24}$$

Equation (24) has two portions. The first term of the current error is due to the current perturbation, and will get smaller provided that the output voltage error satisfies $\Delta V < V$. The second term is introduced by the voltage error and will have an effect of settling the inductor current in a new steady state with an offset ΔI away from the reference. The offset error ΔI can be obtained from (24) by setting $\Delta I = \Delta i(n+1) = \Delta i$

$$\Delta I = \frac{\Delta V}{V - \Delta V}\frac{2V_{in}T_s}{L}. \tag{25}$$

For a power converter with well-regulated output voltage, $\Delta V/V$ is very small and in most cases the offset error can be ignored. We conclude that it is reasonable to use the (constant) output voltage reference instead of the sampled output voltage to simplify the computation in the predictive current controller.

V. Extensions of the Predictive Digital Current Programmed Control to Other Converters

Basic principles of predictive programmed control can be easily extended to other basic converters, i.e., the buck converter and the buck–boost converter. Fig. 12 shows the generic CCM inductor current waveform for switching converters under the trailing edge modulation. In the subinterval when the transistor is on, the inductor current increases with a slope m_1, and then decreases with a slope $-m_2$ during the subinterval when the transistor is off. For the basic nonisolated converters, the slopes are given in Table II.

The predictive control law can be expressed as a function of the slopes m_1, m_2, the switching period, and the duty ratio in the previous cycle as

$$d[n+1] = -d[n] - \frac{1}{(m_1+m_2)T_s}\left[i_s[n] - i_c\right] + 2\frac{m_2}{m_1+m_2}. \tag{26}$$

By using the expressions for m_1 and m_2 from Table II, we obtain the predictive control law for the buck converter

$$d[n+1] = -d[n] - \frac{L}{v_{in}T_s}\left[i_s[n] - i_c\right] + 2\frac{v_o}{v_{in}} \tag{27}$$

and for the buck–boost converter

$$d[n+1] = -d[n] - \frac{L}{(v_{in}+v_o)T_s}\left[i_s[n] - i_c\right] + 2\frac{v_o}{v_o+v_{in}}. \tag{28}$$

The stability condition similar to (11) and (20) can be written more generally as

$$\Delta i(n+1) = -\frac{M_1}{M_2}\Delta i. \tag{29}$$

The condition (29) is valid for all basic converters.

In steady-state, the inductor volt-second balance implies

$$DM_1 - (1-D)M_2 = 0 \tag{30}$$

or

$$\frac{M_1}{M_2} = \frac{D}{1-D}. \tag{31}$$

Equations (30) and (31) show that the stability condition under certain modulation method is the same for all basic nonisolated converters in continuous conduction mode. Moreover, the correlation between the modulation method and the current control objective, and the robustness conditions, which were discussed in Sections III and IV for the boost converter, apply to all basic nonisolated converters.

VI. Experimental Results

To demonstrate performance of the predictive current control, a 100 W single-phase experimental PFC boost converter (as shown in Fig. 1) was designed and tested for avionics applications, which have more demanding specifications, including the line input frequency of 400 to 800 Hz, and low total harmonic distortion (THD) of less than 10% [17], [18]. The predictive current control and the output voltage regulation are realized using

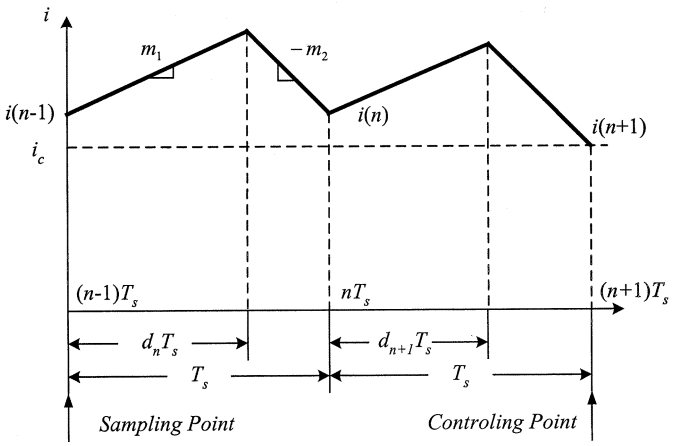

Fig. 12. Generic inductor current waveform under valley current control.

TABLE II
Slope of the Inductor Current Waveform in Basic Converters

Buck converter	$m_1 = \frac{v_{in}-v_o}{L}$	$-m_2 = -\frac{v_o}{L}$
Boost converter	$m_1 = \frac{v_{in}}{L}$	$-m_2 = \frac{v_{in}-v_o}{L}$
Buck-boost converter	$m_1 = \frac{v_{in}}{L}$	$-m_2 = \frac{v_o}{L}$

the Analog Devices ADMC-401 DSP system [19], which has built-in digital PWM, A/D converters, and a 16-bit fixed-point computational unit. The input inductance is 1 mH, the output capacitance is 47 μF, and the output dc voltage is regulated at 190 V.

The two-loop system as shown in Fig. 1 was implemented. The input current and the input voltage are sampled at the switching frequency (100 KHz or 200 KHz) to ensure the high performance of the current loop based on the predictive average current control under triangle modulation. The output voltage loop uses a slow PI regulator that provides a voltage-loop bandwidth of about one third of the line input frequency [20]. The output voltage is sampled at a frequency of 4 KHz, which is sufficient to implement functions of the slow output voltage loop while at the same time being relatively easy to realize using fixed-point arithmetic.

Figs. 13 and 14 show the rectified input voltage (115 Vrms) and the input current waveforms at the switching frequency of 200 KHz and 100 KHz, respectively. This comparison shows that the performance of the current control loop doesn't rely heavily on very high switching frequency. THD of less than 2.5% is achieved under all conditions, even when the input line frequency is 800 Hz with a switching frequency of 100 KHz.

VII. Conclusion

This paper describes predictive digital current programmed control methods. In each switching cycle, based on the sampled value of the current, the duty ratio in the previous cycle, and (possibly) the samples of the input and/or the output voltage, the switch duty ratio in the next switching cycle is computed to

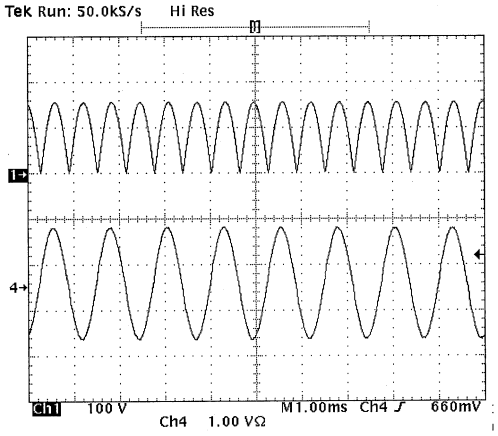

Fig. 13. Rectified input voltage (top, 100 V/div), and the input current (bottom, 1 A/div) at 200 KHz switching frequency, 800 Hz line frequency, THD is 2.2%.

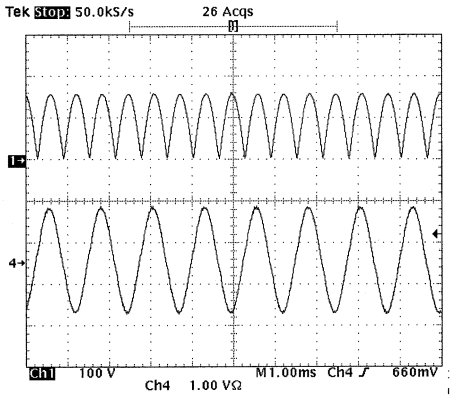

Fig. 14. Rectified input voltage (top, 100 V/div), and the input current (bottom, 1 A/div) at 100 KHz switching frequency, 800 Hz line frequency, THD is 2.4%.

null the error between the actual current and the reference. The implementation requires only one current sample per period and has relatively modest processing requirements.

The predictive digital current programmed control law is derived for all basic converter configurations and for three different control variables of interests: valley, peak or average current. It is found that for each variable of interest (valley, peak or average current) there is a choice of the appropriate modulation method to achieve predictive digital current control without "period-doubling" oscillation problems. It is also shown that the predictive control law is the same for the control technique where the oscillation problem is eliminated:

1) valley current control under trailing edge modulation;
2) peak current control under leading edge modulation;
3) average current control under dual-edge (triangle) modulation.

The proposed digital control techniques can be used in a range of power conversion applications, including dc–dc converters and rectifiers with power factor correction (PFC). A prototype of a 100 W PFC boost rectifier switching at 100 KHz or 200 KHz has been constructed using a DSP system to implement the predictive average current control and a PI voltage loop control. Very low THD ($<2.5\%$) of the input current and high performance that meets rigorous avionics requirements (400–800 Hz line frequency) have been experimentally demonstrated.

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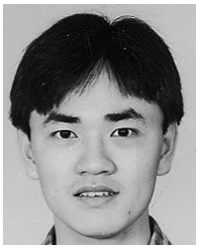

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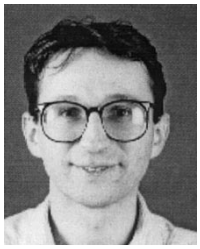

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