

## Research Article

# Presenting of the Magnetic Coupling-Based Transformer-Less High Step-Up DC-DC Converter for Renewable Energy Applications

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This study presents a new high step-up converter based on the voltage multiplier cell and coupled inductor for renewable energy applications such as fuel cell and photovoltaic power systems. This converter achieves a high voltage conversion ratio using a coupled inductor and voltage multiplier cell (VMC). The voltage multiplier cell acts as a passive clamp circuit and reduces the maximum voltage across the power switch. The suggested topology has only one power switch in its structure, which leads to low cost and volume. The other benefits of the proposed structure are low components count, low input current ripple, low voltage stress throughout the semiconductors, high efficiency, zero-current switching (ZCS), and zero-voltage switching (ZVS) of diodes. Besides, due to the soft-switching condition of the diodes, the reverse recovery problem can be decreased. To show the effectiveness of the suggested topology, operation survey, steady-state analysis, and efficiency calculation are provided. Additionally, the comparison study with other similar converters illustrates the superiority of the proposed structure. Finally, an experimental prototype with 150 W rated power, 50 kHz switching frequency, and 24 V input voltage is implemented to prove the mathematical analysis and effectiveness of the proposed DC-DC converter.

## 1. Introduction

Recently, photovoltaic (PV) energy applications for DC supplies are rapidly increased. Also, green energy technologies are noticeably developed due to the carbon emissions problems and need to decrease pollution [1, 2]. This matter has encouraged power engineering researchers, organizations, and governments to expand renewable energy studies [3, 4].

DC-DC power converters could be increased the voltage level to satisfy the load or transmission line requirements' needs [5]. Due to these matters, the expansion of high voltage gain converters has emerged as one of the most influential and notable clarifications for utilizing renewable energy [6]. Various kinds of DC-DC converters were represented to obtain high voltage conversion ratios. Usually,

the high step-up DC-DC structures can be categorized into two groups as follows: isolated or nonisolated category for DC-microgrid applications [7, 8]. A high voltage conversion ratio can be achieved by a classical boost, a switched-capacitor, a cascaded boost, and switched-inductor topologies. Due to diode reverse recovery currents problems, these converters have some restrictions, which reduce the converter efficiency [6, 9]. The classical boost DC-DC converter is a low-cost solution for voltage boosting. However, in this converter, the voltage stresses of the power switches and diode are equal to the output voltage. Also, a large duty cycle is needed for higher voltage gain, which enhances the power switch conduction loss and reduces efficiency [10, 11]. Furthermore, electromagnetic interface (EMI) concerns limit voltage boosting because of the high duty cycle levels. On the other hand, at high step-up voltage ratios, the

associated current stress may be produced a failure and deteriorate element lifetime [12, 13]. These drawbacks can be overcome using the other types of traditional DC-DC converters such as push-pull, forward, and fly-back converters by regulating the transformer's turn ratio. Nonetheless, a high peak voltage was produced across the power switches by the transformer leakage inductance's energy [14, 15]. Additionally, a high number of turn ratio raises the transformer losses, cost, and size, which leads to system efficiency reduction. As discussed beforehand, isolated power converters can attain a high voltage gain by regulating the coupled inductor's turn ratio. Besides, there are infrequent obstacles when a large number of the turn ratio is adjusted for the transformer as follows: (1) high parasitic capacitors of the transformer's secondary winding, (2) parasitic circuit effects such as spikes, (3) increased component heating losses, (4) high leakage inductance, (5) noise production by windings, (6) large required input filters, and (6) cost enhancement.

In references [16, 17], isolated converters were reported with a high voltage gain. However, due to the isolated topology, the cost and volume of these converters are high. The above-mentioned obstacles can be reduced by using nonisolated DC-DC structures. These structures present numerous benefits, such as low cost and volume. The suggested nonisolated converter in reference [18] was suitable for microgrid inverters. Nevertheless, the high input current ripple of this structure can reduce the input PV panel lifetime. In reference [19], a high step-up DC-DC topology was represented based on the voltage multiplier cell (VMC) and a coupled inductor. This converter had high input current ripple. Moreover, the number of used components was high, which leads to low efficiency. In references [20–25], DC-DC converters with high step-up advantage were reported. However, significant problems such as high voltage stress throughout the semiconductor components, diodes reverse recovery problem, high input current ripple, high components count, and low power efficiency still exist in these converters. In reference [26], a steady-state survey of DC-DC structure based on the switched capacitor and magnetic coupling has been introduced. The mentioned converter in reference [26] can achieve high voltage gain by increasing the turn ratio of the coupled inductor. In reference [27], a high step-up DC-DC converter with a single switch has been introduced. The suggested converter can achieve higher and lower voltage gains at different rates of duty cycle. The converter has been experimented under real-time conditions with a 660 W system. However, the voltage stress through the semiconductor of the proposed converter is high, which leads to an increase in the overall system cost. A high voltage rate DC-DC converter with LC network and voltage double circuit has been reported in reference [28]. The presented converter advantages are high voltage gain, low voltage stress across the switches, and high efficiency. However, the input ripple of the proposed converter is high and also it cannot be used for high power applications. Reference [29] introduced a high step-up interleaved DC-DC structure with a wide voltage conversion ratio. The suggested

converter utilized a large number of components to achieve high output voltage. Therefore, the efficiency of the converter is low, and also the overall system cost is high. In reference [30], a soft-switched DC-DC converter was represented with high efficiency. Also, the peak voltage of the semiconductor devices is low.

This study presents a new kind of nonisolated DC-DC converter based on the coupled inductor and VMC for renewable energy applications such as PV power systems. This converter can attain a high voltage conversion ratio using the coupled inductor turns ratio adjustment and used VMC. The suggested nonisolated converter has only one power MOSFET in its structure, which leads to low cost and volume. The other advantages of the proposed topology are as follows: (1) low components count, (2) high efficiency, (3) low input current ripple, and (4) low voltage stress across the semiconductors. The applied VMC acts as a passive clamp circuit and reduces the maximum peak voltage throughout the power switch. Besides, due to the ZVS and ZCS of diodes, the converter's efficiency is high. Operation survey, steady-state analysis, and efficiency calculation are presented in the literature. Moreover, to show the superiority of the suggested structure, the comparison results with other converters in the same family are reported. Finally, a laboratory prototype with 24/180 V input/output voltage at 50 kHz switching frequency is provided to verify the effectiveness and mathematical analysis of the proposed structure.

## 2. Suggested Nonisolated DC-DC Converter and Operation Modes Analysis

The configuration of the suggested converter is shown in Figure 1. The proposed converter includes an input voltage source ( $V_{in}$ ), three diodes ( $D_1$ ,  $D_2$ , and output diode ( $D_o$ )), a coupled inductor with a winding ratio of  $n_1$  (primary winding) and  $n_2$  (secondary winding), one power switch ( $S$ ), and four capacitors ( $C_1$ ,  $C_2$ ,  $C_3$ , and the output filter capacitor ( $C_o$ )). The VMC consists of diodes  $D_1$  and  $D_2$  and capacitors  $C_1$  and  $C_3$ . The coupled inductor is assumed as an ideal transformer, with a turn ratio  $N = (n_1/n_2)$ , magnetizing ( $L_m$ ), and leakage ( $L_k$ ) inductance. The stored energy in  $L_k$  is recycled and transferred to the output capacitor ( $C_o$ ). In addition, capacitor  $C_2$  and diode  $D_1$  act as a snubber circuit, decreasing the maximum voltage stress throughout the switch  $S$ . Thus, a low-cost switch with low on-state resistance ( $R_{DS-ON}$ ) can be used in the suggested topology.

The following assumptions are taken into account for modes analysis and steady-state investigation:

- (i) All semiconductor elements are ideal
- (ii) The voltage ripple of the capacitors is neglected
- (iii)  $L_k$  of the used coupled inductor is neglected

There are three operation modes in each switching period ( $T_s$ ), in which two modes are occurred in on-state and three modes in off-state of switch  $S$ . The main time waveforms of the recommended topology during one  $T_s$  are depicted in Figure 2.

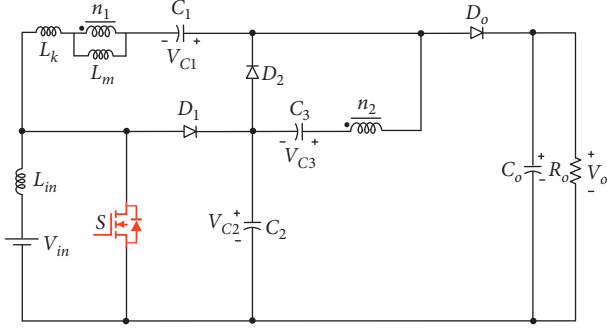


FIGURE 1: Configuration of the suggested high step-up converter.

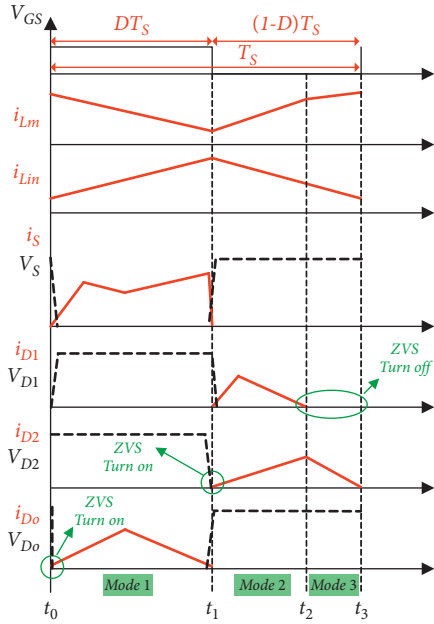


FIGURE 2: Time waveforms of the recommended topology in CCM operation.

**Mode 1.**  $[t_0 < t < t_1]$ : this mode is beginning when the pulse gate is applied to power switch  $S$ . At  $t = t_0$ , the power switch  $S$  is turned on. Also, the diode  $D_o$  is turned on at ZVS condition. Diode  $D_o$  is the only diode that is forward biased in this mode and the other diodes are turned off. The input inductor  $L_{in}$  is charged with the input DC source. Therefore, the input inductor current  $i_{Lin}$  is linearly increased. The energy of the capacitors  $C_2$  and  $C_3$  and the energy of the secondary side of the coupled inductor are delivered to the load through diode  $D_o$ . In this mode, the capacitor  $C_1$  is charged and the capacitors  $C_2$  and  $C$  are discharged. The equivalent configuration of mode 1 is illustrated in Figure 3(a). The following equations are described for this mode:

$$V_{L_{in}} = V_{in}, \quad (1)$$

$$V_{L_m} = \frac{V_{C_1} - V_{C_2} - V_{C_3}}{1 - N}, \quad (2)$$

$$V_o = V_{C_2} + V_{C_3} - NV_{L_m}, \quad (3)$$

$$i_S = i_{in} + i_{C_1}, \quad (4)$$

$$i_{C_3} = i_{C_2} = -i_{n_2}, \quad (5)$$

$$i_{D_o} = i_{C_3} - i_{C_1} = i_{C_o} - i_o, \quad (6)$$

$$i_{C_2} = i_{C_3} = i_{C_1} + i_{D_o}. \quad (7)$$

**Mode 2.**  $[t_1 < t < t_2]$ : at  $t = t_1$ , the power switch  $S$  is turned off. Besides, the diodes  $D_1$  and  $D_2$  are turned on. In this operation time, the diode  $D_2$  is started to conduct at ZVS. The blocking voltage of the switch  $S$  is  $V_{C_2}$ . The equivalent configuration of this mode is shown in Figure 3(b). The stored energy in the input inductor  $L_{in}$  is transferred to the capacitors  $C_2$ . Also, the capacitor  $C_3$  is charged by the energy of the coupled inductor's secondary side. The equations of mode 2 are calculated as follows:

$$V_{L_{in}} = V_{in} - V_{C_2},$$

$$V_{L_m} = V_{C_1} - V_{L_k} = \frac{1}{N}V_{C_3}, \quad (8)$$

$$i_{D_1} = i_{in} - i_{L_k}.$$

**Mode 3.**  $[t_2 < t < t_3]$ : at  $t = t_2$ , the diode  $D_2$  is still in forward bias. Power switch  $S$  and  $D_o$  are in off-state. The stored energy in  $L_{in}$  charges the coupled inductor's magnetizing inductor  $L_m$ . Therefore,  $i_{L_m}$  is linearly raised. Also,  $C_2$  is charged during this mode. The equivalent circuit of this mode is the same as Figure 3(c). For this mode, we have the following equation:

$$-V_{in} + V_{L_m} + V_{L_k} + V_{L_m} - V_{C_1} + V_{C_2} = 0. \quad (9)$$

### 3. Steady-State Analysis

The proposed converter's voltage gain ( $V_o/V_{in}$ ) and the voltage stress across the used semiconductors can be calculated by neglecting the power losses and the coupled inductor's leakage inductance  $L_k$ . Therefore, only the ideal value of the used components is considered for the theoretical steady-state analysis.

**3.1. Voltage Calculation.** Using the volt-second balance principle for input inductor  $L_{in}$  and magnetizing inductance  $L_m$ , the voltage of the capacitor  $C_2$  and  $C_1$  are calculated as follows:

$$V_{C_2} = \frac{1}{1-D}V_{in}, \quad (10)$$

$$V_{C_1} = \frac{D}{(1-D)(1-N)}V_{in}.$$

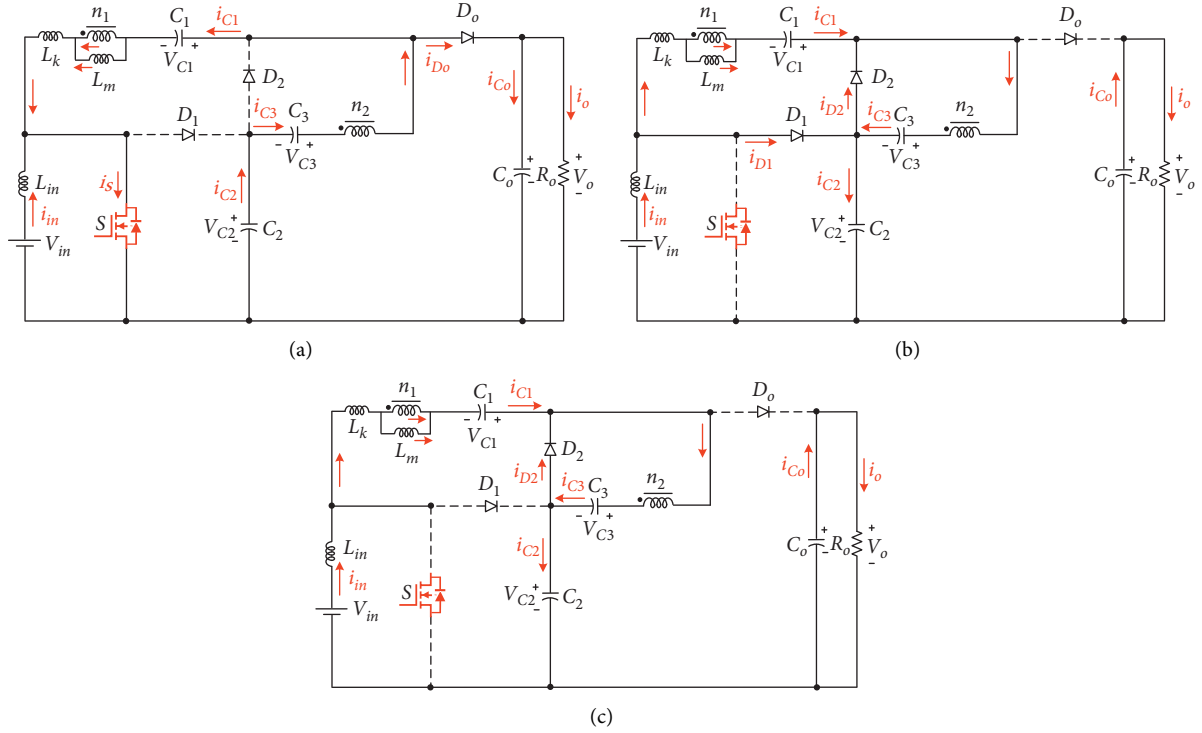


FIGURE 3: The operation modes for the equivalent circuit of the proposed structure. (a) Mode 1, (b) mode 2, and (c) mode 3.

According to the equivalent circuit of the suggested topology in mode 2, the voltage of the capacitor  $C_3$  is given by the following equation:

$$V_{C_3} = NV_{C_1} = \frac{ND}{(1-D)(1-N)}V_{in}. \quad (11)$$

Finally, by using equations (2) and (3), the output voltage can be derived as follows:

$$V_o = V_{C_2} + V_{C_3} + \frac{N}{1-N}(V_{C_1} - V_{C_2} - V_{C_3}). \quad (12)$$

Thus, the voltage gain of the proposed DC-DC topology can be achieved as follows:

$$M = \frac{V_o}{V_{in}} = \frac{1}{(1-D)(1-N)} = \frac{1}{(1-D)(1-(n_1/n_2))}. \quad (13)$$

In addition, for  $N' = 1/N = n_2/n_1$ , the voltage gain can be rewritten as follows:

$$M = \frac{V_o}{V_{in}} = \frac{N'}{(1-D)(N'-1)} = \frac{(n_1/n_2)}{(1-D)((n_1/n_2)-1)}. \quad (14)$$

The voltage gain of the suggested structure versus duty cycle and coupled inductor's turn ratio is shown in Figure 4(a).

As shown in Figure 3(a), during mode 1, the maximum blocking voltage of diode 1 is  $V_{C_2}$ . Besides, during the on-state of switch  $S$ , its maximum blocking voltage is  $V_{C_2}$ . Thus, the voltage stress throughout the power switch  $S$  and diode  $D_1$  are equal together.

$$V_{D_1} = V_S = V_{C_2} = \frac{1}{1-D}V_{in} = (1-N)V_o = \frac{N'-1}{N'}V_o. \quad (15)$$

Furthermore, the voltage stress across the diodes  $D_2$  and  $D_o$  are calculated as follows:

$$V_{D_2} = V_{C_3} - NV_{L_m} = NV_o = \frac{1}{N'}V_o, \quad (16)$$

$$V_{D_o} = V_o - V_{C_2} = V_o - (1-N)V_o = NV_o = \frac{1}{N'}V_o.$$

The obtained voltage stresses of the semiconductor devices versus coupled inductor's turn ratio and power switch's duty cycle are shown in Figure 4(b).

**3.2. Current Calculation.** By using the KCL equations of each mode, which are presented in the previous section, the current stresses of the used semiconductor components are founded as follows:

$$i_S = i_{D_1} = \frac{1-(1-D)(1-N)}{D(1-D)(1-N)}I_o, \quad (17)$$

$$i_{D_2} = i_{D_o} = \frac{2N}{1-D}I_o.$$

According to the proposed converter's configuration, the average currents of the diodes are obtained as follows:

$$I_{D_1}^{avg} = I_{D_2}^{avg} = I_{D_o}^{avg} = I_o. \quad (18)$$

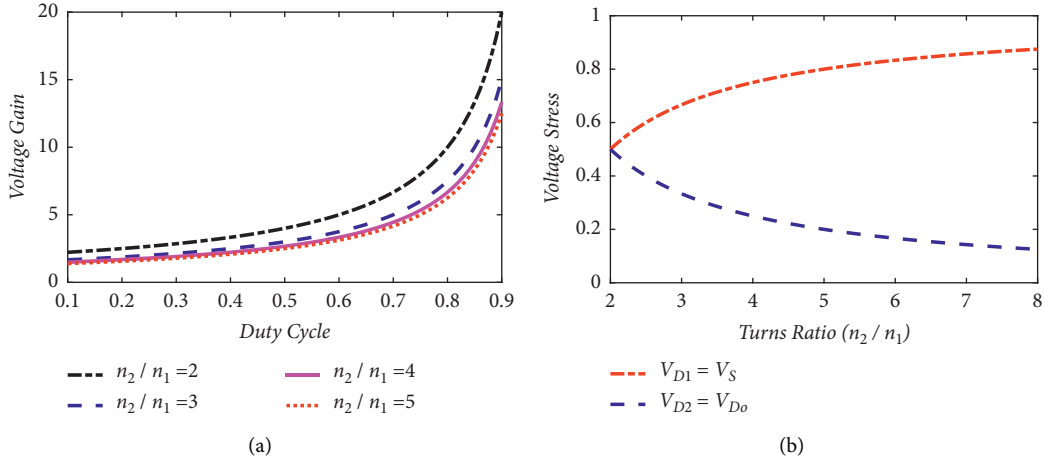


FIGURE 4: The voltage gain and semiconductors voltage stresses of the recommended topology. (a) MCCM curve versus duty cycle and (b) voltage stress curve versus duty cycle.

Using the voltage gain of the converter, the input average current versus output current can be expressed as follows:

$$I_{in} = MI_o. \quad (19)$$

Finally, the average current of the power switch is calculated as follows:

$$I_S^{avg} = I_{in} - I_{D1}^{avg} = (M - 1)I_o = \frac{1 - (1 - D)(1 - N)}{D(1 - D)(1 - N)} I_o. \quad (20)$$

It should be noticed that, for efficiency analysis, root mean square (RMS) currents calculation is necessary. These currents are summarized in Table 1.

**3.3. Efficiency Analysis.** In this section, the proposed converter's efficiency is analyzed. For this study, the parasitic resistance of the used components is assumed as follows: (1)  $R_{DS-ON}$ : turn-on power switch's resistance, (2)  $R_{(D1,D2,D0)}$ : diodes equivalent series resistance, (3)  $R_{(L_{in},n1,n2)}$ : equivalent series resistance of inductors windings, (4)  $R_{(C1,C2,C3,C0)}$ : equivalent series resistance of capacitors, and (5)  $V_{F(D1, D2, D0)}$ : forward voltage of diodes.

Using equations (21) and (22), the converter efficiency can be calculated as follows:

$$\eta_{Converter} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \times 100\%, \quad (21)$$

$$P_{loss} = P_{conduction}^S + P_{switching}^S + P_{conduction}^D + P_{forward}^D + P_{inductors} + P_{capacitors}. \quad (22)$$

In equation (22),  $P_{conduction}^S$  is the conduction power loss of the switch  $S$  and is obtained as follows:

$$P_{conduction}^S = R_{DS-ON} (I_S^{rms})^2. \quad (23)$$

TABLE 1: The RMS currents of the recommended converter's elements.

RMS currents of the used components	
$I_{C1}^{rms} = I_{n1}^{rms} = \sqrt{1/D(1-D)} NI_o / (1-N)$	
$I_{C2}^{rms} = I_{C3}^{rms} = I_{n2}^{rms} = \sqrt{1/D(1-D)} I_o / (1-N)$	
$I_{C0}^{rms} = \sqrt{(1-D)(2N-D)^2 + 1/D(1-D)} I_o$	
$I_S^{rms} = I_{D1}^{rms} = 1 - (1-D)(1-N) / \sqrt{D(1-D)(1-N)} I_o$	
$I_{D2}^{rms} = I_{D0}^{rms} = 2N / \sqrt{D} I_o$	

$P_{switching}^S$  is the active switch  $S$  switching loss and is expressed as follows:

$$P_{switching}^S = \frac{1}{2} f_s (t_r + t_f) V_S I_S^{turn-off}. \quad (24)$$

$P_{conduction}^D$  shows the conduction losses of the used diodes and is given by the following equation (25):

$$P_{conduction}^D = R_{D1} (I_{D1}^{rms})^2 + R_{D2} (I_{D2}^{rms})^2 + R_{D0} (I_{D0}^{rms})^2. \quad (25)$$

$P_{forward}^D$  demonstrates the diodes forward voltage losses as follows:

$$P_{forward}^D = V_{F_{D1}} I_{D1}^{avg} + V_{F_{D2}} I_{D2}^{avg} + V_{F_{D0}} I_{D0}^{avg}. \quad (26)$$

$P_{inductors}$  indicates the sum of the input and coupled inductors conduction losses, which is calculated as follows:

$$P_{inductors} = r_{L_{in}} (I_{L_{in}}^{rms})^2 + r_{n1} (I_{n1}^{rms})^2 + r_{n2} (I_{n2}^{rms})^2. \quad (27)$$

Besides,  $P_{capacitors}$  indicates the power losses of capacitors, which is calculated as follows:

$$P_{capacitors} = r_{C1} (I_{C1}^{rms})^2 + r_{C2} (I_{C2}^{rms})^2 + r_{C3} (I_{C3}^{rms})^2 + r_{C0} (I_{C0}^{rms})^2. \quad (28)$$

## 4. Design Considerations

**4.1. Input and Magnetizing Inductances.** The input magnetizing inductances ( $L_{in}$  and  $L_m$ ) can be obtained by the following equations:

$$\begin{aligned} L_{in} &= \frac{V_{L_{in}} DT_s}{\Delta i_{L_{in}}}, \\ L_m &= \frac{V_{L_m} DT_s}{\Delta i_{L_m}}. \end{aligned} \quad (29)$$

In these equations,  $\Delta i_{L_{in}}$  and  $\Delta i_{L_m}$  show the current ripples of the inductors  $L_{in}$  and  $L_m$ . For continuous current mode (CCM) operation of the suggested structure, the value of  $\Delta i_{L_{in}}$  is considered as follows:

$$\Delta i_{L_{in}} \geq 20\% I_{L_{in}}. \quad (30)$$

Finally, the values of  $L_{in}$  and  $L_m$  can be expressed as equations (31) and (32), respectively:

$$L_{in} \geq \frac{V_{in} D (1 - D) (1 - (n_1/n_2))}{0.2 f_s I_o} \rightarrow L_{in} \geq 434 \mu H, \quad (31)$$

$$L_m \geq \frac{V_{in} D^2 (1 - D)}{f_s (1 - (1 - D) (1 - (n_1/n_2)))} \rightarrow L_m \geq 230 \mu H. \quad (32)$$

**4.2. Capacitors.** The capacitors values should be calculated to adjust the capacitor's voltage in an invariant value. The following equation shows the current and the voltage relation of the capacitors:

$$C = \frac{I_C DT_s}{\Delta V_C}. \quad (33)$$

Assuming  $\Delta V_C \geq 0.02 V_C$ , the values of the used capacitors can be obtained versus input voltage and output current by equations (34)–(37), respectively:

$$C_1 \geq \frac{I_o (1 - D) (n_1/n_2)}{2\% f_s V_{in} D} \rightarrow C_1 \geq 40.8 \mu F, \quad (34)$$

$$C_2 \geq \frac{I_o D}{2\% f_s V_{in} (1 - (n_1/n_2))} \rightarrow C_2 \geq 49 \mu F, \quad (35)$$

$$C_3 \geq \frac{I_o}{2\% f_s V_{in} (1 - D) (1 - (n_1/n_2))} \rightarrow C_3 \geq 163 \mu F, \quad (36)$$

$$C_o \geq \frac{I_o D (1 - D) (1 - (n_1/n_2))}{2\% f_s V_{in}} \rightarrow C_o \geq 290 \mu F. \quad (37)$$

## 5. Comparison Study

To verify the performance of the suggested topology, a comparison among the suggested DC-DC topology and other structures is provided. For this study, voltage gain,

components count, maximum voltage stress across the semiconductors, input current ripple, soft-switching feature, and efficiency are taken into account. The represented comparison is summarized in Table 2. In this comparison, the value of the duty cycle ( $D$ ) is 0.6. Also,  $n_1$  and  $n_2$  are 2 and 3, respectively. According to Table 2, the voltage gain of the recommended topology is 7.5, which is higher than the other structures. Besides, this value of voltage gain is obtained with ten used components, including one power switch, two magnetic cores, three diodes, and four capacitors. The number of used semiconductor devices has a high impact on the converter cost. In the suggested topology, only four semiconductor devices are used. Figure 5(a) shows the voltage gain comparison between the introduced converters in Table 2. The normalized maximum voltage stress across the power switch of the proposed structure is 0.33. Although the recommended converter in reference [17] has lower  $V_S/V_o$  than the suggested topology for  $D = 0.6$  and  $n_2/n_1 = 3/2$ , the voltage gain of this topology is lower than the recommended topology. Besides, the input port current ripple of the represented converter in reference [17] is high and there is no soft-switching condition. Figure 5(b) shows the comparison of the normalized maximum voltage stress across the power switch. Due to this figure,  $V_S/V_o$  of the suggested topology is higher than the other converters for the high coupled inductor's turns ratio. However, for a high number of turn ratio, the power loss of winding is increased. Therefore, it is reasonable to use a coupled inductor with a low turn ratio number. The normalized maximum voltage stresses across diodes are shown in Figure 5(c). As can be seen that the proposed topology has a low value of  $V_D/V_o$  for  $n_2/n_1$  higher than 2. Also, for  $n_2/n_1 = 3/2$ , the converters in references [19, 20, 25] have lower normalized maximum voltage stress across diodes. Nonetheless, these topologies have a lower voltage conversion ratio and higher  $V_S/V_o$ . On the other hand, the input current ripple of the structure in [25] is high, which is not proper for renewable energy systems. The efficiency of the introduced structures in Table 2 is compared at 200 W output power. As can be seen that the proposed topology has higher efficiency than the other converters. Although, the converter [25] has higher efficiency than the proposed converter; nevertheless, the voltage gain in this converter is low and also, the input ripple and voltage stress of the switch are high compared to the suggested converter. Some factors of experimental results are added to Table 2. The operating frequency, output voltage, input voltage, turn ratio of the coupled inductor, and nominal power of all converters in the comparison section and suggested converter are illustrated in Table 2. The efficiency comparison of the suggested converter and other converters based on the output power from 50 W output power to 225 W output power has been shown in Figure 5(d). From this figure, it is obvious that the recommended structure can achieve high efficiency compared to other structures from light load to full load condition. Besides, there are soft-switching conditions through the diodes of the presented converter, which leads to a further increase in efficiency.

TABLE 2: Comparison of the suggested converter and other nonisolated topologies.

Specification	Reference [16]	Reference [17]	Reference [18]	Reference [19]	Reference [20]	Reference [21]	Reference [22]	Reference [25]	Proposed
Number of switches	1	2	1	1	1	2	1	1	1
Number of diodes	2	5	3	3	3	2	4	4	3
Number of inductors	1	0	0	1	1	1	1	0	1
Number of capacitors	2	3	3	3	3	3	3	5	4
Number of coupled inductors	1	1	1	1	1	1	1	1	1
$M$	$n_2/n_1/1-D = 3.75$	$n_2/n_1/2-D/1-D = 5.25$	$n_2/n_1+1/1-D = 6.25$	$n_2/n_1+1/1-D = 6.25$	$n_2/n_1+1/1-D = 6.25$	$n_2/n_1/1-D = 3.75$	$1+n_2/n_1/D/1-D = 4.75$	$1+n_2/n_1/D/1-D = 4.75$	$n_2/n_1/(1-D)$
$V_o/V_o$	$1/n_2/n_1 = 0.66$	$1/2n_2/n_1(2-D) = 0.23$	$1/n_2/n_1+1 = 0.4$	$1/n_2/n_1 = 0.66$	$1/n_2/n_1+1 = 0.4$	$1/n_2/n_1 = 0.66$	$1/1+n_2/n_1/D = 0.52$	$1/n_2/n_1+1 = 0.4$	$(n_2/n_1-1)/n_2/n_1 = 0.33$
$V_D/V_o$	1	$1/2-D = 0.71$	1	$n_2/n_1/n_2/n_1+1 = 0.6$	$n_2/n_1/n_2/n_1+1 = 0.6$	1	$n_2/n_1/1+n_2/n_1/D = 0.78$	$n_2/n_1/n_2/n_1+1 = 0.6$	$1/n_2/n_1 = 0.66$
Input current ripple	Low	High	High	Low	Low	Low	High	High	Low
Efficiency at 200 W (%)	95.9	94.55	95.5	94	-	95.4	93.8	96.2	95.8
Frequency (kHz)	100	50	50	50	24	100	60	100	50
$V_o/V_{in}$	146/38	200/24	200/25	400/24	300/15	400/48	400/42	400/40	180/24
$N$	5	3	3	3	3	4	5	4	1.5
Nominal power (W)	250	200	250	200	100	300	200	350	250
Soft switching	Yes	No	No	Yes	No	Yes	No	No	Yes

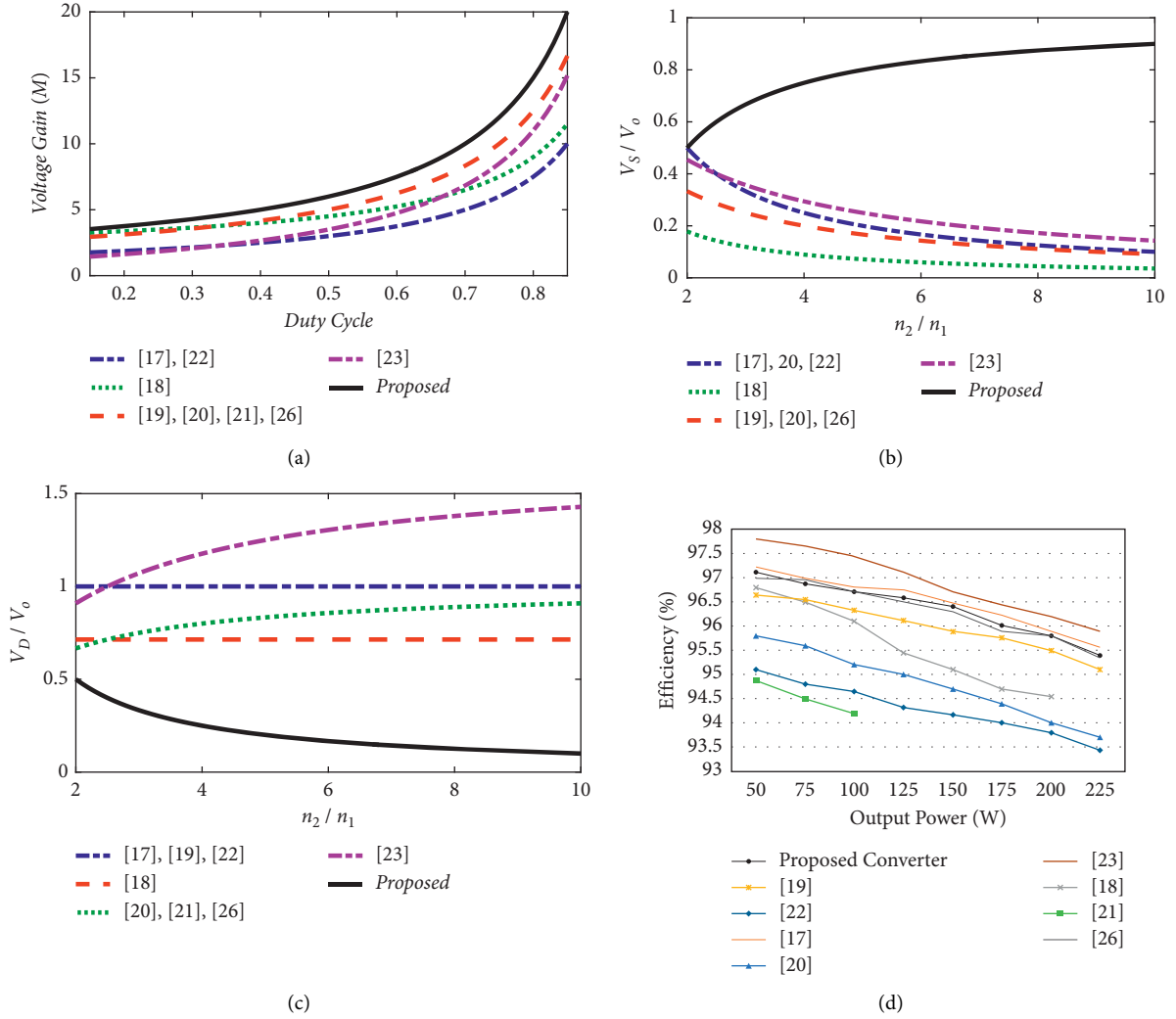


FIGURE 5: Comparison result between the suggested converter and other similar topologies. (a) Voltage gain  $M$ , (b) normalized maximum voltage stress of switches, (c) normalized maximum voltage stress of diodes, and (d) efficiency comparison of the proposed converter and other published works.

It is apparent that the recommended structure can achieve high voltage gain by using the low turn ratio of the coupled inductor in comparison to other structures. Therefore, the overall cost of the suggested topology is decreased. Soft-switching conditions such as ZVS and ZCS on semiconductor devices and the low number of used components are significant reasons to obtain a high-efficiency DC-DC converter. Therefore, with supposing the comparison results, the proposed topology is a suitable choice for renewable energy applications such as PV power systems. Because in these systems, a high voltage gain and high-efficiency DC-DC converter is necessary to enhance DC voltage level.

## 6. Simulation Results

The purpose of the simulation is to examine the relationships and claims expressed in the previous sections. All simulations are performed by PSIM software. The suggested converter is simulated when the switching frequency, input/

output voltages, and coupled inductor turn ratio are set at 50 kHz, 24/180 V, and 3/2 regarding the following parameters:

- (i) Capacitors values:  $C_1 = 220 \mu\text{F}$ ,  $C_2 = 220 \mu\text{F}$ ,  $C_3 = 220 \mu\text{F}$ , and  $C_o = 470 \mu\text{F}$ .
- (ii) Input inductor:  $500 \mu\text{H}$ .
- (iii) Magnetizing inductance:  $250 \mu\text{H}$ .

The gate-source voltage of the main switch is shown in Figure 6(a). The converter duty cycle is 60% and has a switching frequency of 50 kHz. Figure 6(b) indicates the drain-source voltage of the power switch, which is about 60 V. The voltage of the capacitors is shown in Figure 7(a). From this figure, the voltage of the capacitors  $C_1$ ,  $C_2$ , and  $C_3$  are about 108, 63, and 70 V, respectively. The output and input voltage simulation waveforms are indicated in Figure 7(b). The input voltage ( $V_{in}$ ) and output voltage ( $V_o$ ) of the suggested converter ( $V_{in}$ ) is 24 V and approximately 180 V, respectively. Related to this figure, the converter output voltage



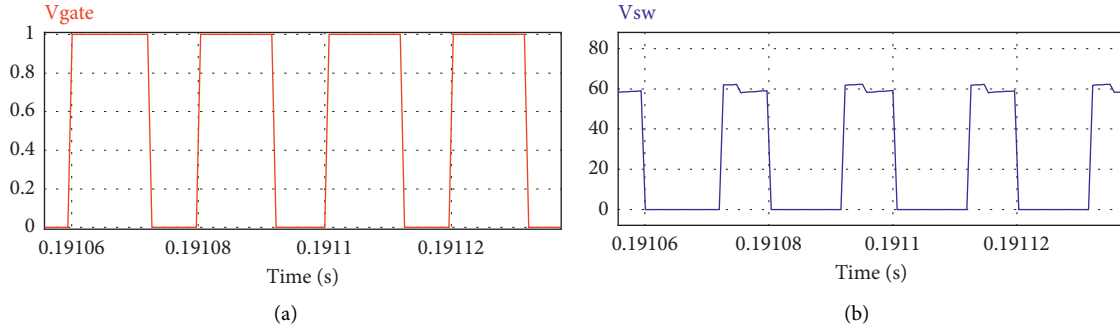


FIGURE 6: The simulation measurement of the recommended topology. (a) Gate-source voltage of switch. (b) Drain-source voltage of switch.

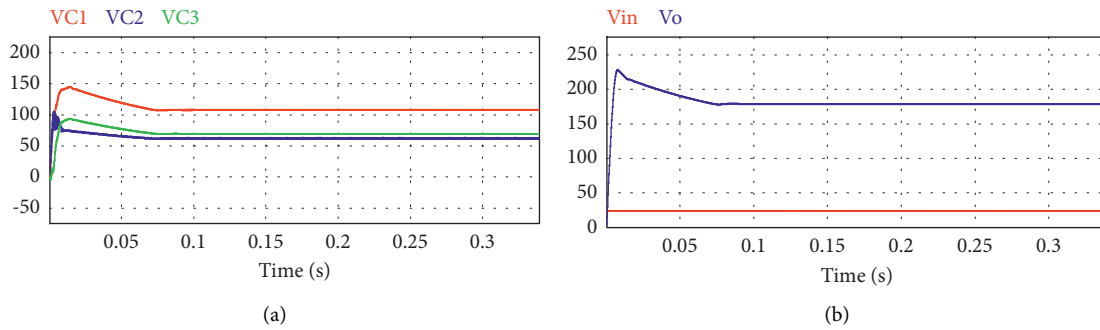


FIGURE 7: The simulation measurement of the recommended topology. (a) Capacitor voltages. (b)  $V_o - V_{in}$ .

ripple is poor and can be neglected. The voltage and current simulation waveforms of diodes  $D_1$ ,  $D_2$ , and  $D_o$  are illustrated in Figures 8(a)–8(c), respectively. As can be seen, the maximum voltage of diodes  $D_1$ ,  $D_2$ , and  $D_o$  are 62, 120, and 120 V and their currents are about 8.9, 3.6, and 2.5 A, respectively. Due to Figure 8, there is ZCS condition throughout diode  $D_1$  and also ZVS condition through the diodes  $D_2$  and  $D_o$ . The input current waveform is indicated in Figure 8(d). As depicted in this figure, the peak current of the input current is about 1.5 A, which is a small amount.

## 7. Experimental Results

In this section, the laboratory result of the proposed structure is provided to indicate the converter's performance by considering  $V_{in} = 24$ ,  $f_s = 50$  kHz, and  $D = 0.6$  in 150 W output power level. The main specifications of the suggested topology are listed in Table 3. The obtained results prove the validity of the technical survey and mathematical calculations. The experimental prototype of the recommended converter is depicted in Figure 9.

As shown in Figure 9, the experimental scheme of the suggested converter includes a power circuit and gate driver circuit. The power circuit includes the following elements:

- (i) Electrolyte capacitors ( $C_1$ ,  $C_2$ , and  $C_3$ ) with the capacity of  $220 \mu\text{F}$ .
- (ii) Electrolyte capacitor with the capacity of  $470 \mu\text{F}$ .
- (iii) The utilized diodes are fast recovery diodes.

- (iv) The power switch is a metal-oxide-semiconductor field-effect transistor (MOSFET).
- (v) The coupled inductor is EPCOS B66344 (Ferrite core EE50) model.
- (vi) The utilized load is the electro-mechanic heating element ( $200 \Omega$ ), which can provide 300 V and 300 W output voltage and output power level.
- (vii) The input inductor is the drum core inductor.

The laboratory results of the proposed converter are achieved by using a digital signal oscilloscope, which is named GDS-10748. The input source is DC supply. In this study, the RN-3005-D laboratory DC power supply, for signaling, the power MOSFET, and for producing the appropriate duty cycle, the ATMEGA16 microcontroller have been utilized. The required frequency and duty cycle are programmed to the microcontroller. Then, the IR2111 is a half-bridge driver that is used for driving the power MOSFET. It is a high voltage, high-speed power MOSFET driver with dependent high and low side referenced output channels. In order to isolate the microcontroller and IR2111 driver, an optocoupler has been employed between them. The selected devices with their voltage and current rating for the proposed structure are given in Table 3.

The voltage and current experimental waveforms of the suggested converter are shown in Figures 10–13. Figure 10 shows the input current waveform. The input current is tolerated between 6.4 and 7 A. Thus, the ripple of the input current is low compared to the other converters in the same

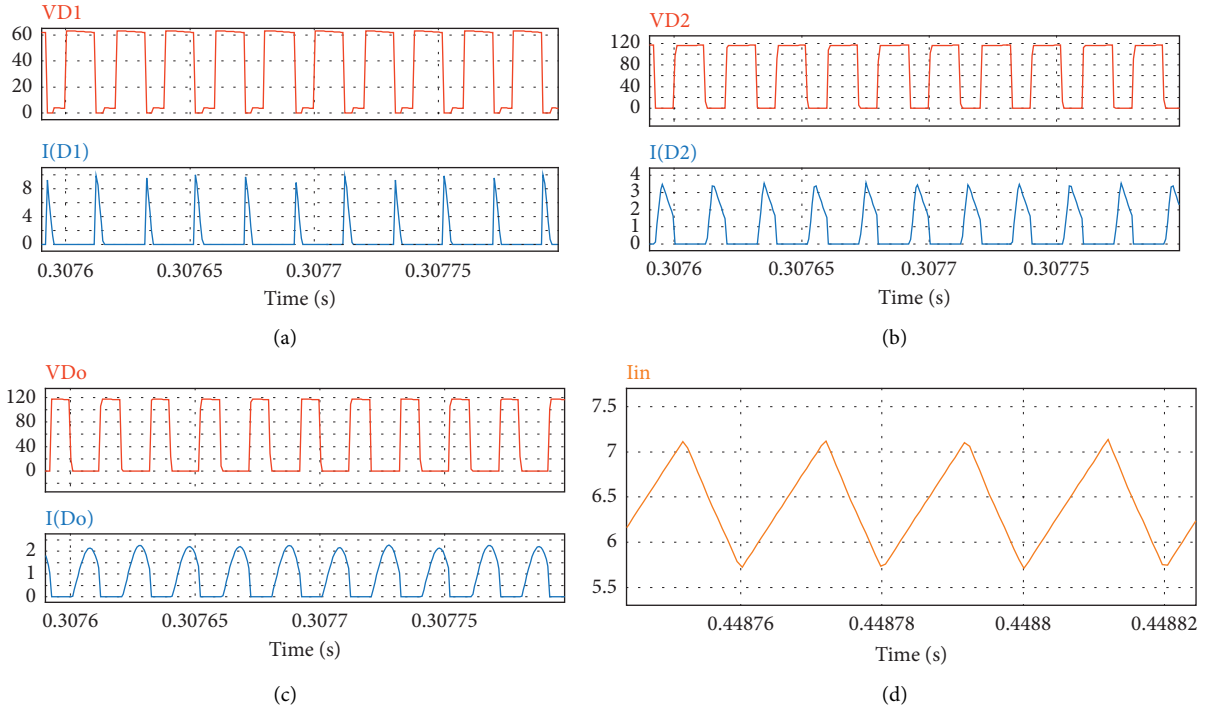


FIGURE 8: The simulation measurement of the recommended topology. (a)  $V_{D1} - i_{D1}$ . (b)  $V_{D2} - i_{D2}$ . (c)  $V_{Do} - I_{Do}$ . (d)  $I_{in}$ .

TABLE 3: List of the circuit components of the prototype.

Element	Specification
Switch	STW55NM60
Diodes	MUR2060
$L_{in}$	500 $\mu\text{H}$
$L_m$	Ferrite core EE50, 250 $\mu\text{H}$ , N2/N1 = 3/2
$C_1, C_2$ , and $C_3$	200 V/220 $\mu\text{F}$
$C_o$	400 V/470 $\mu\text{F}$
$L_{k1}$ and $L_{k2}$	2 $\mu\text{H}$

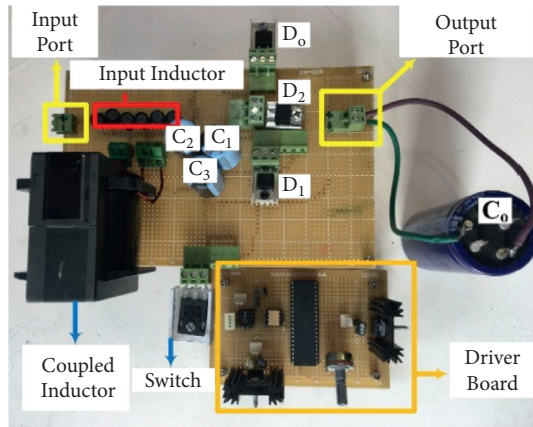


FIGURE 9: Experimental prototype of the proposed converter.

family. The voltage and current waveforms of the diodes are illustrated in Figures 11(a)–11(c). Figure 11(a) shows the voltage and current waveform of diode  $D_1$ , which are about

59 V and 8.3 A, respectively. As can be seen that diode  $D_1$  is turned off in the ZCS condition that decreases the reverse recovery losses of the diode. Due to Figures 11(b) and 11(c), the voltages and currents of diode  $D_2$  and  $D_3$  are about 118 V, 118 V, 3.5 A, and 2.4 A, respectively. Regarding Figures 11(b) and 11(c), there is zero voltage switching condition through diodes  $D_2$  and  $D_o$ , which enhances the overall efficiency of the suggested topology. Besides, the peak voltage of the diodes is low compared to  $V_o$ . The voltage and current waveforms of the main switch are indicated in Figure 11(d). The peak voltage of the switch  $S$  is about 59 V that is three-time smaller than the output voltage, and the peak current is almost 12 A. The capacitor voltage and the output voltage waveforms are depicted in Figures 12(a)–12(d), respectively. The measured voltages of  $C_1$ ,  $C_2$ , and  $C_3$  are about 105, 60, and 69 V, respectively. The obtained values for the capacitor voltage validate the calculated equations (equations (11)–(13)). The output voltage waveform is indicated in Figure 12(d). As can be seen that  $V_o$  is almost 178 V with a poor voltage ripple. The experimental waveforms of the first and secondary side winding of the coupled inductor current are measured and indicated in Figures 13(a) and 13(b), respectively.

Table 4 indicates the values of the recommended converter elements in theoretical, simulation, and experimental states. It is apparent that there is little difference between the results of each state. The reason for this is that the elements are not ideal in practice, and they have conductive losses.

The theoretical and experimental output voltages based on duty cycle are illustrated in Figure 14. Regarding this figure, it is apparent that there is a little difference between the results of each section.

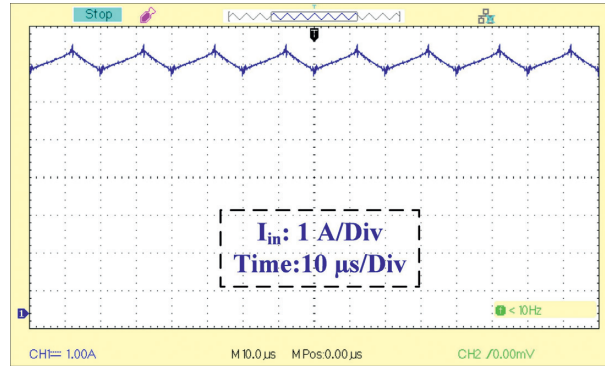
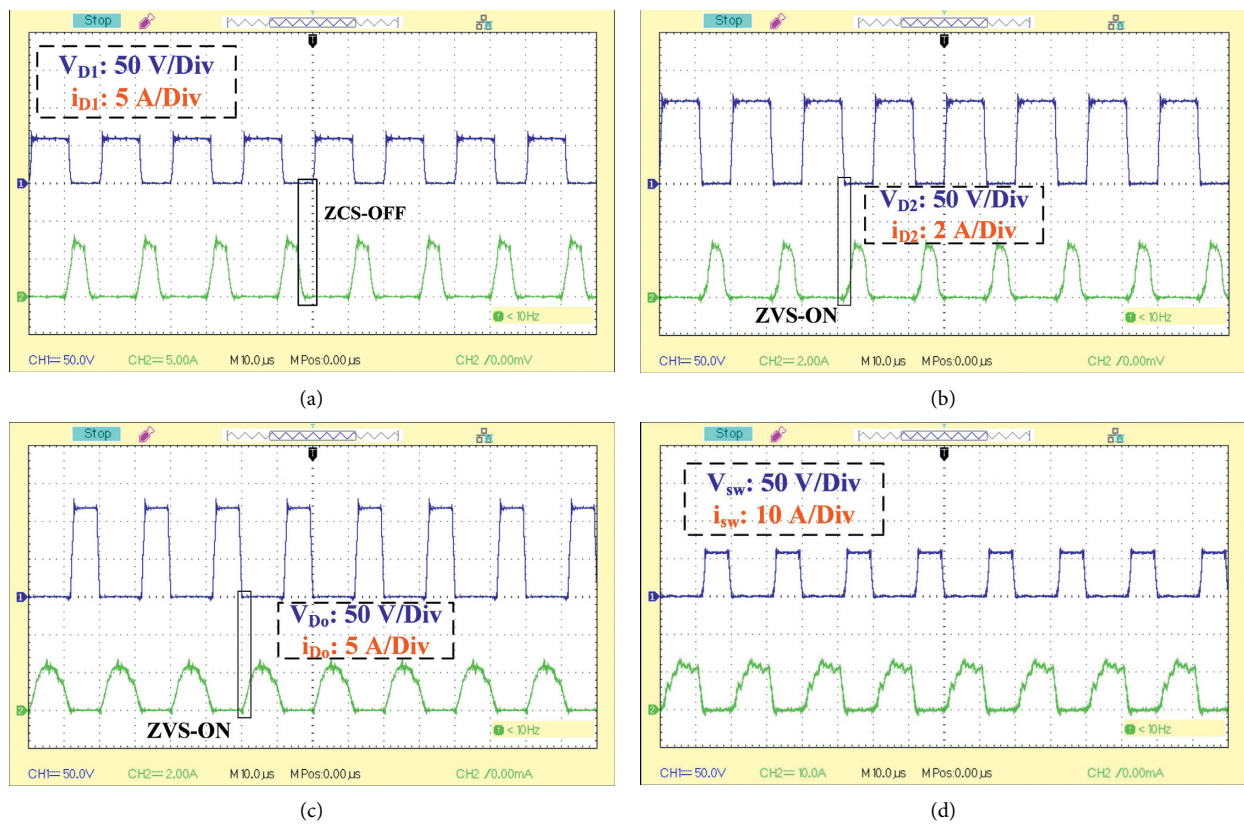


FIGURE 10: The input current measurement of the recommended topology.

FIGURE 11: Experimental measurement of the recommended topology. (a)  $V_{D1} - I_{D1}$ , (b)  $V_{D2} - I_{D2}$ , (c)  $V_{D0} - I_{D0}$ , and (d)  $V_{sw} - i_{sw}$ .

The voltage stress of the switch in experimental results for a different range of duty cycle is measured and indicated in Figure 15. From this figure, it can be found that the voltage stress through the switch is lower than the output voltage for all duty cycles, which leads to achieving higher efficiencies for such converter.

The efficiency curve for different levels of power rating is shown in Figure 16 by considering  $N = 1.5$ ,  $D = 0.6$ , and  $f_s = 50 \text{ kHz}$ . The proposed topology's maximum efficiency is about 96.4% at input voltage 24 V and output power 150 W, which is depicted in Figure 16. The full-load efficiency is approximately 95.4% at 250 W. It is obvious that the

efficiency of the proposed structure is reduced for power tolerance between 100 W and 250 W. However, the overall efficiency of the suggested topology at different output power is greater than 95%. Besides, the theoretical and measured experimental efficiency curve versus output power is indicated in Figure 17. From this figure, it is obvious that the efficiency of the suggested converter is flexible and high. Noted that DC-DC converters with high voltage gain can be used in a different rate of power conversion systems from light power level to high power levels in many applications such as renewable energy systems.

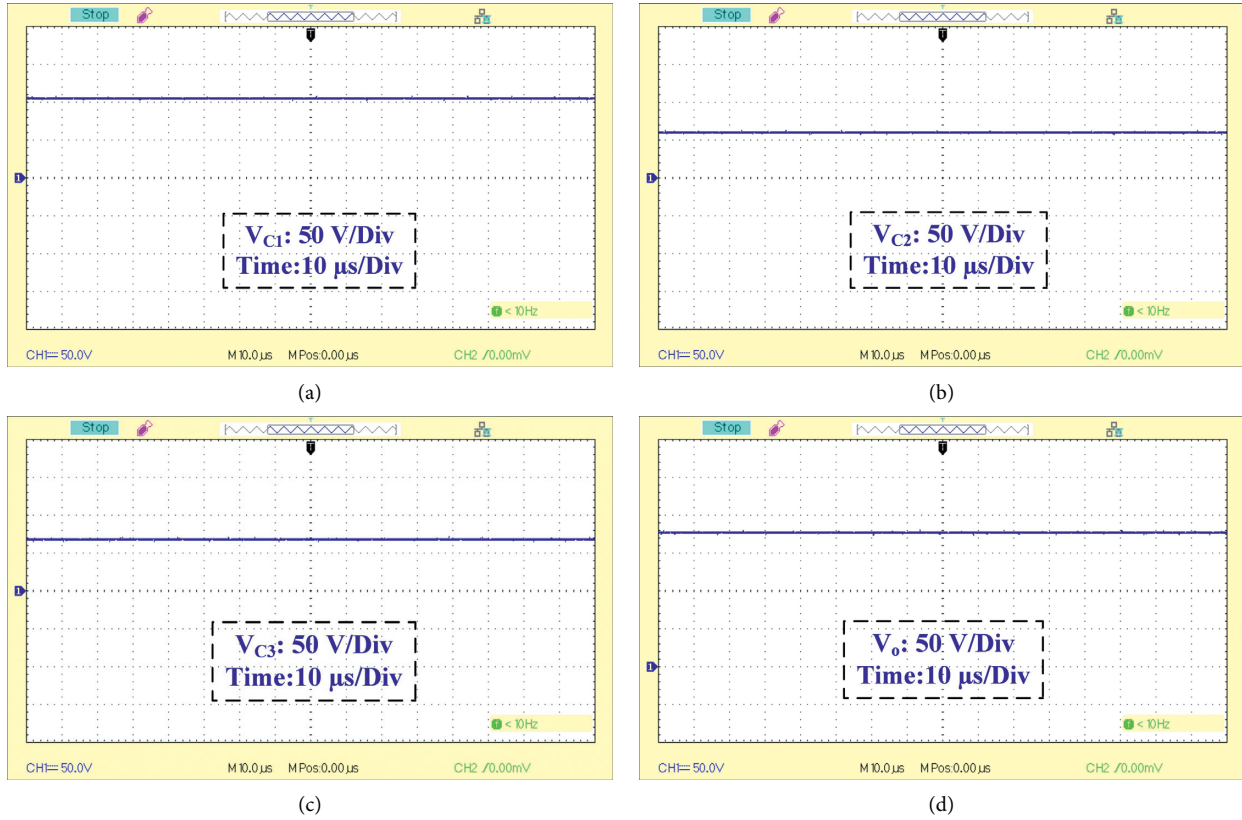


FIGURE 12: Experimental measurement of the recommended topology. (a)  $V_{C1}$ , (b)  $V_{C2}$ , (c)  $V_{C3}$ , and (d)  $V_o$ .

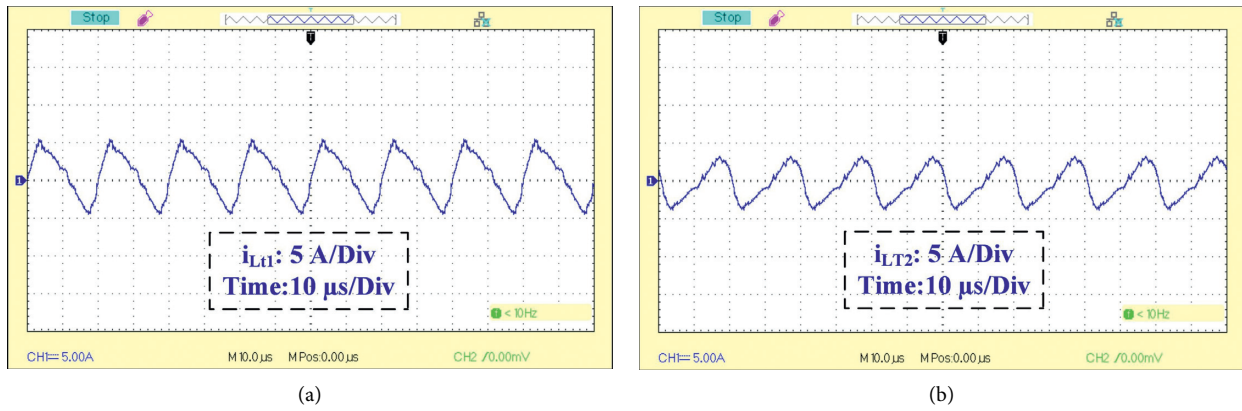


FIGURE 13: The experimental measurement of the recommended topology. (a)  $i_{L1}$  and (b)  $i_{L2}$ .

TABLE 4: Comparison between the values of components.

Value of components	Theoretical value	Simulation value	Experimental value
$V_o$	180	179	178
$V_{DS}$	60	59.5	59
$V_{C1}$	105.88	105	104
$V_{C2}$	60	59.8	60
$V_{C3}$	69.88	69	69
$V_{D1}$	60	59	59
$V_{D2}$	120	119	118
$V_{D_o}$	120	119	118



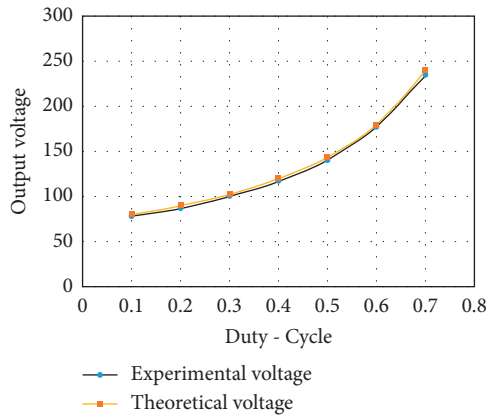


FIGURE 14: Theoretical and experimental output voltage curve versus duty cycle.

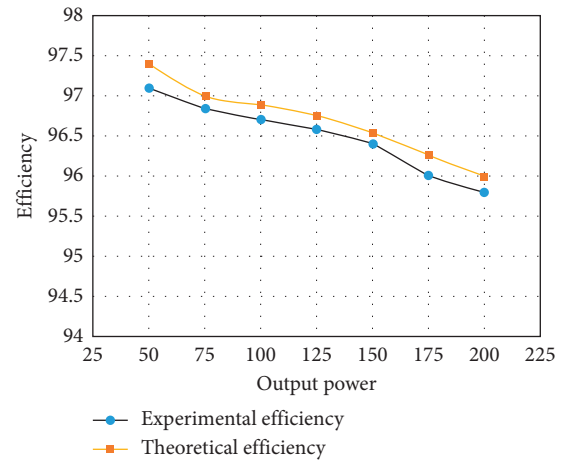


FIGURE 17: experimental and theoretical efficiency of the suggested converter.

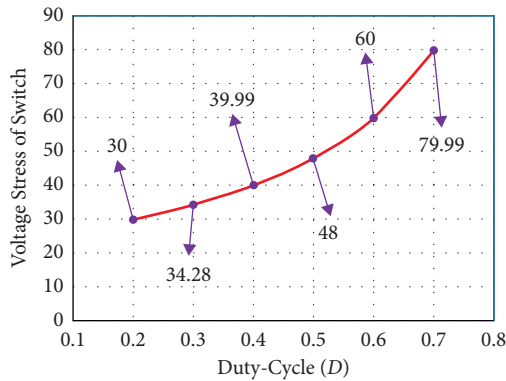


FIGURE 15: Voltage stress of switch versus duty cycle.

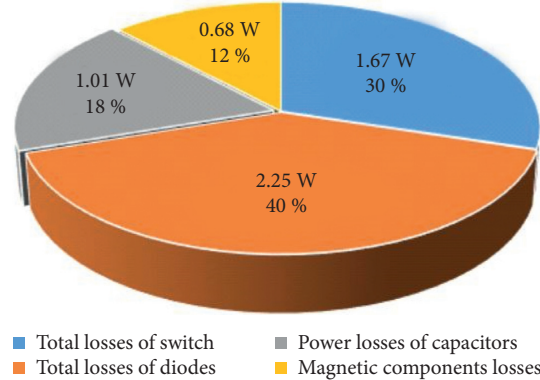


FIGURE 18: Losses curve of the proposed converter in 150 W output power.

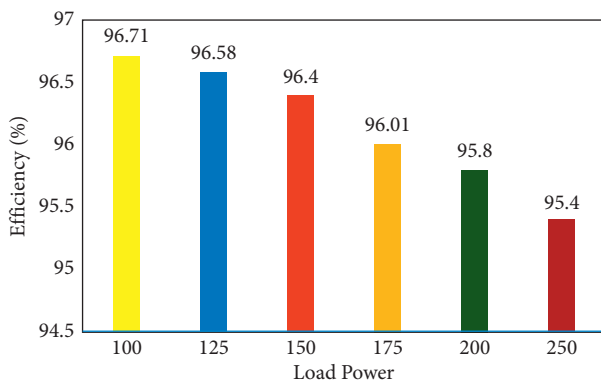


FIGURE 16: The measured efficiency of the presented structure in various load powers.

The total losses analysis of the proposed converter in 150 W output power by considering  $N=1.5$ ,  $D=0.6$ ,  $V_{in}=24$ , and  $f_s=50$  kHz and also based on experimental values and losses calculation section is demonstrated in Figure 18.

Finally, the obtained results of this study verified that the proposed nonisolated DC-DC topology could be a proper choice for renewable energy applications such as fuel cells

and PV networks with many features such as soft-switching ability, low volume and core, high voltage conversion ratio, and high efficiency. Besides, by using high power rating elements in the suggested topology, the proposed structure can be utilized in low power and high power applications such as PV systems, fuel cells, and LED lamps.

## 8. Conclusion

In this study, a novel nonisolated DC-DC converter based on the coupled inductor and VMC for renewable energy applications such as photovoltaic power systems has been proposed. Only one power switch is used in the suggested structure, which leads to low cost and volume. Other benefits of the proposed converters are as follows: (1) low components count, (2) high efficiency, (3) low input current ripple, (4) low voltage stress across the semiconductors, and (5) ZCS and ZVS of diodes. The applied VMC acts as a passive clamp circuit and reduces the maximum voltage across the power switch. The operation principles with steady-state calculation were carried out in this study. The design consideration for the capacitors, coupled inductor, and input inductor has been done. Besides, in order to

demonstrate the proficiency of the suggested converter, comparison results with other similar converters in many aspects were provided in the literature. Based on the comparison study, the proposed structure has a high voltage gain with low voltage stress across diodes. Finally, a 150 W laboratory prototype with 24 V input voltage and 180 V output voltage at 50 kHz operating frequency is provided. In conclusion, the experimental results are verified the theoretical and simulation analysis. Additionally, the measured efficiency for different power levels, which is higher than 95%, validates that the proposed structure could be an appropriate choice for green energy systems.

## Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

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