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Printed circuit board (PCB) miniaturization by embedded passives and sequential build-up (SBU) process methodology

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Abstract

One of the foremost design considerations in microelectronics miniaturization is the use of embedded passives which provide practical solution. In a typical circuit, over 80% of the electronic components are passives such as resistors, inductors, and capacitors that could take up to almost 50% of the entire printed circuit board area. By integrating passive components within the substrate instead of being on the surface, embedded passives reduce the system real estate, eliminate the need for discrete and assembly, enhance electrical performance and reliability. This paper presents an entire process from design and fabrication to electrical characterization and reliability test of embedded passives on multilayered microvia organic substrate. Numerical models of embedded capacitors have been developed to qualitatively examine the effects of process conditions and electrical performance due to thermo-mechanical deformations. Also, a prototype working product with the board-level design including features of embedded resistors and capacitors is presented.

Keywords: Embedded capacitor, embedded resistor, PWB fabrication, thermo-mechanical reliability, SOP, embedded passives.

1. Introduction

1.1. *Background*

Over the last several decades, tremendous progress has been made in electronics industry. In 1959, the first integrated circuit (IC) developed by Jack Kilby contained only two transistors and a resistor, but now a personal computer IC contains more than a billion transistors. Cell phones that were once bulky in size are now slim and integrated with more functionality than ever. Various complex technologies are being successfully integrated together to form a remarkable stand-alone system. And yet, there is a constant demand for faster, smaller, and more reliable low-cost electronic systems. A potential solution to meet the current and future challenges is embedded passives technology. Although surface-mount technology (SMT) is improving, embedded passives can eliminate the approaching limitations of SMT footprints. As an essential component of system-on-package (SOP),

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embedded passives reduce the system real estate, eliminate the need for discrete and assembly, enhance electrical performance and reliability, and potentially reduce the overall cost [1–5].

Current worldwide passive market is approximately USD 25 billion, and although embedded passive was introduced decades ago, less than 2% of components are embedded [6]. To gain greater acceptance and increase market share, several technical challenges must be resolved: tight tolerance, low thermal coefficient of resistance (TCR), low thermal coefficient of capacitance (TCC), high yield and reliability, and availability of wide range of resistance and capacitance. iNEMI (International Electronic Manufacturing Initiative) projects portable and handheld product needs passives with maximum resistance of 100 kohms/sq, maximum capacitance of 250 nF/sq, and tolerance of 5% without trim by 2007 [6]. Another major challenge for the overall success of embedded passives is reliability. Although solder joints are eliminated, rework is not a viable option. A single bad component can lead to scrapping of the entire board. This paper presents a method that offers low-temperature processing for organic board compatibility. An entire process from design and fabrication of multilayered microvia organic substrate to extensive electrical characterization and mechanical reliability tests with some modeling data is presented.

This paper presents a complete and comprehensive detailing of design and fabrication of multilayered microvia organic substrate, extensive electrical characterization and mechanical reliability tests with some modeling data, a portion of which has been already reported by our group earlier [7]. The highlight of the method described here is that it offers low-temperature processing and organic board compatibility.

1.2. *Embedded resistors*

A wide range of resistance is needed for various electronic systems. In embedded resistor technology, a resistor is patterned as a strip of the resisting material with two conducting pads at the ends for interconnection to other components. Therefore, resistance is dependent on the resistivity of the material and the dimensions of the strip. Higher resistance can be achieved by using higher resistivity materials, increasing the length, and using smaller cross-sections. Sheet resistance is the resistance of a square strip. It is another common way of expressing the resistance as shown in eqn (1).

$$R = \left(\frac{\rho}{d}\right)\left(\frac{L}{W}\right) = R_z N_z, \tag{1}$$

where R is the resistance (Ω), ρ, the resistivity of material (Ω-cm), L, the length of the strip (cm), W, the width of the strip (cm), d, the thickness of the strip (cm), Rs, the sheet resistance (ohms/sq) and Ns, the number of squares. As long as the ratio of L and W or the number of squares remains the same, the resistance value does not change. A single value of resistance can be obtained by various sizes of resistor material as long as the number of squares remains the same.

For most applications, resistance range from approximately 10 ohms to 1 Mohms is required [2]. In terms of sheet resistance, number of squares that is outside the range of 0.1 to

100 could mean excessive footprints, yield and tolerance problems, and significant parasitic capacitance for high-frequency applications. Consequently, at least two sheet resistances such as 100 ohms/sq and 10 kohms/sq are needed to cover the desired range of resistance. Materials, for example, with 100 ohms/sq sheet resistance can cover the resistances from 10 ohms to 10 kohms and those with 10 kohms/sq sheet resistance from 10 kohms to 1 Mohm. To narrow down the choice of materials, if thickness can be between 100 Å and 1 μm, then the material should have resistivity in the range of 10^{-4} to 1 Ω-cm. Although there are many materials that are capable of achieving these requirements, some of them are difficult to process or insufficiently stable with respect to temperature or time. Some of the leading types of materials that have shown success are resistive alloys, ceramic-metal nanocomposites and carbon-filled polymers. Besides materials, there are challenges in process integration such as large area fabrication with good reproducibility and yield, material stability, variation in length, width and thickness of the deposited thin film, contact resistance, smoother substrate to reduce noise, trimming, and development of low-cost fabrication processes.

1.2.1. *Embedded resistor fabrication methods*

Embedded resistors have been a major focus in this work especially in the aspect of process technology and adaptability to standard PWB processes. There are three basic methods to produce embedded resistors: (i) polymer thick film, (ii) thin film resistors by foil lamination, and (iii) by electroless deposition of Ni–P alloys. In this study, only PTF and resistor foil lamination methods are presented. Polymer thick film pastes are usually a mixture of conductive carbon powder dispersed in a polymeric media like epoxy with other filler particles tuned to get a particular sheet resistivity range. PTF materials with sheet resistivity from 50–500 ohms/sq are easily available in the market today. In the case of thin film foils, sheet resistance in the range 25–250 Ω/sq is commercially available from Ohmega and Gould. These are basically NiCr or NiCrAlSi resistor materials uniformly deposited on copper. This foil can be laminated on a PWB and then the desired resistor patterns can be photolithographically realized on the board. Fine-tuning of the resistor values can be done by laser trimming of the fabricated resistors to get closer tolerance values (up to 1%). The third method, i.e. electroless plating [8–10] appears to be a good approach to meet the required goal in the low-value resistors. Ni–P or Ni–W–P alloys are currently being explored as the resistor material to be plated. These alloys are deposited on dielectrics or insulators by the well-established surface roughening by chemical and mechanical methods followed by Pd catalysis or seeding and then using suitable reducing agents to deposit the metal or alloy. Copper is then electroplated on Ni-P alloys before lithographically defining for the length and width of the individual resistors.

1.3. *Embedded capacitors*

A wide range of capacitance from 1 pF to many μF is needed for various applications. Some such as filtering and termination require relatively low capacitance of 1 pF to 200 pF, while others such as decoupling and energy storage require much higher capacitance in the range of nF and μF. The two main types of dielectric materials are paraelectrics and ferroelectrics. Paraelectrics tend to have much lower dielectric constant than ferroelectrics, but

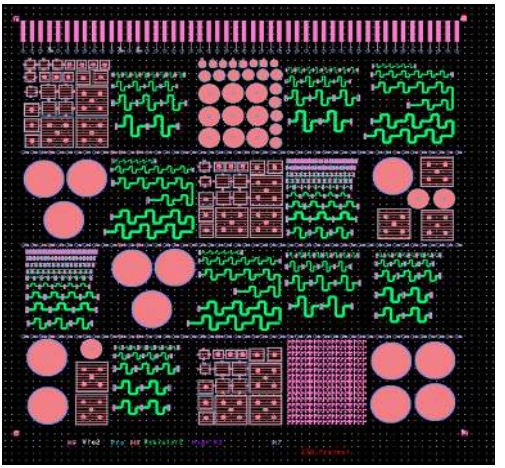

FIG. 1(a). CAD image of the R, and C design.

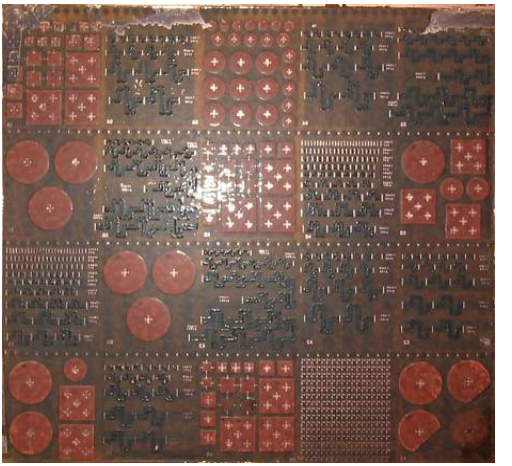

FIG. 1(b). Fabricated test vehicle (TV1) of R and C.

they are more stable with respect to temperature, frequency, voltage and time. Ferroelectrics such as barium titanate can have very high dielectric constants of around 4000. With thickness of one micron, specific capacitance can be potentially up to 1800 nF/cm^2. This material class offers by far the highest energy density, which can be especially useful in energy storage applications.

1.3.1. *Embedded capacitor fabrication methods*

Fabrication techniques for embedded capacitors include sputtering, chemical vapor deposition (CVD), metallo-organic chemical vapor deposition (MOCVD), spin-coating, sol–gel, pulse–laser deposition, dry calcinations, hydrothermal and more [2]. Some of these methods are not suitable for adaptability to PWB processing mainly due to process temperatures being high above the glass transition temperature (*T*g) of PWB substrates. Commercially, Interra and 3M capacitor materials based on barium titanate with fillers are available that offer low dielectric constant of 3–11 with dissipation factor of less than 1%. These are very stable with respect to temperature and frequency and are compatible with the existing PWB processes. In this work, capacitors are fabricated using polymer/ceramic nanocomposite materials which have a capacitance range of 50 pF to 1.5 nF.

2. Design

Two test vehicles (TV1 and TV2) were designed with various sizes, geometries, and values of embedded resistors and capacitors. TV1 is a 6 × 6″ epoxy-based board with eight metal layers. The core is a six-layer subcomposite (Figs 1 and 2). The embedded resistors and capacitors are on metal layer 7, and are connected to probe pads on metal layer 8 by microvias. There are four circular and three rectangular geometry capacitors. Some have center probe connections to reduce the parasitic inductance, while others have edge probe connections for easier fabrication. The resistor design is meant to be universally used for all the three types of resistor fabrication, namely, PTF, foil and electroless deposition and de-

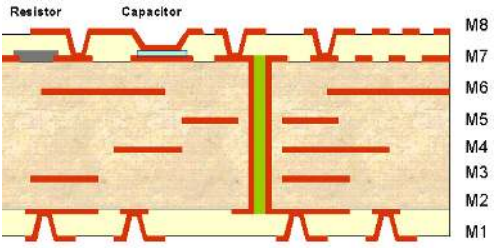

FIG. 2. Cross-section view of R and C on FR-4.

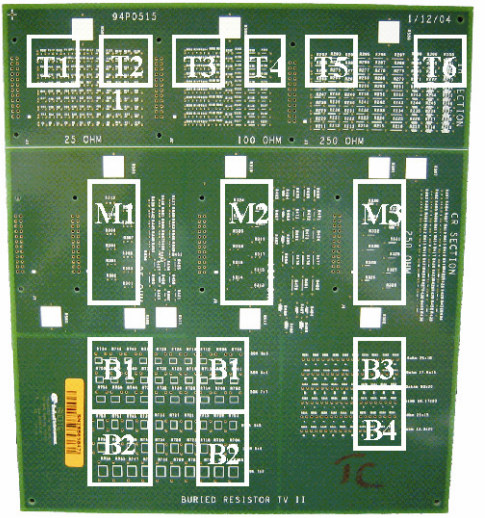

FIG. 3. Completed TV2 and resistor groups examined.

signed to cover a wide range of resistance values. The thicknesses of the R materials in the three types of methods would finally determine the resistance for a given area of the pattern. The capacitor dielectric is based on polymer/ceramic nanocomposite, and the values of these capacitors range from 50 pF to 1.5 nF with capacitance per area of approximately 1.5 nF/cm^2.

TV2 is a 12 × 12″ epoxy-based board with 12 metal layers. It is a dedicated resistor test vehicle as shown in Fig. 3. Top three metal layers contain various sizes, geometries, and values of NiCr foil embedded resistors in the range of 20 ohms–9 kohms.

3. Fabrication

Test vehicles were fabricated at PRC and at Endicott Interconnect Technologies (EIT) through partnership with PRC. There are three main processing steps: capacitors, resistors, and microvia with probe pads. Figure 4 shows the general overview of each step.

3.1. *Polymer/ceramic nano composite capacitors*

The bare core six-metal layer board with bottom copper electrode was surface-treated with acetone to remove any organic residues. It was then microetched, and bond film was applied to increase the adhesion with the dielectric layer.

Polymer/ceramic nanocomposite dielectric was prepared by mixing 44 g of polymeric resin, which contains barium titanate, with 4.24 g of hardener and 5 g of thinner. After mixing them thoroughly, the nanocomposite was spin-coated at 2000 rpm for 30 s on to the bare board to achieve a nominal thickness of 20 μm. Then, the board was soft-cured at 65°C for 45 min. For top copper electrode, a 10-μm copper foil was vacuum-laminated, and then heat-pressed (2 ton) at 70°C to strengthen the lamination. Then, conventional photolithography process was performed using Shipley SP2029 positive photoresist. The exposed

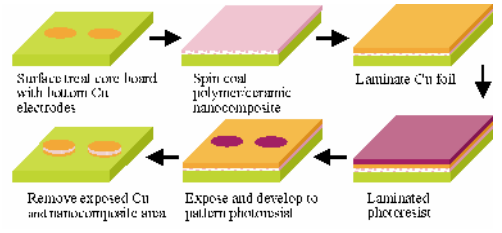

FIG. 4(a). Capacitor fabrication process.

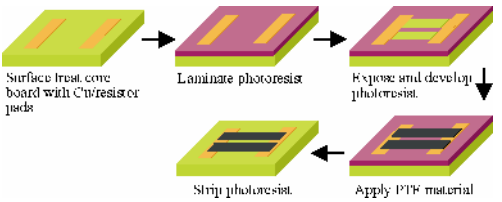

FIG. 4(b). Resistor fabrication process.

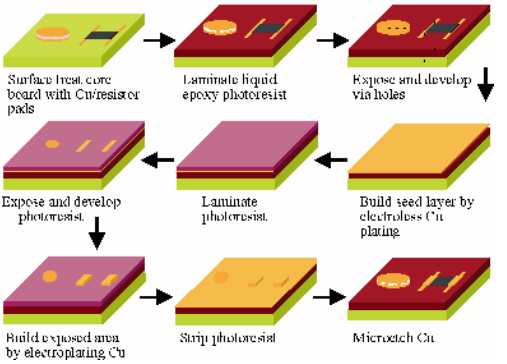

FIG. 4(c). Microvia with probe pad fabrication process.

copper and nanocomposite were removed with 30% ferric chloride solution and GBL (gamma butyrolactone) solvent, respectively, to finish the capacitor process. Simple and low-temperature process exhibited high yield with capacitance per area of ~1.5 nF/cm^2. These capacitors were also fabricated at the EIT using proprietary materials and processes.

3.2. *Resistors using polymer thick film material*

Conventional lift-off process was used to fabricate the embedded resistors. Initially, the board was treated with acetone and microetched to thoroughly remove any organic residue and roughen up the surface to improve adhesion. Then, conventional photolithography was performed using Dupont Riston 4615 dry film. After the photoresist was exposed and developed, carbon ink-based PTF supplied by W.R. Grace was applied into the developed negative pattern of the resist trace. The resist material was soft-cured at 120°C for 1 h. The photoresist is then stripped, and the board fully cured at 150°C for 1 h to complete the resistor process. Both 10 ohms/sq and 10 kohms/sq resistance materials were used.

3.3. *Microvia interconnects with probe pads*

The process of acetone clean and microetch was carried out again to thoroughly clean the surface and improve the adhesion. Then, photoimageable liquid epoxy Vantico Probimer 7081 was spin-coated at 1000 rpm for 40 s to achieve a nominal thickness of 30 μm. This interlayer dielectric has a dielectric constant of 3.4 and loss of 0.015 at 1 GHz. Once the board was soft-cured at 90°C for 30 min, UV radiation of 4 J/cm^2 was exposed to pattern the microvia structures. Then the board was baked at 100°C for 1 h to fully crosslink the exposed area. GBL solvent at room temperature was used to develop the photoresist, and the board was fully cured at 160°C for 1 h. To build the vias and probing pads, conventional electroless copper plating was performed to build a thin seed layer. Probing pad pattern was developed using a conventional photolithography, and electroplating of copper

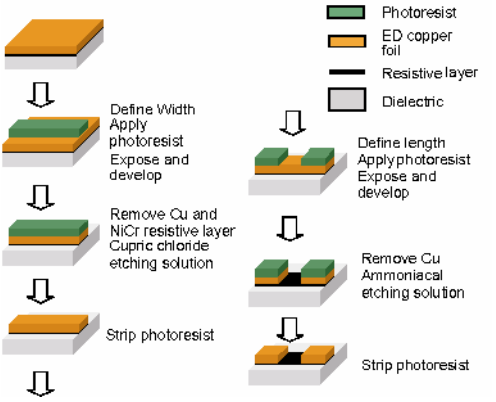

FIG. 5. Gould resistor fabrication process flow chart.

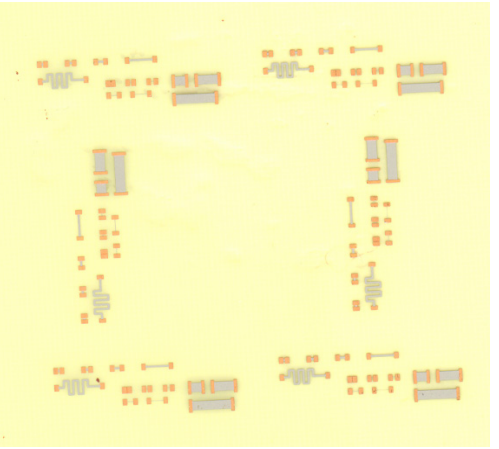

FIG. 6. Fabricated resistors using Gould process.

was performed to build the probing pads. Finally, photoresist was stripped with 3% sodium hydroxide at 55°C, and the copper seed layer was microetched to complete the process.

3.4. *Resistors by foil lamination method on epoxy dielectric*

The Gould TCR NiCrAlSi and NiCr foil resistors were selected for direct lamination experiments on TV2. This is a sputtered NiCrAlSi or NiCr thin film layer on the rough, matte surface of a copper foil. The foil is laminated with the resistor surface in contact with the dielectric. Processing of the resistor proceeds with photolithography and etching of the circuit features and resistor widths. Acidic cupric chloride was used as the first etch to remove Cu and the underneath resistor layer. A second photolithography step using ammoniacal etch chemistry was then performed to define the resistor widths by selectively removing the copper from and over the resistor material. Figure 5 shows a general overview of the Gould thin film resistor fabrication process. Figure 6 shows the fabricated resistors by the above method.

4. Electrical test measurements

Initial measurements of capacitance were made with Hewlett Packard LCR Meter (4263B) at low frequency of 100 kHz. High-frequency measurements were taken using vector net work analyzer (VNA) and 2 G-S (ground-signal) probes. The pitch of the probes is 500 μm, and locations of probes with respect to a capacitor are shown in Fig. 7. High-frequency measurement of the 10-mm-diameter circular capacitor was conducted. The capacitance was extracted by the methodology of Novak and Miller [11]. As can be seen from Fig. 8, the structure resonates at around 900 MHz and becomes inductive after this frequency. The measurements were carried out from 50 MHz to 2 GHz. The extracted capacitance is shown in Fig. 9. The value of the capacitor is 1.37 nF, and it remains relatively constant through the frequency band.

5. Reliability assessment of fabricated test vehicles

Although embedded passives are more reliable by eliminating solder joint interconnects, they are also susceptible to crack and delamination. More layers could be necessary to ac-

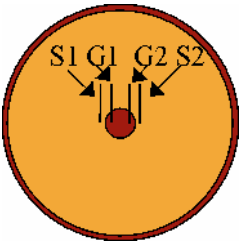

FIG. 7. Two probe locations for capacitance measurements.

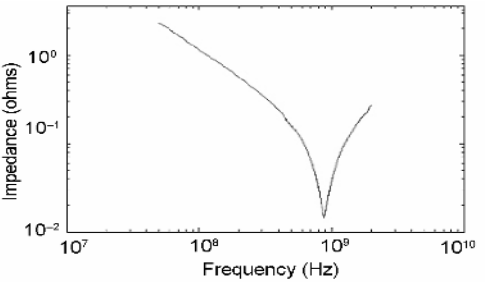

FIG. 8. Impedance profile of the capacitor.

commodate the embedded passives, and therefore, cracks and delamination are more prone to occur. Furthermore, various materials within the substrate can cause significant thermo-mechanical stress due to coefficient of thermal expansion (CTE) mismatch.

5.1. *Test conditions*

Thermal shock and constant temperature humidity tests were performed based on JEDEC standards (No. 22-A104-B and No. 22-A102-C) and others. The thermal shock conditions were –40 to 125°C and –55 to 125°C. Both have dwell time of 10 min and tested for 1000 cycles. Moreover, the constant temperature humidity test conditions were 85°C/85% RH and 121°C/100% RH for 100 h.

For TV1, which contains polymer/ceramic nanocomposite capacitors and PTF resistors, two thermal shock conditions and constant temperature and humidity condition of 85°C/85% RH were used. For TV2, which contains only NiCr foil resistors, thermal shock condition of –55 to 125°C and constant temperature and humidity condition of 121°C/100% RH were used. Table I summarizes the test conditions.

5.2. *TV1 Resistor (PTF) results*

A total of four boards were tested at various conditions. Three boards have the same resistivity of 10 ohms/sq, and the other has 10 kohms/sq. For each board, there are a total of ap-

Table I
Various reliability test conditions

Test cases	Temperature range	Soak time (min)	Humidity	Total cycles or hours
Thermal shock 1	–40 to 125°C	10	N/A	1000 cycles
Thermal shock 2	–55 to 125°C	10	N/A	1000 cycles
Temperature humidity 1	85°C	N/A	85%	100 h
Temperature humidity 2	121°C	N/A	100%	100 h

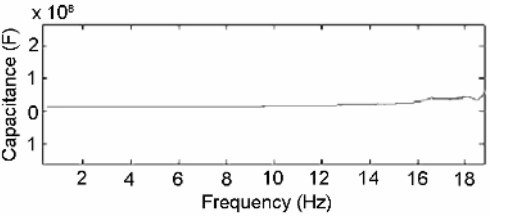

FIG. 9. Extracted capacitance of the structure.

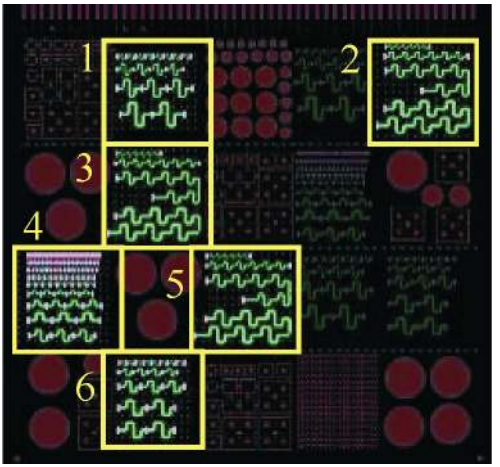

FIG. 10. TV1 resistor groups examined.

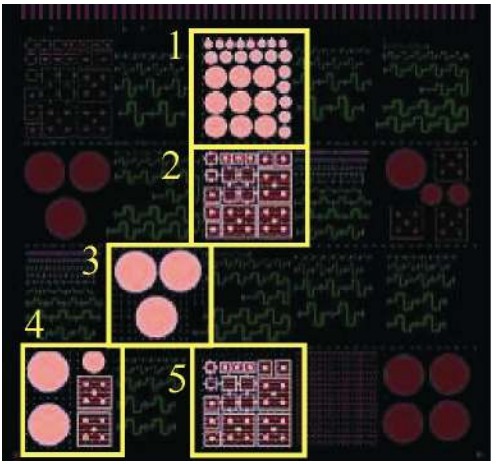

FIG. 11. TV1 capacitor groups examined.

proximately 300 resistors, and 100 resistors divided into six different groups have been examined during the tests. Figure 10 shows the graphical locations of resistor groups examined. Tables II and III summarize the results.

The measured R values of PTF resistors range from 5 to 600 ohms with 10 ohms/sq material and 5 to 400 kohms with 10 kohms/sq material based on resistor area and volume shrinkage during curing. After 1000 cycles of thermal shock, most of the resistors experienced only a slight decrease in resistance, while after 100 h of constant temperature humidity test only a slight increase was experienced. Since group 2 is relatively located further away from the center of the board than groups 3 and 5, higher thermo-mechanical stress due to CTE mismatch is exerted. Therefore, even though these groups are identical in geometry and size, group 2 experienced a slightly higher change in resistance. Moreover, harsher thermal shock condition resulted in higher magnitude of change for the same 10 ohms/sq resistors as expected. Among the examined resistors, none has failed or changed more than 6%.

Table II
TV1 Initial typical resistance range

Resistor group	Typical resistance range	
	PTF 10 ohm/sq	PTF 10 kohm/sq (k)
1	80–130	80
2	400–600	350–400
3	400–600	350–400
4	5–80	5–60
5	400–600	350–400
6	60–100	50–60

Table III
TV1 resistor results

Resistor group	PTF 10 ohms/sq			PTF 10 kohms/sq
	Thermal shock (–55 to 125°C 1000 cycles) (%)	Temperature humidity (85°C/ 85RH 100 h) (%)	Thermal shock (–40 to 125°C 1000 cycles) (%)	Thermal shock (–40 to 125°C 1000 cycles) (%)
1	–2.07	2.21	–0.91	–4.29
2	–2.19	2.22	–1.11	–4.61
3	–1.97	2.09	–1.12	–4.30
4	–3.85	3.08	–1.45	–3.74
5	–1.78	2.16	–1.06	–4.37
6	–2.15	2.36	–1.02	–4.15

5.3. *TV1 Capacitor results*

A total of five capacitor boards were tested at various conditions. For each board, there are a total of 98 capacitors; 68 of them representing various geometries, sizes, and locations have been examined. These are grouped into various geometries and sizes. Circle 1 groups the biggest and Circle 4 the smallest circular capacitors. Similarly, Square 1 groups the biggest and Square 3 the smallest square capacitors. All the measurements were taken at low frequency of 100 kHz. Figure 11 shows the graphical locations of capacitors examined. Table IV summarizes the results.

Initial values of capacitance and quality factor vary significantly in between boards due to different processing conditions. The values of capacitance range approximately from 30 to 1400 pF, and the quality factor ranges approximately from 40 to 85. After 1000 cycles of thermal shock, all the capacitors experienced decrease in capacitance, while some quality factor increased and some decreased. After 100 h of constant temperature and humidity test, capacitance slightly increased and quality factor decreased. Although some capacitors were initially shorted, none that was examined failed during the reliability tests.

Among five boards, board 3 resulted in highest average per cent change. Although it was tested at a harsher thermal shock condition than boards 1 and 2, the differences are quite dramatic especially for smaller size capacitors.

5.4. *TV2 Resistor (FOIL) results*

TV2 contains various geometries, sizes, and values of NiCr foil resistors. A total of four identical boards were tested at various conditions. For each board, approximately 100 out of 550 resistors were monitored, and most experienced only a slight increase of less than 1%. Overall, NiCr resistors show much more reliable results than PTF resistors. Among all the resistors examined, only one resistor from group T3 that was thermal-shocked became open. Figure 3 shows the rough locations of resistor groups examined. Table V summarizes the results.

6. Finite-element analysis

Finite-element models have been developed to qualitatively assess the susceptibility of failures of embedded capacitors. All the material properties and important dimensional parameters are parametric, and thus, they can be changed easily to analyze other materials or different geometric dimensions. Four different cases are compared based on the copper-probing geometries and planar dimensions. Probing pads are either located in the center or at the edge as shown in Fig 12. The main geometric shape difference between them is that center probe has a hole on the center of top electrode while the edge probe has extended bottom electrode. Also, two planar dimensions of 2 and 4 mm are modeled.

Two-dimensional plane elements have been used to analyze the sequential build-up (SBU) process and the thermo-mechanical electrostatic performance of embedded capacitors. Due to complex substrate structure, some of the minor geometric features including vias and probing pads are neglected. Figure 13 shows the center-probe finite-element model with the boundary conditions. Since the capacitor is symmetric, only half of the capacitor was modeled.

Table IV
TV1 capacitor results

Capacitor group	Average initial capacitance at 100 kHz (pF)	Average % change	Average initial Q-factor at 100 kHz	Average % change
Board 1: Thermal shock (–40 to 125°C 1000 cycles)				
Circle 1	1050	–1.79	52	52.49
Circle 2	269	–2.20	46	49.83
Circle 3	73	–2.67	44	26.89
Circle 4	70	–2.74	44	27.98
Square 1	997	–1.90	51	42.07
Square 2	187	–2.05	46	30.70
Square 3	49	–3.15	42	25.68
Board 2: Thermal shock (–40 to 125°C 1000 cycles)				
Circle 1	1188	–1.92	50	43.78
Circle 2	357	–2.62	46	34.94
Circle 3	129	–2.62	40	22.04
Circle 4	111	–2.66	41	22.57
Square 1	1043	–2.18	48	33.80
Square 2	239	–2.84	43	27.99
Square 3	73	–3.00	39	19.95
Board 3: Thermal Shock (–55 to 125°C 1000 cycles)				
Circle 1	613	–2.09	61	42.50
Circle 2	149	–8.88	45	65.44
Circle 3	61	–20.22	38	102.20
Circle 4	54	–22.78	37	103.47
Square 1	432	–3.50	55	49.73
Square 2	93	–13.37	43	74.84
Square 3	48	–24.66	38	99.14
Board 4: Thermal shock (–55 to 125°C 1000 cycles)				
Circle 1	1404	–3.74	85	–25.61
Circle 2	376	–4.50	72	–24.96
Circle 3	131	–6.62	59	–29.01
Circle 4	107	–7.98	60	–26.97
Square 1	1032	–3.38	77	–28.02
Square 2	200	–5.26	66	–27.69
Square 3	91	–9.88	58	–27.38
Board 5: Constant temperature humidity (85°C/85% RH 100 h)				
Circle 1	534	2.10	66	–24.77
Circle 2	131	3.95	54	–21.11
Circle 3	46	0.68	54	–16.50
Circle 4	40	1.18	55	–18.71
Square 1	358	4.03	58	–21.24
Square 2	72	1.09	52	–14.84
Square 3	30	0.61	50	–9.88

Table V
Summary of TV2 resistor results

Resistor group	NiCr foil		
	Typical resistor range (ohms)	Thermal shock (–55 to 125°C/1000 cycles) (%)	Temperature humidity (121°C/100% RH 100 h) (%)
T1	~20	0.43	0.38
T2	~100	0.07	0.08
T3	~75	0.06	0.05
T4	~1 k	0.04	0.09
T5	~3 k	0.38	0.84
T6	~9 k	0.41	0.69
M1	20–100	0.21	0.07
M2	70–100	0.06	0.08
M3	~9 k	0.30	0.70
B1	~60	0.31	0.52
B2	~100	0.30	0.53
B3	5–10	0.51	0.68
B4	~15	0.07	0.72

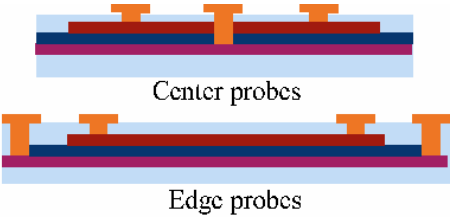

FIG. 12. Side view of different probe locations.

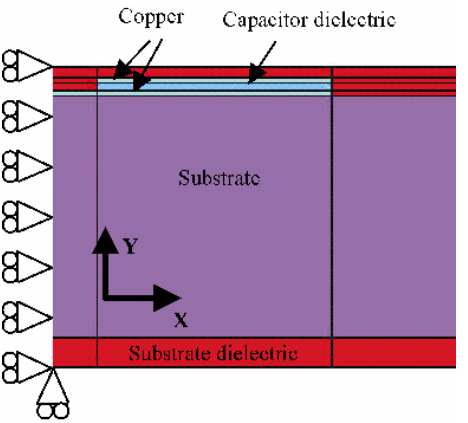

FIG. 13. Center probe capacitor model.

To apply this boundary condition, the nodes on the left edge are constrained in the x direction. In addition, the bottom left node is fully constrained to prevent any rigid body motion.

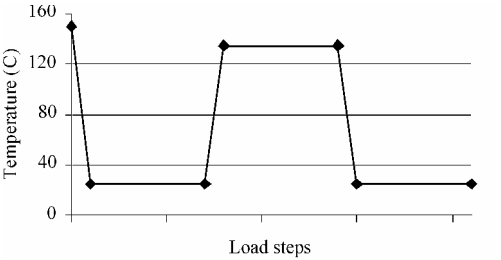

FIG. 14. Thermal load profile.

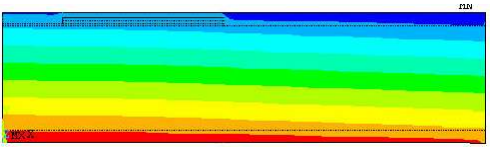

FIG. 15. Warpage results for 2-mm center probe.

6.1. *Material models*

The four materials used for the numerical models are the base substrate, the capacitor dielectric, the copper electrodes, and the build-up dielectric. The base substrate is Driclad from EI. It is a high *T*g FR4 with dielectric constant of 3.9 and dielectric loss of 0.014 [12]. This material is modeled as orthotropic and temperature independent. The capacitor dielectric is a mixture of polymer and nano-particles to achieve high dielectric constant and stable mechanical and electrical properties. This material is modeled as linear isotropic and temperature dependent. The copper electrodes are modeled as linear isotropic and temperature independent. The plastic behaviour of copper was modeled with a multilinear kinematic hardening relationship [13]. Finally, the substrate dielectric is modeled as linear viscoelastic using Prony Series [14].

6.2. *Process model*

During the SBU process, each layer is created at different process conditions. Some materials require higher curing temperature than others, and thus the substrate experiences various thermal loads during the fabrication. Therefore, the SBU process was modeled using element birth and death feature in ANSYS^{TM} to represent the addition of different materials at different thermal conditions as shown in Fig. 14.

Finite-element analysis focused on several thermo-mechanical results: warpage, axial stress, von Mises stress, and interfacial stress. Axial stresses and von Mises stresses were used as damage metric for crack growth, and interfacial stresses were used as damage metric for interfacial delamination. Figures 15–17 show typical warpage and stress distributions based on 2-mm center-probe capacitors, and Figs 18–20 compare the results.

The warpage results are based on the y-component relative displacement. Since warpage is dependent on the length of the board, 2- and 4-mm capacitors should not be compared directly. For 2-mm capacitors, edge probe geometry shows three times higher warpage than the center probe due to higher copper content. The 4-mm capacitors also show similar trend of higher warpage on edge probe.

Stress results are based on the maximum stress observed. For all four cases, maximum stresses occurred between the copper and capacitor dielectric layers and at the edge of the capacitor. As shown in Fig. 19, the size or probe location does not seem to affect the crack growth. All four cases show similar axial stresses of 21 MPa and von Mises stresses of

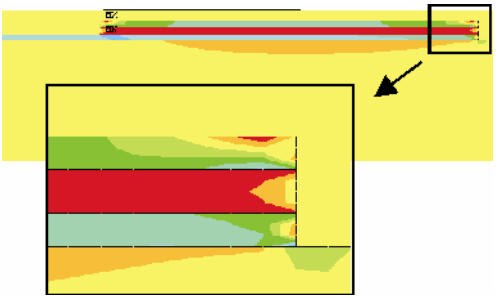

FIG. 16. Axial stress contour for 2-mm center probe.

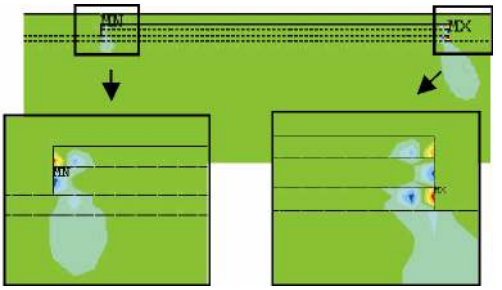

FIG. 17. Interfacial stress contour for 2-mm center probe.

23.5 MPa. In terms of interfacial delamination, size of capacitors does not seem to affect the results; however, center probes show approximately 11% higher interfacial stresses than edge probes. Qualitatively, center-probe connectors are more prone to delamination. Also, sizes or probe locations do not play a significant role in crack propagation.

6.3. *Thermo-mechanical electrostatic analysis*

Thermo-mechanical electrostatic analysis was performed to understand the thermo-mechanical behaviour and their effects on the embedded capacitors. It is essentially a two-step process. First, thermo-mechanical analysis is performed to investigate the deformation of the capacitor, and then its displacement boundary condition is transferred to electrostatic analysis to investigate its effect on the capacitance [15]. The temperature range of thermal cycling is –40 to 125°C.

The theoretical value of capacitance is calculated by eqn (2).

$$C = \frac{\varepsilon_r A}{t}, \tag{2}$$

where C is capacitance, ε_r, the relative permeability of dielectric, A, the area of effective capacitor electrodes, and t, the thickness of dielectric. Although theoretical capacitances are very similar to the simulated results, all four cases show slightly higher simulation results as shown in Table VI. This is due to the extra area of capacitor electrodes that is not considered in the theoretical calculations. The small tab of extension on the edge probe capacitors and the via areas of center probes store electrical charge and contribute to the capacitance calcula-

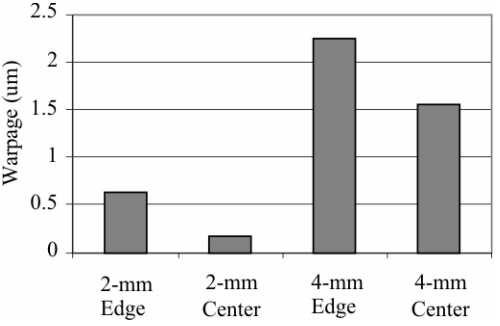

FIG. 18. Warpage results.

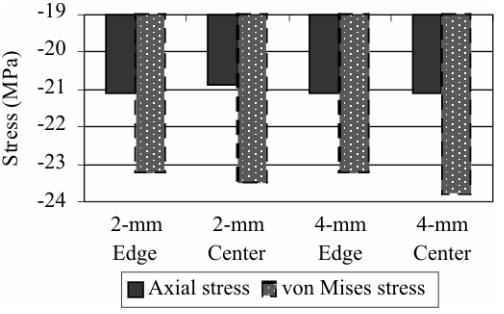

FIG. 19. Axial and von Mises stress results.

Table VI
Effects of thermo-mechanical deformation

Test cases	Theoretical capacity (pF)	Simulation before cycling (pF)	Simulation after cycling (pF)	% change
2-mm edge	19.48	19.55	19.60	0.26
2-mm center	12.73	12.84	12.87	0.23
4-mm edge	77.92	78.06	78.26	0.26
4-mm center	63.31	63.52	63.69	0.27

Table VII
Embedded resistor reliability test results

	Test condition	Average % change
PTF 10 ohms/sq	TC –55 to 125°C	–2.92
PTF 10 ohms/sq	HAST 85/85	2.12
PTF 10 ohms/sq	TC –40 to 125°C	–1.24
PTF 10 kohms/sq	TC –40 to 125°C	3.99
NiCr	TC –55 to 125°C	0.16
NiCr	121°C/100 RH	0.81

tion. Overall, there is only a very small change in the capacitance after thermal cycling simulation. The per cent change is much smaller than the experimental results. This is most likely due to inadequate material models. The results are only based on the thermo-mechanical deformation, and any material degradation is not considered since such models were not available. Inclusion of change in dielectric constant due to thermal cycling should give more accurate results.

7. Conclusion

Embedded passives have been designed successfully and fabricated onto multilayered microvia organic substrate using low-temperature processes. Their unique design with microvia interconnects and integration of multiple materials mimic SOP concept of package as a system to integrate digital, RF, optical, and sensor functions. High-frequency measurement showed polymer/ceramic nanocomposite capacitor performing up to 900 MHz without resonance. Furthermore, extensive reliability tests based on JEDEC standards were per-

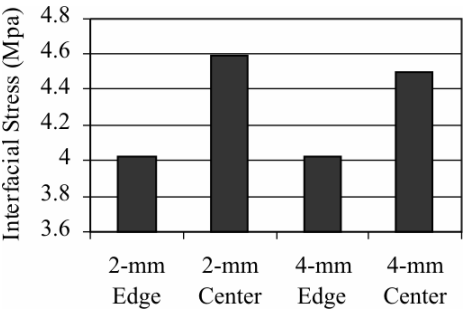

FIG. 20. Interfacial stress results.

Table VIII
Embedded capacitor reliability test results

Capacitor	Test condition	Average % change in capacitance	Average % change in Q-factor at 100 kHz (%)
Board 1	TC –40 to 125	–2.38%	35.18
Board 2	TC –40 to 125	–2.67%	28.39
Board 3	TC –55 to 125	–6.09%	–27.06
Board 4	TC –55 to 125	–14.73%	78.85
Board 5	HAST 85/85	2.04%	–18.20

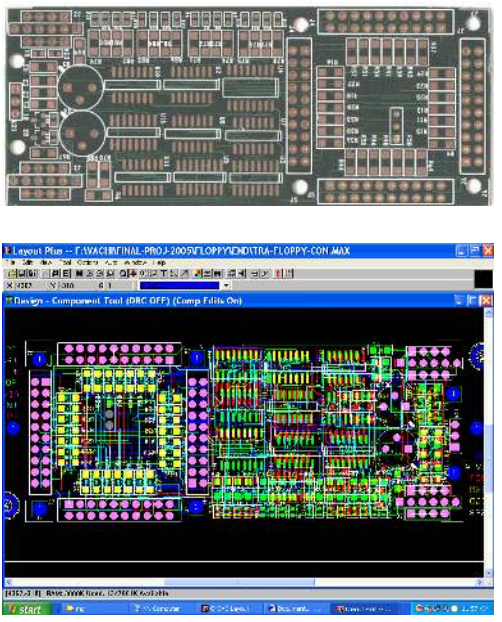

FIG. 21. Product miniaturization with embedded R.

formed. Both PTF and NiCr foil resistors show stable results; however, some capacitor boards show significant change in capacitance and quality factors (Tables VII and VIII). Future work will include evaluation of the effect of accelerated reliability assessments on high frequency behavior of polymer/ceramic embedded capacitors and electroless NiP alloys for resistors.

In addition, we have realized working prototype boards (low-frequency mixed signal circuit for traffic signal control application) using embedded R and C. The PWB design for this purpose is fully loaded with fine-pitch SMD components and uses microvias to interconnect electrical layers. The focus is to achieve miniaturization. As a first step, by eliminating all SMD resistors on the board and designing them as embedded components, a reduction in board size of up to 40% has been achieved. Further reduction employing embedded C will be the ultimate target. The finished prototype functional board is shown in Fig. 21.

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References

1. Rao R. Tummala, *Fundamentals of microsystems packaging*, McGraw-Hill (2001).
2. R. Ulrich, and L. Schaper, (eds), *Integrated passive component technology*, IEEE Press/Wiley (2003).
3. R. Ulrich, Embedded resistors and capacitors for organic-based SOP, *IEEE Trans. Advanced Packaging*, **27**, 326–331 (2004).
4. D. Balaraman, J. Choi, V. Patel, P. M. Raj, I. R. Abothu, S. Bhattacharya, L. Wan, M. Swaminathan, and R. R. Tummala, Simultaneous switching noise suppression using hydrothermal barium titanate thin film capacitor, *54th Electronic Components and Technology Conf.*, IEEE-CPMT and EIA, Las Vegas, NV, pp. 282–288 (2004).
5. M. Damani, R. V. Pucha, S. Bhattacharya, R. R. Tummala, and S. K. Sitaraman, Physics-based reliability assessment of embedded passives, *54th Electronic Components and Technology Conf.*, IEEE-CPMT and EIA, Las Vegas, NV, pp. 2027–2031 (2004).
6. iNEMI website, http://www.inemi.org.
7. K. J. Lee, Swapan Bhattacharya, Mahesh Varadarajan, Lixi Wan, Isaac Robin Abothu, Venky Sundaram, Prathap Muthana, Devarajan Balaraman, P. M. Raj, Madhavan Swaminathan, Suresh Sitaraman, Rao Tummala, Puligandla Viswanadham, Steven Dunford, and John Lauffer, Reliability assessment of embedded passives on multilayered microvia organic substrates, *IEEE-CPMT Int. Symp. and Exhibition on Advanced Packaging Materials,* Irvine, CA, USA, March 16–18, 2005.

8. I. Koiwa, M. Usada, and T. Osaka, Effect of heat-treatment on the structure and resistivity of electroless Ni–W–P alloy films, *J. Electrochem. Soc*., **135**, 1222–1228 (1988).
9. H. Aoki, Study of mass production of low ohm metal film resistors prepared by electroless plating, *IEICE Trans.*, **E-74**, 2049–2054 (1991).
10. H. Sawai, T. Kanamori, I. Koiwa, S. Shibata, K. Nihei, and T. Osaka, A study on the low energy consumption thermal head using electroless Ni-W-P alloy films as heating resistors, *J. Electrochem. Soc*., **137**, 3653–3659 (1990).
11. I. Novak, and J. R. Miller, Frequency-dependent characterization of bulk and ceramic bypass capacitors, Poster material, *12th Topical Meeting on Electrical Performance of Electronic Packaging*, Princeton, NJ, USA, October 2003.
12. Endicott Interconnect Technology Inc. website, http://www.endicottinterconnect.com
13. R. Iannuzzelli, Predicting plated-through-hole reliability in high-temperature manufacturing process, *Proc. 41st Electronics Components and Technology Conf*., Atlanta, GA, USA, 1991, pp. 410–421.
14. G. Ramakrishna, F. Liu, and S. K. Sitaraman, Experimental and numerical investigation of microvia reliability, *The Eighth Intersociety Conf. on Thermal and Thermo-mechanical Phenomena in Electronic Systems*, ITHERM'2002, IEEE-CPMT, ASME, and IMAPS, San Diego, CA, pp. 932–939 (2002).
15. Y. Rao, J. Qu, and C. P. Wong, RF electrical simulation of embedded capacitor, *Proc. IEEE-CPMT Int. Symp. and Exhibition on Advanced Packaging Materials*, Braselton, GA, pp. 286–292, March 11–14, 2001 (2001).