Printed, Sub-3V Digital Circuits on Plastic from Aqueous Carbon Nanotube Inks

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ABSTRACT Printing electronic components on plastic foils with functional liquid inks is an attractive approach for achieving flexible and low-cost circuitry for applications such as bendable displays and large-area sensors. The challenges for printed electronics, however, include characteristically slow switching frequencies and associated high supply voltages, which together impede widespread application. Combining printable high-capacitance dielectrics with printable high-mobility semiconductors could potentially solve these problems. Here we demonstrate fast, flexible digital circuits based on semiconducting carbon nanotube (CNT) networks and high-capacitance ion gel gate dielectrics, which were patterned by jet printing of liquid inks. Ion gel-gated CNT thin-film transistors (TFTs) with 50 μm channel lengths display ambipolar transport with electron and hole mobilities >20 cm^2/V · s; these devices form the basis of printed inverters, NAND gates, and ring oscillators on both polyimide and SiO_2 substrates. Five-stage ring oscillators achieve frequencies >2 kHz at supply voltages of 2.5 V, corresponding to stage delay times of 50 μs. This performance represents a substantial improvement for printed circuitry fabricated from functional liquid inks.

KEYWORDS: carbon nanotube · printed electronics · flexible electronics · thin-film transistor · ion gel · ambipolar · delay time

Expanding applications for microelectronics in large-area sensor arrays, disposable sensor tapes, time−temperature smart labels, radio frequency identification tags, and roll-up displays[1−4] motivate efforts to integrate electronics onto flexible plastic, paper, or metal substrates. A principal strategy for achieving flexible electronics is to employ graphic arts methods such as flexographic or ink-jet printing to pattern metallic, semiconducting, and insulating inks onto foils and paper.[5−10] Liquid phase printing offers the potential for high-throughput roll-to-roll or sheet-to-sheet processing of electronics on large-area substrates, facilitating applications where large areas are necessary (*e.g.*, displays) and also potentially translating into low production cost. Yet the challenge for printed electronics is to achieve high-performance circuits. The inherently low carrier mobilities of many printable organic or nanoparticle-based semiconductors lead to reduced transistor switching frequencies and high circuit supply voltages. Alternative strategies in which silicon chips are bonded to flexible substrates (by transfer printing or pick-and-place methods) are also attractive because they benefit from the superior electronic properties of silicon and the very advanced state of silicon microelectronics technology.[11] In a competitive environment, the success of liquid phase printed electronics depends on substantial performance improvements, in particular, the development of faster, lower power printed circuits.

Figure 1a displays a summary of reported signal delay times *versus* supply voltages for ring oscillator circuits based on organic semiconductors and carbon nanotube (CNT) arrays. It is evident that for *nonprinted* organic ring oscillators (open blue symbols) signal delays of 1−10 μs have been achieved but only for supply voltages of 10−100 V,[12−24] while for supply voltages in the range of 4−10 V, the delay is above 10 μs for the fastest circuits, with most displaying >1 ms switching times.[25−28] Reports of *printed* ring oscillators are less common (solid green symbols in Figure 1a), and these circuits have generally required tens of volts to achieve switching times on the order of 1 ms.[29−32] Such large voltages are not practical for many potential applications of flexible electronics where power will be supplied by thin-film batteries or radio frequency fields. Very recently, unipolar, p-type electrolyte-gated ring oscillator circuits have been demonstrated that indeed operate at very low

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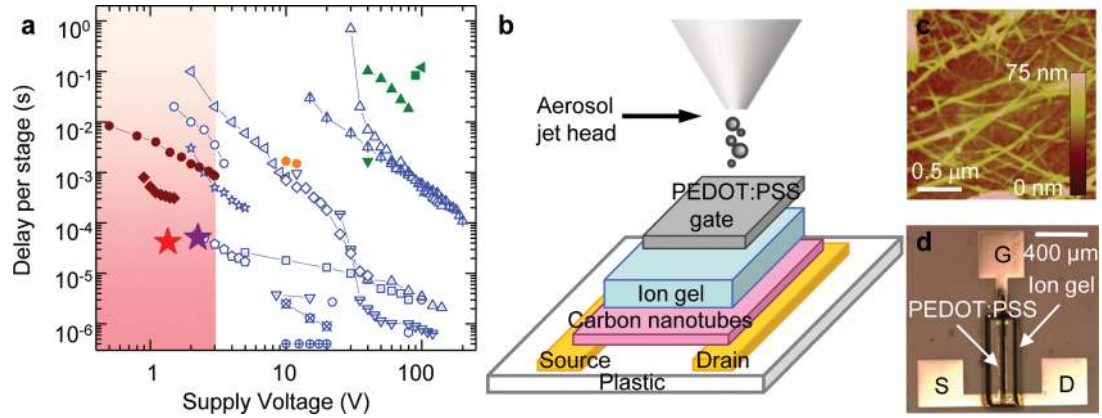

Figure 1. Printed carbon nanotube transistors and circuits. (a) Summary of literature results for signal delay times per stage *versus* supply voltages for ring oscillators based on organic semiconductors or carbon nanotube networks. Conventionally fabricated (nonprinted) organic circuit delays are displayed as open blue symbols;[12−28] solid green symbols represent results for printed ring oscillators;[29−32] electrolyte-gated organic circuits are shown in solid brown;[33,34] and previous results for a printed CNT thin-film ring oscillator are shown in orange.[35] The results in this paper are represented by the purple (on plastic substrate) and red stars (on SiO_2 substrate). Pink shaded area indicates the desired regime with low supply voltage and short delay. (b) Schematic sketch of aerosol jet printing of a CNT TFT. The CNT network, ion gel dielectric, and conducting polymer gate electrode (PEDOT:PSS) are printed sequentially from liquid inks. The Au source and drain electrodes were patterned by photolithography. (c) AFM topography image of the printed CNT network on polyimide. (d) Optical image of a printed ion gel-gated CNT TFT on polyimide substrate.

supply voltages (brown symbols), but the shortest delay times were 200 μs for devices with rather short (2.5 μm) channel lengths.[33,34] Thus, a major challenge for printed electronics is to develop inks and printing methodologies that allow shorter delay times at low supply voltages, that is, to move further into the pink shaded region of Figure 1a.

Single semiconducting carbon nanotubes are known to exhibit very high intrinsic mobility (~100 000 $cm^2/V \cdot s$)[36] and consequently can be incorporated in high-frequency (short delay time) devices.[37] Yet the difficulties associated with circuit fabrication based on single CNTs have hindered their wide application. To overcome this, CNT thin films deposited from solution or by dry transfer printing process have become attractive alternatives.[35,38−43]

Here we report printed digital carbon nanotube (CNT) circuits on flexible plastic and rigid SiO_2 substrates that operate at sub-3V supply voltages with signal delays as short as 50 μs per stage (stars in Figure 1a). These circuits are printed using a high-performance aqueous CNT ink in which 98% of the tubes are semiconducting (*i.e.*, the fraction of metallic tubes is ~2%).[44] This high-purity ink ensures that good ON/OFF current ratios are achieved easily for printed CNT transistors without subsequent processing or chemical treatment to eliminate metallic tubes. Furthermore, the printed CNT networks are intrinsically ambipolar and exhibit effective mobilities of both holes and electrons in the range of 20−50 $cm^2/V \cdot s$ depending on the printing conditions. The mobilities are comparable to or better than that of CNT networks fabricated by other methods.[35,39−43,45−47] Ambipolar operation in turn allows fabrication of complementary-like logic circuits,[16,46,48,49] which is desirable from a circuit design perspective.

Key to achieving low-voltage CNT TFTs is the use of a high-capacitance gel electrolyte dielectric that we have described previously.[33,50] The combination of high-purity, high-mobility semiconducting CNT networks and high capacitance ion gel dielectrics affords the fastest and lowest voltage jet-printed electronic circuits to date.

RESULTS AND DISCUSSION

Device Fabrication. Figure 1b shows the device structure and the printing process. The TFT channels were 50 μm in length and 500 μm in width as defined by lift-off Au electrodes prefabricated on plastic or SiO_2/Si substrates. The CNT channel and subsequent layers were printed sequentially using aerosol jet printing[50] (see Methods). From the atomic force microscopy (AFM) topographic image in Figure 1c, it is evident that the printed CNTs formed a distributed random network. The coverage of nanotubes can be tuned by varying the concentration of the aqueous CNT ink and printing speed. We found that an apparent surface coverage of ~30% CNTs, as assessed by AFM, yielded optimized ON/OFF current ratios in the resulting TFTs. After printing the CNT layer, the high capacitance ion gel dielectric ink was printed over the channel. Evaporation of the ethyl acetate solvent resulted in an ionically conducting, electronically insulating gel electrolyte with an elastic modulus of ~10 kPa. To finish the device, a layer of conducting polymer poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate) (PEDOT:PSS) was printed on top of the gel to form the gate electrode. A photomicrograph of a completed CNT TFT on polyimide is shown in Figure 1d.

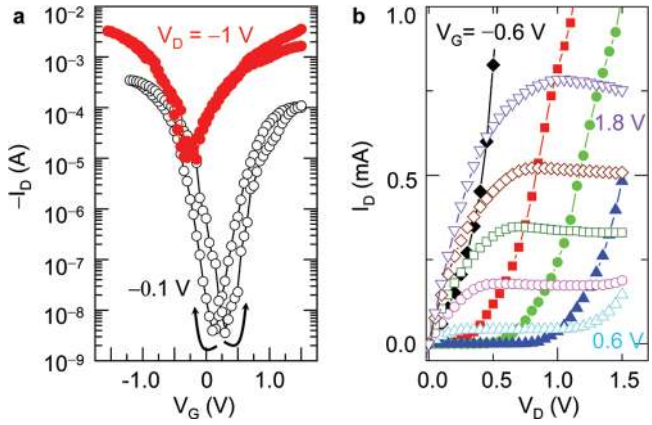

Figure 2. Electrical characterization of ion gel-gated CNT TFTs showing ambipolar transport. (a) Transfer characteristics of a TFT (channel width = 500 μm, length = 50 μm) printed on polyimide substrate at $V_D = -1$ V (red solid circles) and at $V_D = -0.1$ V (black open circles). The linear mobility obtained from the black curve is $\mu_h \sim 20$ cm^2/V · s (hole), $\mu_e \sim 30$ cm^2/V · s (electron). The subthreshold swing is 130 mV/decade. The ON/OFF current ratio is above 10^4 at $V_D = -0.1$ V. (b) Output characteristics showing both n- (open symbols) and p-type transport (solid symbols) at $V_G = -0.6$ V (black), -0.3 V (red), 0 V (green), 0.3 V (blue), 0.6 V (light blue), 0.9 V (pink), 1.2 V (dark green), 1.5 V (brown), 1.8 V (purple).

Transistor Performance. The electrical properties of printed CNT transistors were tested in vacuum (10^{-6} Torr). Clear ambipolar behavior can be seen from the transfer curves shown in Figure 2a. The ON/OFF current ratio is above 10^4 at $V_D = -0.1$ V for this device with a subthreshold swing of 130 mV/decade. The effective mobilities of holes and electrons are 30 and 20 cm^2/V · s, respectively, for an estimated 10 μF/cm^2 gate sheet capacitance.[50] It should be noted, however, that the quantum capacitance of carbon nanotubes (10^{-10} F/m)[51] is on the order of several μF/cm^2 if the CNT coverage is ~50%. For CNT TFTs gated with a high-capacitance dielectric such as the ion gel, the quantum capacitance may be smaller than the dielectric capacitance; if this is the case, the quantum capacitance will dominate and thus the effective mobilities will be larger than our estimation. The typical output characteristics ($I_D - V_D$), as shown in Figure 2b, also indicate ambipolar behavior. For $V_G > 0.6$ V, the output characteristics show clear linear and saturation regimes typical of n-type (electron) transport. For $V_G < 0.6$ V, the transistor exhibits p-type transport in which holes are injected from the drain electrode. The ambipolar behavior of the CNT networks indicates that the injection of both electrons and holes is facile from the high work function Au source and drain contacts, which may result from enhancement of the electric fields at the electrode/CNT interfaces due to the presence of electrolyte.[45,52,53]

Table 1 displays the statistics for key device parameters (ON/OFF current ratio, mobility, conductance, and threshold voltage) based on 28 printed CNT TFTs on polyimide substrates, as well as 50 CNT TFTs printed on SiO_2 substrates (Supporting Information, Figures S1 and S2). The transistors had either high (~60%) or low (~30%) CNT coverages as determined by the printing conditions (see Methods). Film coverage refers to the tube density as assessed by AFM. On plastic substrates, we report the results for high-coverage films (which were employed for the results in the rest of this article) and low-coverage films separately to demonstrate how the network density affects the transistor performance. The general observation is that the ON/OFF current ratio is significantly greater for low-density films than for high-density films, presumably because of the presence of metallic CNT impurities that raise the OFF current.[54] With a low network density, a metallic CNT "short" is less likely. Likewise, the mobility appears larger for the high-density CNT film, which again may reflect the influence of metallic impurities that effectively shorten the channel.

Circuit Performance. Realization of ambipolar CNT transistors allows the development of complementary-like, digital-printed circuits.[46,55] The most basic circuit unit, the inverter, can be achieved by combining two identical ambipolar transistors together, as shown in the inset of Figure 3a. At a given supply (V_{DD}) and input voltage (V_{IN}), transistors ***a*** and ***b*** will work under different bias conditions. When V_{IN} is "low" (*e.g.*, 0 V), transistor ***a*** operates in a strong p-type regime (lower resistance) while transistor ***b*** works in a weak p-type regime (higher resistance). Thus, the output voltage (V_{OUT}) will be

TABLE 1. Key Parameters of Transistors Printed on Flexible Polyimide and on SiO_2 Substrates[a]

		I_{ON}/I_{OFF}	μ (cm^2/V · s)	g (ms/mm)	V_{TH} (V)
high-density films on polyimide substrate	hole transport	$(2.7 \pm 0.9) \times 10^3$	31 ± 9	5 ± 1	-0.62 ± 0.03
	electron transport	$(1.8 \pm 0.7) \times 10^3$	17 ± 3	7 ± 1	0.50 ± 0.08
low-density films on polyimide substrate	hole transport	$(3 \pm 2) \times 10^5$	9 ± 4	1.3 ± 0.6	-0.53 ± 0.04
	electron transport	$(2 \pm 1) \times 10^5$	3 ± 1	1.1 ± 0.5	0.66 ± 0.08
high-density films on SiO_2 substrate	hole transport	3×10^3	50 ± 17	7 ± 4	-0.5 ± 0.1
	electron transport	3×10^3	40 ± 15	8 ± 4	0.8 ± 0.1

[a]Results on polyimide are reported for high-density (~60% network coverage) and low-density (~30% coverage) CNT films. The high-density film data are based on 11 TFTs, and the low CNT density film results are based on 17 TFTs. For SiO_2 substrates, the data are based on 50 TFTs. All of the values are acquired with $V_D = -0.1$ V. The ON/OFF current ratios (I_{ON}/I_{OFF}), mobilities ($\mu = (dI_D/dV_G)(1/C_iV_D)(L/W)$), and the normalized conductances ($g = I_D/V_DW$) are obtained at $V_G \sim 1$ V (holes) and $V_G \sim +1.5$ V (electrons).

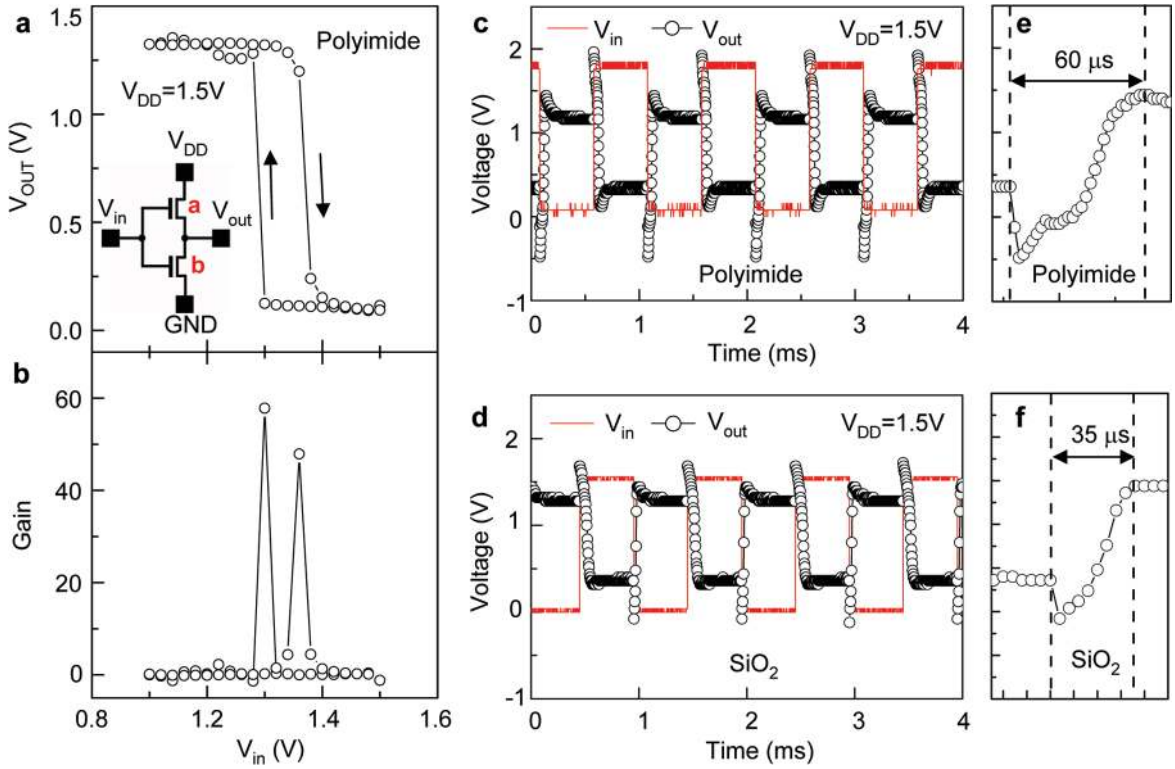

Figure 3. Electrical characterization of printed complementary-like inverters based on ambipolar ion gel-gated CNT transistors. (a) Input−output characteristics of a CNT inverter printed on polyimide substrate. The inset shows the circuit diagram of the inverter based on two identical ambipolar CNT TFTs. (b) Maximum inverter gain is 58 at V_{DD} = 1.5 V. (c) Dynamic response of an inverter on polyimide substrate acquired with V_{DD} = 1.5 V. The output voltage (open circles) tracks the 1 kHz square signal (red), which ranges from 0 to 1.8 V. (d) Inverter printed on SiO_2 substrate, where input voltage ranges from 0 to 1.6 V, with V_{DD} = 1.5 V. The rising time of the inverter is 60 μs on polyimide substrate (e) and 35 μs on SiO_2 substrate (f).

"high" (close to V_{DD} as shown in Figure 3a). On the other hand, when V_{IN} is "high" (*e.g.*, 1.5 V), transistor ***a*** operates in a weak n-type regime and transistor ***b*** works in a strong n-type regime, such that V_{OUT} is low. The ambipolar nature of CNT TFTs means that the switching mechanism of CNT inverters is different from the classic silicon complementary (CMOS) inverter in which only one of the two transistors turns ON and the other remains in the OFF state. It is therefore better to describe the CNT inverters as "complementary-like" instead of "complementary".[13,14] A more detailed discussion of the ambipolar inverter operation and power dissipation is included in Supporting Information (Figure S3).

The input−output voltage characteristics of a typical printed CNT inverter on polyimide (Figure 3a) demonstrate that the output swing reached 1.2 V (80% V_{DD}) for V_{DD} = 1.5 V. The inverter switched sharply at the threshold voltage and achieved a gain as high as 58 (Figure 3b), which is higher than that of previously reported inverters based on CNT films[43,46,56] and other printed organic semiconductors. The hysteresis between the forward and backward sweeps is likely related to hysteresis in the TFT transfer curve (Figure 2a). Figure 3c,d shows the dynamic responses of inverters printed on polyimide and SiO_2 substrates, respectively. For a 1 kHz input square-wave signal, the output swing reached ~1 V for V_{DD} = 1.5 V for inverters on polyimide and SiO_2. The best inverter on polyimide functioned well at 5 kHz, and the best device on SiO_2 tracked a 50 kHz signal (Figure S4, Supporting Information).

The rise time of the inverter on plastic is 60 μs (Figure 3e), while on SiO_2 it is 35 μs (Figure 3f). The overshoot peaks in Figure 3c,d, which may limit the highest working frequency of CNT inverters, derive from parasitic (or "overlap") capacitance. Parasitic capacitance is a particularly important issue for electrolyte-gated transistors because the capacitance of electrolytes is so large.[33,50] Its origin is the capacitive coupling of the gate to source and drain electrodes, which causes momentary current spikes when the voltage on the gate electrode is switched suddenly. To reduce these effects, the electrolyte/metal interfacial capacitance must be minimized. We return to this point below.

We also tested the operational stability of the printed CNT inverter at 100 Hz input frequency (Figure S5, Supporting Information). After 10 min of operation, the output voltage did not detectably decrease, but the transfer (I_D−V_G) characteristics of the individual TFTs revealed a 10-fold decrease of both the ON and OFF currents, reflecting an overall resistance increase. The consequences of the increased device resistance are not evident in the inverter operating at 100 Hz but do appear in the output of ring oscillators as described here.

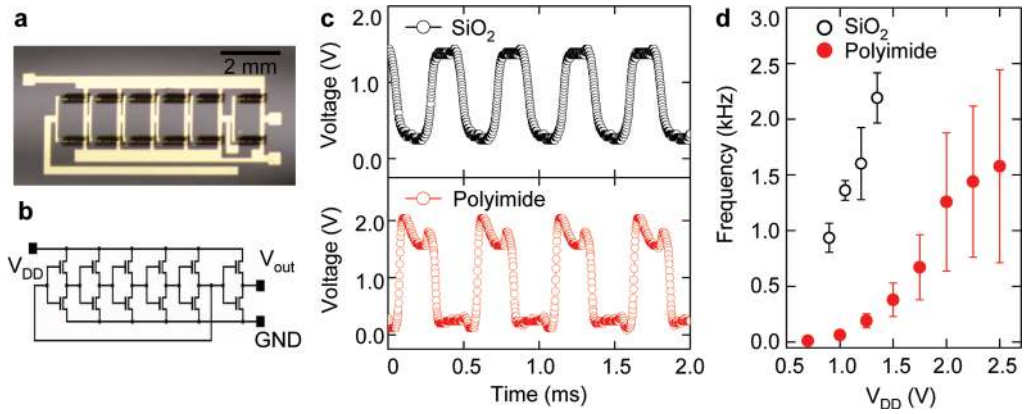

Figure 4. Five-stage ion gel-gated complementary-like CNT ring oscillator with output buffer. (a) Photomicrograph of a printed ring oscillator on polyimide substrate. (b) Circuit diagram of the device. (c) Top panel shows the output characteristics of a device printed on SiO_2 substrate with 2.3 kHz oscillation frequency at $V_{DD} = 1.5$ V; bottom panel shows the response of a device printed on polyimide substrate with 1.9 kHz oscillation frequency at $V_{DD} = 2.5$ V. (d) Output frequency as a function of V_{DD} of devices on polyimide (red solid circles) and SiO_2 (black open circles). Error bars represent one standard deviation.

Figure 4a,b displays the optical micrographs and circuit layout of a five-stage, printed CNT TFT ring oscillator. As soon as the supply voltage V_{DD} reached a critical value (~0.5 −1 V), spontaneous oscillation of the output signal commenced, as observed in Figure 4c. The oscillation frequency is 2.3 and 1.9 kHz on SiO_2 and polyimide substrates, respectively. There is some signal distortion for the oscillator on plastic because of parasitic capacitance. The parasitic capacitance is estimated to be 22% of the total capacitance (see Supporting Information, Figure S6) and is more pronounced for oscillators on polyimide because the substrates and thus the metal electrodes are rougher, meaning there is more contact area associated with the metal/electrolyte interfaces. We have investigated the use of self-assembled monolayer (SAM) coatings on the Au source and drain electrodes to minimize capacitance effects (Figure S7, Supporting Information). It is clear that thiol SAMs (either hexadecane thiol or anthracene thiol) improve the ring oscillator output, and thus these SAMs were used to treat electrodes in all of the devices reported here (see Methods).

On both plastic and SiO_2 substrates, the output frequencies increase with V_{DD}, as expected (Figure 4d). However, the oscillation frequency of ring oscillators on plastic is generally lower than on SiO_2. This is likely due to the somewhat lower mobility (Table 1) and the higher parasitic capacitance, which both can increase the RC time constant of the individual stages. The best devices on plastic and SiO_2 achieved frequencies above 2 kHz at 2.5 V supply voltage. The delay time for a single stage of the oscillator, $t_D = 1/2Nf$, where N is the number of stages and f is the frequency, is 53 μs for the fastest device on plastic and 42 μs for the fastest on SiO_2. These stage delays are a significant improvement over previous reports, as shown in Figure 1a.

The time stability of the ring oscillators on plastic were also tested (Figure S8, Supporting Information). After 30 min of continuous operation, the output frequency decreased by 90% for ring oscillators on polyimide. The decrease of the oscillating frequency can be explained by the 10-fold increase in resistance of the individual stages as was observed in our investigation of discrete inverters (Figure S4). Probably the cause for the resistance increase is "burn out" of metallic tube shorts in the network. Higher purity CNT inks will mitigate this issue and enhance stability. The time stability of CNT ring oscillator circuits is currently an ongoing area of investigation. Nevertheless, the speed of the printed CNT ring oscillators is promising for printed electronics applications, and there is considerable potential for improvement. We note that the channel lengths of the devices used here are relatively long at 50 μm. On the basis of the carrier mobility of the CNT network, one can initially estimate the delay time from $t = \pi L(L + 2dL)/\mu V_{DD}$, where L is the channel length (50 μm) and dL is the overlapping width between the source (drain) and gate electrodes (10 μm). The calculated delay time is on the order of 1 μs. Therefore, the switching frequencies for a five-stage ring oscillator could be on the order of 100 kHz. However, in electrolyte-gated devices, the switching speed will ultimately be controlled by the RC time constant of the electrolyte layer because the mobilities of ions are much lower than the carrier mobilities in the CNT network. The resistance R of the ion gel depends on the film thickness, and therefore, thinner printed ion gel layers will result in shorter switching times (smaller RCs). The gel layer thickness in the devices reported here is on the order of 10 μm; decreasing that to 1 μm would result in a 10-fold decrease in the RC time constant, potentially allowing switching in the 100 kHz regime (single stage delays between 10^{-6} and 10^{-5} s). Achieving such speed increases will also require that parasitic capacitance is reduced further. Strategies to accomplish this include changing the channel or electrode geom-

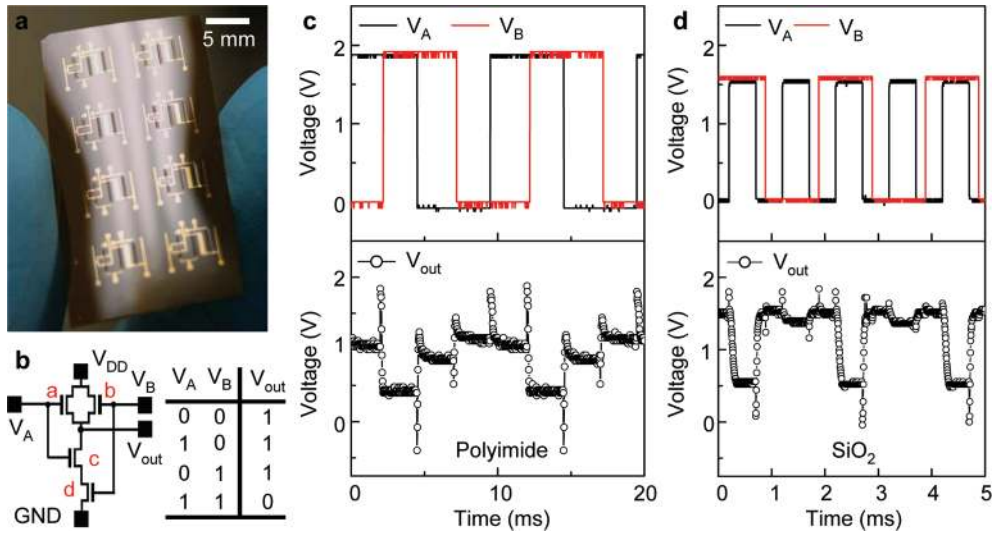

Figure 5. NAND logic gate based on ion gel-gated printed CNT transistors. (a) Printed CNT NAND gate array on flexible polyimide substrate. (b) Circuit diagram and logic sequence of the NAND gate. (c) Dynamic response of the device printed on polyimide substrate showing proper NAND logic at 100 Hz, V_{DD} = 1.5 V. Black and red lines are input voltages V_A and V_B, and the output voltage (black open circles) registers "low" only when V_A and V_B are both "high". (d) Dynamic response of the device printed on SiO_2 substrate showing proper NAND logic at 1 kHz, V_{DD} = 1.5 V.

etry, the addition of insulating layers over the source and drain electrodes, and higher resolution printing of the gel within the channel.

Finally, printed CNT NAND logic gates were also demonstrated on plastic substrates. Figure 5a displays an array of printed NAND gates on polyimide. Each NAND gate has two TFTs in parallel (labeled ***a*** and ***b*** in Figure 5b) and two transistors in series (***c*** and ***d***) and only registers low when two input voltages (V_A and V_B) are both high. As discussed above, the ambipolar TFTs cannot be completely turned OFF, which usually leads to an output voltage swing smaller than conventional complementary circuits.[46] Here we designed the widths of ***c*** and ***d*** (the "pull-down" transistors) to be 4 times larger than transistors ***a*** and ***b*** to balance the network strength. In this way, the output swing is maximized and the rising and falling times are equalized. NAND gates printed on plastic can respond to two input voltages at 100 Hz, as shown in Figure 5c. It can be seen from Figure 5d that, for devices on the SiO_2 substrates, the peaks in the output signal caused by parasitic capacitances are much smaller compared with those on plastic substrates, which leads to higher working frequency (1 kHz).

SUMMARY

In summary, the combination of high mobility, ambipolar semiconducting CNT networks, and high-capacitance ion gel dielectrics affords printed digital circuits that operate at sub-3V supply voltages with 40−60 μs signal delays. These results represent a significant improvement for printed circuits processed from liquid inks, and several prospects exist for further performance enhancements. Continued improvement of electronically functional inks enhances the potential application space for printed electronics.

METHODS

Materials. Water-based sorted CNT inks were prepared by density gradient ultracentrifugation[44] using arc-discharge grown CNTs (Carbon Solutions, Inc.). The purity level of the CNTs was determined to be 98% using optical absorbance spectroscopy. Prior to printing, the sorted CNT inks were dialyzed into 0.2% w/v sodium cholate aqueous solution to remove the density gradient medium iodixanol and to lower the levels of surfactant present in solution.

The ion gel ink is a mixture of 1.5 wt % of triblock copolymer poly(styrene-*b*-methylmethacrylate-*b*-styrene) (PS-PMMA-PS) (M_n = 8.9k−67k−8.9k, polydispersity 1.17) and 8.5 wt % of ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]) (from Merck) and 90 wt % ethyl acetate. The PEDOT:PSS ink (PH 500, 1−1.4 wt % polymer in water, from H.C. Stark), diluted with 10% by volume of ethylene glycol to enhance the conductivity, was used for printing the gate electrodes.

Device Fabrication. The metal contacts and interconnections of CNT TFTs and circuits were patterned by photolithography and electron-beam evaporation to form the Cr (2 nm)/Au (28 nm) electrodes. The width of source and drain electrodes was 10 μm. The transistor channel width was 500 μm and length was 50 μm, unless specified otherwise. The substrates were either polyimide or oxidized Si wafer SiO_2(300 nm)/Si. Before printing, substrates were immersed in a 1 mM ethanol solution of hexadecanethiol (for polyimide substrates) or anthracene thiol (for SiO_2 substrates) for 12 h in order to make a self-assembled monolayer on the Au electrodes. The substrates were then immersed into neat ethanol for 30 min, rinsed with ethanol, and dried under flowing N_2.

Printing was accomplished in ambient conditions using a commercially available aerosol jet printing system (Optomec, Inc.). Substrates were heated at 60 °C during printing to dry the solvent. CNT, ion gel, and PEDOT:PSS layers were sequentially printed on the channel area to fabricate transistors and circuits.

The water-based CNT ink was printed on the channel area with a printing speed of 3 mm/s (5 mm/s for low-coverage films).

After printing the nanotubes, the substrate was rinsed with deionized water to remove residual sodium cholate and allowed to dry at 105 °C for 1 h before printing of the ion gel layer. To complete the TFT, a channel-aligned PEDOT:PSS gate electrode was printed and extended to a Au pad outside the channel for connection. The TFTs were then heated at 105 °C in a glovebox for 1 h to remove residual solvent and water. Due to the differences in surface energy, the CNT ink does not wet untreated polyimide surfaces as well as hydrophilic SiO_2. It was observed that the same printing conditions usually resulted in less final coverage of CNTs on the polyimide substrates; there was some coverage loss during the water rinse step.

Electrical Measurements. The electrical characterization of CNT TFTs and circuits was accomplished using two Keithley 236 source measurement units and a Keithley 6517 electrometer. The dynamic responses of logic circuits were measured using Agilent 33220 and 33250 arbitrary-waveform generators to input voltages and a Tektronix TDS1002B digital oscilloscope to measure the output voltages. All of the electrical characterizations were carried out in a Lakeshore vacuum probe station under 10^{-6} Torr at room temperature.

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Supporting Information Available: Reproducibility of printed CNT TFTs on plastic and SiO_2 substrates, modeling of ambipolar CNT inverter behavior and power dissipation, dynamic response and operational stability of printed CNT inverters, estimation and reduction of parasitic capacitance, and operational stability of printed CNT ring oscillators. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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