On the Design of Two Single Event Tolerant Slave Latches for Scan Delay Testing

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***Abstract*—This paper proposes two new slave latches for improving the Single Event Upset (SEU) tolerance of a flip-flop in scan delay testing. The two proposed slave latches utilize additional circuitry to increase the critical charge of the flip-flop compared to designs found in the technical literature. The first (second) latch design achieves a 5.6 (2.4) times larger critical charge with 11% (4%) delay and 16 % (9%) power consumption overhead at 32nm feature size as compared to the best design found in the technical literature. Moreover, it is shown that the proposed slave latches have also superior performance in the presence of a single event with a multiple node upset.**

Index terms: Radiation hardening, soft error, flip-flop, Single Event Upset.

I. Introduction

The so-called *soft error* is a transient induced event that may result in a fault at circuit and system levels. The transient nature of the induced fault can be caused by an internal source such as power supply noise, capacitive and inductive crosstalk, or an external source such as α-particles emitted from packaging materials [1] or cosmic ray neutrons [2]. If these events cause a transient voltage pulse at a node of a flip-flop (or latch), changing the logic value stored, a *single event upset* (SEU) is said to occur. The SEU tolerance of a flip-flop can be usually assessed by considering the so-called critical charge as a metric to evaluate the tolerance of a circuit to a SEU [1]. To reduce the impact of soft errors on memory elements, different strategies have been used. Error correcting codes are the most widely adopted solution for protection of large memory arrays. Depending on the size and the use of the memory to be protected (cache memories, main memories, storage memories), different ECCs have been used [3], [4], [5], [6]. Instead, for the protection of single memory elements such as latches, hardening techniques based on the circuit level design have been proposed [7], [8], [9], [10]. An example of a widely used hardening design has been reported in [7] and is commonly known as DICE. The DICE memory cell uses a feedback mechanism that can be driven back to its previous state a single node of the cell that is affected by a SEU. The DICE cell uses two times the number of transistors with respect to the standard memory cell. The design proposed in [8] relies on two latches and corresponding paths to recover the original data. This scheme achieves a 10 times lower Soft Error Rate (SER) at a 1.0V supply with a 44% area overhead. Although this method avoids error propagation, it has an extensive area overhead and many transistors in the latch design are very sensitive to a soft error. A different Soft Error Hardened (SEH) latch is proposed in [9], and modified in [10]. In [11], this SEH latch was found to be very efficient when considering design trade-offs, such as power, performance, and soft error tolerance. When a particle strikes on a SEH latch, an error does not appear if the charge of the particle is within an expected range. The SEH latch encounters problems as related to short retention time, slow recovery time, and weakness to coupling noise. Several works have been reported to exploit the redundancy already presents in a flip-flop for DFT (Design For Test) and error resilience too [12]. Based on the SEH latch [9] has proposed two SEU tolerant flip-flops for enhanced scan to overcome the limitation of Launch on Capture and Launch on Shift delay testing methods (i.e. not allowing to provide an arbitrary pair of test vectors to the circuit under test [13]). Enhanced Scan flip-flops overcome this limitation at the cost of a higher overhead. The goal of this paper is to use the redundancy of this structure also to enhance error resilience. [14] proposes two designs for a SEU tolerant Enhanced Scan flip-flops for scan delay testing that uses the SEH latch as master and a modified slave latch. The two flip-flops have good SEU tolerance at 180nm. However, as shown in a later section of this paper, the SEU tolerance decreases significantly by decreasing the feature size of the transistors below 90nm. To improve the SEU tolerance in sub-90nm feature sizes, this paper proposes two modifications to the slave latches used in [14]. Using these novel slave latches, the flip-flop has a higher tolerance to single and multiple node upsets with small delay and power consumption overheads. Moreover, it is shown that the proposed latches and related flip-flops are robust when PVT variations are introduced in the design process.

This paper is organized as follows. Section II presents a review of soft error modeling and current designs for SEU tolerant flip-flops for scan delay testing. Section III deals with a detailed treatment of the proposed flip-flop design. Section IV presents the simulation results for single and multiple node upsets. The performance evaluation of the flip-flop with respect to metrics (delay, area and power consumption) is reported in Section V. Section VI details the results under PVT (process, voltage and temperature) variations and Section VII concludes the paper.

This research was partially funded by the Italian Ministry for University and Research; Program "Incentivazione alla mobilità di studiosi stranieri e italiani residenti all'estero", D.M. n.96, 23.04.2001

978-1-4673-3044-2/12/$31.00 ©

II. Review

In this section, the two SEU tolerant flip-flops proposed in [14] are reviewed. Both of these flip-flops (referred to as Type-I and Type-II) use the SEH latch as master latch. The Type-I and II flip-flops have similar designs; the only difference between them is the design of the slave latch. The two types of latch provide the same level of SEU tolerance during the operation mode and differ only during the scan-shift operation mode. As shown in Figure 1 a), a flip-flop consists of three parts: a selector, the master latch and the slave latch. There are six inputs (SE, D, SEB, SCI-PDH, SCI-NDH, and CNF) and three outputs (Q, SCO-PDH, and SCO-NDH).

The selector is used to select the input nodes for the different operational modes of the flip-flop. During normal system operation, D is selected as input to the flip-flop and the slave latch works in functional mode. In the scan-shift mode, the two scan-inputs (SCI-PDH and SCI-NDH) are selected as inputs of the flip-flop. The input node CNF splits the slave latch in two slave latches and the whole flip-flop becomes an enhanced scan flip-flop.

During system operation mode, both master and slave latches tolerate a SEU caused by a particle striking on the flip-flop. During the scan-shift operation, the flip-flop cannot tolerate a single event upset. As shown in Figure 1 a), the flip-flop has two scan inputs (SCI-PDH, SCI-NDH) and two scan outputs (SCO-PDH, SCO-NDH). The scan chain is constructed by connecting the scan output nodes (SCO-PDH and SCO-NDH) of the current stage to the scan input nodes (SCI-PDH and SCI-NDH) of the next stage. Figure 1 b) shows the implementation of the SEH (master) latch as proposed in [9]. The SEH latch has three inputs (CK, CKB and D) and one output (Q). It works in the transparent (normal) mode when CK is ”1” and CKB is ”0”. The input data passes through the clock controlled inverter (that consists of P5, P6, N5 and N6), and then goes through the inverter (P7 and N7) to finally reach the output node Q. In the transparent mode, the only difference between the SEH and a normal latch is that for the SEH latch, two additional copies of the input data are stored at PDH and NDH. These two copies are used to correct the soft error, that may have occurred in the hold mode. In the hold mode, PDH and NDH keep the original data, while DH keeps the opposite value of the input data through two separate feedback loops. As discussed previously, a particle may strike on any transistor of the SEH latch. Therefore, a soft error may occur at five nodes, i.e. DH, PDH, P2-P3, NDH and N2-N3. In a traditional latch, if the width of the pulse is longer than the feedback delay, an error will occur and appear at the output. However, for the SEH latch, when the SEU occurs at DH, the original input data stored at PDH and NDH can be used for correction by the two feedback loops. The SEU can also occur at PDH, P2-P3, NDH and N2-N3 in the two feedback loops. It can be shown that a soft error cannot occur on both PDH and NDH at the same time, i.e. at least one of these two nodes keeps the correct data. This copy of the original input data will then correct the soft error through the two feedback loops if the charge of the striking particle is smaller than the critical charge. Figure 1 c) shows the slave latch of the Type-I SEU tolerant flip-flop. This latch requires adding four transistors (P8, N8, P9 and N9) to realize the enhanced scan testing operation. During system operation, the four additional transistors are on and this latch operates as the SEH latch. During the scan-shift operation, CNF is high and CNFB is low; the additional transistors P8, P9, N8 and N9 are off. The slave latch is divided into two small latches, i.e. a dynamic latch SL1 (consisting mostly of DH) and a dynamic latch SL2 (consisting mostly of PDH and NDH). The SEU tolerant mechanism is the same as the SEH latch during system operation, and hence, the improvement in SEU tolerance for this latch is only marginal. The implementation of the slave latch of the Type-II flip-flop is shown in Figure 2 a). Similarly to the slave latch of Type-I, this latch has two modes, the system operation mode and the scan-shift operation mode. For this latch, six transistors are added to realize the scan-shift operation.

The implementation of the slave latch of the Type-II flip-flop uses two more transistors than the Type-I. This slave latch works the same as the SEH latch during system operation. Instead, for the scan-shift operations mode, the slave latch splits into two latches, i.e. a static latch SL1 a dynamic latch SL2. The static latch SL1 works better than the dynamic latch for a long scan-shift operation, avoiding loss of data due to the leakage currents. The two types of latch provides the same level of SEU tolerance during the operation mode.

III. Proposed slave latch

In this section, the proposed slave latches for SEU tolerant flip-flops are presented.

A. Proposed-I Slave Latch

The proposed slave latch for a SEU tolerant flip-flop is presented in figure 2 b). As discussed previously, DH can be in a high impedance state when the strike occurs at PDH or NDH; in this case, the charge stored at DH decays gradually. If the width of the pulse at PDH or NDH is larger than the decay time of DH, the strike occurring at PDH or NDH will not be corrected by the original data stored at the other node. Thus, the SEU appears at the output of the flip-flop. In this new design, four transistors (N10, N11, P10, and P11) are added to the design of [14]. The four additional transistors guarantee that DH is always connected to either the power supply or ground, even if there is a strike at PDH or NDH. During system operation CNF is ”0”, hence P8, N8, P9, and N9 are on. When the clock is high, P4 and N4 are on. The value D at the input is transmitted to PDH, NDH and Q, while DH stores the opposite value $\overline{D}$. (i) If DH=”1” it is connected to the power supply through P1 and P9. (ii) If DH=”0” it is connected to ground through N1 and N9.

When the clock is low, P4 and N4 are off; the correct data is stored using two separate feedback loops. At this time, suppose that the latch stores ”0” and that a strike occurs at PDH, changing its value. As a result, P1 is off momentarily. For the slave latch of the Type-I flip-flop, both P1 and N1 are off at that time, so DH is in a high impedance state and the correct data stored at DH leaks gradually (due to leakage current). In

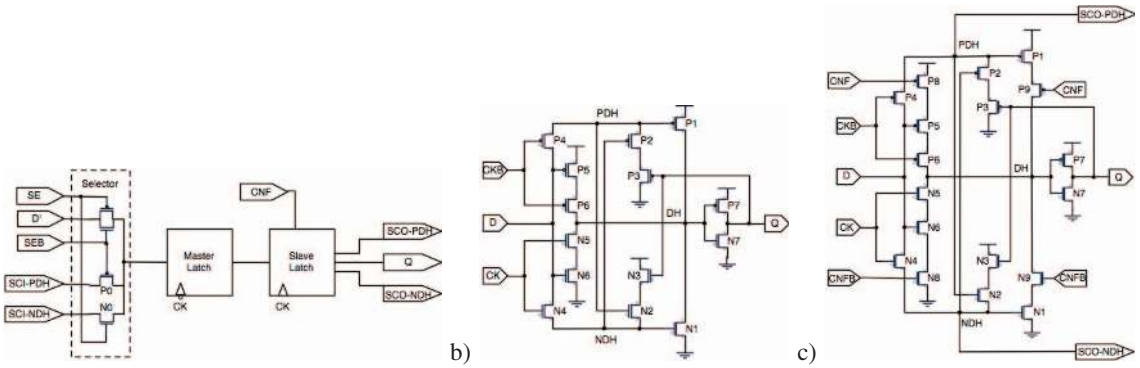

Fig. 1. a) Master-slave enhanced scan flip-flop [14] b) Soft Error Hardened latch (SEH) of [9] c) Slave latch of Type-I SEU tolerant flip-flop [14]

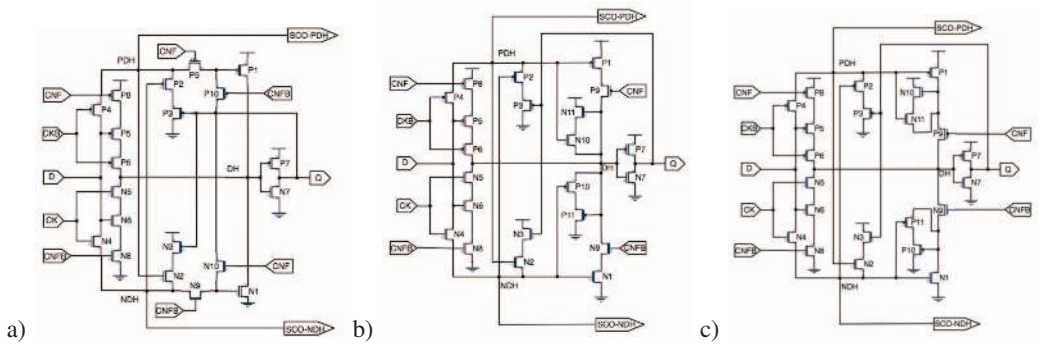

Fig. 2. a) Slave latch of Type-II SEU tolerant flip-flop [14] b) Proposed-I slave latch c) Proposed-II slave latch

the proposed slave latch, when the clock is high the original data "0" is stored at PDH and NDH, while DH is "1". The additional transistors N11 and P10 are on, but P11 and N10 are off. Therefore DH is connected to V_{dd} through P1 rather than N11 and N10. When the SEU changes the value of PDH P1 is switched off, but the error also turns on N10. DH is connected to V_{dd} through N10 and N11, and therefore, it is not in a high impedance state. The strike at PDH is recovered by the correct data stored at NDH and DH through P2 and P3. Similarly to the slave latch of Type-I flip-flop, only the "$0 \rightarrow 1$" transition may occur on PDH, because the gate of N10 (rather than its drain) is connected to PDH. For the same reason, only the "$1 \rightarrow 0$" transition may occur on NDH. During normal system operation, N10 (P10) and P11 (N11) are not turned on at the same time, because the data stored in DH is opposite in value to PDH (NDH).

B. Proposed-II Slave Latch

The Proposed-I slave latch suffers from the disadvantage that the additional transistors cause a delay at the Q output. To achieve better performance, a new SEU tolerant flip-flop is proposed by modifying the Proposed-I flip-flop. Figure 2 c) shows the slave latch of the Proposed-II flip-flop. The SEU tolerant mechanism of the Proposed-II flip-flop is the same as the Proposed-I flip-flop. However, to reduce the delay, the gates of N10, P10 and the drains of N11, P11 are connected to the drains of P1 and N1, rather than DH. Since DH of the Proposed-II flip-flop is directly connected to only two transistors (P9 and N9) rather than four transistors (as in the Proposed-I flip-flop), the parasitic capacitance of DH is smaller. Therefore, the decay time of the dynamic node DH (when a soft error occurs at PDH or NDH) is shorter than in the Proposed-I flip-flop. As discussed previously, the decay time of DH affects the critical charge of the flip-flop. Thus, although the Proposed-II flip-flop uses the same improvement mechanism as the Proposed-I flip-flop, its critical charge is smaller.

In system operation mode, the Proposed-II flip-flop works the same as the Proposed-I flip-flop. In the scan-shift operation mode, CNF is 1, and P8, P9, N8, and N9 are off. The slave latch of the Proposed-II flip-flop is divided into 2 dynamic latches. The first dynamic latch keeps the data in DH. DH keeps the stored value using the parasitic capacitance as long as CNF is high. Since P8 and N8 are off in the scan-shift mode, a change of CK does not change the value of DH. The additional transistors N10, N11, P10 and P11 do not affect the value stored in DH, because P9 and N9 are off and the extra circuit is not connected to DH during that time. The second dynamic latch keeps the data in PDH and NDH. Since PDH and NDH are connected to D through P4 and N4 (that are controlled by CK), the values stored in PDH and NDH are updated by CK. The SEU tolerance improvement mechanism does not affect the values stored in PDH and NDH and the scan-shift operation of the Proposed-II flip-flop, is similar to the scan-shift operation described in [14].

IV. Simulation Results

The SEU tolerance of flip-flops made of the slave latches are assessed and compared in this section. Unless otherwise specified, simulation is performed using HSPICE at $90nm$, $65nm$, $45nm$, and $32nm$ feature sizes (as gate length) using the corresponding Predictive Technology Model (PTM) [15]. The power supply for each PTM is $1.2V$, $1.1V$, $1.0V$, and $0.9V$ for the $90nm$, $65nm$, $45nm$ and $32nm$ PTMs, respectively. Simulation is performed at room temperature (25°); rising and falling times for all input signals (including the clock signals) are 100 ps. The four flip-flops have the same structure, and utilize as master latch the SEH latch of [9]. They only differ in the slave latch, i.e. Type-I and Type-II of [14] and the Proposed-I and Proposed-II slave latches. The flip-flops are named using the same notation as the slave latch employed in the design.

A. Single Node Upset

The single event upset tolerance of the four flip-flops is assessed; the critical charge is used as figure of merit. The behavior of a particle striking on a transistor (single node) is simulated using the current source based transient model and the critical charge of each flip-flop is measured. As the master latch is the same in all flip-flops, only the different slave latches are considered. Table I shows that the lowest charge (i.e. the critical charge) occurs always at the same node, independently of feature size and design. This is the PDH node.

TABLE I
Charges (in fC) of the vulnerable nodes in each flip-flop at different feature size

Size	FFs	P2-P3	PDH	N2-N3	NDH	Lowest
90nm	Type-I	426	197	1109	644	197
	Type-II	535	307	17742	3534	307
	Proposed-I	2162	1515	9690	3021	1515
	Proposed-II	873	599	6213	2158	599
65nm	Type-I	375	178	1277	620	178
	Type-II	464	273	13908	2166	273
	Proposed-I	1972	1231	12654	3249	1231
	Proposed-II	777	524	8060	2200	524
45nm	Type-I	337	176	2850	832	176
	Type-II	398	245	7980	1026	245
	Proposed-I	2770	1211	27930	6840	1211
	Proposed-II	770	470	18810	4218	470
32nm	Type-I	283	146	2394	638	146
	Type-II	283	158	946	308	158
	Proposed-I	2027	827	23028	4560	827
	Proposed-II	657	354	14250	2622	354

Figure 3 shows the effects of a soft error at the output node (D) for the Proposed-I flip-flop (at 32nm) due to a particle striking at the node of critical charge, i.e. PDH (the waveforms for the Proposed-II flip-flop are similar and are not shown due to space limitation). In the timing diagram, the clock period is 20 ns. After 21 ns, a single event strikes PDH of our proposed flip-flop; no error appears at the output as the effects of the single event upset are mitigated by the design. Note that by utilizing the same incident charges, both flip-flops of [14] would generate an erroneous output. Figure 4 plots the output voltages of the four flip-flops (at 32nm) as the value of the charge for the injected particle is increased at the critical node PDH. As the charge of the particles increases, the height of the voltage pulse increases too. Eventually, the output will change to a high value (0.9V) when the charge of the injected particle is at least equal to the critical charge. Therefore, for the Proposed-I and Proposed-II flip-flops, the error due to the SEU occurs when the charge of the particle increases to a 2.95 dB and 2.60 dB level respectively; the SEU appears at the output of the Type-I and Type-II flip-flops when the particle charge is increased to a 2.15 dB and 2.18 dB level, respectively. So, the Proposed-I and Proposed-II have better single event (node) upset tolerance compared to the two flip-flops of [14].

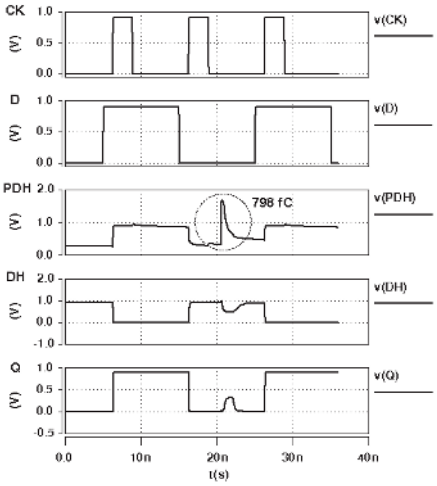

Fig. 3. *Timing diagram for the Proposed-I flip-flop when a particle (798fC) strikes at PDH node, 32nm*

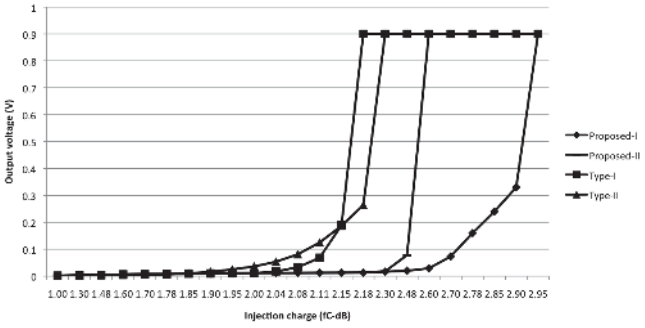

Fig. 4. *Output voltage of each flip-flop versus charge of particle striking at PDH, 32nm*

B. Multiple Node Upset

The previous subsection has evaluated the single event (node) upset tolerance of the flip-flops, i.e. when the particle deposits at only one node; this assumption, however, is only valid when transistors are far away in the layout. At nano scales, the density of integrated circuits is very high, hence a particle striking on a circuit may be collected by multiple nodes [16]. For nano scale VLSI, the assessment of the capability to tolerate a single event with a multiple node upset is very important [17]. In this case, all possible pairwise

combinations of nodes must be simulated for each flip-flop [18]. The flip-flops considered in this paper, are prone and vulnerable to a state change due to a particle strike and need to be further considered to find the so-called critical pair. As discussed previously, only the "0-to-1" transition may occur at PDH and P2-P3, while only the "1-to-0" transition can be captured by NDH and N2-N3. Therefore, a single event may result in only two possible node pairs, i.e. either the (PDH, P2-P3) pair or the (NDH, N2-N3) pair. By simulation, it has been found that the critical pair of all flip-flops is (PDH, P2-P3).

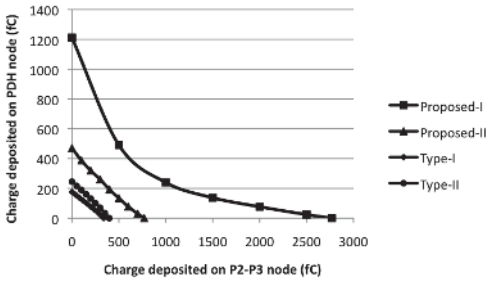

Fig. 5. *Critical Pair Plot for the flip-flops at 45nm*

Figure 5 shows the plot of the charge on the critical pair for every flip-flop at 45nm. If a charge pair is in the region below the curve, a single event with a multiple node upset will not affect the output, i.e. larger the area under the curve better is the tolerance. The intersection point of the plot curve with the y-axis gives the critical charge for single node tolerance. The proposed flip-flops achieve higher tolerance to a single event with multiple node upset; moreover, simulation shows that the higher tolerance to a multiple node upset of the Type-I flip-flop compared to the Type-II flip-flop is reduced when feature size is reduced (at 32nm, the areas under the curves of the two flop-flops of [14] are almost identical).

V. Performance evaluation

This section assesses different figures of merit as related to performance metrics for flip-flop design.

A. Timing and delay

The delay for the four flip-flops is reported in Table II at different feature size. The Type-I flip-flop has the smallest delay. At 32nm technology, the delay of the Type-I flip-flop is 122 ps while the Proposed-I flip-flop has a delay of 135 ps, that is 11% higher than Type-I. Instead, the Proposed-II flip-flop has a delay of 127 ps, only 4% higher than Type-I.

TABLE II
Timing of the four flip-flops (ps)

FF	90nm	65nm	45nm	32nm
Type-I	130	120	119	122
Type-II	134	124	124	130
Proposed-I	143	132	134	135
Proposed-II	137	126	125	127

B. Area

The area of the SEH realized in 32 nm can be computed as 4.12 μm^2, the area of the Type I latch is 5.02 μm^2 and the area of the proposed latch is 5.90 μm^2. The layouts of the latches are shown in Figure 6.

C. Power Consumption

For simulating and assessing the power consumption, the alternating data sequence 010101... is provided as input data, i.e. the flip-flops operate at the highest frequency, and the data value stored in the flip-flops is changed at every clock cycle. The power consumptions of the flip-flops at different feature sizes are reported in Table III. The Proposed-I flip-flop has consistently the highest power consumption.

TABLE III
Power Consumption of flip-flops (mW)

FF	90nm	65nm	45nm	32nm
Type-I	0.0968	0.0548	0.0276	0.0154
Type-II	0.1062	0.0597	0.0305	0.0172
Proposed-I	0.1118	0.0634	0.0317	0.0178
Proposed-II	0.1073	0.0602	0.0302	0.0168

VI. PVT variations

To evaluate the impact of PVT variations on the four flip-flops simulation has been performed under the combinations of two NMOS process corners (fast(f), slow(s)), two PMOS process corners (fast(f), slow(s)), three temperatures ($25^\circ \pm 50^\circ$), and three power supply voltages (low (0.8), typical (0.9), high (1.0)). The average results at 32nm feature size are given in Tables IV and V. The following features have been reported from the simulation results for the PVT variations.

Temperature variation

The delay and critical charge of each flip-flop change slightly with temperature; in all cases, the delay increases with temperature. However, if the temperature increases, the critical charge of a flip-flop decreases, because a higher temperature results in a higher leakage current. Consequently, the decay at DH becomes shorter, decreasing the critical charge.

Voltage and process variations: delay

Compared to temperature, the delays of all four flip-flops are more sensitive to supply voltage and process variations. The largest delays occur at the ss corner and 0.8v supply voltage. The least delays occur when the PMOS and NMOS are in the ff corner, and the supply voltage is 1.0v. The process variation impacts the performance of the flip-flops more significantly than the power supply voltage variation. The average change in delay due to PVT variations is not very pronounced for the four flip-flops.

Voltage and process variations: critical charge The variations of process parameters and power supply voltage have a significant impact on the critical charge. The smallest critical charges for all flip-flops are measured when the supply voltage is 1V, and the NMOS and PMOS transistors are in the Fast-Slow corner (fs corner). The largest critical charges are measured when the NMOS and PMOS transistors are in the Slow-Slow corner (ss corner) at 0.8V power supply voltage. At

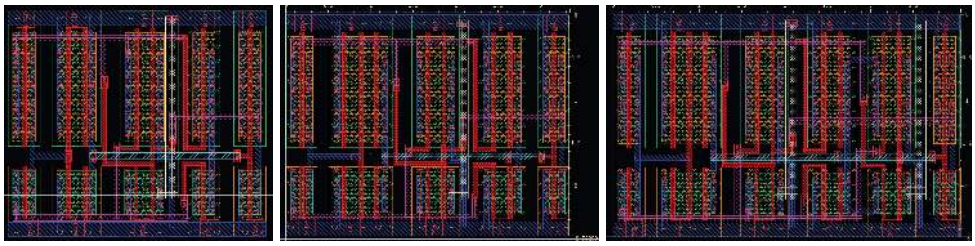

Fig. 6. *Layout of a) SEH, b) Type-I and c) proposed latch*

the ss corner the dimensions of the transistors are larger, this results in a higher parasitic capacitance and therefore higher decay time for the nodes in high impedance.

TABLE IV
AVERAGE CHANGE (%) IN DELAY DUE TO PVT VARIATIONS

FFs	Temperature	Voltage	Process
Type-I	7.4	15.11	28.5
Type-II	7.7	19.8	22.1
Proposed-I	7.9	18.5	21.9
Proposed-II	8.1	17	25.7

TABLE V
AVERAGE CHANGE (%) IN CRITICAL CHARGES DUE TO PVT VARIATIONS

FFs	Temperature	Voltage	Process
Type-I	31.3	49	25
Type-II	30.8	15.3	34.6
Proposed-I	20.3	21.7	47.9
Proposed-II	21.9	37.6	36.7

The critical charge of the Proposed-I and Proposed-II flip-flops are more sensitive than the Type-I and Type-II flip-flops. However, even in the worst case of variation, the critical charges of the two proposed flip-flops are significantly larger than the two flip-flops of [14].

The critical charge of each flip-flop is strongly dependent on the decay time of node DH and therefore the leakage current of a transistors. This heavily depends on temperature and power supply voltage [19]. If the temperature or supply voltage increases (decreases), also the leakage current increases (decreases). Thus, the delay time and the critical charge decrease at high temperature or supply voltage, as verified by the simulation results.

VII. CONCLUSION

In this paper, two novel slave latches for improved SEU tolerance have been proposed; the slave latches can be used with a master latch in a flip-flop scheme for scan delay testing. The proposed latches improve the single and multiple node tolerance to a single event of the flip-flops. They have a higher critical charge, hence resulting in a better SEU tolerance for the flip-flop. The proposed designs incur in modest area and delay overheads compared with the design of [14]. Extensive simulation results have been presented by varying the feature size of the transistors. At 32nm, the critical charge of the Proposed-I flip-flop is 5.6 times larger than the Type-I flip-flop [14], with 11% delay, 18% area and 15.6% power overhead, while the Proposed-II flip-flop has 2.4 times larger critical charge compared to the Type-I flip-flop, and suffers only a 4% delay, a 20% area and a 9% power overhead.

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