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# Process-Variation Effect, Metal-Gate Work-Function Fluctuation, and Random-Dopant Fluctuation in Emerging CMOS Technologies — Source link

Yiming Li, Chih-Hong Hwang, Tien-Yeh Li, Ming-Hung Han

**Institutions:** National Chiao Tung University

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# Process-Variation Effect, Metal-Gate Work-Function Fluctuation, and Random-Dopant Fluctuation in Emerging CMOS Technologies

Yiming Li, *Member, IEEE*, Chih-Hong Hwang, *Student Member, IEEE*, Tien-Yeh Li, and Ming-Hung Han, *Student Member, IEEE*

***Abstract*—This paper, for the first time, estimates the influences of the intrinsic-parameter fluctuations consisting of metal-gate work-function fluctuation (WKF), process-variation effect (PVE), and random-dopant fluctuation (RDF) on 16-nm-gate planar metal–oxide–semiconductor field-effect transistors (MOSFETs) and circuits. The WKF and RDF dominate the threshold-voltage fluctuation ($\sigma V_{\rm th}$); however, the WKF brings less impact on the gate capacitance and the cutoff frequency due to the screening effect of the inversion layer. The fluctuation of timing characteristics depends on the $\sigma V_{\rm th}$ and is therefore proportional to the trend of $\sigma V_{\rm th}$. The power fluctuation consisting of the dynamic, short-circuit, and static powers is further investigated. The total power fluctuation for the planar MOSFET circuits is 15.2%, which is substantial in the reliability of circuits and systems. The static power is a minor part of the total power; however, its fluctuation is significant because of the serious fluctuation of the leakage current. For an amplifier circuit, the high-frequency characteristics, the circuit gain, the 3-dB bandwidth, the unity-gain bandwidth power, and the power-added efficiency are explored consequently. Similar to the trend of the cutoff frequency, the PVE and RDF dominate both the device and circuit characteristic fluctuations due to the significant gate-capacitance fluctuations, and the WKF is less important at this simulation scenario. The extensive study assesses the fluctuations on circuit performance and reliability, which can, in turn, be used to optimize nanoscale MOSFETs and circuits.**

***Index Terms*—Circuit, coupled device–circuit simulation, emerging device technology, intrinsic-parameter fluctuation, modeling and simulation, nanoscale MOSFET, power fluctuation.**

## I. Introduction

THE VARIABILITY of performance and yield in nanoscale complementary metal–oxide–semiconductor (CMOS) devices is of great interest and has become crucial for circuit design. For state-of-art nanoscale CMOS circuits and systems, the intrinsic device parameter fluctuations that result from line-edge roughness [1], [2], the granularity of the polysilicon gate [3]–[5], random discrete dopants [6]–[33], and other causes have substantially affected signal system timing [31], [32] and high-frequency characteristics [33]. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, fluctuations in process parameters, and other factors, are known as indispensable components of the robust circuit-design procedure [34]–[37]. Diverse approaches have recently been presented to investigate the intrinsic-parameter fluctuations in semiconductor devices [10]–[26] and circuits [27]–[33]. Various suppression technologies have been proposed [10], [18]–[21], [23], [24], [33]. Among these approaches, the high-$\kappa$/metal-gate technology is the key to reduce the intrinsic-parameter fluctuations. However, the use of metal as a gate material introduces a new source of random variation due to the dependence of work function on the orientation of metal grains. The WKF-induced threshold-voltage ($V_{\rm th}$) fluctuation has been reported, and the scope is limited to the transistors [39], [40]. Additionally, the device and circuit performance may depend on different device characteristics. The identification of the dominant fluctuation source in the device and circuit characteristic fluctuations is urgent for the development of nanoscale systems. Several approaches have addressed the impact of RDF on timing and high-frequency characteristics [31]–[33]; however, the associated impacts on power and power efficiency are lacking. A comprehensive understanding of the intrinsic-parameter fluctuations on nanoscale transistors and circuits is urgent.

In this paper, for the first time, we extensively estimate the influences of the intrinsic-parameter fluctuations [the metal-gate work-function fluctuation (WKF), process-variation effect (PVE), and random-dopant fluctuation (RDF)] on 16-nm-gate bulk MOSFETs' dc/ac and circuits' timing/power/high-frequency characteristics. The importance of WKF in device and circuit characteristics is identified. The preliminary results show that the WKF and RDF affect device threshold voltage ($V_{\rm th}$) most and impact the timing and power of digital circuits. The fluctuation of the dynamic, short-circuit, and static powers is estimated. The total power fluctuation exceeds 15%, which may degrade the reliability of circuits and systems. For the high-frequency characteristics, the device ac characteristics, including gate-capacitance and cutoff fluctuations, the high-frequency property, and the power-added efficiency of a common-source (CS) amplifier, are then advanced. The WKF is found to bring less impact on these two characteristics due to

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Y. Li is with the Department of Electrical Engineering and the Institute of Communication Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the National Nano Device Laboratories, Hsinchu 300, Taiwan (e-mail: ymli@faculty.nctu.edu.tw).

C.-H. Hwang, T.-Y. Li, and M.-H. Han are with the Institute of Communication Engineering, National Chiao Tung University, Hsinchu 300, Taiwan.

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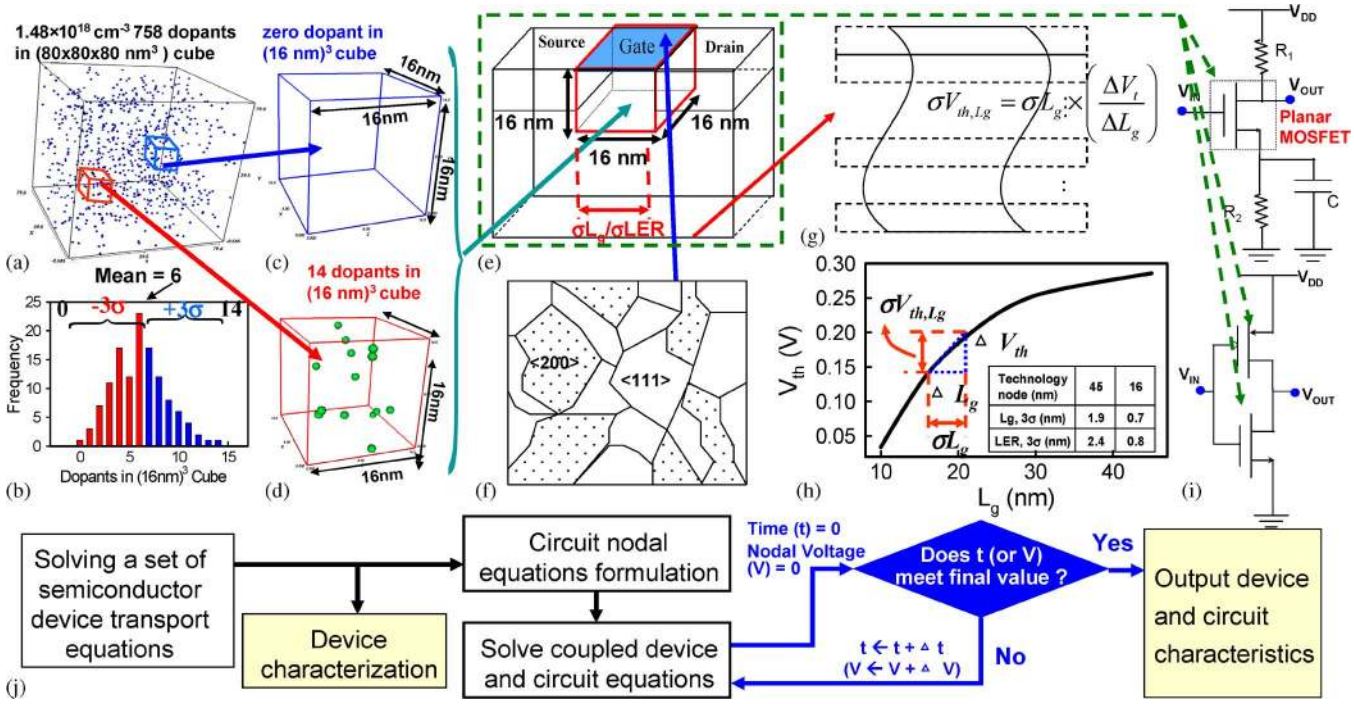


Fig. 1. (a) In a large cube of $80 \times 80 \times 80$ nm$^3$, 758 dopants are randomly generated, in which the equivalent doping concentration is $1.48 \times 10^{18}$ cm$^{-3}$. The large cube is then partitioned into 125 subcubes of $16 \times 16 \times 16$ nm$^3$. (b)–(d) The number of dopants in a subcube may vary from 0 to 14, and the average number is six. (e) These 125 subcubes are equivalently mapped into the device channel of bulk planar MOSFETs for the 3-D device simulation with discrete dopants. (f) Metal-gate material surface morphology, which is composed by a small number of grains. (g) PVE-induced $\sigma V_{\rm th}$ fluctuation is estimated from (h) the $V_{\rm th}$ roll-off characteristics. (i) Tested CS amplifier and inverter circuits in this paper. (j) Simulation flowchart for the coupled device–circuit approach.

the screening effect of the inversion layer. Similar to the trend of the cutoff frequency, the PVE and RDF dominate the device and circuit characteristic fluctuations. The major fluctuation sources in nanoscale transistors and circuits have been presented herein and then verified by the related device and circuit characteristics. The vast study assesses the fluctuations on digital-circuit performance and reliability, which may benefit CMOS design and technology in the sub-22-nm era.

This paper is organized as follows. Section II introduces the simulation technique for studying the effect of intrinsic-parameter fluctuations in nanoscale devices and circuits. Section III studies the characteristic fluctuations in 16-nm-gate devices and circuits. Finally, conclusions are drawn, and the future work is suggested.

## II. Nano-MOSFET Circuit and Simulation Technique

The devices we examined are the 16-nm-gate bulk MOSFETs (width: 16 nm) with amorphous-based TiN/HfSiON gate stacks with an EOT of 1.2 nm [39]. The RDF simulation mainly follows our recent work [20], [23], [24], [33], in which 758 dopants are randomly generated in a large cube, in which the equivalent doping concentration is $1.48 \times 10^{18}$ cm$^{-3}$, as shown in Fig. 1(a). The large cube is then partitioned into subcubes. The number of dopants may vary from 0 to 14, and the average number is six, as shown in Fig. 1(b)–(d). These subcubes are mapped into the device channel for the 3-D device simulation with discrete dopants, as shown in Fig. 1(e). The device simulation is performed by solving a set of 3-D drift-diffusion equations with quantum corrections by the density gradient method [42]–[49], which is conducted using a parallel computing system [56]–[58]. The mobility model used in the device simulation, according to Mathiessen's rule [59], [60], can be expressed as

$$\frac{1}{\mu} = \frac{D}{\mu_{\rm surf\_aps}} + \frac{D}{\mu_{\rm surf\_rs}} + \frac{1}{\mu_{\rm bulk}} \tag{1}$$

where $D = \exp(x/l_{\rm crit})$, $x$ is the distance from the interface, and $l_{\rm crit}$ is a fitting parameter. The mobility consists of the following three parts:

1) the surface contribution due to acoustic phonon scattering $\mu_{\rm surf\_aps} = (B/\mathbf{E}) + [C(N_i/N_0)^\tau/\mathbf{E}^{1/3}(T/T_0)^K]$, where $N_i = N_A + N_D$, $T_0 = 300$ K, $\mathbf{E}$ is the transverse electric field normal to the interface of the semiconductor and the insulator, $B$ and $C$ are parameters which are based on physically derived quantities, $N_0$ and $\tau$ are fitting parameters, $T$ is lattice temperature, and $K$ is the temperature dependence of the probability of surface phonon scattering;
2) the contribution attributed to surface roughness scattering $\mu_{\rm surf\_rs} = ((E/E_{\rm ref})^\chi/\delta + E^3/\eta)^{-1}$, where $\chi = A + \alpha(n+p)N_{\rm ref}/(N_i + N_1)^\nu$, $\mathbf{E}_{\rm ref} = 1$ V/cm is a reference electric field to ensure a unitless numerator in $\mu_{\rm surf\_rs}$, $N_{\rm ref} = 1$ cm$^{-3}$ is a reference doping concentration to cancel the unit of the term raised to the power $\nu$ in the denominator of $\chi$, $\delta$ is a constant that depends on the details of the technology, such as oxide growth conditions, $N_1 = 1$ cm$^{-3}$, and $A$, $\alpha$, and $\eta$ are fitting parameters;

3) the bulk mobility $\mu_{\rm bulk} = \mu_L (T/T_0)^{-\xi}$, where $\mu_L$ is the mobility due to bulk phonon scattering and $\xi$ is a fitting parameter.

The mobility model is quantified with our device measurements for the best accuracy, and the characteristic fluctuation has been validated with the experimentally measured dc base band data [23]. Note that, in "atomistic" device simulation, the resolution of individual charges within classical device simulation using a fine mesh creates problems associated with singularities in the Coulomb potential [15], [16], [22]. The potential becomes too steep with fine mesh, and therefore, the majority carriers are unphysically trapped by ionized impurities, and the mobile carrier density is reduced [25], [26], [31]. Thus, the density-gradient approximation is used to handle discrete charges by properly introducing the quantum–mechanical effects [42]–[49]. The physical model and accuracy of such large-scale simulation approach have been quantitatively calibrated by experimentally measured results [23].

For WKF, considering the size of metal grains and the gate area of the devices, the device gate area is composed of a small number of grains, as shown in Fig. 1(f). Each grain orientation has a different work function; therefore, the gate work function is a probabilistic distribution rather than a deterministic value. A statistically sound Monte Carlo approach is advanced here for examining such distribution. At first, the gate area is partitioned into several parts according to the average grain size, as shown in Fig. 2(a). Then, the grain orientation of each part and the total gate work function are randomly generated based on the properties of metal, as shown in Fig. 2(b) [39], [40], [50]–[53]. The work function of each partitioned area $(WK_i)$ is a random value. The summation of $WK_i$ is then averaged to obtain the effective work function of the transistor and is then used for WKF-induced $\sigma V_{\rm th}$ estimation. Fig. 2(c)–(e) shows the probability distributions of work function for devices with 1, 4, 9, and 16 grains on the gate area. The distribution is similar to the normal distribution as the number of grains increases. In other words, in a nanoscale transistor with scaled gate area, the distribution is not a normal distribution, and therefore, the WKF-induced $\sigma V_{\rm th}$ may not be a normal distribution as the gate area scales. Fig. 2(f) shows the dependence of the WKF-induced $\sigma V_{\rm th}$ versus the average grain size on a $16 \times 16$ nm$^2$ gate area. The material is TiN. The WKF-induced $\sigma V_{\rm th}$ increases significantly as the average grain size increases, which implies the importance of controlling the metal-gate grain size in reducing the WKF effect. The WKF-induced $\sigma V_{\rm th}$ saturates after the 16-nm average grain size because the average grain size becomes larger than the gate area. The average grain size of this study is 4 nm [39]. Notably, the different process of gate formulation, namely, gate first or replacement gate, may change the thermal budget and change the grain size of the metal material. As for the PVE in Fig. 1(g), the $V_{\rm th}$ roll-off characteristics in Fig. 1(h) are used to estimate the effect of PVE. The $\Delta L_g$ and $\Delta V_{\rm th}$ are obtained from the $V_{\rm th}$ roll-off curve. $\sigma L_g$ is the standard deviation of the generated effective device gate length. The $\sigma V_{\rm th,PVE}$ can thus be calculated from the equations in the inset of Fig. 1(g). The PVE includes the gate-length deviation and the line-edge roughness, whose magnitude follows the projections of the ITRS roadmap [54] that

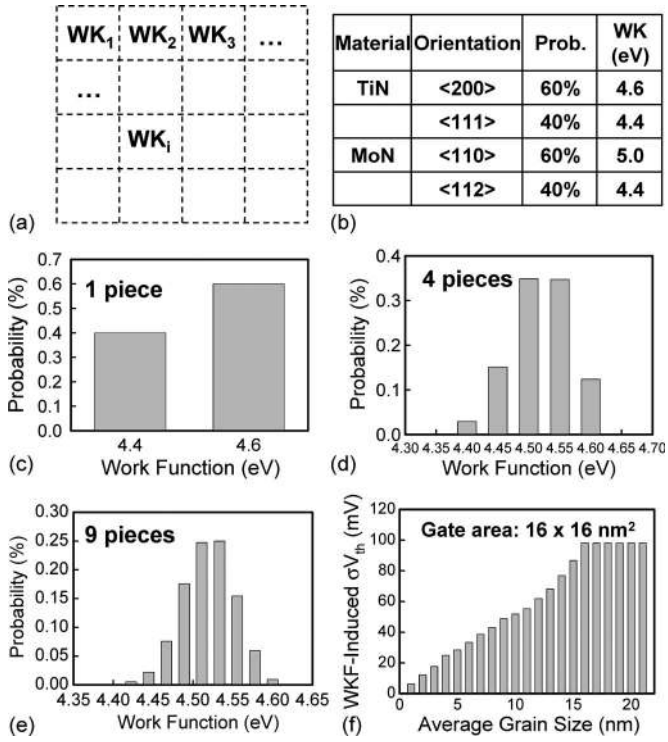


Fig. 2. Gate area is partitioned into several pieces according to the average grain size. The work function of each partitioned area $(WK_i)$ is a random value, whose probability follows (b). The obtained probability distributions of TiN work function for devices with (c) one, (d) four, and (e) nine grains on the gate area. (f) Dependence of TiN metal-gate-induced $\sigma V_{\rm th}$ versus the average grain size.

$3\sigma_{L_g} = 0.7$ nm and $3\sigma_{\rm LER} = 0.8$ nm for the 16-nm technology node.

The CS amplifier and the CMOS inverter are used as test circuits, as shown in Fig. 1(i). Similarly, PMOSFETs with intrinsic-parameter fluctuations are generated according to Figs. 1 and 2. Then, the NMOSFETs and PMOSFETs are randomly selected and used to study the circuit characteristic fluctuations. To compare fairly the NMOSFET- and PMOSFET-induced characteristic fluctuation and eliminate the effect of transistor size on fluctuation, the dimensions of the PMOSFET were the same as those of the NMOSFET, and the absolute value of the nominal threshold voltages for both the NMOSFET and PMOSFET were 140 mV. In estimating circuit characteristics, since no well-established compact model of ultrasmall nanoscale devices is available, to capture the discrete-dopant-position-induced fluctuations, a coupled device–circuit simulation approach [29], [33], [41] is employed, as shown in Fig. 1(j). At first, an initial guess for device bias condition is assumed, and the device characteristics in the test circuit are estimated by solving the device transport equations. The obtained result is the initial guess for the coupled device–circuit simulation. Then, based on Kirchhoff's current law, the nodal equations of the tested circuits are formulated. The formulated circuit equations are coupled to the device transport equations to form a large matrix that contains both circuit and device equations. The large matrix is then solved for simultaneously obtaining device and circuit characteristics. Since the device equations are solved in the coupled device–circuit simulation, the effects of intrinsic-parameter fluctuations on the device and

TABLE I
SUMMARIZED $V_{\rm th}$ FLUCTUATION FOR 16-nm-GATE PLANAR NMOSFETS AND PMOSFETS, IN WHICH THE DEVICE $V_{\rm th}$ IS CALIBRATED TO 140 mV

| | PVE (mV) | WKF (mV) | RDF (mV) | Total (mV) |
|---|---|---|---|---|
| NMOSFET | 18.1 | 24.3 | 61 | 69 |
| PMOSFET | 16.7 | 72.8 | 58.8 | 95.1 |

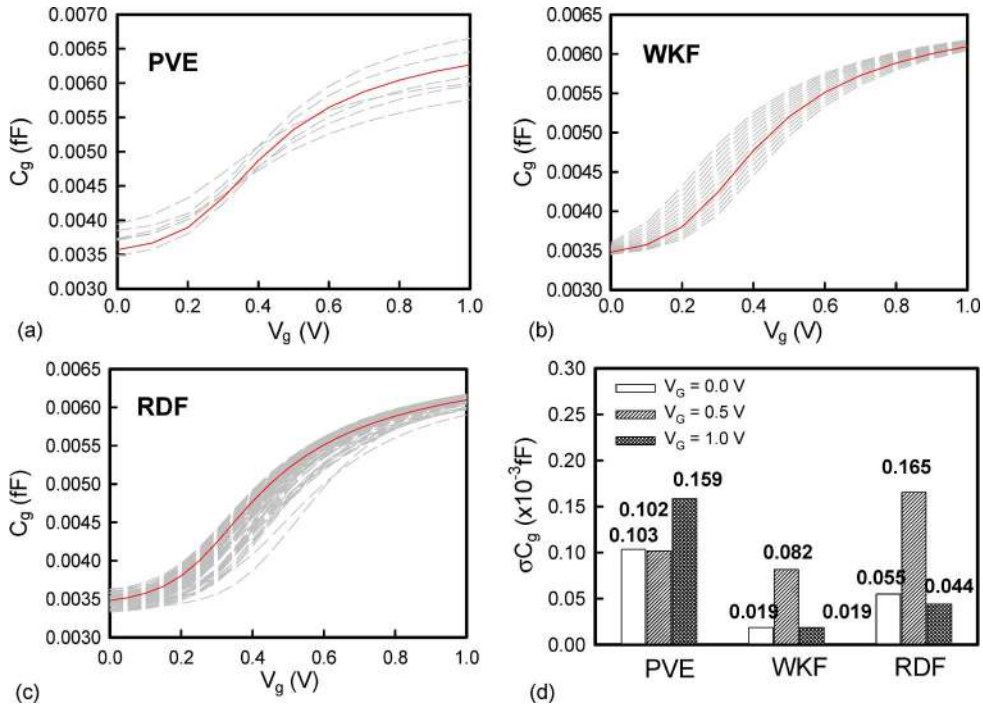


Fig. 3. $C_g$–$V_G$ characteristics for the explored devices with (a) PVE, (b) WKF, and (c) RDF. (d) $C_g$ fluctuation at $V_G = 0$, 0.5, and 1 V for 16-nm-gate MOSFETs with WKF, PVE, and RDF.

circuit characteristics are thus properly captured. The coupled simulation is solved iteratively until the solution is converged in each time step and bias condition. The characteristic fluctuation of devices was validated with reference to the experimentally measured data [23] to ensure the best accuracy.

## III. RESULTS AND DISCUSSION

In this section, the device intrinsic-parameter fluctuations for the 16-nm-gate bulk planar MOSFETs are examined in terms of $V_{\rm th}$, the gate capacitance $(C_g)$, and the cutoff frequency $(F_T)$. Then, the intrinsic-parameter fluctuation on various electrical characteristics including the delay, the power, and the high-frequency characteristic fluctuations are explored.

### A. Device-Level Characteristics

The $V_{\rm th}$ fluctuations of NMOSFETs and PMOSFETs are examined in Table I. According to the statistical independence of the fluctuation components, the total $V_{\rm th}$ fluctuation $(\sigma V_{\rm th,total})$ could be approximately given by

$$(\sigma V_{\rm th,total})^2 \approx (\sigma V_{\rm th,RDF})^2 + (\sigma V_{\rm th,WKF})^2 + (\sigma V_{\rm th,PVE})^2 \quad (2)$$

in which $\sigma V_{\rm th,RDF}$, $\sigma V_{\rm th,WKF}$, and $\sigma V_{\rm th,PVE}$ are the RDF-, WKF-, and process-variation-induced $V_{\rm th}$ fluctuation, respectively. The results show that the RDF dominates the $V_{\rm th}$ fluctuation in NMOSFETs; however, for the $V_{\rm th}$ fluctuation of PMOS, the WKF becomes the dominating factor because of the large deviation of the work function for different grain orientations in Fig. 2(b). Notably, the statistical addition of individual fluctuation sources herein, i.e., (2), simplifies the variability analysis of nanodevices and circuits significantly [25]. The dominant source of fluctuation will not be significantly altered. The WKF-, PVE-, and RDF-fluctuated $C_g$'s are shown in Fig. 3(a)–(c), where the solid line shows the nominal case with 16-nm-gate $1.48 \times 10^{18}$ cm$^{-3}$ channel doping and the dashed lines are the fluctuated cases. The different intrinsic-parameter fluctuations induced rather different $C$–$V$ characteristics. Fig. 3(d) shows the gate-capacitance fluctuations $(\sigma C_g)$ with 0-, 0.5-, and 1.0-V gate biases. Different to the results of $V_{\rm th}$ fluctuation, the WKF brought less impact on gate-capacitance fluctuation. At low or negative gate bias, the accumulation layer screens the impact of WKF. Additionally, at low gate bias, the total capacitance decreases because of the increased depletion region. The associated value of $C_g$ fluctuation is small. The capacitive response is then dominated by increment of inversion in the moderate inversion. The device characteristics are then impacted by intrinsic-parameter-fluctuated electrostatic potentials. If the high $V_G$ is achieved, the inversion layer is formed below the surface of the gate

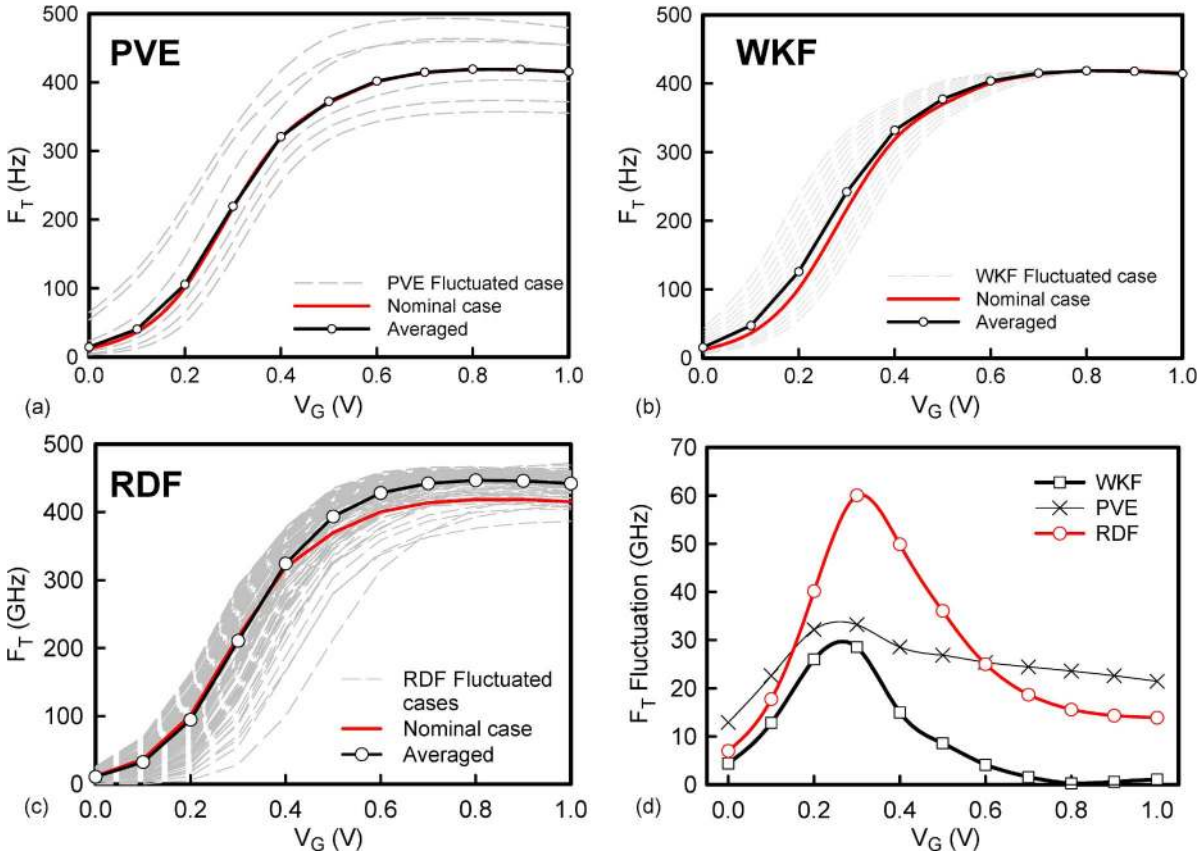


Fig. 4. $F_T$ characteristic fluctuation induced by (a) PVE, (b) WKF, and (c) RDF. (d) Summarized $F_T$ fluctuations with for the studied planar MOSFETs.

oxide, and the total gate capacitance is mostly contributed by the gate-oxide capacitance $(C_{\rm ox})$. Therefore, the variation of capacitance now again becomes the variation of the capacitance of the gate oxide $(C_{\rm ox})$. Under strong inversion, the gate capacitance is dominated by the inversion layer, and a small change resulting from the WKF in the voltage across the MOS structure will induce a differential change in the inversion layer charge density. The WKF is therefore bringing less impact on the gate-capacitance fluctuation because the inversion charge responds to the change in capacitor voltage (i.e., the WKF is now screened by the inversion layer). Similarly, in RDF, the impact of the individual dopant-induced electrostatic potential variation is screened by the inversion layer itself. However, the screening effect of the inversion layer is weakened by discrete dopants positioned near the channel surface. Therefore, the gate-capacitance fluctuation is still obviously fluctuated at high gate bias. Our preliminary results show that the RDF and PVE dominate the gate-capacitance fluctuations at all gate-bias conditions, respectively. The impacts of the WKF on $C_g$ are reduced significantly at low and high gate voltage $(V_G)$ due to the screening effect. Notably, the PVE brings direct impact on gate length and therefore influences the gate capacitance. The PVE-induced gate-capacitance fluctuation is independent of screening effect and should be noticed when the transistor operated in high gate bias, as shown in Fig. 3(d).

Fig. 4(a)–(c) shows the cutoff frequency $(F_T = v_{\rm sat}/2\pi L_g = g_m/2\pi C_g)$ and its fluctuation versus $V_G$, in which the solid line shows the nominal case with $1.48 \times 10^{18}$ cm$^{-3}$ channel doping, the dashed lines are fluctuated cases, and the symbol line shows the averaged result. The $g_m$ and $v_{\rm sat}$ are the transconductance and the saturation velocity of the transistors, respectively. The planar MOSFETs possess higher $F_T$'s than those of FinFETs due to the smaller gate capacitance [61]; WKF-induced $F_T$ fluctuation diminished as the saturation of the carrier velocity occurs. However, the PVE-induced $F_T$ fluctuation is still significant, owing to the direct influence of gate length $(L_g)$ on gate capacitance. As for RDF, the carrier-impurity scattering alters the saturation velocity, and therefore, $F_T$ fluctuation does not diminish in the high-field region. Note that the nominal and the averaged values of $F_T$ are similar to the results of WKF and PVE. However, in RDF, the deviation between the nominal and the averaged $F_T$ increases as $V_G$ increases due to the randomness of carrier-impurity scattering events and carrier velocity variations [20]. The intrinsic-parameter-induced $F_T$ fluctuations are shown in Fig. 4(d), where the RDF and PVE are the two major factors. The RDF and PVE play the dominating factor in the $F_T$ fluctuation. Notably, the impacts of RDF and WKF on $F_T$ fluctuation are suppressed at higher $V_G$ ($> 0.6$ V) due to the screening effect. The obtained results are similar to the results, as shown in Fig. 3(d), in which the WKF bring insignificant impact on $C_g$ and $F_T$.

### *B. Digital Integrated Circuits*

Fig. 5(a) shows the high-to-low and low-to-high transition characteristic of the output signal, and the high-to-low delay

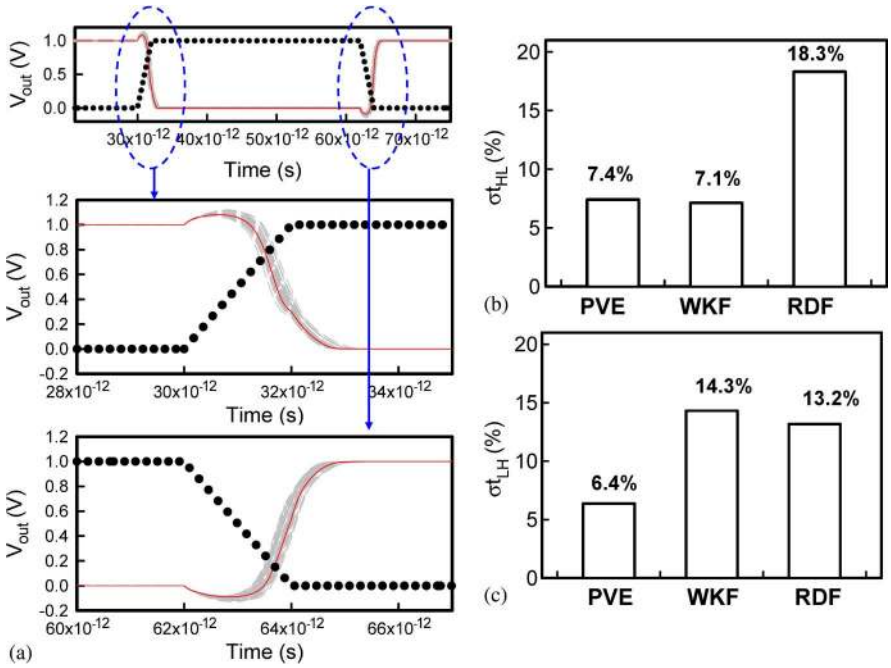


Fig. 5. (a) Timing of planar MOSFET inverter circuits [(symbols) input signal and (lines) output signal]. The fluctuations of (b) $t_{\rm HL}$ and (c) $t_{\rm LH}$ with respect to WKF, PVE, and RDF for the MOSFET inverters.

time $(t_{\rm HL})$ and low-to-high delay time $(t_{\rm LH})$ are shown in Fig. 5(b) and (c), respectively. Since the $t_{\rm HL}$ and $t_{\rm LH}$ are dependent on the $V_{\rm th}$ fluctuations for the NMOSFET and PMOSFET, respectively. The fluctuations of delay time and static noise margin depend on the $V_{\rm th}$ fluctuation which follows the trend of $V_{\rm th}$ fluctuation. Therefore, the delay-time fluctuation follows the trend of $\sigma V_{\rm th}$, as shown in Table I. The RDF and WKF are the greatest effects upon timing fluctuations, and WKF introduces the largest $t_{\rm LH}$ fluctuation due to the large work-function deviation within the scaled gate area. The WKF has shown its increasing importance in nanoscale transistors, particularly for PMOSFETs' characteristics. Notably, we herein use the transistors' gate capacitance as the load capacitance $(C_{\rm load})$ and focused on the device intrinsic-parameter-fluctuation-induced circuit variability. The result of the nominal propagation delay may be changed as we take an additional load capacitance into consideration.

Fig. 6 shows the power for the studied transistors. The total power $(P_{\rm total})$ consists of the dynamic power $(P_{\rm dyn})$, the short-circuit power $(P_{\rm sc})$, and the static power $(P_{\rm stat})$. Their definitions are given by

$$P_{\rm dyn} = C_{\rm load} V_{\rm dd}^2 f_{0->1} \tag{3}$$

$$P_{\rm sc} = f_{0->1} V_{\rm DD} \int_T I_{\rm sc}(\tau) d\tau \tag{4}$$

$$P_{\rm stat} = V_{\rm DD} I_{\rm leakage}. \tag{5}$$

The $f_{0->1}$ is the clock rate. $I_{\rm sc}$ is the short-circuit current, which is observed as both NMOSFET and PMOSFET are turned on, resulting a dc path between the power rails. $T$ is the switching period. $I_{\rm leakage}$ is the leakage current that flows between the power rails in the absence of switching activity. The short-circuit power is determined by the time of existence of the dc path between the power rails and the short-circuit current. Since the $V_{\rm th}$ for the explored devices are calibrated, the $P_{\rm sc}$ is then determined by the $I_{\rm sc}$. The $I_{\rm sc}$ is dependent on the saturation current of the devices. The $P_{\rm dyn}$ and $P_{\rm sc}$ are the two significant factors in total power consumption. The corresponding power fluctuations are further shown in Fig. 7. Fig. 7(a) shows the fluctuations of the dynamic power $(\sigma P_{\rm dyn})$ of the bulk planar MOSFET inverter circuits with WKF, PVE, and RDF. The RDF and PVE dominate the dynamic power fluctuation; additionally, the WKF shows less impact due to the smaller gate-capacitance fluctuations. Fig. 7(b) shows the short-circuit-power fluctuation $(\sigma P_{\rm sc})$ for the studied inverter circuits. The short-circuit power is defined by the time of existence of the dc path between the power rails and the short-circuit current and depends on the threshold voltage of NMOSFETs and PMOSFETs, as shown in the inset of Fig. 7(b). The short-circuit-power fluctuation is therefore determined by the $\sigma V_{\rm th}$ of the transistors. Thus, the RDF and WKF dominate the $\sigma P_{\rm sc}$, which is similar to the result of Table I. The WKF starts to play an important role in the $\sigma P_{\rm sc}$ of planar MOSFETs because of the significant $\sigma V_{\rm th}$ induced by WKF. Fig. 7(c) shows the static

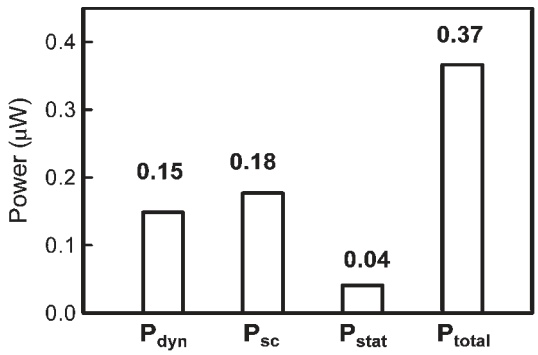


Fig. 6. Nominal power for the bulk planar MOSFET circuits.

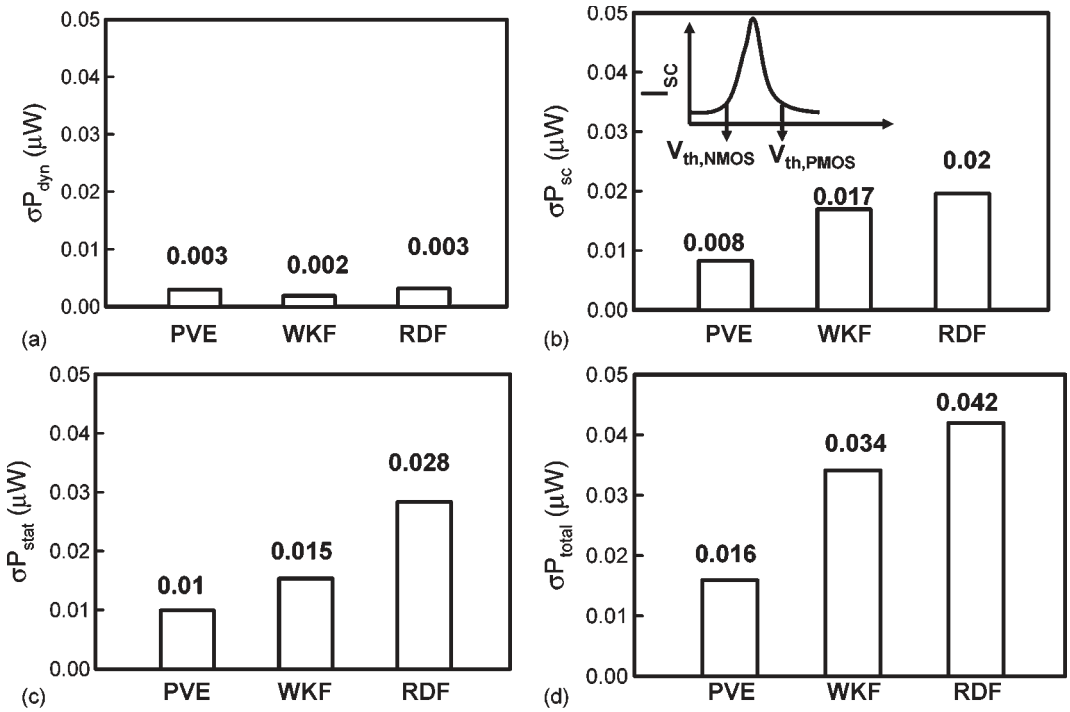


Fig. 7. (a) Dynamic power. (b) Short-circuit power. (c) Static power. (d) Total power fluctuations for the explored devices with WKF, PVE, and RDF.

power fluctuation ($\sigma P_{\rm stat}$). Since the leakage current is an exponential function of $V_{\rm th}$($I_{\rm leakage} \propto \exp(-qV_{\rm th}/nkT)$) [55], the static power fluctuation becomes significant even though the static power is not an important part in total power dissipation. Moreover, the RDF dominates the $\sigma P_{\rm stat}$ due to the larger $V_{\rm th}$ fluctuation. Fig. 7(d) shows the total power fluctuations ($\sigma P_{\rm total} = [(\sigma P_{\rm PVE})^2 + (\sigma P_{\rm WKF})^2 + (\sigma P_{\rm RDF})^2]^{0.5}$), where the RDF dominates the total power fluctuation. The total power fluctuation is 0.0564 $\mu$W, which is 15.2% ($\sigma P_{\rm total}/P_{\rm total} = 0.0564/0.37$) of the total power. The significant power fluctuation may bring sizable impacts on the reliability of circuits, such as temperature, and, in turn, degrades the device performance. The remarkable components of the intrinsic-parameter fluctuations in circuit power are the RDF and WKF.

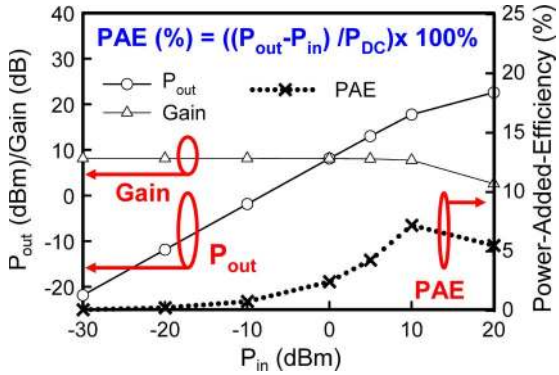


Fig. 8. Output power, circuit gain, and power-added efficiency of the explored devices as a function of input power. The calculation of PAE follows the formula, as shown in the inset.

### *C. Analog/High-Frequency Circuits*

Fig. 8 shows the characteristics of the employed CS power-amplifier circuits. The nominal output power, the circuit gain, and the power-added efficiency of the CS power amplifier as a function of the input power are plotted, where $P_{\rm out}$ and $P_{\rm in}$ are output and input powers, respectively. A sinusoid input wave with 0.5-V offset voltage is used as input signal. The device channel is continuously doped, and the operation frequency is $10^8$ Hz. Owing to the limitation of output signal swing, the nominal value of $P_{\rm out}$ is saturated after 10-dBm input power, which, in turn, decreases the gain of the circuit. The gain fluctuations of the planar MOSFETs resulted from WKF, PVE, and RDF are then shown in Fig. 9(a)–(d). Since the PVE and RDF dominate gate-capacitance fluctuations due to the significantly affected channel length and depletion region, the PVE and RDF play important roles in high-frequency characteristic fluctuation, as shown in Fig. 9(d). The effects of WKF in high-frequency characteristics are negligible in this scenario. Additionally, the input signal is a sinusoid wave; therefore, the device may operate in a different operational region if the amplitude of the sinusoid wave is large enough. The enlarged gain fluctuation with increasing input power is resulted from the larger portion of device operation in the linear region. While the magnitude of the input signal swing increases larger than 0.178 V (the input power is larger than 15 dBm), a part of device operation enters the cutoff region and therefore decreases the gain fluctuation. The high-frequency characteristic fluctuations are then shown in Fig. 10(a), where the fluctuation of the high-frequency circuit gain, the 3-dB bandwidth, and the unity-gain bandwidth are extracted, as shown in Fig. 10(b)–(d), respectively. Similar to the result of Figs. 2 and 3, the RDF and PVE dominate the high-frequency characteristic fluctuations, and WKF becomes marginal in this analyzing skeleton.

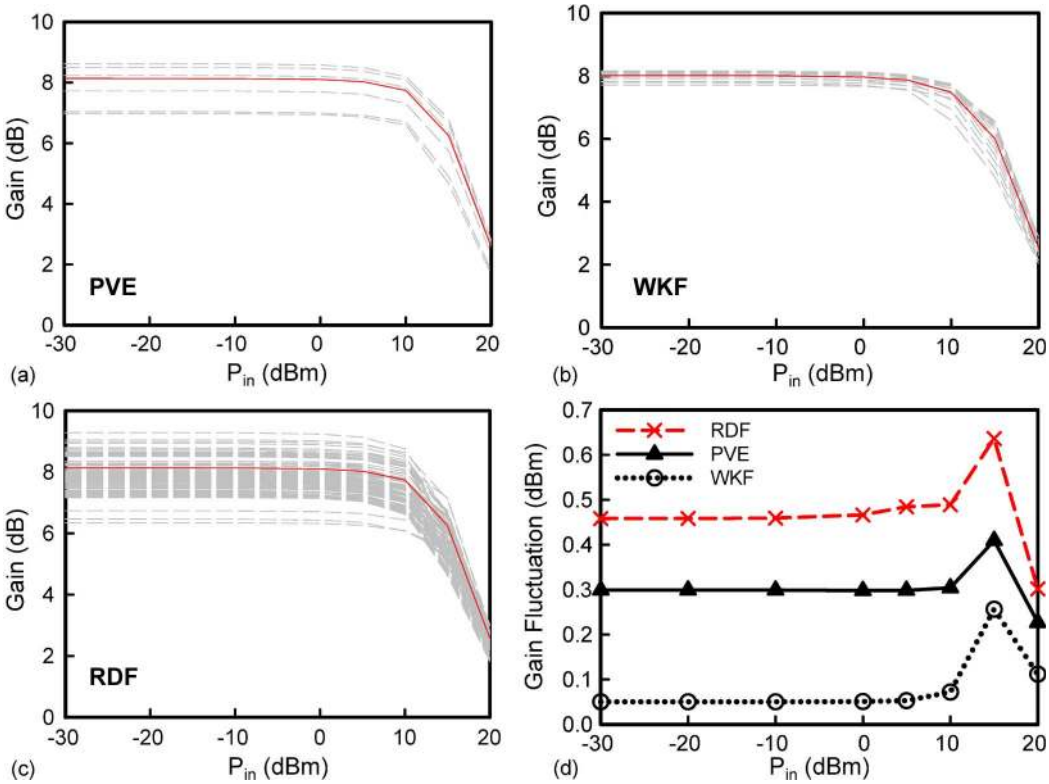


Fig. 9. Circuit gain characteristics of the planar MOSFETs with (a) PVE, (b) WKF, and (c) RDF fluctuations, respectively. (d) Summarized circuit gain fluctuations.

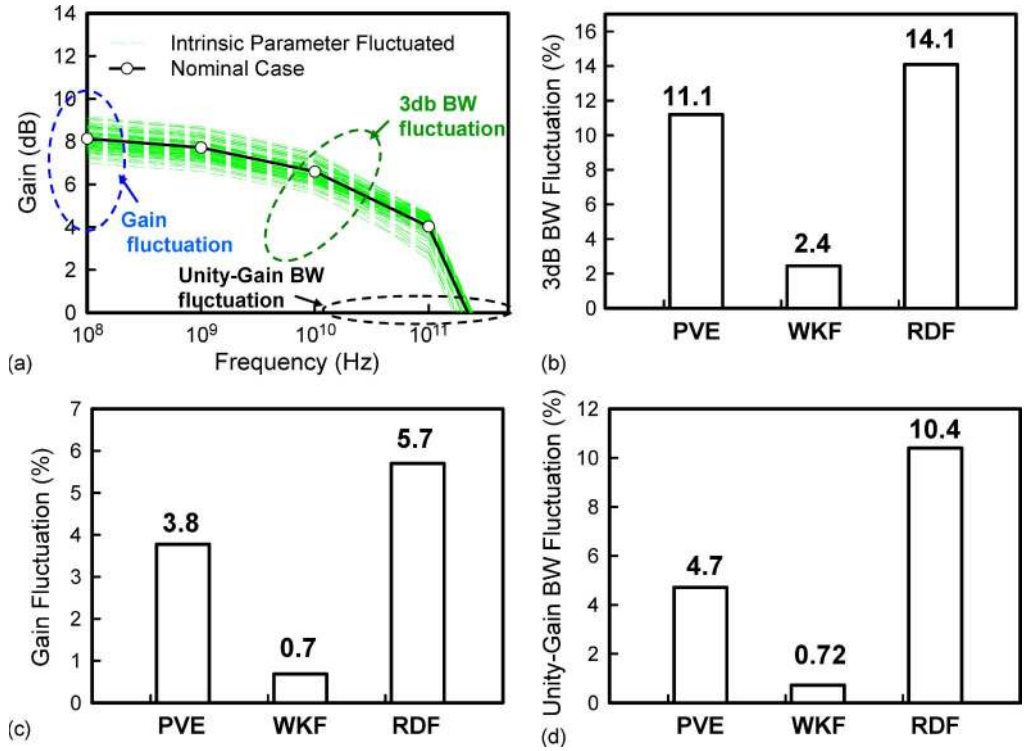


Fig. 10. (a) Frequency response of the planar MOSFET CS amplifiers, in which (b) 3-dB bandwidth, (c) gain, and (d) unity-gain bandwidth fluctuations are extracted.

## IV. Conclusion

In this paper, we have estimated the influences of the intrinsic-parameter fluctuations in 16-nm planar MOSFETs and circuits. Our preliminary results have shown that the WKF and RDF dominate the device threshold-voltage fluctuation and therefore rule the delay time of the explored digital inverter circuits. The fluctuation of delay time depends on the $V_{\rm th}$ fluctuation which follows the trend of $V_{\rm th}$ fluctuation. The

WKF effect in PMOSFETs may bring significant impact on $t_{\mathrm{LH}}$ characteristics due to the large difference of work function in different grain orientations. The total power fluctuation including the fluctuations of the dynamic, short-circuit, and static powers is about 15.2% for the planar MOSFETs, which may induce significant performance uncertainties, such as temperature and timing, to degrade the reliability of circuits and systems. The dynamic and short-circuit powers are the most important power-dissipation sources. However, the static-power fluctuation dominates the total power fluctuation due to the exponential relationship between the leakage current and the $V_{\mathrm{th}}$. The significant leakage-power fluctuation was further investigated, which should be considered in robust circuit and system design. For the high-frequency characteristics, the circuit gain, the power, and the power-added efficiency were also explored. Similar to the trend of the device cutoff frequency, the PVE and RDF dominate the device and circuit characteristic fluctuations, and the WKF shows less impact on high-frequency characteristics, owing to the small gate-capacitance fluctuation. The sensitivities of circuit performance with respect to device parameter fluctuation have been reported. It is necessary to include both the WKF and RDF effects in studying digital-circuit reliability; however, for the high-frequency applications, the PVE and RDF effects are dominating factors. We are currently working on the study of the possible correlations between each fluctuation source. The interaction of $V_{\mathrm{th}}$ change due to different sources may be important and need to be properly incorporated. Additionally, the 3-D Monte Carlo device simulation with, for example, *ab initio* impurity scattering [17], [26], may provide more rich physical insights and accurate estimations, which will also be addressed in our future work.

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**Yiming Li** (M'02) received the B.S. degree in applied mathematics and electronics engineering, the M.S. degree in applied mathematics, and the Ph.D. degree in electronics from the National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1996, 1998, and 2001, respectively.

In 2001, he joined the National Nano Device Laboratories (NDL), Hsinchu, as an Associate Researcher, and the Microelectronics and Information Systems Research Center (MISRC), NCTU, as an Assistant Professor, where he has been engaged in the field of computational science and engineering, particularly in modeling, simulation, and optimization of nanoelectronics and very large scale integration (VLSI) circuits. In the fall of 2002, he was a Visiting Assistant Professor with the Department of Electrical and Computer Engineering, University of Massachusetts, Amherst. From 2003 to 2004, he was a Research Consultant with the System on a Chip (SoC) Technology Center, Industrial Technology Research Institute, Hsinchu. From 2003 to 2005, he was the Director of the Departments of Nanodevice and Computational Nanoelectronics, NDL, and since the fall of 2004, he was an Associate Professor with MISRC. From the fall of 2005 to fall of 2008, he was an Associate Professor with the Department of Communication Engineering, NCTU, where he is currently a Full Professor with the Department of Electrical Engineering, is the Deputy Director of the Modeling and Simulation Center, and conducts the Parallel and Scientific Computing Laboratory. He is also the Deputy Director General of NDL. His current research areas include computational electronics and physics, physics of semiconductor nanostructures, device modeling, parameter extraction, VLSI circuit simulation, development of technology computer-aided-design (CAD) and electronic CAD tools and SoC applications, bioinformatics and computational biology, advanced numerical methods, parallel and scientific computing, optimization techniques, and computational intelligence. He has authored or coauthored over 120 research papers appearing in international book chapters, journals, and conferences. He has served as a Reviewer, Guest Associate Editor, Guest Editor, Associate Editor, and Editor for many international journals.

Dr. Li is a member of Phi Tau Phi, Sigma Xi, the American Physical Society, the American Chemical Society, the Association for Computing Machinery, the Institute of Electronics, Information and Communication Engineers, Japan, and the Society for Industrial and Applied Mathematics. He is included in *Who's Who in the World*. He was the recipient of the 2002 Research Fellowship Award presented by the Pan Wen-Yuan Foundation, Taiwan, and the 2006 Outstanding Young Electrical Engineer Award from the Chinese Institute of Electrical Engineering, Taiwan. He has served as a Reviewer for the IEEE TRANSACTIONS ON EVOLUTIONARY COMPUTATION, the IEEE TRANSACTIONS ON NANOTECHNOLOGY, the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE ELECTRON DEVICE LETTERS, and the IEEE TRANSACTIONS ON ELECTRON DEVICES. He has organized and served on several international conferences and was an Editor for proceedings of international conferences.

**Chih-Hong Hwang** (S'08) received the B.S. degree in engineering and system science and the M.S. degree in electronics engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2001 and 2003, respectively. He is currently working toward the Ph.D. degree in the Parallel and Scientific Computing Laboratory, Institute of Communication Engineering, National Chiao Tung University, Hsinchu.

His research interests focus on modeling and simulation of semiconductor nanodevices and variability of nano-CMOS devices and circuits.

Mr. Hwang was the recipient of the Bronze Medal of the 2008 TSMC Outstanding Student Research Award presented by Taiwan Semiconductor Manufacturing Company, Hsinchu, and the 2008 EDA Top-Notch International Conference Paper Award from Electronic Design Automation Consortium, Taiwan.

**Tien-Yeh Li** received the B.S. degree in electrical engineering from National Taiwan Ocean University, Keelung, Taiwan, in 2006. He is currently working toward the M.S. degree in the Parallel and Scientific Computing Laboratory, Institute of Communication Engineering, National Chiao Tung University, Hsinchu, Taiwan.

His research interests focus on modeling and simulation of semiconductor nanodevices, particularly nanomemory devices.

Mr. Li was the recipient of the 2008 EDA Top-Notch International Conference Paper Award from the Electronic Design Automation Consortium, Taiwan.

**Ming-Hung Han** (S'09) received the B.S. degree in communication engineering from National Chiao Tung University, Hsinchu, Taiwan in 2006, where he is currently working toward the M.S. degree in the Parallel and Scientific Computing Laboratory, Institute of Communication Engineering.

His research interests focus on modeling and simulation of high-frequency semiconductor nanodevices.