Processing and characterization of monolithic passive-matrix GaN-based microLED arrays with pixel sizes from 5 to 50 µm

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***Abstract* - MicroLED arrays with the capability of switching each pixel separately with high frequency can serve as structured micro-illumination light engines for applications in sensing, optogenetics, microscopy and many others. We describe a scalable chip process chain for the fabrication of passive-matrix microLED arrays, which were integrated with PCB-based driving electronics. The arrays were produced by deep-etching of conventional planar LED structures on sapphire, followed by filling and planarization steps. The pixel resolution lies in the range of 254 to 2540 pixels-per-inch (ppi), the arrays consist of 32 x 32 pixels. Optical output powers up to 50 µW per pixel were measured. In comparison to CMOS-based approaches, the presented technology is a simplified strategy to produce microLED arrays with high pixel counts.**

***Index Terms*—III-V semiconductor materials, Inorganic light-emitting diodes, Micro-light emitting diode array**

I. Introduction

InGaN/GaN-based LED technology has revolutionized the lighting sector in the past decades. Besides highly efficient solid-state lighting, ongoing developments of GaN LEDs have driven additional fields of applications, e.g. micro-display [1]–[4] or sensing [5]–[7]. For those purposes, shaping µm-sized emitters with individual control over each pixel is required, most conveniently in a periodic 2D array. GaN LEDs have substantial advantages over alternative technologies, including OLED and LCD, especially concerning brightness, lifetime and switching speed [3], [8], [9].

In the last years, several strategies for the realization of microLED arrays have been presented. In active matrix designs, an LED chip is directly bonded onto a CMOS backplane [8], [10]. This approach is favourable in terms of pixel reliability and performance. However, a sophisticated and expensive CMOS circuitry is required, which is affordable only in mass production. Moreover, hybrid integration of the LED array with the CMOS contacts is challenging, in particular when the dimensions approach the micrometer range [10], [11]. MicroLED arrays can also be realized monolithically on GaN, using one common contact (cathode or anode) and individual wires for the opposite contacts, which are arranged in a 2D array [12], [13]. Due to required space for wiring, this architecture only allows a limited number of pixels, but can be brought to a very high level of miniaturization with pixel sizes as low as 200 nm [14]. Still monolithic, but with enhanced scaling capabilities concerning the pixel number, passive-matrix approaches have been developed as an alternative [1], [15]–[17]. In this architecture, pixels are defined by orthogonal cathode and anode lines, which both need to be set to the according potential to activate the pixel located at the crossover of the two electrode lines.

Starting with a planar LED epilayer stack on sapphire, electrically insulated cathode lines can most conveniently be formed by etching through the complete semiconductor stack down to the insulating substrate, resulting in isolated fin structures. Particularly in case of small pixel sizes below 10 µm, this involves aspect ratios approaching unity, so that the fabrication of undisrupted crossing metal lines as anodes is not straightforward. Also, short circuits along the nearly vertical fin sidewalls must be prevented. So far, different strategies to address this issue have been presented, e.g. a multi-step or tapered etching profile of the fins to avoid high vertical steps [15], [17]. In other designs, the gaps in between the fins are filled, e.g., with SiO_2 or a polymer [1], [16], [18], [19]. Electrical access to the *p*-GaN is then provided by chemical mechanical polishing (CMP) or subsequent etching of openings into the dielectric layer.

The approach we present here uses a filling procedure based on benzocyclobuthene (BCB), which is planarized after spin-on by mechanical polishing to directly access the *p*-GaN surface. We demonstrate that this design enables the fabrication of small pixels down to the size of 5 µm, i.e., resolutions of up to 2540 ppi, which is smaller than what has previously been reported for the passive-matrix approach [16], [17]. Current transport in the cathodes is realized without additional metallization. Arrays of 32 x 32 pixels have been fabricated and integrated with PCB-based driving electronics, which can be controlled by a customized software. The fabrication scheme intends to enable the combination of small pixel sizes down to the micrometer

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range with high pixel numbers up to > 1000, without the need for a separate CMOS backplane. Such arrays can, for instance, be applied in chip-based microscopy techniques or optogenetics [20], [21].

II. MicroLED Array Fabrication and Driving Electronics

The microLED arrays are based on InGaN/GaN layers, which are produced in-house by metal-organic vapour phase epitaxy on c-plane sapphire substrates. They consist of a 4.4 µm thick *n*-GaN stack with silicon concentrations varying between $1x10^{18}$ and $3x10^{19}$ cm^{-3}, followed by a 4-fold InGaN multi-quantum well, an AlGaN-based electron blocking layer and 130 nm of *p*-doped GaN. The overall thickness of the LED epilayer is ~ 5.5 µm.

The entire processing chain is depicted in Fig. 1. As a first step, the cathode lines are fabricated. This is achieved by deep-etching fin structures with vertical sidewalls down to the insulating sapphire substrate, employing a combination of dry and wet chemical etching steps. A hardmask of 500 nm Cr is deposited via electron-beam evaporation and lift-off. In a first etching step, the sample is etched for 70 minutes by inductively-coupled plasma reactive ion etching (ICP-RIE) with SF_6 and H_2, removing most of the GaN material in the exposed areas. Remaining spikes are flattened by wet-etching in 1-molar KOH solution at 80 °C for 20 minutes. The resulting fin pattern is depicted in Fig. 2 a). At the ends of the fin structures, *n*-contact openings are defined by a second etching procedure, this time only removing the first 2 µm of GaN (see Fig. 1, step 5).

As a next step, undisrupted orthogonal metal lines without shorts to the *n*-GaN at the fin sidewalls need to be fabricated. Regarding the targeted pixel sizes of down to 5 µm, a planar surface is required for this step. Therefore, we developed a strategy to fill and subsequently planarize the trenches. BCB was chosen as a filling material, since it is known to be well suited for planarization issues from other applications [22], [23]. The BCB is spun onto the wafer at 4000 rpm, resulting in a roughly 2 to 3 µm thick film on top of the unetched GaN regions. After spin-coating, the polymer is hard-baked at 250 °C in nitrogen atmosphere for one hour. Across the fin structures, the BCB height varies with the topology of the sample, resulting in a wavy profile, as shown in Fig. 2 b). In particular for the smaller pixel sizes, the metal lines cannot overcome extended vertical steps, so that the height of the BCB over the GaN surface needs to be reduced and the whole surface needs to be planarized. We employed a mechanical polishing procedure for this, as sketched in Fig. 1, steps 6 to 8. A synthetic cloth and diamond particles of 1 µm size are used for polishing. The Cr hardmask, still covering the *p*-GaN, acts as a protective layer, since its removal rate during polishing is lower in comparison to BCB. Complete removal of the BCB on top of the GaN can easily be detected in an optical microscope. If polishing too long, unwanted dishing effects may occur, i.e., ongoing removal of BCB in between the fin structures [24],

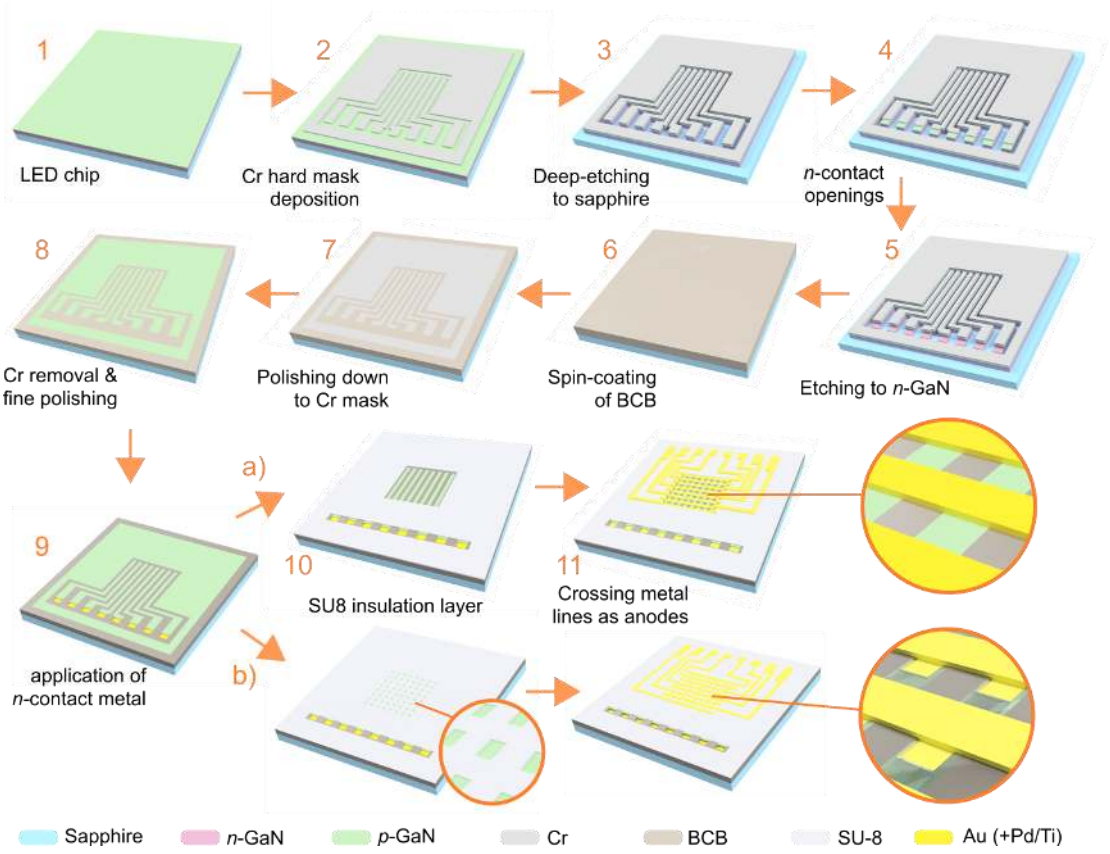

Fig. 1. Sketch of the processing scheme for matrix-addressed microLED arrays. The number of pixels was reduced to clarify the process. After step 9, two different schemes have been developed. In b), the SU-8 insulation layer covers the whole array and features pixel openings, into which the contact metal is then deposited, as visible in the detail view in step 11. In contrast to the previous images, the SU-8 is visualized transparent here.

[25]. The surface flatness can be optimized by designing the insulating trenches as small as possible. However, if chosen too small (< 5 µm), complete electrical separation by deep-etching becomes increasingly challenging, considering the GaN layer thickness of at least 5 µm.

After the first polishing step, the Cr hardmask is etched away wet-chemically. A fine polishing step with softer silica particles of 250 nm is conducted to level small surface inhomogeneities resulting from the Cr removal. The outcome of the complete polishing procedure is depicted in Fig. 2 c) and d). If polishing is done carefully, a smooth surface with alternating sections of GaN and BCB is reached. Subsequently, *n*-contact metal pads of 10 nm Ti and 300 nm Au are applied via electron beam deposition and lift-off (Fig. 1, step 9). On top of the planarized array, the orthogonal anode metal lines are deposited, as sketched in Fig. 1, step 11 a). They consist of 5 nm Pd and 35 nm Au. The thickness was chosen in order to ensure sufficient electrical conductivity at a certain level of optical transparency. Each anode is connected to a bond pad at the edge of the chip by a thicker lead of 300 nm Au. Prior to that, the wiring region is covered by an insulating layer of SU-8 to suppress electrical crosstalk.

A cross-section of an as-produced array is shown in Fig. 2 c). The active area is just 130 nm underneath the surface, meaning that short circuits of the above lying anodes to the *n*-GaN layer can easily occur, as also experienced within similar approaches [15]. This is particularly true at the interfaces between fins and BCB, where shallow grooves tend to form during the mechanical polishing. In order to increase the reliability of the devices, a second version of the LED arrays has been fabricated, where an additional 600 nm thick insulating layer of SU-8 also covers the region of the actual LED array (see Fig. 1, step 10 b). The layer contains pixel openings slightly smaller than the width of the fin structures. Again, an ohmic contact to the *p*-GaN is formed by evaporation of 5 nm Pd and 35 nm Au within the pixel openings, as captured by the SEM cross-section in Fig. 2 d). The pixels are connected with each other along one row and with the corresponding bond pad by 300 nm thick Au wires, forming just a partial overlap with the pixel area to avoid full shadowing of the light output. Microscopic images of the array geometry for both types are shown in Fig. 3.

An integrated circuit (IC) was designed in a standard HV-CMOS 0.35 µm process to drive the LED arrays. The driver consists of 32 anode and 32 cathode driving circuits, integrated in a 1.76 mm x 7.32 mm chip, as depicted in Fig. 4 a). The

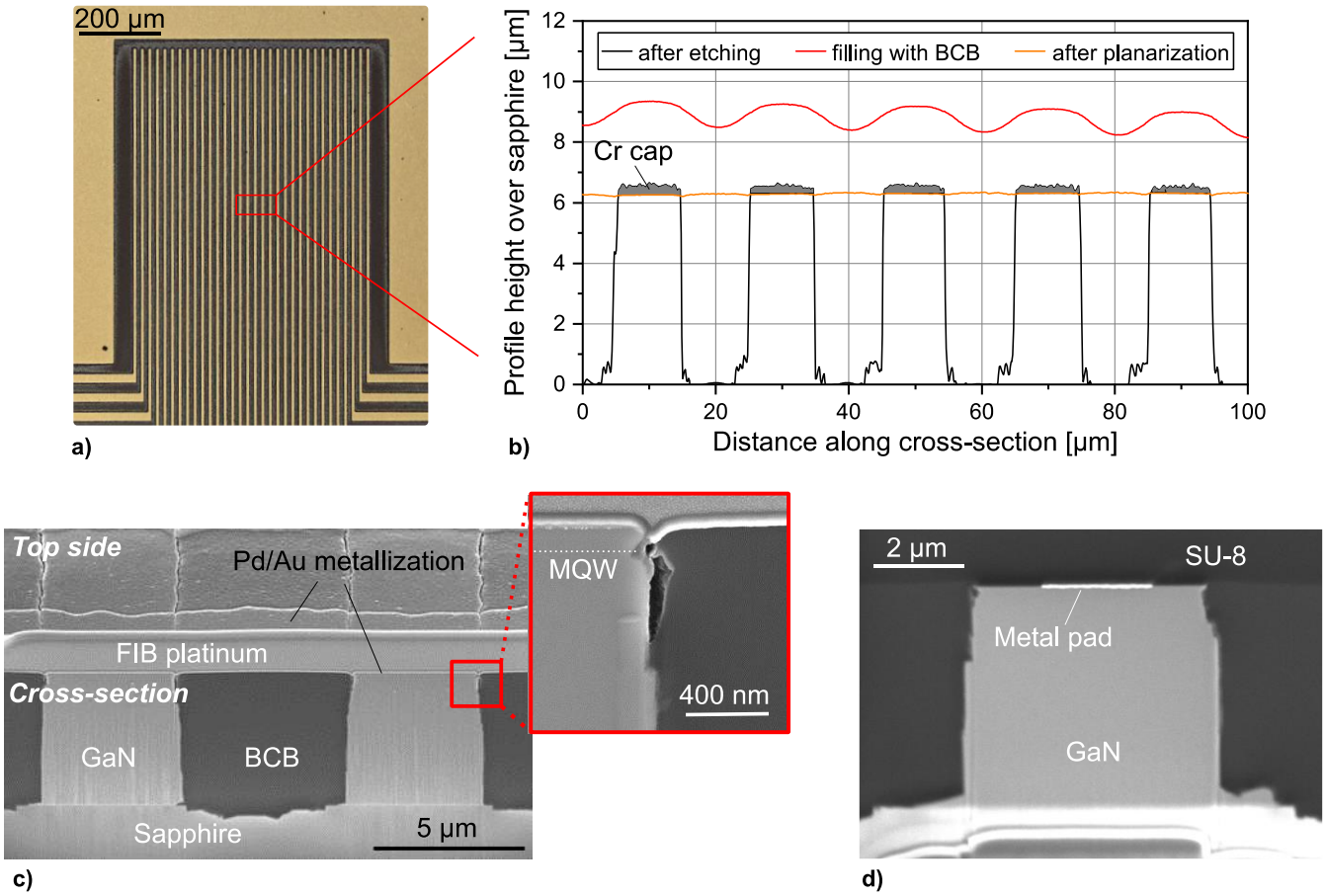

Fig. 2. a) Microscopic image of processed fins with 10 µm width as cathodes of a microLED array. b) Cross-sectional height profile along a line as marked in a) at different stages in the processing. The data was obtained by a confocal laser-scanning-microscope (LSM). c) Cross-sectional view of an array with 5 µm pixel size, without the insulating SU-8 interlayer in the pixel area. The inset shows a detailed view of the edge between GaN fin and BCB filling, revealing a high risk for short circuits. The cross-section was prepared in an SEM with a focused ion beam (FIB) unit. d) Similar to c), here showing the cross-section through a single fin with the additional SU-8 interlayer, reducing the risk of short circuits.

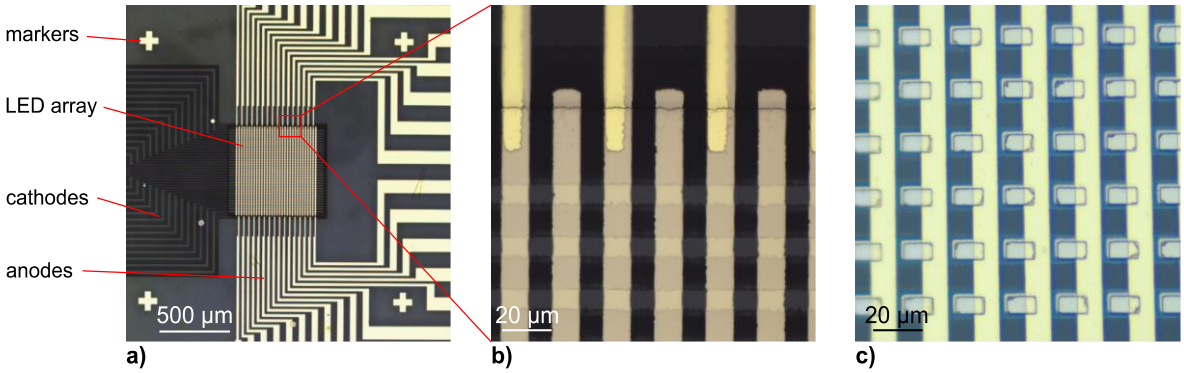

Fig. 3. Microscopic images of completely processed microLED arrays. a) Overview. b) Margin area of an array without SU-8 based insulation layer in the pixel area. Vertically running anodes made of thin, semi-transparent metal partly overlap with the thicker wires leading to the bond pads. c) Modified approach with additional thin insulation layer and opening for each pixel, which are covered with a thin metallization.

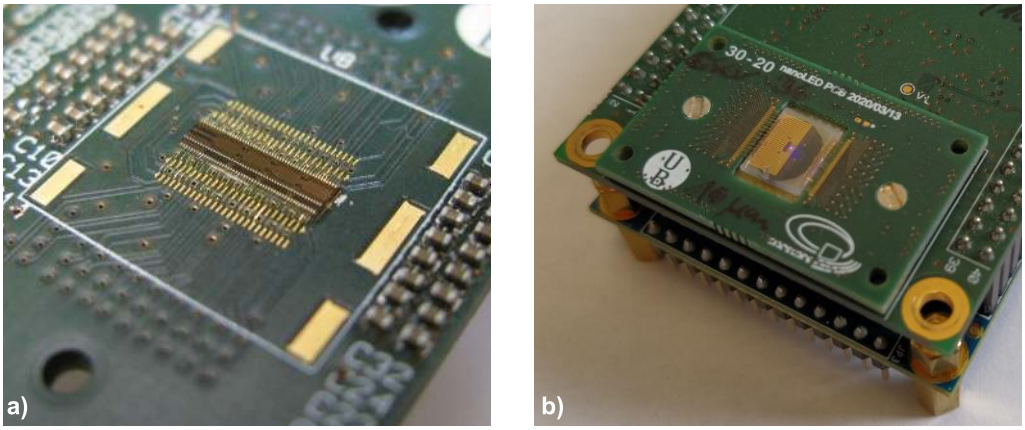

Fig. 4. a) The LED driver is wire-bonded to the main PCB with 64 wires. b) The separate PCB with the mounted GaN LED chip, which is connected to the main PCB by an interposer.

distribution of the driving circuits on the chip consists of two rows, one with the anode drivers and the other one with the cathode drivers. Therefore, the driving chip can manage up to 1024 LEDs arranged in a 32 x 32 matrix-addressable array. The driving circuits can perform pulses up to 10 V and supply signals from DC down to 700 ps and 10 ns full width half maximum (FWHM) for the anode and cathode driver, respectively. To operate, the driving circuit sets the voltage in the anode nodes to 0 V and the voltage in the cathode nodes to the desired LED bias voltage (up to 10 V). Then, to turn on an LED in the array, the cathode circuit switches the selected LED cathode to 0 V. After that, the anode circuit switches the anode of the LED to the bias voltage, which causes only the desired LED to emit light. The rest of the LEDs in the same row and column of the activated LED remain at 0 V anode-cathode voltage and the rest of the array remains reverse-biased, with a cathode-anode voltage of LED bias voltage.

The driver IC is connected to the main PCB by wire bonds, as shown in Fig. 4 a). For the GaN-based LED array, a separate smaller PCB has been designed, which features a recess for the chip, as depicted in Fig. 4 b). Also here, 2 x 32 wire bonds are used for electrical connections. The separate PCB is connected to the main board by an interposer, which enables an easy exchange of the LED array.

III. Electrical Characterization of the MicroLED Arrays

In Fig. 5 d), microscopic images of functional microLED arrays with pixel sizes from 5 to 50 µm are depicted, demonstrating the scalability of the presented approach. In Fig. 5 a), characteristic IV curves from arrays with and without the additional SU-8 layer on top of the planarized BCB in the pixel area are compared. For voltages below the threshold of ~ 3 V, the benefit of the additional insulation layer with respect to leakage currents becomes apparent, since the current is reduced by 2 to 3 orders of magnitude by this measure. A drastic reduction of leakage current by the SU-8 layer is also present under reverse bias conditions, as shown in the inset in Fig. 5 a). For the 5 µm pixels, no measurable leakage current can be detected up to -5 V. For voltages above the turn-on of ~ 3 V, the arrays with additional insulation still show noticeably lower currents. This feature is probably caused by higher contact resistances between the *p*-GaN and the Pd/Au metallization and is not generally related to the modified structure. For a further analysis of the IV behaviour in the high-current regime, arrays with good contact quality have been employed, i.e., without the additional SU-8 layer. In this regime, when the actual LED junction becomes highly conductive, leakage currents play a minor role for the IV behaviour.

Characteristic IV curves for such arrays are plotted in Fig. 5 c), using a linear current scale. For voltages > 4 V, the IV curves approach a constant slope, which is defined by the series resistance R_S. The value of R_S varies with the pixel size, resulting in an increased current through the bigger pixels, as discussed in more detail below. In Fig. 5 b), the resulting current density through the LED junction is plotted. Apparently, the turn-on voltage is slighty lower for smaller pixels. In contrast to the absolute value of the current, the smaller microLEDs draw a higher current density at the same voltage compared to their larger counterparts. To understand this behaviour, the contributions to the series resistance are analyzed in more detail:

$$R_S = R_{Pad} + R_{Cathode} + R_{Anode} + R_{LED}$$
$$= R_{Pad} + \sum_k R_{\square,GaN} \cdot \frac{l_k}{d_k} + \sum_j R_{\square,Metal} \cdot \frac{l_j}{d_j} + \frac{R_{LED,\perp}}{d_P^2}. \quad (1)$$

In this consideration, R_{Pad} is the resistance of the contact pads, which should be independent of the pixel size. The leads from the bond pads on both sides to the pixels are composed of different segments with widths d_n and lengths l_n, as visible in the images in Fig. 5 d). These contributions sum up to the total cathode and anode resistances $R_{Cathode}$ and R_{Anode}. Finally, the series resistance R_{LED} of the emitting area itself is inversely proportional to the pixel area d_P^2. If R_{LED} was the main contribution to R_S, a comparable current density for all pixel sizes should be expected [26]. However, the current density decreases with the pixel size, as shown in Fig. 5 b), indicating that the remaining contributions in (1) constitute the main portion to the overall series resistance. On the side of the cathodes, the LED current is driven through the 4.4 µm thick *n*-GaN, without any metallization layer. Assuming a specific resistivity of ~ 0.05 Ωcm, the expected sheet resistance for the full GaN stack is in the range of 10 Ω/□ [27]. Even though the metal stack on the side of the anodes is just 300 nm thick, a two

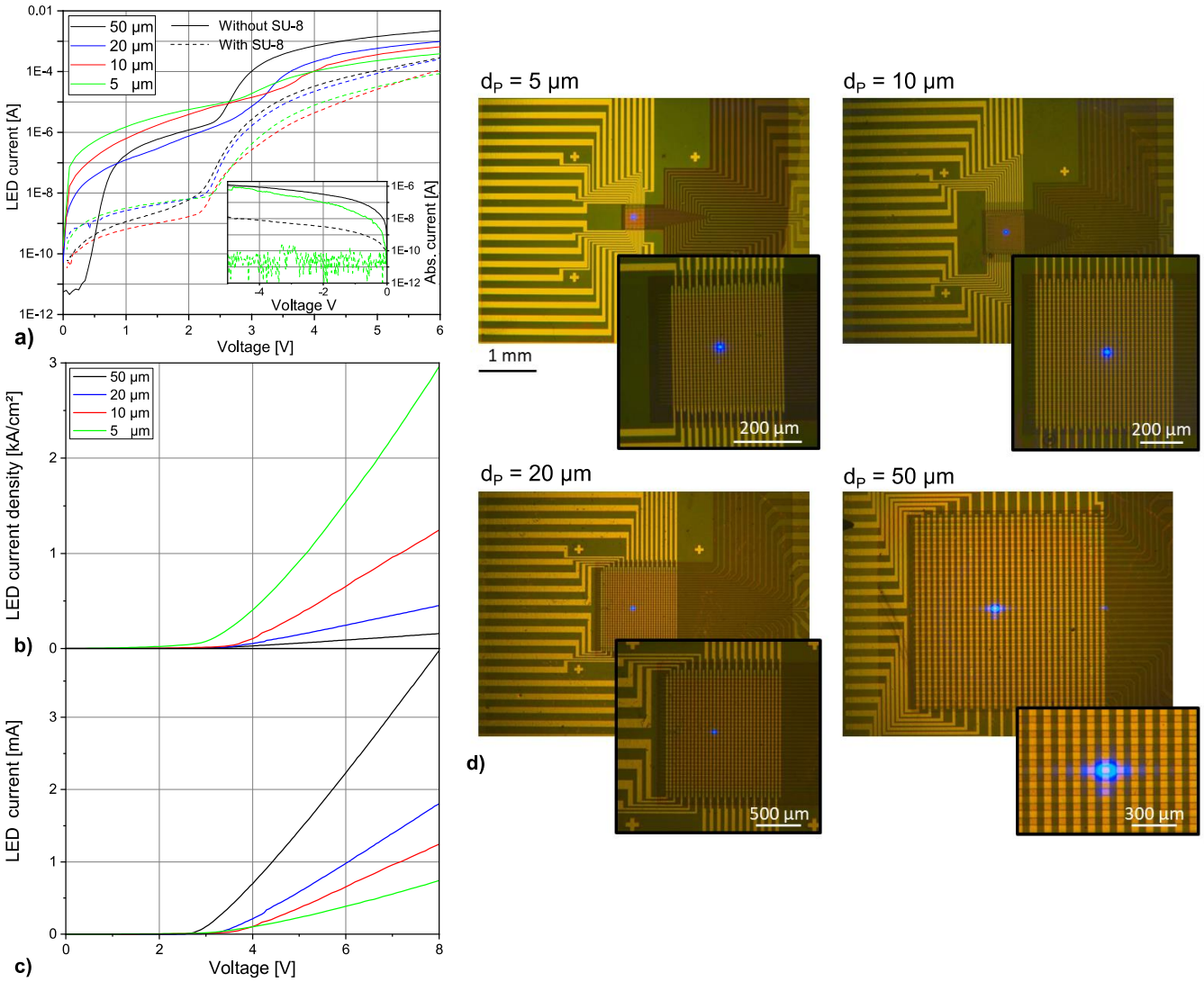

Fig. 5. a) Comparison of characteristic IV behaviour of the LED array with and without additional SU-8 protection layer, as introduced in Fig. 1. The inset shows the reverse bias behaviour for 5 and 50 µm pixels. b) and c) Characteristic LED current density and current as a function of bias voltage for different pixel sizes (LED arrays without additional SU-8 insulation layer). d) Microscopic images of different LED arrays with one active pixel. Note that the large images all share the same scale bar.

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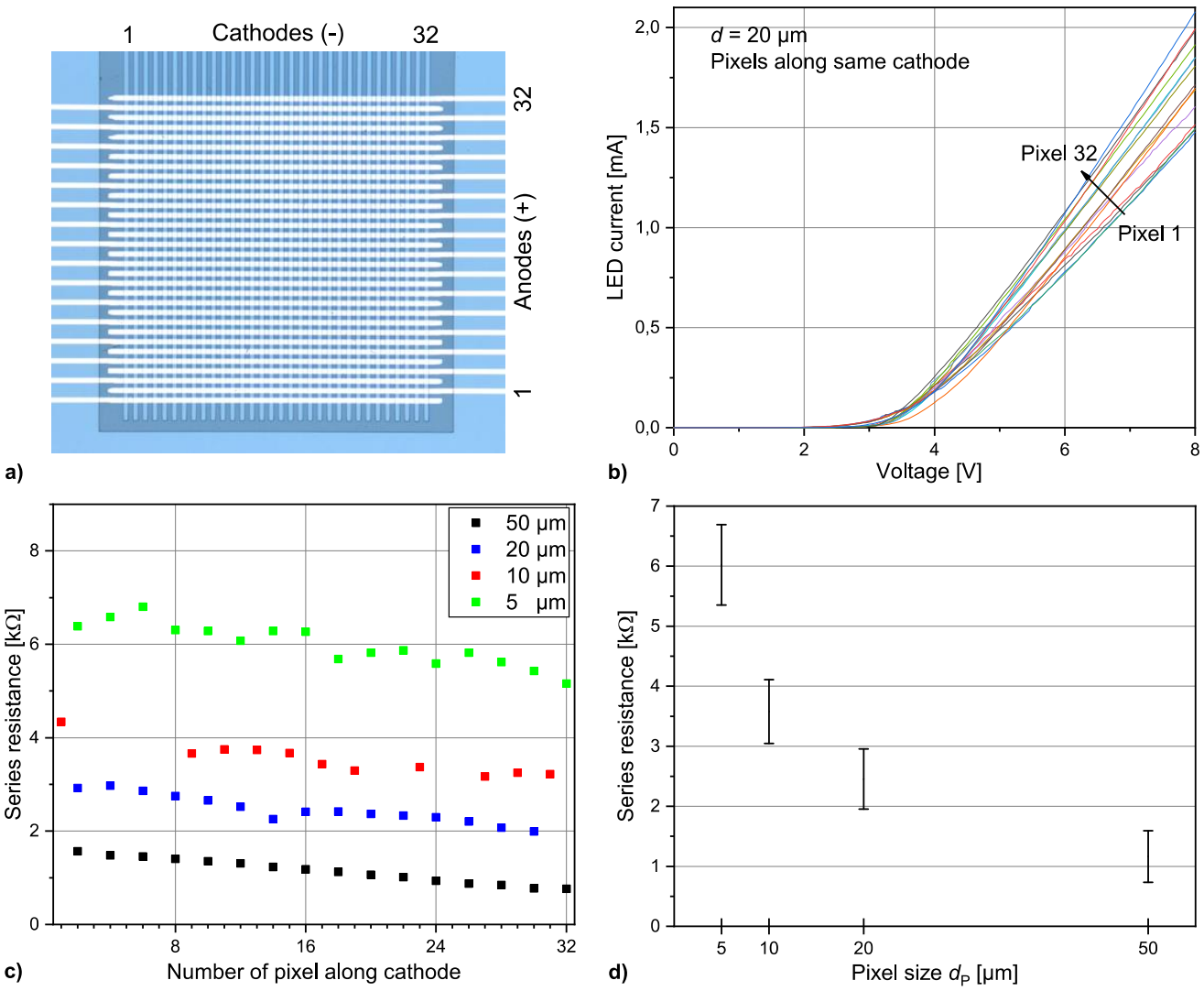

Fig. 6. a) Micrograph of an LED array with choice of indices. b) IV curves of various pixels along the same cathode for an array with 20 µm pixel size. c) Series resistances from IV curves as in b), for pixel sizes from 5 to 50 µm, obtained by a linear fit between 6 and 8 V. d) Span of the data points in c), plotted as a function of pixel size. R_S rougly scales with ${d_P}^{-1}$.

orders of magnitude smaller sheet resistance of $\sim 0.1\ \Omega/\square$ can be assumed due to the high specific resistivity of Au of $\rho \approx 2.5 \times 10^{-8}\ \Omega$m [28].

The impact of the sheet resistance $R_{\square,\mathrm{GaN}}$ can experimentally be analyzed when considering different pixels along the same cathode. Since $R_{\mathrm{Cathode}} \gg R_{\mathrm{Anode}}$ is assumed, the series resistance along the same cathode should differ by $R_{\square,\mathrm{GaN}} \cdot l/d_P$, where l describes the distance between two pixels and d_P their width. Exemplary plots for this analysis are shown in Fig. 6 b) and c). In Fig. 6 c), it can be seen that the series resistances show a linear trend along the cathodes, with similar slopes for all pixel sizes. Considering $l = 2 \cdot d_P$ for two neighbouring pixels, the GaN sheet resistances $R_{\square,\mathrm{GaN}}$ can be extracted, which yields the values listed in Table I. A slight variation with the fin width is apparent, especially in case of the 5 µm pixels. Due to the small fin width, the etched sidewalls may already have a reducing impact on the conductivity.

By building the sum $\sum_n R_{\square,\mathrm{GaN}} \cdot l_n/d_n$ with respect to the corresponding array design, the calculated values of the sheet resistances were utilized to estimate the corresponding cathode resistance $R_{\mathrm{C,Cath}}$ to the central pixels along the same cathode as before. As the results in Table I indicate, that sum coincides well with the measured total series resistance $R_{\mathrm{C,total}}$ of the central pixel, which was obtained from Fig. 6 c). Hence, the cathode leads create by far the largest part of the series resistance, which is composed as described in (1). The biggest fraction of the cathode wire resistance is contributed by the narrowest sections, i.e., by the fins of the LED array itself. Thus, the overall scaling law for the resistance should roughly follow ${d_P}^{-1}$, as confirmed by the data points in Fig. 6 d).

As a consequence, the design of the leads, especially on the cathode side, has a massive impact on the obtained IV behaviour and also dominates the variation of the series resistances across the array. As shown in a similar approach for an array of 50 µm pixels, the homogeneity of the IV curves improves noticeably when applying a buried metallization

along the cathodes [16]. However, due to the intention to scale the pixel pitch down to the low micrometer regime, this additional fabrication step was not pursued in the approach presented here.

Table I. Slopes from Fig. 6 c) and deduced sheet resistances $R_{\square,GaN}$ of the GaN fins. Those values were used to calculate the overall cathode resistance $R_{C,Cath}$ from the contact pad to the central pixel of the according cathode. For comparison, the measured series resistance $R_{C,total}$ of the central pixel is also listed.

Pixel size d_P [µm]	Slope from Fig. 6 c) [Ω]	$R_{\square,GaN}$ [Ω/□]	$R_{C,Cath}$ [kΩ]	$R_{C,total}$ [kΩ]
50	27.8±0.5	13.9±0.3	0.99±0.02	1.16±0.02
20	32±3	16.2±1.5	2.2±0.2	2.45±0.08
10	34±5	17.1±2.4	2.9±0.3	3.58±0.13
5	43±5	21.6±2.5	5.7±0.6	6.02±0.13

IV. Optical Characterization of Individual Pixels

A relative measurement of the emission properties has been conducted inside a scanning electron microscope (SEM) equipped with a customized cathodoluminescence (CL) detection setup. The CL setup consists of a parabolic mirror for light collection as well as a Czerny-Turner monochromator with a CCD camera. With a pair of microprobes a current can be driven through a selected pixel of the array. While the electron beam is blanked, the generated electroluminescence is detected by the CL setup with very high sensitivity. The fraction of light which is collected depends on the pixel position relative to the mirror. Hence, it can be regarded as constant when measuring spectra for different driving currents through the same pixel. Examples of the obtained spectra are depicted in Fig. 7 a). Arrays with the additional SU-8 insulation layer have been employed. The current densities have been calculated by measuring the exact area of the metal pads on top of the *p*-GaN in an optical microscope. Due to the very limited current spreading in *p*-GaN, this can well be assumed to correspond to the actual emission area [14]. The LED arrays emit at a central

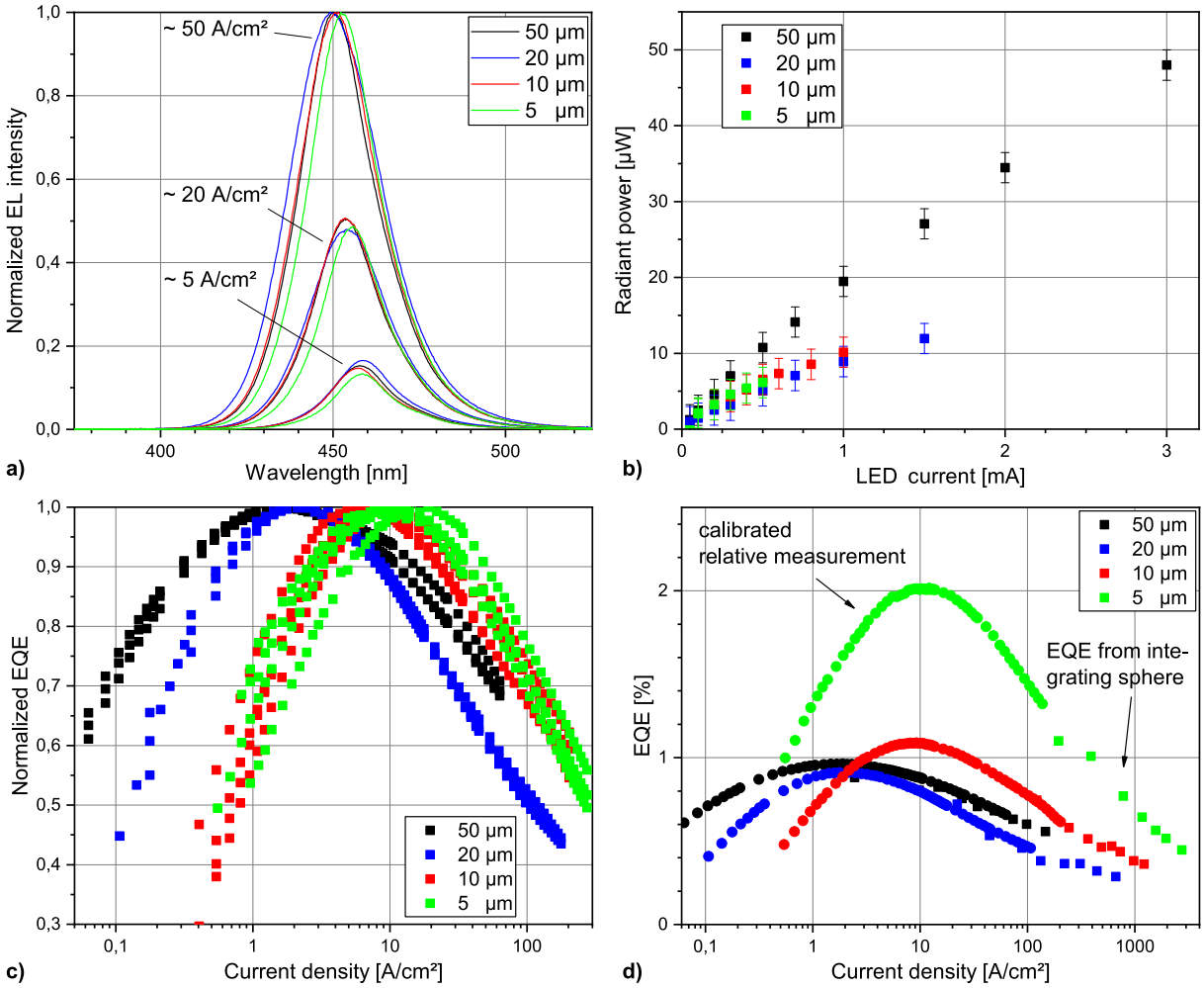

Fig. 7. Characterization of the light output of microLED arrays with an additional SU-8 insulation layer. In each case single pixels have been measured. a) Spectra obtained by electroluminescence inside the SEM. The maximum value at ~ 50 A/cm² driving current was taken as the reference for each pixel. b) Radiant power as a function of driving current, measured in a calibrated integrating sphere. c) Normalized efficiency of pixels of different sizes as a function of driving current. d) EQE obtained from the data points shown in b) (square points). The round points correspond to the data in c) and were fitted to the high-current points to complete the graph, assuming a constant LEE over current density.

wavelength of 450 to 460 nm and exhibit a blue shift with increasing current density, which is generally attributed to a screening of spontaneous and piezoelectric fields in the quantum wells at higher carrier densities [29], [30]. This trend appears for all pixel sizes, but is less prominent in case of the small 5 µm pixels, which might be due to a more homogeneous current spreading or higher non-radiative recombination and therefore smaller carrier concentration [26].

By an integration of the spectra over the relevant wavelength range, division by the driving current and subsequent normalization, relative external quantum efficiency (EQE) curves as depicted in Fig. 7 c) have been calculated. As consistently described in literature, the EQE shows a maximum at a certain current density. For low densities, non-radiative Shockley-Read-Hall (SRH) recombination dominates and for high densities, Auger recombination sets in [31]. The current density of maximum EQE shifts towards higher values for smaller pixel sizes, which is reported by other studies on size-dependent efficiency behaviour of microLEDs in a similar way [31]–[33]. Increased non-radiative SRH recombination at the plasma-etched sidewalls is a possible cause for this behaviour, which is promoted in case of high perimeter-to-area ratios, i.e., smaller pixel sizes [34]. The relative EQE curves show a good reproducibility for different pixels, even down to 5 µm pixel size.

In addition to the relative measurement inside the SEM, absolute values of the radiant power P_{opt} have been determined by using an integrating sphere of 10" diameter, connected to a calibrated spectrometer via a fiber. Due to the large diameter of the sphere, it is conceived for devices with higher output powers. Optical powers as low as 1 µW can be measured if the integration time is set accordingly (30 s in our case). However, a light output could not be detected for driving currents below 50 µA. The results of the absolute power measurement are depicted in Fig. 7 b). For all pixels, the slope decreases with the driving current since the data points are already situated in the droop regime. The maximum detected output power does not exceed 50 µW per pixel, which is reached for a 50 µm pixel around 100 A/cm² driving current. This is rather low when compared to conventional high-power LEDs and presumably due to a limited light extraction efficiency (LEE), caused by the metallic spreading layer for the top-emitting devices. The LEE could be increased by applying a *p*-contact with higher transparency, e.g., based on indium tin oxide (ITO) [16]. The obtained data points enable the calculation of absolute EQE values in the following manner:

$$\eta_{\mathrm{EQE}} = \frac{P_{\mathrm{opt}}}{I_{\mathrm{LED}} \cdot E_{\mathrm{Ph}}/e}\,. \qquad (2)$$

E_{Ph} corresponds to the average photon energy, which was deduced from the obtained spectra and ranged between 2.7 and 2.8 eV. The values of η_{EQE} are plotted in Fig. 7 d). In addition, the efficiency curves from the relative light output measurement shown in c) have been fitted to the course of the data points from the integrating sphere. Even though the data were obtained from different pixels, this matching is reasonable, since the relative shape of the efficiency curve is well reproducible for different pixels and can be assumed to behave identically in both setups. From the integrating sphere measurements, EQEs up to 1 % can be extracted, which rise up to 2 % when taking into account the values at lower current densities. These low values are again connected to the small LEE [34].

A clear trend in EQE with pixel size is not apparent, the values for the 5 µm pixels seem relatively high. Considering that EQE is the product of internal quantum efficiency (IQE) and LEE, one can try to further estimate the influences of the two factors on the resulting EQE. Drawing back onto the ABC model for recombination processes, the outcome of the relative measurement depicted in in Fig. 7 c) can be used to estimate corresponding IQE values [35]. This procedure has been conducted, yielding the values of maximum IQE listed in Table II. For the small pixel sizes, the measured efficiency curves increasingly deviate from the expectations of the ABC model, which leads to an inexact IQE analysis for the 5 µm pixels. It can be assumed that the decreasing trend of the IQE, as listed in Table II, continues for the 5 µm pixel size, again caused by a rising impact of SRH recombination [34]. Based on the maximum EQE and IQE values, the LEE has been calculated. Its increasing tendency with smaller emitter size can be explained geometrically, since emission to the metal covered top facet is facilitated at the pixel edges [32]. Counteracting size-dependent influences of IQE and LEE lead to the EQE behaviour depicted in Fig. 7 d).

Table II. Values of IQE_{max} calculated from Fig. 7 c), EQE_{max} taken from Fig. 7 d) and the deduced LEE.

Pixel size d_{P} [µm]	$\mathrm{IQE_{max}}$ [%]	$\mathrm{EQE_{max}}$ [%]	LEE [%]
50	75±3	1.0±0.2	1.3±0.3
20	46±5	0.9±0.2	2.0±0.5
10	39±10	1.1±0.2	2.8±0.9
5	< 40	2.0±0.4	> 5

V. Array Functionality

In Fig. 8, examples of LED arrays in operation are depicted, for pixel sizes from 5 to 50 µm. Basically, the functionality of the arrays is demonstrated for both types, i.e., with and without the insulating SU-8 layer. The presented images were recorded pixel by pixel, setting the integration time of the camera accordingly. In particular in case of the smaller pixel sizes, malfunctions may occur, as indicated in Fig. 8 c). A whole vertical row is activated here even though only two pixels of this row are addressed. This behaviour occurs when one anode is not properly connected to the corresponding pad of the PCB. Its potential is then set by the crossing cathodes, enabling the undesired crosstalk. The occurrence of such errors may be reduced by a redundant pair of leads to the anodes, connecting both ends of the anodes with the same potential on the PCB.

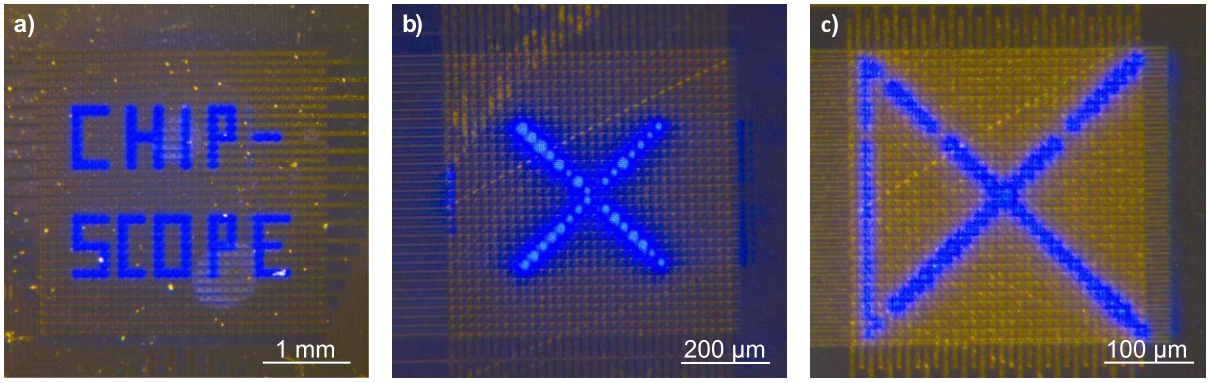

Fig. 8. Images of microLED arrays in operation. The pattern was displayed pixel by pixel, with an active time of several ms. a) Pixel size 50 µm, b) pixel size 10 µm, c) pixel size 5 µm. The vertical line on the left of c) was unintended and caused by a defect.

The polymers BCB and SU-8, which are used as passivation materials in this passive-matrix microLED array design, feature rather low thermal conductivities around 0.2 W m^{-1} K^{-1} [36], [37]. However, severe thermal degradation effects after longer operation times could not be detected at moderate driving currents. This is demonstrated by the long-time optical output measurement shown in Fig. 9.

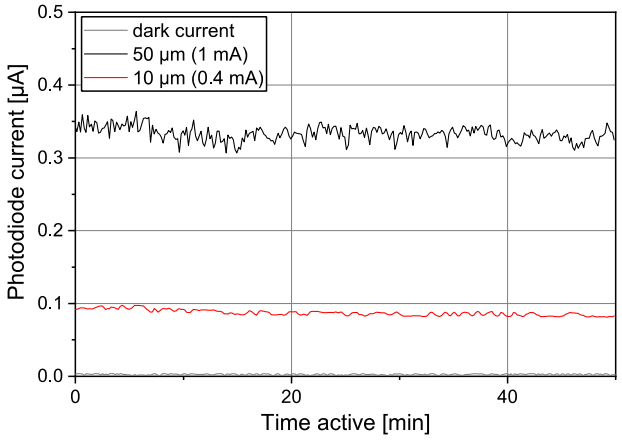

Fig. 9. Output power of a single pixel (10 and 50 µm pixel size) measured over 50 min. The signal was recorded by a photodiode, which was biased at -0.5 V.

VI. CONCLUSION

A fabrication scheme for passive-matrix microLED arrays based on GaN LED wafers with an emission wavelength of 450 to 460 nm has been implemented and analyzed. Arrays with 32 x 32 pixels and pixel sizes between 5 and 50 µm, with a pitch between 10 and 100 µm, have been realized. While etching fin structures as cathodes of the LED matrix is quite straightforward, the application of orthogonally running metal lines is more complex, since a planarization step is required. We solved this by using BCB as a filling material, which is then planarized by a mechanical polishing procedure. Even though direct application of the anode metal lines onto the as-prepared surface is feasible, an improved IV behaviour with a 2-3 orders of magnitude reduced leakage current is obtained by adding a thin SU-8 insulation layer with pixel openings smaller than the actual fin width. The series resistance of the individual pixels is mostly determined by the contribution of the GaN fin structures. The resistance depends on the fin width, which corresponds to the pixel size, and ranges between 1 and 7 kΩ. Resistance inhomogeneities over the array can potentially be accounted for by driving the pixels at constant current rather than voltage.

The light output characteristics have been studied in detail. The microLEDs reach a maximum IQE at current densities of 1 to 10 A/cm², which corresponds to the value of large-area LEDs. Obtained output powers, measured in an integrating sphere, reach up to 50 µW at currents of 3 mA. The corresponding EQEs are mostly restricted by a low LEE, which is due to the fact that the top-side emitting LEDs are covered by a thin metallization layer for current spreading. Size-dependent LEEs between 1 and 5 % have been calculated. These values could be enhanced by using *p*-GaN spreading layers with a higher optical transparency, e.g., ITO [16]. Alternatively, a flip-chip approach with backside emission through the sapphire substrate would increase the extraction efficiency [17]. The impact of sidewall defects at the plasma-etched fins, especially affecting the IQE in case of smaller pixels, could be reduced by additional passivation measures [38], [39].

The presented approach shows a possible path to implement passive-matrix LED arrays even down to pixel sizes in the low µm regime, i.e., with over 2500 ppi. The complexity of fabrication for such an array type is lower than utilizing a CMOS backplane. However, the produced arrays are more failure-prone when reducing the pixel size. Drawbacks like systematic variations in series resistance or a low LEE could be improved by a careful optimization of the design. Especially for larger pixel sizes, an additional cathode metallization should be used.

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REFERENCES

[1] W. C. Chong, W. K. Cho, Z. J. Liu, C. H. Wang, and K. M. Lau, "1700 pixels per inch (PPI) passive-matrix micro-LED display powered by ASIC," *Tech. Dig. - IEEE Compd. Semicond. Integr. Circuit Symp. CSIC*, pp. 6–9, 2014.

[2] T. Wu *et al.*, "Mini-LED and Micro-LED: Promising candidates for the next generation display technology," *Appl. Sci.*, vol. 8, no. 9, 2018.

[3] K. Ding, V. Avrutin, N. Izyumskaya, Ü. Özgür, and H. Morkoç, "Micro-LEDs, a manufacturability perspective," *Appl. Sci.*, vol. 9, no. 6, 2019.

[4] Y. Huang, E. L. Hsiang, M. Y. Deng, and S. T. Wu, "Mini-LED, Micro-LED and OLED displays: present status and future perspectives," *Light Sci. Appl.*, vol. 9, no. 1, 2020.

[5] H. S. Wasisto, J. D. Prades, J. Gülink, and A. Waag, "Beyond solid-state lighting: Miniaturization, hybrid integration, and applications of GaN nano-and micro-LEDs," *Appl. Phys. Rev.*, vol. 6, no. 4, 2019.

[6] O. Casals *et al.*, "A Parts per Billion (ppb) Sensor for NO 2 with Microwatt (μW) Power Requirements Based on Micro Light Plates," *ACS Sensors*, vol. 4, no. 4, pp. 822–826, 2019.

[7] G. Scholz *et al.*, "Continuous live-cell culture imaging and single-cell tracking by computational lensfree LED microscopy," *Sensors (Switzerland)*, vol. 19, no. 5, pp. 1–13, 2019.

[8] J. Herrnsdorf *et al.*, "Active-Matrix GaN Micro Light-Emitting Diode Display With Unprecedented Brightness," vol. 62, no. 6, pp. 1918–1925, 2015.

[9] M. S. Wong, S. Nakamura, and S. P. DenBaars, "Review—Progress in High Performance III-Nitride Micro-Light-Emitting Diodes," *ECS J. Solid State Sci. Technol.*, vol. 9, no. 1, p. 015012, 2020.

[10] F. Templier, "GaN-based emissive microdisplays: A very promising technology for compact, ultra-high brightness display systems," *J. Soc. Inf. Disp.*, vol. 24, no. 11, pp. 669–675, 2016.

[11] M. Y. Soh *et al.*, "Design and Characterization of Micro-LED Matrix Display with Heterogeneous Integration of GaN and BCD Technologies," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4221–4227, 2019.

[12] E. Xie *et al.*, "Design, Fabrication, and Application of GaN-Based Micro-LED Arrays with Individual Addressing by N-Electrodes," *IEEE Photonics J.*, vol. 9, no. 6, 2017.

[13] H. Huang *et al.*, "Characteristics of Micro-Size Light-Emitting Diode for Illumination and Visible Light Communication," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 215, no. 24, pp. 1–9, 2018.

[14] D. D. Bezshlyakh *et al.*, "Directly addressable GaN-based nano-LED arrays: fabrication and electro-optical characterization," *Microsystems Nanoeng.*, vol. 6, no. 1, 2020.

[15] W. Guo, J. Tai, J. Liu, and J. Sun, "Process Optimization of Passive Matrix GaN-Based Micro-LED Arrays for Display Applications," *J. Electron. Mater.*, vol. 48, no. 8, pp. 5195–5201, 2019.

[16] S. H. Yuan, S. S. Yan, Y. S. Yao, C. C. Wu, R. H. Horng, and D. S. Wuu, "Process Integration and Interconnection Design of Passive-Matrix LED Micro-Displays with 256 Pixel-Per-Inch Resolution," *IEEE J. Electron Devices Soc.*, vol. 8, no. July 2019, pp. 251–255, 2020.

[17] P. W. Chen *et al.*, "Improved Performance of Passive-Matrix Micro-LED Displays Using a Multi-Function Passivation Structure," *IEEE Photonics J.*, vol. 12, no. 4, 2020.

[18] C.-M. Kang *et al.*, "Fabrication of a vertically-stacked passive-matrix micro-LED array structure for a dual color display," *Opt. Express*, vol. 25, no. 3, p. 2489, 2017.

[19] C. Jeon, K. Kim, and M. D. Dawson, "Fabrication of Two-Dimensional InGaN-Based Micro-LED Arrays," vol. 328, no. 2, pp. 325–328, 2002.

[20] N. Franch *et al.*, "Nano illumination microscopy: a technique based on scanning with an array of individually addressable nanoLEDs," *Opt. Express*, vol. 28, no. 13, p. 19044, 2020.

[21] N. Grossman *et al.*, "Multi-site optical excitation using ChR2 and micro-LED array," *J. Neural Eng.*, vol. 7, no. 1, 2010.

[22] T. M. Stokich, C. C. Fulks, M. T. Bernius, D. C. Burdeaux, P. E. Garrou, and R. H. Heistand, "Planarization with Cyclotene™ 3022 (BCB) Polymer Coatings," *MRS Proc.*, vol. 308, pp. 517–526, 1993.

[23] D. Burdeaux, P. Townsend, J. Carr, and P. Garrou, "Benzocyclobutene (BCB) dielectrics for the fabrication of high density, thin film multichip modules," *J. Electron. Mater.*, vol. 19, no. 12, pp. 1357–1366, 1990.

[24] B. H. Kwon, J. H. Lee, H. J. Kim, S. S. Kweon, Y. G. Ryu, and J. G. Lee, "Dishing and erosion in STI CMP," *ICVC 1999 - 6th Int. Conf. VLSI CAD*, pp. 456–458, 1999.

[25] V. H. Nguyen, R. Daamen, H. van Kranenburg, P. van der Velden, and P. H. Woerlee, "A Physical Model for Dishing during Metal CMP," *J. Electrochem. Soc.*, vol. 150, no. 11, p. G689, 2003.

[26] Z. Gong *et al.*, "Size-dependent light output, spectral shift, and self-heating of 400 nm InGaN light-emitting diodes," *J. Appl. Phys.*, vol. 107, no. 1, 2010.

[27] M. R. Krames *et al.*, "Status and future of high-power light-emitting diodes for solid-state lighting," *IEEE/OSA J. Disp. Technol.*, vol. 3, no. 2, pp. 160–175, 2007.

[28] R. A. Matula, "Electrical Resistivity of Cu, Au, Pd, and Ag," *J. Phys. Chem*, vol. 6, no. 4. p. 1147, 1979.

[29] I. Otto *et al.*, "Micro-pixel light emitting diodes: Impact of the chip process on microscopic electro- and photoluminescence," *Appl. Phys. Lett.*, vol. 106, no. 15, 2015.

[30] H. W. Choi, C. W. Jeon, M. D. Dawson, P. R. Edwards, R. W. Martin, and S. Tripathy, "Mechanism of enhanced light output efficiency in InGaN-based microlight emitting diodes," *J. Appl. Phys.*, vol. 93, no. 10 1, pp. 5978–5982, 2003.

[31] A. Daami, F. Olivier, L. Dupré, F. Henry, and F. Templier, "59-4: *Invited Paper:* Electro-optical size-dependence investigation in GaN micro-LED devices," *SID Symp. Dig. Tech. Pap.*, vol. 49, no. 1, pp. 790–793, 2018.

[32] P. Tian *et al.*, "Size-dependent efficiency and efficiency droop of blue InGaN micro-light emitting diodes," *Appl. Phys. Lett.*, vol. 101, no. 23, 2012.

[33] Y. B. Tao *et al.*, "Size effect on efficiency droop of blue light emitting diode," *Phys. Status Solidi Curr. Top. Solid State Phys.*, vol. 9, no. 3–4, pp. 616–619, 2012.

[34] S. S. Konoplev, K. A. Bulashevich, and S. Y. Karpov, "From Large-Size to Micro-LEDs: Scaling Trends Revealed by Modeling," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 215, no. 10, pp. 1–6, 2018.

[35] S. Karpov, "ABC-model for interpretation of internal quantum efficiency and its droop in III-nitride LEDs: a review," *Opt. Quantum Electron.*, vol. 47, no. 6, pp. 1293–1303, 2015.

[36] S. Hwan Oh, K. C. Lee, J. Chun, M. Kim, and S. S. Lee, "Micro heat flux sensor using copper electroplating in SU-8 microstructures," *J. Micromechanics Microengineering*, vol. 11, no. 3, pp. 221–225, 2001.

[37] C. Hu, M. Kiene, and P. S. Ho, "Thermal conductivity and interfacial thermal resistance of polymeric low k films," vol. 79, no. 25, pp. 4121–4123, 2001.

[38] M. S. Wong *et al.*, "Size-independent peak efficiency of III-nitride micro-light-emitting-diodes using chemical treatment and sidewall passivation," *Appl. Phys. Express*, vol. 12, no. 9, 2019.

[39] S. Wolter *et al.*, "Size-dependent electroluminescence and current-voltage measurements of blue ingan/gan μleds down to the submicron scale," *Nanomaterials*, vol. 11, no. 4, 2021.