Open Forum

Prognostics and Health Management of Electronics

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***Abstract*—There has been a growing interest in monitoring the ongoing "health" of products and systems in order to predict failures and provide warning to avoid catastrophic failure. Here, health is defined as the extent of degradation or deviation from an expected normal condition. While the application of health monitoring, also referred to as prognostics, is well established for assessment of mechanical systems, this is not the case for electronic systems. However, electronic systems are integral to the functionality of most systems today, and their reliability is often critical for system reliability.**

This paper presents the state-of-practice and the current state-of-research in the area of electronics prognostics and health management. Four current approaches include built-in-test (BIT), use of fuses and canary devices, monitoring and reasoning of failure precursors, and modeling accumulated damage based on measured life-cycle loads. Examples are provided for these different approaches, and the implementation challenges are discussed.

***Index Terms*—Built-in-test (BIT), prognostics and health management (PHM).**

I. Introduction

Most products and systems contain some electronics to provide functionality and performance. These electronics are often the first item of the product or system to fail [1]–[3]. Assessing the extent of deviation or degradation from an expected normal operating condition (i.e., health) for electronics provides data that can be used to meet several critical goals, which include: 1) advance warning of failures; 2) minimizing unscheduled maintenance, extending maintenance cycles, and maintaining effectiveness through timely repair actions; 3) reducing the life-cycle cost of equipment by decreasing inspection costs, downtime, and inventory; and 4) improving qualification and assisting in the design and logistical support of fielded and future systems.

The term "diagnostics" pertains to the detection and isolation of faults or failures. "Prognostics" is the process of predicting a future state (of reliability) based on current and historic conditions. Prognostics and health management (PHM) is a method that permits the reliability of a system to be evaluated in its actual life-cycle conditions, to determine the advent of failure, and mitigate the system risks.

Safety-critical mechanical systems and structures—such as propulsion engines, aircraft structures, bridges, buildings, roads, pressure vessels, rotary equipment, and gears—have benefited from advanced sensor systems developed specifically for *in-situ* fault diagnosis (condition monitoring), and health and usage monitoring [4]–[9]. As a result, a considerable body of knowledge exists on prognostics and health management of mechanical systems, with research conducted in establishing failure precursors (such as changes in vibration signatures of roller bearings and variations in acoustic levels due to wear) and developing reasoning algorithms.

Degradation in electronics is more difficult to detect and inspect than most mechanical systems and structures, due to the micro- to nano-scale and the complex architecture of most electronic products. And since faults in electronic products may not necessarily lead to failure or loss of designated electrical performance or functionality, it is difficult to quantify product degradation and the progression from faults to final failure. In addition, there is a significant shortage of knowledge about the failure precursors in electronics [10]. Consequently, it can be more difficult to implement diagnostic and prognostic systems that can directly monitor the faults or conditions in which fault occurs in electronics.

In recent years, PHM has emerged as one of the key enablers for achieving efficient system-level maintenance and lowering life-cycle costs. In November 2002, the U.S. Deputy Under Secretary of Defense for Logistics and Materiel Readiness released a policy called condition-based maintenance plus (CBM+), [11]. CBM+ represents an effort to shift unscheduled corrective equipment maintenance of new and legacy systems to preventive and predictive approaches that schedule maintenance based upon the evidence of need.

The importance of PHM implementation was explicitly stated in the DoD 5000.2 policy document on defense acquisition, which states that "program managers shall optimize operational readiness through affordable, integrated, embedded diagnostics and prognostics, and embedded training and testing, serialized item management, automatic identification technology (AIT), and iterative technology refreshment" [12]. Thus, PHM has become a requirement for any system sold to the DOD. A 2005 survey of eleven CBM programs highlighted "electronics prognostics" as one of the most needed maintenance-related features or applications, without regard for cost [13], a view also shared by the avionics industry [14].

The Electronic Prognostics and Health Management Research Center at the University of Maryland has categorized the main approaches for PHM implementation as: 1) built-in-test (BIT); 2) use of expendable devices, such as "canaries" and fuses that fail earlier than the host product to provide advance warning of failure; 3) monitoring and reasoning of parameters that are precursors to impending failure, such as shifts in performance parameters; and 4) modeling of stress and damage in electronic parts and structures utilizing exposure conditions (e.g., usage, temperature, vibration, radiation) to compute accumulated damage. Challenges are posed for *in-situ* monitoring, fault diagnosis, and remaining life prediction.

II. Built-in-Test

The first efforts in diagnostic health monitoring of electronics involved the use of BIT. BIT is defined as an on-board hardware-software diagnostic means to identify and locate faults, and includes error detection and correction circuits, totally self-checking circuits, and self-verification circuits [15]. The equipment manufacturer sometimes provides BIT circuitry and software to allow the user to verify system functionality by providing access to internal nodes for comparison with known voltages or data patterns. BIT can also be used to debug, troubleshoot, and perform preventive maintenance.

Various levels of BIT include: 1) circuit-level BIT [also referred as built-in self-test (BIST)] for fault logging and diagnostics of individual circuits; 2) module- or assembly-level BIT that supports one or more circuit card assemblies, such as line-replaceable units; and 3) system-level BIT that performs diagnostics and operational testing of entire electronic systems. Among the earliest equipment available with BIT was the HP-3325A (1980) synthesizer function generator. BIT has

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since been used in diverse applications, including oceanographic systems, multichip modules, large-scale integrated circuits, power supply systems, avionics, and even passenger entertainment systems for the Boeing 767 and 777 [16].

Two types of BIT concepts are employed in electronic systems-interruptive BIT (I-BIT) and continuous BIT (C-BIT). The concept behind I-BIT is that normal equipment operation is suspended during BIT operation. Such BITS are typically initiated by the operator or occur during the power-up process. The concept behind C-BIT is that equipment is monitored continuously and automatically without affecting normal operation. Periodic BIT (P-BIT) is an I-BIT system that interrupts normal operation periodically in order to carry out a pseudocontinuous monitoring function. BIT concepts are still being developed to reduce the occurrence of spurious failure indications.

The nature of BIT depends on the nature of the equipment that it monitors. System-wide BIT may be centralized, controlling all BIT functions, or may comprise a number of BIT centers (often at the level of line-replaceable units) that communicate with each other and with a master processing unit that processes the results. A centralized BIT will often require dedicated hardware. BIT can also be incorporated and processed at the level of line-replaceable units to test the functionality of key circuits within a unit or on individual circuit cards. The advantage of BIT at this level is to help identify problems closer to the root cause, thus allowing cost-effective assembly and maintenance [16].

For example, a board-level BIT implemented by Motorola (MBIT), consisted of a diagnostic hardware and software package designed to verify the correct operation of board-mounted logical devices [17]. All tests could be executed at boot-up and selected tests ran continuously in the background of user applications. An application programming interface (API) was included to provide access to test results and to control the operation of device tests. The board-level MBIT consisted of hardware diagnostics and an API to control operation of the test driver suite. Examples of tested devices are the processor, L2 cache, VMEbus ASIC, ECC RAM, serial EPROM, Flash, NVRAM and real-time clock. Internal operation tests included checking register stuck-at conditions, register manipulations, and device setup instructions. The system-level MBIT, connects to all board-level versions to enable system-wide testing [17].

One of the early efforts in using monitored BIT and operational loads for maintenance analysis was the development of the time stress measurement device (TSMD). Broadwater, *et al.*, [18], [19] proposed the use of a microprocessor-based TSMD that can serve as a single-chip BIT and maintain logs between users and depot repair facilities. The primary objective of the TSMD was to store sub-system fault testing and environmental stress data. Thus, when a sub-system failure occurred, the TSMD would record the time stamp, the BIT fault code and the system mode. This data could be analyzed with the environmental stress data measured before, during, and after the fault event, and then used to constitute a fault signature for future diagnosis. However, this study identified intermittent failures and fault isolation ambiguity in electronic systems as a major obstacle in achieving the complete benefits of TSMD. Fault isolation ambiguity occurs in systems where the BIT is unable to discriminate failures between the BIT computer, various LRU's, and system interconnections.

Despite the apparent sophistication of BIT, there has been some concern that the requirement for BIT and the actual capabilities of BIT are not easy to match. For example, airline experience with modern avionics systems has indicated that spurious fault detection is unacceptably high. In 1996, Johnson [20] reported that the Lufthansa Airbus A 320 had a daily average of two thousand error logs on its BIT. About seventy of these corresponded with faults reported by pilots, while another seventy or so pilot reports of faults had no corresponding BIT log. Of the seventeen line-replaceable units replaced daily, typically only two were found to have faults that correlated with the fault indicated by the reports. Several studies [16], [20]–[23] conducted on the use of BIT for fault identification and diagnostics showed that BIT can be prone to false alarms and can result in unnecessary costly replacement, re-qualification, delayed shipping, and loss of system availability. However, there is also reason to believe that many of the failures were "real," but intermittent in nature [24].

The persistence of such issues over the years is perhaps due to the fact that the use of BIT has been restricted to low-volume systems. Thus, BIT has generally not been designed to provide prognostics or remaining useful life due to accumulated damage or progression of faults. It has served primarily as a diagnostic tool.

III. Fuses and Canaries

Expendable devices such as fuses and canaries have been a traditional method of protection for structures and electrical power systems. Fuses and circuit breakers are examples of elements used in electronic products to sense excessive current drain and to disconnect power from the concerned part. Fuses within circuits safeguard parts against voltage transients or excessive power dissipation, and protect power supplies from shorted parts. For example, thermostats can be used to sense critical temperature limiting conditions, and to shut down the product, or a part of the system, until the temperature returns to normal. In some products, self-checking circuitry can also be incorporated to sense abnormal conditions and to make adjustments to restore normal conditions, or to activate switching means to compensate for the malfunction [25].

The word "canary" is derived from one of coal mining's earliest systems for warning of the presence of hazardous gas using the canary bird. Because the canary is more sensitive to hazardous gases than humans, the death or sickening of the canary was an indication to the miners to get out of the shaft. The canary thus provided an effective early warning of catastrophic failure by providing advance warning that was easy to interpret. The same approach, using canaries, has been employed in prognostic health monitoring (PHM).

Canary devices mounted on the actual product can also be used to provide advance warning of failure due to specific wearout failure mechanisms. Mishra, *et al.*, [26] studied the applicability of semiconductor-level health monitors by using pre-calibrated cells (circuits) located on the same chip with the actual circuitry. The prognostics cell approach has been commercialized by Ridgetop Group (known as Sentinel Semiconductor technology) to provide an early-warning sentinel for upcoming device failures [27]. The prognostic cells are available for 0.35-, 0.25-, and 0.18-μn complementery metal oxide semiconductor (CMOS) processes; the power consumption is approximately 600 mW. The cell size is typically 800 μm^2 at the 0.25-μm process size. Currently, prognostic cells are available for semiconductor failure mechanisms such as electrostatic discharge (ESD), hot carrier, metal migration, dielectric breakdown, and radiation effects.

The time to failure of these prognostic cells can be precalibrated with respect to the time to failure of the actual product. Because of their location, these cells contain and experience substantially similar dependencies as does the actual product. These stresses that contribute to degradation of the circuit include voltage, current, temperature, humidity, and radiation. Since the operational stresses are the same, the damage rate is expected to be the same for both the circuits. However, the prognostic cell is designed to fail faster through increased stress on the cell structure by means of scaling.

Scaling can be achieved by controlled increase of the current density inside the cells. With the same amount of current passing through both circuits, if the cross-sectional area of the current-carrying paths in the cells is decreased, a higher current density is achieved. Further control

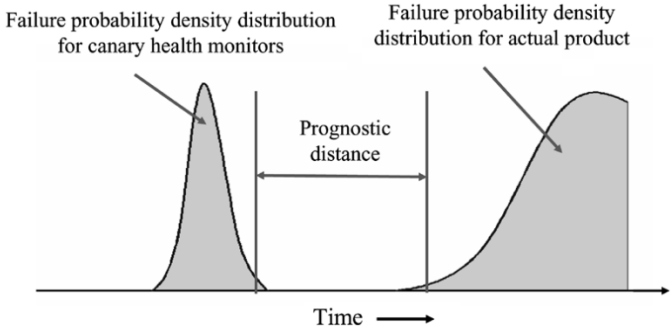

Fig. 1. Advance warning of failure using canary structures.

in current density can be achieved by increasing the voltage level applied to the cells. A combination of both of these techniques can also be used. Higher current density leads to higher internal (joule) heating, causing greater stress on the cells. When a current of higher density passes through the cells, they are expected to fail faster than the actual circuit [26].

Fig. 1 shows the failure distribution of the actual product and the canary health monitors. Under the same environmental and operational loading conditions, the canary health monitors wearout faster to indicate the impending failure of the actual product. Canaries can be calibrated to provide sufficient advance warning of failure (prognostic distance) to enable appropriate maintenance and replacement activities. This point can be adjusted to some other early indication level. Multiple trigger points can also be provided, using multiple cells evenly spaced over the bathtub curve.

The extension of this approach to board-level failures was proposed by Anderson, *et al.*, [28], who created canary components (located on the same printed circuit board) that include the same mechanisms that lead to failure in actual components. Anderson *et al.*, identified two prospective failure mechanisms: 1) low cycle fatigue of solder joints, assessed by monitoring solder joints on and within the canary package and 2) corrosion monitoring using circuits that will be susceptible to corrosion. The environmental degradation of these canaries was assessed using accelerated testing, and degradation levels are calibrated and correlated to actual failure levels of the main system. The corrosion test device included an electrical circuitry susceptible to various corrosion-induced mechanisms. Impedance Spectroscopy was proposed for identifying changes in the circuits by measuring the magnitude and phase angle of impedance as a function of frequency. The change in impedance characteristics would be correlated to indicate specific degradation mechanisms.

There remain unanswered questions with the use of fuses and canaries. For example, if a canary monitoring a circuit is replaced, what is the impact when the product is reenergized? What protective architectures are appropriate for post-repair operations? What maintenance guidance must be documented and followed when fail-safe protective architectures have or have not been included? This approach is difficult to implement in legacy systems, because it may require requalification of the entire system with the canary module. Also, the integration of fuses and canaries with the host electronic systems could be an issue with respect to real estate on semiconductors and boards. Finally, the company has to ensure that the additional cost of implementing PHM can be recovered through increased operational and maintenance efficiencies.

IV. Monitoring Precursors to Failure

A failure precursor is an event that signifies impending failure. A precursor indication is usually a change in a measurable variable that can be associated with subsequent failure. For example, a shift in the output voltage of a power supply would suggest impending failure due to damaged feedback regulator and opto-isolator circuitry. Failures can then be predicted by using a causal relationship between a measured variable that can be correlated with subsequent failure.

TABLE I
Potential Failure Precursors for Electronics

Electronic Subsystem	Failure Precursor Parameter
Switching power supply	- DC output (voltage and current levels) - Ripple - Pulse width duty cycle - Efficiency - Feedback (voltage and current levels) - Leakage current - RF noise
Cables and connectors	- Impedance changes - Physical damage - High-energy dielectric breakdown
CMOS IC	- Supply leakage current - Supply current variation - Operating signature - Current noise - Logic level variations
Voltage controlled oscillators	- Output frequency - Power loss - Efficiency - Phase distortion - Noise
FET	- Gate leakage current/resistance - Drain-source leakage current/resistance
Ceramic chip capacitors	- Leakage current/resistance - Dissipation factor - RF noise
General purpose diodes	- Reverse leakage current - Forward voltage drop - Thermal resistance - Power dissipation - RF noise
Electrolytic capacitors	- Leakage current/resistance - Dissipation factor - RF noise
RF power amplifier	- Voltage standing wave ratio (VSWR) - Power dissipation - Leakage current

A first step in PHM is to select the life-cycle parameters to be monitored. Parameters can be identified based on factors that are crucial for safety, that are likely to cause catastrophic failures, that are essential for mission completeness, or that can result in long downtimes. Selection can also be based on knowledge of the critical parameters established by past experience and field failure data on similar products and on qualification testing. More systematic methods, such as failure mode mechanisms and effects analysis (FMMEA) [29], can be used to determine parameters that need to be monitored.

Born and Boenning, [30] and Pecht *et al.*, [31] proposed several measurable parameters that can be used as failure precursors for electronic switching power supplies, cables and connectors, CMOS integrated circuits, and voltage-controlled high-frequency oscillators (see Table I). Testing was conducted to demonstrate the potential of select parameters to be viable for detection of incipient failures in electronic systems.

Supply current monitoring is routinely performed for testing of CMOS integrated circuits (ICs). This method is based upon the notion that defective circuits produce an abnormal or at least significantly different amount of current than the current produced by fault-free circuits. This excess current can be sensed to detect faults. The power supply current (I_{dd}) can be defined by two elements: the I_{ddq}-quiescent current and the I_{ddt}-transient or dynamic current. I_{ddq} is the leakage current drawn by the CMOS circuit when it is in a stable (quiescent) state. I_{ddt} is the supply current produced by circuits under test (CUT) during a transition period after the input has been applied. I_{ddq} has been reported to have the potential for detecting defects such as bridging, opens, and parasitic transistor

defects. Operational and environmental stresses such as temperature, voltage, and radiation can quickly degrade previously undetected faults and increase the leakage current (I_{ddq}). There is extensive literature on I_{ddq} testing, but only little has been done on using I_{ddq} for *in-situ* PHM. Monitoring I_{ddq} has been more popular than monitoring I_{ddt} [32]–[34].

Smith and Campbell [31] developed a quiescent current monitor (QCM) that can detect elevated I_{ddq} current in real time during operation. The QCM performed leakage current measurements on every transition of the system clock to get maximum coverage of the IC in real time. Pecuh *et al.* [33] and Xue and Walker [34] proposed a low-power built-in current monitor for CMOS devices. In the Pecuh *et al.* study, the current monitor was developed and tested on a series of inverters for simulating open and short faults. Both fault types were successfully detected and operational speeds of up to 100 MHz were achieved with negligible effect on the performance of the circuit under test. The current sensor developed by Xue and Walker enabled I_{ddq} monitoring at a resolution level of 10 pA. The system translated the current level into a digital signal with scan chain readout. This concept was verified by fabrication on a test chip.

It has been proposed by GMA Industries [35]–[37] to embed molecular test equipment (MTE) within ICs to enable them to continuously test themselves during normal operation and to provide a visual indication that they have failed. The molecular test equipment could be fabricated and embedded within the individual integrated circuit in the chip substrate. The molecular-sized sensor "sea of needles" could be used to measure voltage, current, and other electrical parameters, as well as sense changes in the chemical structure of integrated circuits that are indicative of pending or actual circuit failure. This research focuses on the development of specialized doping techniques for carbon nanotubes to form the basic structure comprising the sensors. The integration of these sensors within conventional IC circuit devices, as well as the use of molecular wires for the interconnection of sensor networks, is an important factor in this research. However, no product or prototype has been developed to date.

Kanniche and Mamat-Ibrahim [38] developed an algorithm for health monitoring of pulse-width modulation (PWM) voltage source inverters (VSIs). The algorithm was designed to detect and identify transistor open circuit faults and intermittent misfiring faults occurring in electronic drives. The mathematical foundations of the algorithm were based on discrete wavelet transform (DWT) and fuzzy logic (FL). Current waveforms were monitored and continuously analyzed using DWT to identify faults that may occur due to constant stress, voltage swings, rapid speed variations, frequent stop/start-ups, and constant overloads. After fault detection, "if–then" fuzzy rules were used for very large scale integration (VLSI) fault diagnosis to pinpoint the fault device. The algorithm was demonstrated to detect certain intermittent faults under laboratory experimental conditions.

Lall *et al.* [39], [40] have developed a damage precursor based residual life computation approach for various package elements to prognosticate electronic systems prior to the appearance of any macro-indicators of damage. In order to implement the system-health monitoring, precursor variables have been identified for various package elements and failure mechanisms. Model-algorithms have been developed to correlate precursors with impending failure for computation of residual life. Package elements investigated include, first-level interconnects, dielectrics, chip interconnects, underfills, and semiconductors. Examples of damage proxies include phase growth rate of solder interconnects, intermetallics, normal stress at chip interface, and interfacial shear stress. Lall *et al.* suggest that the precursor based damage computation approach eliminates the need for knowledge of prior or posterior operational stresses and enables the management of system reliability of deployed nonpristine materials under unknown loading conditions. The approach can be used on redeployed parts, subsystems, and systems, since it does not depend on availability of prior stress histories.

TABLE II
MONITORING PARAMETERS BASED ON RELIABILITY CONCERNS IN HARD DRIVES

Reliability Issues	Parameters Monitored
• Heads/head assembly - crack on head - head contamination or resonance - bad connection to electronics module • Motors/bearings - motor failure - worn bearing - excessive run-out - no spin • Electronic module - circuit/chip failure - interconnection/solder joint failure - bad connection to drive or bus • Media - scratch/defects - retries - bad servo - ECC corrections	• Head flying height: A downward trend in flying height will often precede a head crash. • Error Checking and Correction (ECC) use and error counts: The number of errors encountered by the drive, even if corrected internally, often signals problems developing with the drive. • Spin-up time: Changes in spin-up time can reflect problems with the spindle motor. • Temperature: Increases in drive temperature often signal spindle motor problems. • Data throughput: Reduction in the transfer rate of data can signal various internal problems.

Self-monitoring analysis and reporting technology (SMART) currently employed in select computing equipment for hard disk drives (HDDs) is another example of precursor monitoring [41], [42]. HDD operating parameters, including the flying height of the head, error counts, variations in spin time, temperature, and data transfer rates, are monitored to provide advance warning of failures (see Table II). This is achieved through an interface between the computer's start-up program (BIOS) and the hard disk drive.

Systems for early fault detection and failure prediction are being developed using variables such as current, voltage, and temperature, continuously monitored at various locations inside the system. Sun Microsystems refers to this approach as continuous system telemetry harnesses [43]. Along with sensor information, soft performance parameters such as loads, throughputs, queue lengths, and bit error rates are tracked. Prior to PHM implementation, characterization is conducted by monitoring the signals (of different variables) to learn a multivariate state estimation technique (MSET) model. Once the model is established using this data, it is used to predict the signal of a particular variable based on learned correlations among all variables [44]. Based on the expected variability in the value of a particular variable during application, a sequential probability ratio test (SPRT) is constructed. During actual monitoring the SPRT will be used to detect the deviations of the actual signal from the expected signal based on distributions (and not on single threshold value) [45], [46].

During implementation, the performance variables are continuously monitored using sensors already existing in Sun's servers and recorded in a circular file structure. The file retains data collected at high sampling rates for 72 h and data collected at a lower sampling rate for 30 days. For each signal being monitored, an expected signal is generated using the MSET model. This signal is generated in real time based on learned correlations during characterization (see Fig. 2). A new signal of residuals is generated, which is the arithmetic difference of the actual and expected time-series signal values. These differences are used as input to the SPRT model, which continuously analyzes the deviations and provides an alarm if the deviations are of concern [44]. The

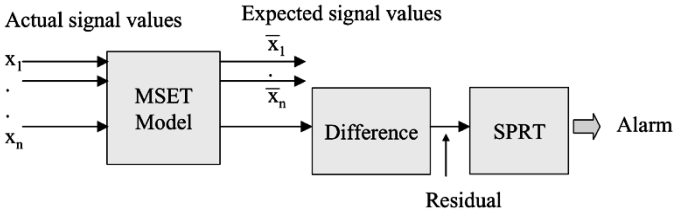

Fig. 2. SUN's approach to PHM.

monitored data is analyzed to 1) provide alarms based on leading indicators of failure and 2) enable use of monitored signals for fault diagnosis, root cause analysis of no-fault-founds (NFF), and analysis of faults due to software aging [43], [47].

Brown *et al.* [48] demonstrated that the remaining useful life of a commercial global positioning system (GPS) system can be predicted by using precursor to failure approach. The failure modes for GPS included precision failure due to an increase in position error and solution failure due to increased outage probability. These failure progressions were monitored *in-situ* by recording system-level features reported using the national marine electronics association (NMEA) protocol 0183. The GPS was characterized to collect the principal feature value for a range of operating conditions. The approach was validated by conducting accelerated thermal cycling of the GPS with the offset of the principal feature value measured *in-situ*. Based on experimental results, parametric models were developed to correlate the offset in the principal feature value with solution failure. During the experiment the BIT provided no indication of an impending solution failure [48].

In general to implement a precursor reasoning-based PHM system, it is necessary to identify the precursor variables for monitoring, and then develop a reasoning algorithm to correlate the change in the precursor variable with the impending failure. This characterization is typically performed by measuring the precursor variable under an expected or accelerated usage profile. Based on the characterization, a model is developed—typically a parametric curve-fit, neural-network, Bayesian network, or a time-series trending of a precursor signal. This approach assumes that there is one or more expected usage profiles that are predictable and can be simulated in a laboratory setup. In some products the usage profiles are predictable, but this is not always true.

For a fielded product with highly varying usage profiles, an unexpected change in the usage profile could result in a different (noncharacterized) change in the precursor signal. If the precursor reasoning model is not characterized to factor in the uncertainty in life-cycle usage and environmental profiles, it may provide false alarms. Additionally, it may not always be possible to characterize the precursor signals under all possible usage scenarios (assuming they are known and can be simulated). Thus, the characterization and model development process can often be time-consuming and costly and may not work.

V. Monitoring Environmental and Usage Loads

The life-cycle environment of a product consists of manufacturing, storage, handling, operating and nonoperating conditions. The life-cycle loads (Table III), either individually or in various combinations, may lead to performance or physical degradation of the product and reduce its service life [10]. The extent and rate of product degradation depends upon the magnitude and duration of exposure (usage rate, frequency, and severity) to such loads. If one can measure these loads *in-situ*, the load profiles can be used in conjunction with damage models to assess the degradation due to cumulative load exposures.

The assessment of the impact of life-cycle usage and environmental loads on electronic structures and components was studied by Ramakrishnan and Pecht [49]. This study introduced the life consumption monitoring (LCM) methodology (Fig. 3), which combined *in-situ* measured loads with physics-based stress and damage models for assessing the life consumed.

TABLE III
Examples of Life-Cycle Loads

Load	Load Conditions
Thermal	Steady-state temperature, temperature ranges, temperature cycles, temperature gradients, ramp rates, heat dissipation
Mechanical	Pressure magnitude, pressure gradient, vibration, shock load, acoustic level, strain, stress
Chemical	Aggressive versus inert environment, humidity level, contamination, ozone, pollution, fuel spills
Physical	Radiation, electromagnetic interference, altitude
Electrical	Current, voltage, power

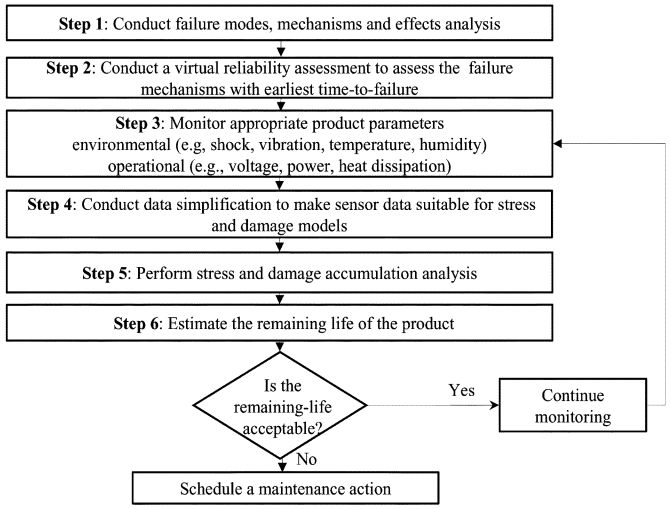

Fig. 3. CALCE life consumption monitoring methodology.

The application of the LCM methodology to electronics PHM was illustrated with two case studies [49], [50]. The test vehicle consisted of an electronic component-board assembly placed under the hood of an automobile and subjected to normal driving conditions in the Washington, DC, area. The test board incorporated eight surface-mount leadless inductors soldered onto an FR-4 substrate using eutectic tin-lead solder. Solder joint fatigue was identified as the dominant failure mechanism. Temperature and vibrations were measured *in-situ* on the board in the application environment. Using the monitored environmental data, stress and damage models were developed and used to estimate consumed life. The LCM methodology accurately predicted remaining life.

Mathew *et al.* [51] applied the LCM methodology in conducting a prognostic remaining-life assessment of circuit cards inside a space shuttle solid rocket booster (SRB). Vibration time history recorded on the SRB from the prelaunch stage to splashdown were used in conjunction with physics-based models to assess the damage caused due to vibration and shock loads. Using the entire life-cycle loading profile of the SRBs, the remaining life of the components and structures on the circuit cards were predicted. It was determined that an electrical failure was not expected within another 40 missions. However, vibration and shock analysis exposed an unexpected failure of the circuit card due to a broken aluminum bracket mounted on the circuit card. Damage accumulation analysis determined that the aluminum brackets had lost significant life due to shock loading.

Shetty *et al.* [52] applied the LCM methodology for conducting a prognostic remaining-life assessment of the end effector electronics unit (EEEU) inside the robotic arm of the space shuttle remote manipulator system (SMRS). A life-cycle loading profile for thermal and

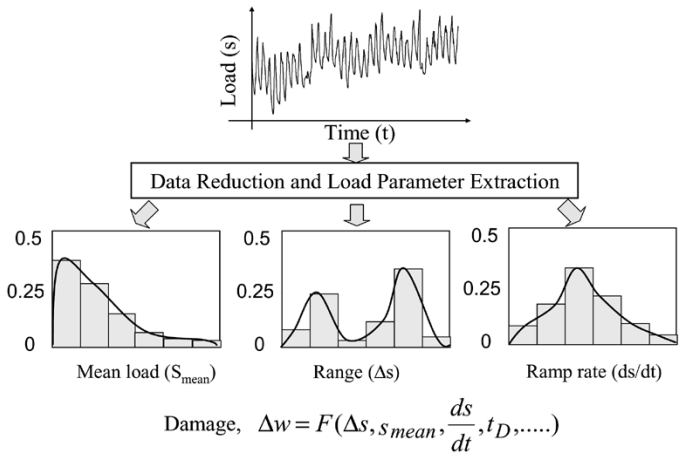

Fig. 4. CALCE PHM using monitored load histories.

vibrational loads was developed for the EEEU boards. Damage assessment was conducted using physics-based mechanical and thermomechanical damage models. A prognostic estimate using a combination of damage models, inspection, and accelerated testing showed that there was little degradation in the electronics and they could be expected to last another 20 years.

Vichare *et al.* [10] outlined generic strategies for *in-situ* load monitoring, including selecting appropriate parameters to monitor and designing an effective monitoring plan. Methods for processing the raw sensor data during *in-situ* monitoring to reduce the memory requirements and power consumption of the monitoring device were presented. Approaches were also presented for embedding intelligent front-end data processing capabilities in monitoring systems to enable data reduction and simplification (without sacrificing relevant load information) prior to input in damage models for health assessment and prognostics.

Embedding the data reduction and load parameter extraction algorithms in to the sensor modules as suggested by Vichare *et al.* [10] can lead to reduction in on-board storage space, low power consumption, and uninterrupted data collection over longer durations. As shown in Fig. 4, a time-load signal can be monitored *in-situ* using sensors, and further processed to extract (in this case) cyclic range (Δs), cyclic mean load (S_{mean}), and rate of change of load (ds/dt) using embedded load extraction algorithms. The extracted load parameters can be stored in appropriately binned histograms to achieve further data reduction. After the binned data is downloaded, it can be used to estimate the distributions of the load parameters. The usage history is used for damage accumulation and remaining life prediction.

Efforts to monitor life-cycle load data on avionics modules can be found in time-stress measurement device (TSMD) studies. Over the years the TSMD designs have been upgraded using advanced sensors [53], and miniaturized TSMD's are being developed due to advances in microprocessor and nonvolatile memory technologies [54].

Searls *et al.* [55] undertook *in-situ* temperature measurements in both notebook and desktop computers used in different parts of the world. In terms of the commercial applications of this approach, IBM has installed temperature sensors on hard drives (Drive-TIP) [56] to mitigate risks due to severe temperature conditions, such as thermal tilt of the disk stack and actuator arm, off-track writing, data corruptions on adjacent cylinders, and outgassing of lubricants on the spindle motor. The sensor is controlled using a dedicated algorithm to generate errors and control fan speeds.

Strategies for efficient *in-situ* health monitoring of notebook computers were provided by Vichare *et al.* [57]. In this study, the authors monitored and statistically analyzed the temperatures inside a notebook computer, including those experienced during usage, storage, and transportation, and discussed the need to collect such data both to improve the thermal design of the product and to monitor prognostic health. The temperature data was processed using two algorithms: 1) ordered overall range (OOR) to convert an irregular time-temperature history into peaks and valleys and also to remove noise due to small cycles and sensor variations and 2) a three-parameter Rainflow algorithm to process the OOR results to extract full and half cycles with cyclic range, mean, and ramp rates. The effects of power cycles, usage history, CPU computing resources usage, and external thermal environment on peak transient thermal loads were characterized.

The European Union funded a project from September 2001 through February 2005 named environmental life-cycle information management and acquisition for consumer products (ELIMA), which aimed to develop ways of better managing the life cycles of products using technology to collect vital information during a product's life to lead to better and more sustainable products [58], [59]. Though the focus of this work was not on prognostics, the project demonstrated the monitoring of the life-cycle conditions of electronic products by field trials. ELIMA partners built and tested two special prototype consumer products with data collection features, and investigated the implications for producers, users, and recyclers. The ELIMA technology included sensors and memory built into the product to record dynamic data such as operation time, temperature, and power consumption. This was added to static data about materials and manufacture. Both a direct communication (via GSM module) as well as a two-step communication with the database (RFID data retrieval followed by an Internet data transfer) was applied. As a case study, the member companies monitored the application conditions of a game console and a household fridge-freezer.

Skormin *et al.* [60] developed a data mining model based for failure prognostics of avionics units. The model provides a means of efficiently clustering data on parameters measured during operation, such as vibration, temperature, power supply, functional overload, and air pressure. These parameters are monitored *in-situ* on the flight using time-stress measurement devices. The objectives of the model are: 1) to investigate the role of measured environmental factors in the development of particular failure; 2) to investigate the role of combined effects of several factors; and 3) to reevaluate the probability of failure on the basis of known exposure to particular adverse conditions. Unlike the physics-based assessments made by Ramakrishnan and Pecht [49], the data mining model relies on the statistical data available from the records of a time-stress measurement device (TSMD) on cumulative exposure to environmental factors and operational conditions. The TSMD records, along with calculations of probability of failure of avionics units, are used for developing the prognostic model. The data mining enables an understanding of the usage history and allows tracing the cause of failure to individual operational and environmental conditions.

VI. PHM Integration

Implementing an effective PHM strategy for an entire system will involve integrating different health monitoring approaches. An extensive analysis may be required to determine the weak link(s) in the system to enable a more focused monitoring process. Once the potential failure modes, mechanisms, and effects have been identified, a combination of BIT, canaries, precursor reasoning, and life-cycle damage modeling may be necessary, depending on the failure attributes. In fact, different approaches can be implemented based on the same sensor data. For example, operational loads, such as temperature, voltage, supply current, and acceleration, can be collected by BIT. The current and temperature data can be used with damage models to calculate the susceptibility to

electromigration between metallizations. Also, the supply-current data can be used with precursor reasoning algorithms for identifying signs of transistor degradation.

Case studies of the integration of different approaches of PHM can be found in work by CALCE [61], [52] and R. Orsagh *et al.* [62], which used physics-based models for damage accumulation and precursor reasoning for system assessment. A detailed FMMEA[1] [29] was conducted and time to failure was assessed for the failure mechanisms identified by the FMMEA using appropriate failure models. The time-to-failures were ranked and a risk assessment was made based on severity and occurrence before PHM implementation [61]. In another PHM study [63], an off-the-shelf 50-W, dc-to-dc converter from a commercial power supply manufacturer was used. As in the CALCE studies [61], [52], a detailed *a-priori* analysis of power supply reliability issues was conducted in this case using the Pareto analysis of failures reported by the manufacturer. PHM techniques were then aimed at monitoring and predicting the most common failures.

Future electronic system designs will integrate sensing and processing modules that will enable *in-situ* PHM. Advances in sensors, microprocessors, compact nonvolatile memory, battery technologies, and wireless telemetry have already enabled the implementation of sensor modules and autonomous data loggers. For *in-situ* health monitoring, integrated, miniaturized, low-power, reliable sensor systems operated using portable power supplies (such as batteries) are being developed. These sensor systems have self-contained architecture requiring minimum or no intrusion into the host product in addition to specialized sensors for monitoring localized parameters. Sensors with embedded algorithms will enable fault detection, diagnostics, and remaining life prognostics that would ultimately drive the supply chain. The prognostic information will be linked via wireless communications to relay needs to maintenance officers and automatic identification techniques (RFID being the most common current example) will be used to locate parts in the supply chain—all integrated through a secure web portal to acquire and deliver replacement parts quickly on an as-needed basis.

REFERENCES

[1] C. T. Leonard and M. G. Pecht, "Improved techniques for cost effective electronics," in *Proc. Reliability Maintainability Symp.*, Jan. 29–31, 1991, pp. 174–182.

[2] M. Karyagina, "Designing for fault-tolerance in the commercial environment," in *Proc. Reliability Maintainability Symp.*, Jan. 22–25, 1996, pp. 258–262.

[3] A. A. Shapiro, S. X. Ling, S. Ganesan, R. S. Cozy, D. J. Hunter, D. V. Schatzel, M. M. Mojarradi, and E. A. Kolawa, "Electronic packaging for extended mars surface missions," in *Proc. IEEE Aerospace Conf.*, vol. 4, Mar. 6–13, 2004, pp. 2515–2527.

[4] I. Tumer and A. Bajwa, "A survey of aircraft engine health monitoring systems," in *Proc. AIAA*, 1999, pp. 1–6.

[5] E. P. Carden and P. Fanning, "Vibration based condition monitoring: A review," *J. Struct. Health Monitoring*, vol. 3, no. 4, pp. 355–377, 2004.

[6] P. Chang, A. Flatau, and S. Liu, "Review paper: Health monitoring of civil infrastructure," *J. Struct. Health Monitoring*, vol. 3, no. 3, pp. 257–267, 2003.

[7] M. Krok and K. Goebel, "Prognostics for advanced compressor health monitoring," in *Proc. SPIE*, vol. 5107, 2003, pp. 1–12.

[8] G. J. Kacprzynski, M. J. Roemer, G. Modgil, and A. Palladino, "Enhancement of physics of failure prognostic models with system level features," in *Proc. IEEE Aerospace Conf.*, vol. 6, 2002, pp. 2919–2925.

[9] J. Xie and M. Pecht, "Application of *in-situ* health monitoring and prognostic sensors," in *Proc. 9th Pan Pacific Microelectron. Symp. Exhibits Conf.*, Oahu, HI, Feb. 10–12, 2004.

[1]FMMEA is based on an understanding of the relationships between product requirements and the physical characteristics of the products (and their variation in the production process); the interactions of product materials with loads (stresses at application conditions); and their influence on product failure susceptibility with respect to use conditions.

[10] N. Vichare, P. Rodgers, V. Eveloy, and M. G. Pecht, "Monitoring environment and usage of electronic products for health assessment and product design," in *Proc. IEEE Workshop Accelerated Stress Testing Reliability (ASTR)*, Austin, TX, Oct. 2–5, 2005.

[11] Condition Based Maintenance Plus (2005). [Online]. Available: http://www.acq.osd.mil/log/mppr/CBM%2B.htm

[12] Department of Defense, *Performance Based Logistics: DoD 5000.2 Policy Document*. Washington, DC: Defense Acquisition Guidebook, Dec. 2004, ch. 5.3.

[13] D. Cutter and O. Thompson, "Condition-Based Maintenance Plus Select Program Survey," Tech. Rep. LG301T6, http://www.acq.osd.mil/log/mppr/CBM%2B.htm, Jan., Oct. 2005.

[14] L. V. Kirkland, T. Pombo, K. Nelson, and F. Berghout, "Avionics health management: Searching for the prognostics grail," in *Proc. IEEE Aerospace Conf.*, vol. 5, Mar. 6–13, 2004, pp. 3448–3454.

[15] R. Drees and N. Young, "Role of BIT in support system maintenance and availability," *IEEE A&E Syst. Mag.*, vol. 19, no. 8, pp. 3–7, Aug. 2004.

[16] M. Pecht, M. Dube, M. Natishan, and I. Knowles, "An evaluation of built-in test," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 37, no. 1, pp. 266–272, Jan. 2001.

[17] Motorola Built-In Test Diagnostic Software (2002). [Online]. Available: http://www.dot21rts.com/products/mbit%20datasheet.pdf

[18] S. P. Broadwater, T. A. Oblak, and L. J. Popyack, "Maintenance processor/time stress measurement device (MP/TSMD) use for failure trend analysis," in *Proc. Annu. Reliability Maintainability Symp.*, 1992, pp. 228–38.

[19] S. P. Broadwater and E. A. Cockey, "Time stress measurement device use for on-board diagnostic support," in *Proc. IEEE AUTOTESTCON'93*, Sep. 1993, pp. 251–8.

[20] D. Johnson, "Review of fault management techniques used in safety critical avionic systems," *Progr. Aerosp. Sci.*, vol. 32, no. 5, pp. 415–431, Oct. 1996.

[21] D. Allen, "Probabilities associated with a built-in-test system, focus on false alarms," in *Proc. IEEE Systems Readiness Technology Conf. (AUTOTESTCON)*, Sep. 22–25, 2003, pp. 643–645.

[22] R. X. Gao and A. Suryavanshi, "BIT for intelligent system design and condition monitoring," *IEEE Trans. Instrum. Meas.*, vol. 51, no. 5, pp. 1061–1067, Oct. 2002.

[23] D. Rosenthal and B. Wadell, "Predicting and eliminating built-in test false alarms," *IEEE Trans. Rel.*, vol. 39, no. 4, pp. 500–505, Oct. 1990.

[24] R. Williams, J. Banner, I. Knowles, M. Natishan, and M. Pecht, "An investigation of 'cannot duplicate' failure," *Qual. Rel. Eng. Int.*, vol. 14, pp. 331–337, 1998.

[25] A. Ramakrishnan, T. Syrus, and M. Pecht, Eds., *Avionics Handbook*. Boca Raton, FL: CRC, Dec. 2000, pp. 22–1–22–21.

[26] S. Mishra and M. Pecht, "*In-situ* sensors for product reliability monitoring," in *Proc. SPIE*, vol. 4755, 2002, pp. 10–19.

[27] "Hot Carrier (HC) Prognostic Cell," Ridgetop Semiconductor-Sentinel Silicon™ Library, Aug. 2004.

[28] N. Anderson and R. Wilcoxon, "Framework for prognostics of electronic systems," in *Proc. Int. Military Aerospace/Avionics COTS Conf.*, Seattle, WA, Aug. 3–5, 2004.

[29] S. Ganesan, V. Eveloy, D. Das, and M. G. Pecht, "Identification and utilization of failure mechanisms to enhance FMEA and FMECA," in *Proc. IEEE Workshop Accelerated Stress Testing Reliability (ASTR)*, Austin, Texas, Oct. 3–5, 2005.

[30] F. Born and R. A. Boenning, "Marginal checking—A technique to detect incipient failures," in *Proc. IEEE Aerospace Electron. Conf.*, May 22–26, 1989, pp. 1880–1886.

[31] M. G. Pecht, R. Radojcic, and G. Rao, *Guidebook for Managing Silicon Chip Reliability*. Boca Raton, FL: CRC, 1999.

[32] P. A. Smith and D. V. Campbell, "Practical implementation of BICS for safety-critical applications," in *Proc. IEEE Int. Workshop Current Defect Based Testing (DBT'00)*, Apr. 30, 2000, pp. 51–56.

[33] I. Pecuh, M. Margala, and V. Stopjakova, "1.5 Volts iddq/iddt current monitor," in *Proc. IEEE Can. Conf. Elect. Comput. Eng.*, vol. 1, May 9–12, 1999, pp. 472–476.

[34] B. Xue and D. M. H. Walker, "Built-in current sensor for IDDQ test," in *Proc. IEEE Int. Workshop Current Defect Based Testing (DBT'04)*, Apr. 25, 2004, pp. 3–9.

[35] R. G. Wright and L. V. Kirkland, "Nano-scaled electrical sensor devices for integrated circuit diagnostics," in *Proc. IEEE Aerospace Conf.*, vol. 6, Mar. 8–15, 2003, pp. 2549–2555.

[36] R. G. Wright, M. Zgol, D. Adebimpe, and L. V. Kirkland, "Functional circuit board testing using nanoscale sensors," in *Proc. IEEE Systems Readiness Technology Conf. (AUTOTESTCON'03)*, Sep. 22–25, 2003, pp. 266–272.

[37] R. G. Wright, M. Zgol, S. Keeton, and L. V. Kirkland, "Nanotechnology-based molecular test equipment (MTE)," *IEEE Aerosp. Electron. Syst. Mag.*, vol. 16, no. 6, pp. 15–19, Jun. 2001.
[38] M. S. Kanniche and M. R. Mamat-Ibrahim, "Wavelet based fuzzy algorithm for condition monitoring of voltage source inverters," *Electron. Lett.*, vol. 40, no. 4, Feb. 2004.
[39] P. Lall, N. Islam, K. Rahim, J. Suhling, and S. Gale, "Leading indicators-of-failure for prognosis of electronic and MEMS packaging," in *Proc. Electron. Comp. Technol. Conf.*, Las Vegas, NV, Jun. 1–4, 2004, pp. 1570–1578.
[40] P. Lall, N. Islam, and J. Suhling, "Prognostication and health monitoring of leaded and lead free electronic and MEMS packages in harsh environments," in *Proc. 55th IEEE Electron. Comp. Technol. Conf.*, Orlando, FL, Jun. 1–3, 2005, pp. 1305–1313.
[41] Self-Monitoring Analysis and Reporting Technology (SMART) (2005). [Online]. Available: http://www.pcguide.com/ref/hdd/perf/qual/featuresSMART-c.html
[42] G. F. Hughes, J. F. Murray, K. Kreutz-Delgado, and C. Elkan, "Improved disk-drive failure warnings," *IEEE Trans. Rel.*, vol. 51, no. 3, pp. 350–357, Sep. 2002.
[43] K. Gross, "Continuous System Telemetry Harness," Tech. Rep., [Online] Available: research.sun.com/sunlabsday/docs.2004/talks/1.03_Gross.pdf, 2005.
[44] K. Whisnant, K. Gross, and N. Lingurovska, "Proactive fault monitoring in enterprise servers," in *Proc. IEEE Int. Multiconf. Comput. Sci. Comput. Eng.*, Las Vegas, NV, Jun. 2005.
[45] K. Mishra and K. C. Gross, "Dynamic stimulation tool for improved performance modeling and resource provisioning of enterprise servers," in *Proc. 14th IEEE Int. Symp. Software Reliability Eng. (ISSRE'03)*, Denver, CO, Nov. 2003.
[46] K. Cassidy, K. C. Gross, and A. Malekpour, "Advanced pattern recognition for detection of complex software aging phenomena in online transaction processing servers," in *Proc. Int. Performance Dependability Symp.*, Washington, DC, Jun. 23–26, 2002.
[47] K. Vaidyanathan and K. C. Gross, "MSET performance optimization for detection of software aging," in *Proc. 14th IEEE Int. Symp. Software Reliability Eng. (ISSRE'03)*, Denver, CO, Nov. 2003.
[48] D. Brown, P. Kalgren, C. Byington, and R. Orsagh, "Electronic prognostics—A case study using global positioning system (GPS)," *Proc. IEEE AUTOTESTCON'05 Conf.*, Sep. 2005.
[49] A. Ramakrishnan and M. Pecht, "A life consumption monitoring methodology for electronic systems," *IEEE Trans. Comp. Packag. Technol.*, vol. 26, no. 3, pp. 625–634, Sep. 2003.
[50] S. Mishra, M. Pecht, T. Smith, I. McNee, and R. Harris, "Remaining life prediction of electronic products using life consumption monitoring approach," in *Proc. Eur. Microelectron. Packag. Interconnection Symp.*, Cracow, Poland, Jun. 16–18, 2002, pp. 136–142.
[51] S. Mathew, D. Das, M. Osterman, M. G. Pecht, and R. Ferebee, "Prognostic assessment of aluminum support structure on a printed circuit board," *ASME J. Electron. Packag.*, to be published.
[52] V. Shetty, D. Das, M. Pecht, D. Hiemstra, and S. Martin, "Remaining life assessment of shuttle remote manipulator system end effector," in *Proc. 22nd Space Simulation Conf.*, Ellicott City, MD, Oct. 21–23, 2002.
[53] N. Harchani, F. Jimenez, M. Almohamed, D. Esteve, and M. Courvoisier, "Time stress measurement device: System design and synthesis," in *Proc. SPIE*, vol. 4051, 2000, pp. 337–48.
[54] V. Rouet and B. Foucher, "Development and use of a miniaturized health monitoring device," in *Proc. IEEE Int. Reliability Phys. Symp.*, 2004, pp. 645–6.
[55] D. Searls, T. Dishongh, and P. Dujari, "A Strategy for enabling data driven product decisions through a comprehensive understanding of the usage environment," in *Proc. IPACK'01*, Kauai, HI, Jul. 8–13, 2001, pp. 1279–1274.
[56] G. Herbst, "IBM's Drive Temperature Indicator Processor (drive-TIP) Helps Ensure High Drive Reliability," Tech Rep., IBM, [Online] Available: www.hc.kz/pdf/drivetemp.pdf, Sep. 2005.
[57] N. Vichare, P. Rodgers, V. Eveloy, and M. G. Pecht, "*In-situ* temperature measurement of a notebook computer—A case study in health and usage monitoring of electronics," *IEEE Trans. Device Mater. Rel.*, vol. 4, no. 4, pp. 658–663, Dec. 2004.
[58] K. Bodenhoefer, "Environmental life cycle information management and acquisition—First experiences and results from field trials," in *Proc. Electron. Goes Green* 2004+, Berlin, Germany, Sep. 5–8, 2004, pp. 541–546.
[59] D-19 Final Report on ELIMA Prospects and Wider Potential for Exploitation (2005). [Online]. Available: www.ELIMA.org
[60] V. A. Skormin, V. I. Gorodetski, and L. J. Popyack, "Data mining technology for failure prognostic of avionics," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 38, no. 2, pp. 388–403, Apr. 2002.
[61] S. Mishra, S. Ganesan, M. Pecht, and J. Xie, "Life consumption monitoring for electronics prognostics," in *Proc. IEEE Aerospace Conf.*, vol. 5, Mar. 6–13, 2004, pp. 3455–3467.
[62] R. Orsagh, D. Brown, M. Roemer, T. Dabney, and A. Hess, "Prognostic health management for avionics power supplies," in *Proc. IEEE Aerospace Conf.*, Mar. 2005, pp. 1–7.
[63] D. Goodman, B. Vermeire, P. Spuhler, and H. Venkatramani, "Practical application of PHM/prognostics to COTS power converters," in *Proc. IEEE Aerospace Conf.*, Big Sky, MT, Mar. 5–12, 2005, pp. 1–6.

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