Program/Erase Scheme for Suppressing Interface Trap Generation in HfO_2-Based Ferroelectric Field Effect Transistor

Jinhong Min, Nicolo Ronchi, Sean R. C. McMitchell, Barry O'Sullivan, Kaustuv Banerjee, Geert Van den bosch, *Member, IEEE*, Jan Van Houdt, *Fellow, IEEE*, and Changhwan Shin, *Senior Member, IEEE*

***Abstract*— The endurance of the HfO_2-based ferroelectric FET (FeFET) is investigated using various program/erase (PG/ER) pulse schemes. The ramp time (T_{ramp}), which is the time to reach the PG/ER voltage, and the hold time (T_{hold}), which is the time duration to maintain the PG/ER voltage, are adjusted, and thereafter, their influence on endurance is observed through the memory window, subthreshold slope, and threshold voltage of the FeFET while the FeFET is cycled up to 10^4 by a sequence of PG/ER pulses. Both parameters are closely related to depassivating interface traps, and it turns out that a long T_{ramp} but short T_{hold} are desirable to suppress the interface trap generation in FeFET. The relation between T_{ramp}, T_{hold} and the interface trap generation is explained by the transient built-in electric field (which is generated by the transiently trapped carrier in the gate oxide when the gate voltage is swept rapidly).**

***Index Terms*— Ferroelectrics, FeFET, reliability, endurance.**

I. Introduction

THE discovery of ferroelectricity in doped hafnium oxide thin film resolved the long-standing retention and scalability problems of perovskite-based ferroelectric FET (FeFET) [1]–[4]. The HfO_2-based FeFET gate stack structure can be similar in structure to the one of NAND flash memory, therefore, being CMOS-process-compatible and capable of operating at low voltage. These properties make the HfO_2-based FeFET interesting as a next-generation memory device [4], [5]. A wide range of studies has been done on HfO_2-based FeFET to figure out optimal memory performance, as the Hf-based ferroelectric thin film can exhibit various properties depending on doping materials and fabrication condition [6]–[10].

Since the size of the memory window (MW), which is the threshold voltage (V_T) difference between program (PG) state and erase (ER) state, is one of the most important performance factors of the memory device, the evolution of the MW by PG/ER cycling has been extensively investigated [12]–[16]. At the initial stage of PG/ER cycling, the MW increases due to the wake-up effect of ferroelectric thin film. However, the MW widening by the wake-up is only observed at $\sim$ 0.1 % of the total number of PG/ER cycles. On the other hand, the MW closure is observed at $\sim$ 99 % of the number of P/E cycles because of the device degradation. Therefore, it is essential to minimize the influence of the degradation of the FeFET to stably store the data. For this purpose, the understanding of degradation mechanism of the FeFET according to PG/ER cycling has been studied [17], [18].

The FeFET has a thin interfacial oxide layer between the ferroelectric layer and the Si channel, which is closely related to the degradation of the FeFET. When PG/ER pulse is applied to the FeFET, electron tunneling occurs through the interfacial oxide, consequently the oxide trapping and/or interface trapping states are created. These oxide traps and interface traps cause MW closure and positive V_T shift. These two types of trapping are mainly known to affect the degradation of the FeFET.

There are many studies on the effects of various cycle waveforms adjusted for frequency or amplitude on the endurance of the ferroelectric capacitors, which is key component of the FeFET [19]–[21]. However, limited studies have investigated the influence of the shape of PG/ER pulse on the endurance of FeFET. In this work, the impact of the parameters constituting PG/ER pulse on the MW and SS of FeFET is intensively investigated, and the influence is explained with bipolar bias-temperature-instability (BTI) [22],[23]. As a result, PG/ER scheme for enhancing the endurance of the FeFET will be proposed.

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Jinhong Min is with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon-si 16419, South Korea, also with imec, 3001 Leuven, Belgium, and also with KU Leuven, 3001 Leuven, Belgium.

Nicolo Ronchi, Sean R. C. McMitchell, Barry O'Sullivan, Kaustuv Banerjee, and Geert Van den bosch are with imec, 3001 Leuven, Belgium.

Jan Van Houdt is with imec, 3001 Leuven, Belgium, and also with KU Leuven, 3001 Leuven, Belgium.

Changhwan Shin is with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon-si 16419, South Korea (e-mail: cshin@skku.edu).

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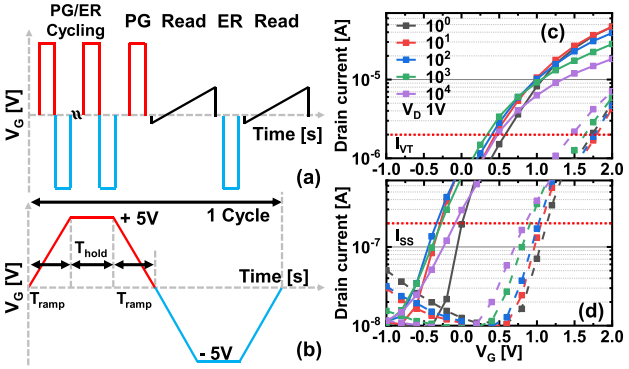

Fig. 1. (a) Test sequence used for measuring the endurance of FeFETs. (b) Timing definition of the PG/ER pulse. (c), (d) Current-vs.-gate voltage (I_D-vs.-V_G) of a FeFET after $10^0 \sim 10^4$ cycles. The solid line and dashed line indicate the PG state and the ER state of a FeFET, respectively. Note that the V_T and SS are extracted at their respective current level, i.e., 2 μA and 0.2 μA (see the red-colored dotted line in the figure).

II. Experiment

Using gate first process, ferroelectric field effect transistors (FeFETs) with TiN/Si/Si:HfO_2/SiO_2/Si gate stack were fabricated on 300 mm wafer. In the gate stack, 1nm-thick SiO_2 interfacial oxide layer was chemically grown on the Si surface. On top of it, 9.5nm-thick Si:HfO_2 and 5nm-thick TiN layer were deposited by atomic layer deposition (ALD). Between Si:HfO_2 and TiN layer, a 2nm-thick Si buffer layer was deposited by physical vapor deposition (PVD), to reduce the strain between the ferroelectric and the metal gate electrode. The FeFETs were annealed in N_2 ambient at 900°C to crystallize the Si:HfO_2 film. The channel length/width of FeFETs were 1 μm/1 μm.

The endurance of FeFETs was measured using the pulse train [which is shown in Fig. 1(a)]. The PG/ER pulses were applied to the FeFETs over $10^0 \sim 10^4$ cycles. Afterwards, I_D-vs.-V_G of PG state and ER state of FeFETs were measured by the readout.

The evolution of I_D-vs.-V_G of a FeFET over many cycles is represented in Fig. 1(c), (d). The subthreshold swing (SS) and threshold voltage (V_T) at PG state or ER state were extracted at their respective constant current level, i.e., 0.2 μA and 2 μA respectively, while the MW was calculated as the difference of V_T between the PG state and the ER state.

When measuring the current-vs.-voltage curve for extracting V_T, the characterization was completed within 20 μs using a 1mA measurement range option to minimize interference by the read gate voltage [11]. In the case of the current-vs.-voltage curve for SS, characterization was completed within $\sim$ 1 ms seconds using a 1μA measurement range option to extract in the deeper current region to present a convincing SS. For the 1μA-range measurement the interference during the readout was limited by a smaller Vg sweep (i.e., up to 1.4 V instead of 2 V). The lowest current level (i.e., $\sim$ 10 nA) shown in fig. 1 (d) is not an actual leakage drain current but the minimum measurement resolution of the readout. 1 s of delay time was inserted between the PG/ER pulse and readout, to avoid the influence of bulk trapping in the HfO_2 [12]. To define the waveform of PG/ER pulse, the ramp time (T_{ramp}) and hold time (T_{hold}) was adjusted while the magnitude of PG/ER voltage was fixed as |5 V| through optimization.

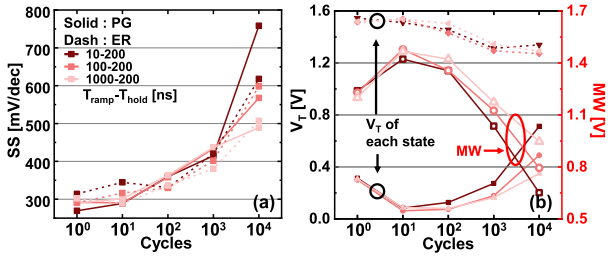

Fig. 2. Median value of (a) SS and (b) MW, V_T of FeFETs for various cycles up to 10^4 cycles. Note that T_{ramp} is varied from 10 ns to 1000 ns while T_{hold} was fixed as 200 ns. The solid line and dashed line indicate the PG state and the ER state, respectively. Note that PG/ER pulse with a longer T_{ramp} shows better MW and SS after 10^4 cycles.

III. Results and Discussion

It is well known that FeFETs processed on the same wafer are affected by device-to-device variation due to the grain distribution in the ferroelectric thin film [16], [24]–[26]. Each time different PG/ER pulse schemes were used to provide statistically reliable data, up to 20 devices were measured for each extraction of V_T and SS. In this discussion, every figure represents the median value of measurement data.

To begin with, T_{ramp} was adjusted to see the impact of ramp time on the endurance of FeFETs. Using the fixed T_{hold} of 200 ns, T_{ramp} was varied from 10 ns to 1000 ns. The evolution of MW, SS and V_T at each PG/ER state were plotted to analyze the endurance of FeFETs (see Fig. 2).

The MW widening by wake-up effect occurs between 10^0 and 10^1 cycles [see Fig. 2(b)]. Then, at 10^4 cycles, V_T of each PG/ER state increases significantly. This is because of the rapid degradation of SS (which strongly depends on T_{ramp}). With a shorter T_{ramp}, larger SS degradation and positive V_T shift were observed, especially at 10^4 cycles.

In addition, PG/ER pulse schemes with shorter T_{ramp} deteriorates the MW more than other schemes. This is because the degree of the degradation of SS depends on whether FeFETs' state was at the PG state or at the ER state. It was observed that the SS at the PG state is more deteriorated than the SS at the ER state at 10^4 cycles. As a result, a longer T_{ramp}, which prevents the SS deterioration in both states, not only prevents the positive V_T shift, but also was able to improve the MW of FeFETs. With the shortest T_{ramp}, the MW was median of 0.65 V. However, with the longest T_{ramp} case, the MW was median of 0.95 V at 10^4 cycles.

The rapid SS degradation with a short T_{ramp} seems to agree with the interface trap depassivation by bipolar BTI [22], [23]. Some previous BTI studies showed that the amount of depassivated interface traps (which are depassivated by the bipolar BTI) is more than the sum of interface traps measured in each of the positive BTI and negative BTI measurements. In addition, the bipolar BTI exhibited frequency dependency: a higher frequency stress can generate more interface trap. This was mainly elucidated by the built-in electric field which is generated by transiently trapped carriers (see Fig. 3). If the gate voltage is quickly swept, the trapped carriers are still trapped in the oxide even if the gate voltage is switched. This is mainly because the emission rate of trap is finite [see Fig. 3(b)]. Therefore, the transiently trapped carrier can form the built-in electric field.

The additional built-in electric field could enhance the band bending between SiO_2 and Si than the energy band at

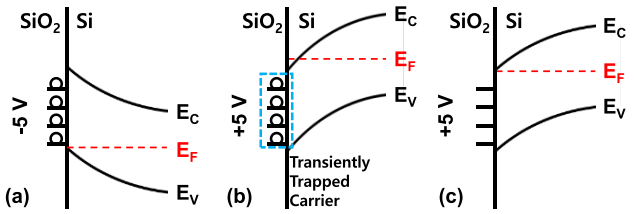

Fig. 3. Qualitative depiction of band diagram between SiO_2 interfacial layer and Si channel when sweeping the gate voltage sweep from − 5 V to + 5 V. (a) and (c) represent the band diagram at steady-state under |5 V|, and (b) represents the band diagram at transient-state between (a) and (c). Note that the transiently-trapped carriers should cause more band bending [compare (b) against (c)].

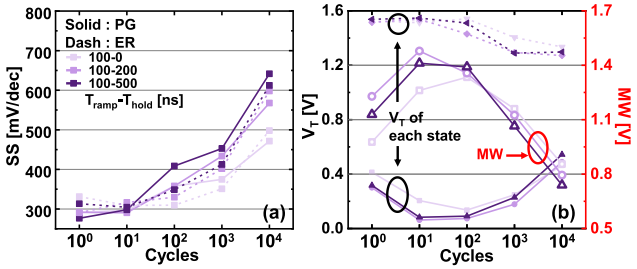

Fig. 4. (a) SS, (b) MW and V_T of FeFETs for various cycles up to 10^4 cycles. Note that T_{hold} is varied from 0 ns to 500 ns while T_{ramp} was fixed as 100 ns. The solid line and dashed line indicate the PG state and the ER state, respectively. Note that PG/ER pulse with a shorter T_{hold} shows better MW and SS after 10^4 cycles.

steady stress state, and it enhances BTI effects. Moreover, these trapped carriers could provide recombination energy that intensifies the BTI effect. In this respect, it can be estimated that the impact of T_{ramp} would be similar because the FeFETs were exposed to similar stress such as bipolar BTI. If the PG/ER pulse has a shorter T_{ramp}, it could confine more carriers transiently and generate a larger built-in electric field. As a result, severe BTI effects would happen, and thereby, more interface traps would be created.

There are many studies that have investigated the impact of T_{hold} to look for an appropriate PG/ER pulse width. It is well known that the properly long T_{hold} widens the MW [26], [27]. However, there are few studies on the impact of T_{hold} on endurance. Therefore, the impact of T_{hold} was investigated in this work.

Using the fixed T_{ramp} of 200 ns, T_{hold} was varied from 0 ns to 500 ns. For T_{hold} of 200 ns and 500 ns, they performed better initial MW due to the wake-up effect and practically long PG/ER pulses. However, the MW began to degrade earlier than T_{hold} of 0 ns because of the trapping in the oxide induced by the long T_{hold}[see Fig. 4(a)]. At 10^3 cycles, the SS in the case of long T_{hold} is further increased. Thus, V_T at each PG/ER state shifted/increased and MW decreased. This happened because more carriers were accumulated in the oxide by the influence of T_{hold}, before sweeping the gate voltage, and the accumulated carriers were generated by a larger built-in electric field while sweeping the gate voltage.

Last but not least, the waveforms of triangle PG/ER pulse, which has T_{hold} of 0 ns, were compared to each other (see Fig. 5). In this comparison, T_{ramp} shorter than 100 ns was not used because it was too short to program or erase the ferroelectric layer of FeFETs. Thus, only the T_{ramp} of 100 ns and 1000 ns cases are displayed. Same as previous schemes,

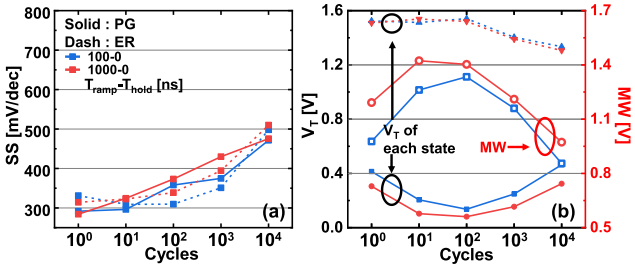

Fig. 5. (a) SS, (b) MW and V_T of FeFETs for various cycles up to 10^4 cycles. Note that T_{ramp} is set to either 100 ns or 1000 ns while T_{ramp} was fixed as 0 ns. The solid line and dashed line indicate the PG state and the ER state, respectively.

T_{ramp} of 1000 ns performed better MW thanks to 10 times longer pulse length.

In terms of SS, T_{ramp} of 100 and 1000 ns shows similar SS up to 10^4 cycles. However, in the case of T_{ramp} of 100ns, especially the V_T of the program state was not set better than 1000ns due to the short PG/ER pulse scheme. In addition, the device deterioration occurred faster than the case of T_{ramp} of 1000ns between 10^3 and 10^4 cycles, resulting in a sharp degradation in MW and SS. This implies that when using short T_{ramp}, the device may deteriorate faster. Among all the PG/ER pulse schemes, we can find that the waveform of triangle PG/ER pulse which has T_{ramp} of 1000 ns not only secured a wider MW, but also suppressed the SS degradation after 10^4 cycles of program and erase endurance test because it reduced the amount of transiently-trapped carriers.

IV. Conclusion

The influence of various PG/ER pulse schemes on the endurance of FeFET was studied. T_{ramp} and T_{hold} was varied from 10 ns to 1000 ns and 0 ns to 500 ns, respectively, to modulate the PG/ER pulse. The MW, SS and V_T were measured to quantitatively evaluate the endurance of FeFETs. If T_{ramp} is short but T_{hold} is long, the amount of interface trap generated is surged up, and thereby, the MW and SS become worse. This is because the built-in electric field is generated by the transiently trapped carrier, and thereafter, the built-in electric field accelerates the interface trap generation.

In the worst case, when the PG/ER pulse has T_{ramp} of 10 ns and T_{hold} of 200 ns, the MW was deteriorated to median of 0.65 V after 10^4 cycles. On the other hand, when the PG/ER pulse has T_{ramp} of 1000 ns and T_{hold} of 0 ns, the MW was maintained at median of 0.97 V after 10^4 cycles, representing the best endurance.

In this study, when PG/ER pulse is applied, both rising time (which is the time that it takes to reach the PG/ER voltage) and falling time (which is the time that it takes to reach the ground voltage) were considered equally as the ramp time. However, it turned out that the generation of interface trap under the bipolar stress condition is controlled by either the rising or falling time, and the amount of interface traps generated varies depending on the doping type of devices [22]. Therefore, it is necessary to further investigate the effect of the PG/ER scheme on the endurance of FeFET in future, and it is expected to help improve and understand the endurance of FeFET.

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