Programmable Analog-to-Digital Converter for Low-Power DC–DC SMPS

Amir Parayandeh, *Student Member, IEEE*, and Aleksandar Prodić, *Member, IEEE*

***Abstract*—An application-specific delay-line based windowed analog-to-digital converter (ADC) with programmable reference voltage, conversion time, and accuracy of voltage regulation, is introduced. The ADC can be fully implemented on a small silicon area and is suitable for implementation in various integrated digital controllers for high-frequency low-power switch-mode power supplies. The programmable characteristics are achieved through the utilization of the inherent averaging effect of the delay line and through the adjustments of delay cells' propagation times. The ADC is implemented in a standard 0.18 μm CMOS technology, as a part of a high-frequency digital controller integrated circuit, and tested with a 1.5 MHz, 1 W buck dc–dc converter.**

***Index Terms*—DC–DC SMPS, digital control, integrated circuit (IC), low-power.**

I. Introduction

DIGITAL controllers that can be fully implemented in the latest CMOS integrated circuit (IC) processes and have programmable parameters, such as switching frequency, voltage reference, and the accuracy of its regulation, can bring numerous advantages in low-power switch-mode power supplies (SMPS). In cell-phones, personal data assistants (PDA), and other portable devices they can increase reliability and significantly reduce the overall system size and battery operating time. Multiple application-specific analog controller ICs are generally used in order to provide regulated voltages for various functional blocks that in most cases consist of digital components. As a result the systems often have a sub-optimal size and number of components. If implemented in the same CMOS process as their predominantly digital loads, the programmable controllers can be easily integrated on the same silicon die and programmed to satisfy specific power supply requirements. In addition to the resulting size reduction, they provide design portability and can practically eliminate the time-consuming analog redesign required each time the IC implementation technology and, hence, supply voltage requirements change [1].

Another advantage is that the programmable controllers simplify implementation of power-savings techniques based on dynamic voltage scaling (DVS) [2] where the supply voltage is changed in accordance with the processing load. They can eliminate the need for interconnecting circuits and improve communication between the power supply and its digital load.

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A. Parayandeh is with the Laboratory for Low-Power Management and Integrated SMPS, Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 1A7 Canada (e-mail: amiran@eecg.toronto.edu).

A. Prodić is with the Electrical and Computer Engineering Department, University of Toronto, Toronto, ON M5S 1A7 Canada (e-mail: prodic@ele.utoronto.ca).

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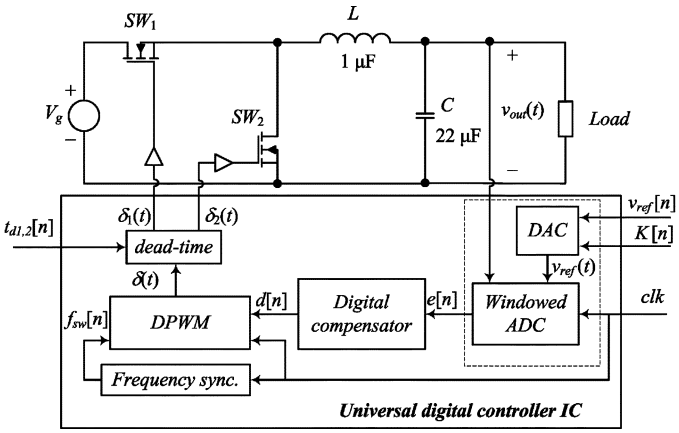

Fig. 1. Digital IC controller with programmable ADC regulating operation of a buck converter.

In principle, a possible conceptual solution for a programmable controller is easy to visualize. As shown in Fig. 1, it can consist of a digital-to-analog converter (DAC) that provides programmable reference voltage $v_{\rm ref}(t)$, and a windowed analog-to-digital converter (ADC) for conversion of the output voltage error into its digital equivalent $e[n]$, a compensator that based on $e[n]$ creates a duty-ratio control signal $d[n]$, and a digital pulsewidth modulator (DPWM) capable of operating at programmable switching frequencies. However, from a practical point of view the implementation of the structure in Fig. 1 is quite challenging and often results in sub-optimal system characteristics [3]. Compared to most of the existing digital solutions, analog controllers still have significant advantages in terms of power consumption and silicon area required for implementation. As these are among the most important IC parameters in low-power applications, they are still preferred options in modern portable devices [3].

Recent research publications [4]–[8] show high-frequency digital controllers whose power and silicon area consumption are comparable to those of analog solutions [9]. Several of them can change the mode of operation [4]–[6], providing overall efficiency improvement and functionality similar to that of widely available analog counterparts [9]. Still, most are designed to regulate voltage in a narrow range around a fixed analog reference only and do not allow full utilization of digital control advantages. This is because power and area-efficient windowed-based ADC architectures [4]–[8], [10] are commonly used. These ADC architectures are an effective alternative to full-range ADCs, whose complexity significantly exceeds that of a whole analog controller. Solutions consisting of a windowed-based ADC and a conventional DAC for reference adjustment also do not result in optimal architectures, and, in some cases, are not even feasible in up-to-date IC technologies. Current-source, switch-capacitor and resistive network based DACs [11] often require analog blocks whose supply voltages exceed the maximum allowable value of the

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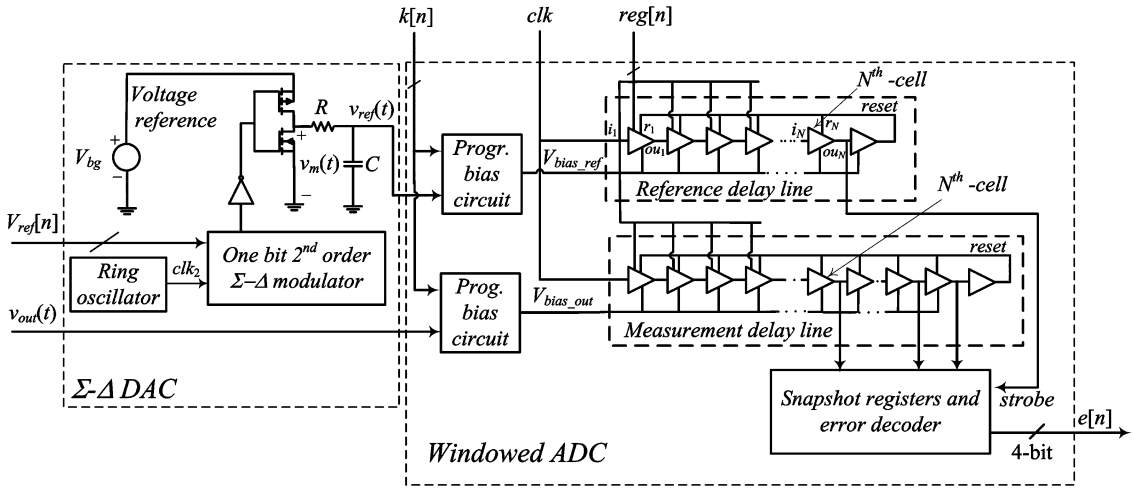

Fig. 2. Block diagram of the flexible ADC for low-power dc-dc SMPS.

digital circuits implemented in the latest CMOS processes [12]. On the other hand, fully-digital sigma-delta modulator based architectures [13] require a large *RC* filter, which cannot be simply implemented on a chip without taking a huge amount of silicon area and/or power.

The main goal of this letter is to introduce a new low-power ADC architecture that has a programmable reference voltage and can be implemented on a small chip area. The ADC conversion time and accuracy of the output voltage regulation can also be programmed. These features allow programmable digital controllers to have silicon area and power consumption comparable to analog systems while allowing better utilization of digital control advantages.

II. System Description and Principle of Operation

The programmable ADC, shown in Fig. 2, consists of two main blocks: a delay-line based windowed ADC with digitally programmable quantization steps and a Σ–Δ DAC that sets reference $v_{\rm ref}(t)$ proportional to the $N_{\rm ref}$-bit digital input $V_{\rm ref}[n]$. The reference voltage in this system is changed similarly to the solution presented in [13] where a Σ–Δ DAC and an off-chip *RC* filter are used. However, performance-wise, and from a practical realization point of view, the architecture presented here is more suitable for low-power applications. Its complete on-chip implementation requires a silicon area an order of magnitude smaller and consumes less power, and, as shown in the following sections, it has optimal voltage regulation over the full range of operation.

The single-bit second order Σ–Δ modulator [11], [14], transistors, and voltage reference (band gap) $V_{\rm bg}$ of the DAC are used to create a pulse-density modulated (PDM) signal $v_m(t)$ whose average value is $V_{\rm bg}V_{\rm ref}[n]/(2^{\rm Nref}-1)$ with the carrier frequency equal to that of internal clock $\rm clk_2$. A two-stage low-pass filter, instead of a large *RC* circuit [13], is used to extract the dc value of the PDM signal. The PDM signal is first passed to a small RC circuit, and then further filtered through the natural averaging effect of the ADC reference delay line. As a result, implementation of the full structure on a small silicon area is made possible.

A more detailed explanation of this averaging effect is given through the following analysis of the ADC operation. The ADC of Fig. 2 is a modified version of the architecture presented in [8]. Our solution consists of two delay lines having identical current-starved delay cells [15] but different numbers of them, two programmable bias circuits, a snapshot register, and an error decoder. The first reference delay line has $N+1$ cells whose propagation time is controlled by the reference voltage $v_{\rm ref}(t)$ through a bias circuit. The bias circuit is used as a digitally programmable voltage-to-current converter that regulates conversion time. The second delay line has $N+M$ delay cells and propagation time inversely proportional to the power stage output voltage $v_{\rm out}(t)$. At the beginning of each switching interval, a *clk* signal simultaneously sends two pulses through the delay lines. When the pulse propagating through the reference delay line reaches the Nth cell, a strobe signal is created and the state of the measurement delay line is captured by the snapshot register. If the number of cells through which the signal has propagated is smaller than N, the output voltage is lower than $v_{\rm ref}(t)$. Therefore a positive error $e[n]$ proportional to the difference in the number of cells is created by the error decoder. Similarly, propagation through a larger number of cells indicates a higher output voltage resulting in a negative error. The $(N+1)$th cell of the reference line is used to reset all the cells before the next *clk* pulse arrives.

It is important to note that this ADC actually measures the difference in the average values of $v_{\rm ref}(t)$ and $v_{\rm out}(t)$ over the conversion period, where t_{d1} is the propagation time through a reference delay cell. It behaves as a moving average filter whose transfer function can be described with the following equation and the diagram plotted in Fig. 3:

$$V_{\rm ref\_av}(j\omega) = V_{\rm ref}(j\omega).\sin c\frac{\omega T_{av}}{2\pi}.e^{-j\omega(T_{av}/2)}. \quad (1)$$

As described earlier, this averaging effect significantly reduces the size of the *RC* filter and allows on-chip implementation of the DAC. Practically, it would be possible to completely eliminate the passive filter by increasing the $\rm clk_2$ frequency or propagation times of the delay cells. However, this would come at the price of increased power consumption and/or a slower conversion time of the ADC. Hence, a small *RC* filter, which gives good overall system performance, is kept. It should be

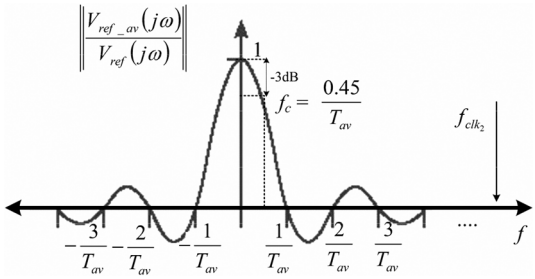

Fig. 3. Magnitude characteristic of a delay line.

noted that the averaging effect can also be used with ADC architectures based on a ring oscillator and counters [4].

A. Digitally Adjustable Accuracy of Voltage Regulation

In this subsection we describe the advantages of programmable voltage regulation, address regulation problems of conventional delay-line based architectures, and show a design modification that provides solutions for both of them.

In digitally controlled SMPS, the accuracy of the output voltage regulation can be defined as $V_{q0}/(2V_{\rm ref})$, where V_{q0} is the size of the ADC quantization step around voltage reference $V_{\rm ref}$, i.e., the width of the zero error bin, assuming that the steady-state value lies right at the middle of the bin. If an overly conservative requirement for the output voltage regulation, i.e, V_{q0}, is set, undesirable limit-cycle oscillations (LCO) [16] can occur. As a consequence, the size and power consumption of the whole digital controller can significantly increase. This is because no-LCO conditions [16] require DPWMs with higher resolution. In most of the existing DPWMs, improved resolution comes at the price of an exponential increase in power consumption and/or silicon area [17]. Hence, a universal ADC whose output voltage regulation accuracy can be programmed according to design requirements can result in design optimization.

To find the accuracy of voltage regulation for the system in Fig. 2, the dependence of $e[n]$ on output voltage deviations is observed. First, we adopt an approximation that the propagation times of a reference and a measurement delay cells around a certain operating point are $t_{d1} \approx k/V_{\rm ref}$ and $t_{d2} \approx k/V_{\rm out}$, respectively [7], where k is a parameter depending on the cell structure, operating point, and, in some cases ambient temperature. Then $e[n]$, which is equal to the difference in the number of cells the signals have propagated through the delay lines over the period Nt_{d1}, can be expressed as:

$$e[n] = N - N_m = N - \frac{Nt_{d1}}{t_{d2}} = N\left(1 - \frac{V_{\rm out}}{V_{\rm ref}}\right) \quad (2)$$

where N_m is the captured state of the measurement delay line.

Next, let us assume that the output voltage was at the middle of the ADC zero error bin and that a minimum variation of $v_{\rm out}(t)$ causing $e[n] = -1$ has occurred, i.e., $V_{\rm out} = V_{\rm ref} + V_{q0}/2$. Then (2) becomes

$$1 = N\frac{V_{q0}}{2V_{\rm ref}}. \quad (3)$$

This equation shows an interesting result: For the ADC of Fig. 2, the quantization step does not depend on the structure of the delay cells but on their number only. In other words, the accuracy of regulation, $V_{q0}/(2V_{\rm ref})$, is defined by the ratio of the time step around the Nth measurement cell and the total propagation time through the reference line. It also shows that in conventional delay-line structures [8], a large number of cells is needed for tight voltage regulation. For example, to obtain $\pm 0.2\%$ regulation, at least 500 identical cells occupying a large silicon area for the reference line only would be needed. To minimize the area and allow digital adjustment of the voltage regulation, two types of delay cells are used. The ADC is designed to operate in the $-4 < e[n] < 4$ range and the first $N-4$ cells of both delay lines are made to have r times larger delay than the remaining ones, where the value of r is controlled by a 2-b digital signal $\mathrm{reg}[n]$. As a result, the ratio of propagation times through the Nth cell and the reference line becomes smaller, thus improving regulation. For this case, (3) can be rearranged to obtain the following expression for the voltage regulation accuracy:

$$\frac{1}{r\,(N-4)+4} = \frac{V_{q0}}{2V_{\rm ref}}. \quad (4)$$

III. Practical Implementation

This ADC architecture relies on logic gates and current-starved delay cells [15]. Current-starved cells are chosen for their simplicity and the possibility of implementation in the latest CMOS processes. They have a structure similar to digital logic, and unlike most existing analog circuits, can operate at low voltages used in modern digital systems. Compared to digital gates, which are also used as delay cells [8], the current-starved structure has a much more predictable and controllable delay, due to lower susceptibility to temperature variations [18].

A. Delay Cells

In this design 16 slow cells in both delay lines are used. They have a digitally programmable propagation time up to eight times longer than that of the fast cells. Fig. 4 shows the transistor level schematics of the fast and slow cells. The fast cell has a conventional current-starved architecture [15]. Its propagation time depends on the current-discharging equivalent capacitance seen at node A. This discharge is controlled by Q_1, which behaves as a bias-circuit-controlled current source. The transistor Q_2 operates as a switch that, at the instance when the cell is triggered, passes the current through Q_1. The transistor Q_3, also operating as a switch, is used to reset the cell. Its current quickly charges the node A to $V_{\rm dd}$ when the reset signal r occurs. The slow delay works on the same principle. The main difference is that, in this case, the discharge current is much smaller and can be digitally programmed by enabling/disabling current through differently sized transistors Q_{1_a} to Q_{1_d}. The 2-b binary delay control input $\mathrm{reg}[n]$ sets the discharge current to be 1/32, 2/32, 3/32 or 4/32 times smaller than that of the faster cell. Based on (4), it can be seen that the selected number of delay cells and current ratio values approximately correspond to the voltage regulations of $\pm 0.2\%$, $\pm 0.4\%$, and $\pm 0.8\%$, respectively. A simple size comparison shows that, for the most accurate voltage regulation, this modification requires a silicon area

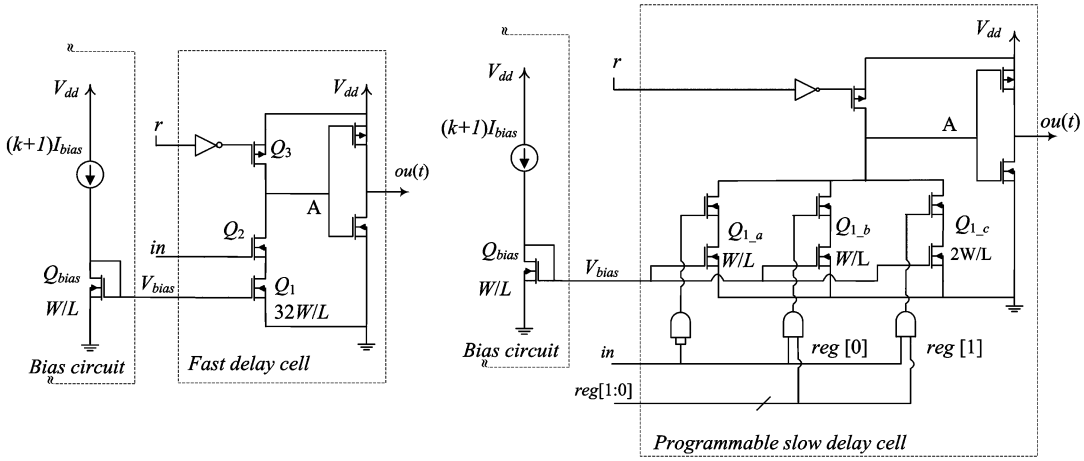

Fig. 4. Fast and slow programmable current-starved delay cells.

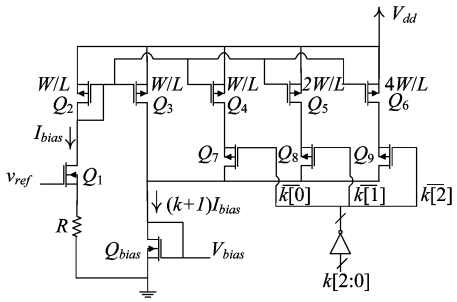

Fig. 5. Digitally programmable bias circuit.

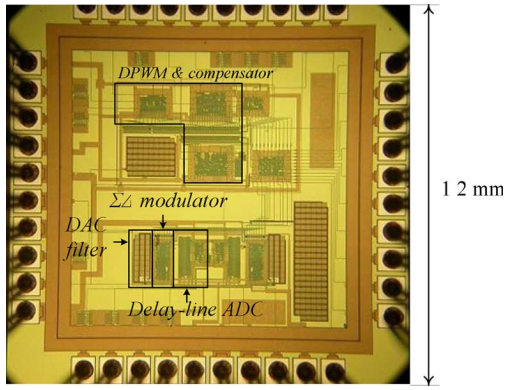

Fig. 6. Photograph of the experimental chip.

about 25 times smaller than the conventional delay-line ADC requiring 500 fast-delay cells for the reference line.

B. Programmable Bias Circuit

Even though regulation accuracy is independent of the delay cell propagation time (3), the ADC power consumption, conversion time and, consequently, filtering properties are not. To allow further controller optimization and reduce power consumption when a fast conversion is not required, the digitally programmable bias circuit of Fig. 5 is implemented. The current through the transistor $Q_{\rm bias}$, $(k[n]+1)I_{\rm bias}$ and, consequently, $V_{\rm bias}$ are controlled with the 3-b input $k[n]$. By turning on and off switches Q_7 to Q_9, $k[n]$ changes the currents produced by logarithmically-sized current mirror transistors Q_5 to Q_7. As a result, $V_{\rm bias}$ and the ADC conversion time change as well.

C. Σ–Δ DAC

The DAC of Fig. 2 is implemented using a second order 1-b digital Σ–Δ modulator [14]. In this application, it is preferred to the first order Σ–Δ solutions [13]. For the same clock frequency, the 2nd order modulator requires a smaller *RC* filter and minimizes possible low-frequency tones [6], a characteristic of the 1st order systems. The DAC is clocked with an internal ring oscillator operating at 80 MHz. Clock frequency is relatively high, as shown in the following section, but modulator power consumption is modest, because its simple structure requires only a small number of active logic gates to burn power.

TABLE I
MAIN CHARACTERISTIC OF THE PROGRAMMABLE ADC

Conversion time	Programmable ≥ 150 ns
Input voltage range	1V to 3.3V
Power consumption	ADC: 28 µA/MHz; DAC: 25µA/MHz
Voltage regulation	Programmable ≥ +/- 0.2 %
ADC area	0.011 mm^2
Σ-Δ DAC filter area	0.008 mm^2 (R=40 kΩ, C=8pF)
Σ-Δ DAC total area	0.018 mm^2
DAC quant. step	3 mV

IV. Chip Prototype and Experimental Verification

The architectures of Figs. 2 and 3 were implemented on an experimental digital controller IC, whose block diagram is shown in Fig. 1. The IC was realized in a standard 0.18 μm process and its DPWM and compensator are designed as a single-phase version of the multi-phase architecture presented in [19]. The IC was tested with an experimental 1W, 1.5 MHz buck converter with 5 V input and a programmable output between 1 and 3.3 V. A photograph of the chip and its main characteristics shown in Fig. 6 and Table I verify that the new ADC architecture has a low power consumption of 53 μA/MHz for 150 ns conversion time and occupies a very small silicon area of 0.029 mm^2. The ADC has an external reference. However, as shown in [20], a

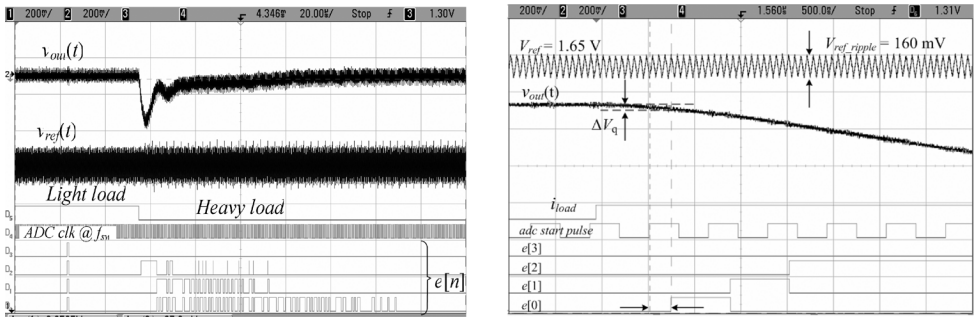

Fig. 7. Operation of the ADC in closed loop during a 0.2 A to 1 A load transient for $V_{\rm out} = 1.8$ V. Complete transient (left) and a reduced time scale around the load change time instance (right). Ch.1: $v_{\rm out}(t)$; Ch.2: voltage across filtering capacitor $v_{\rm ref}(t)$; d_5: load transient signal; d_4: ADC's clock signal at the switching frequency; $d_3 - d_0$: 4-b digital error value $e[n]$.

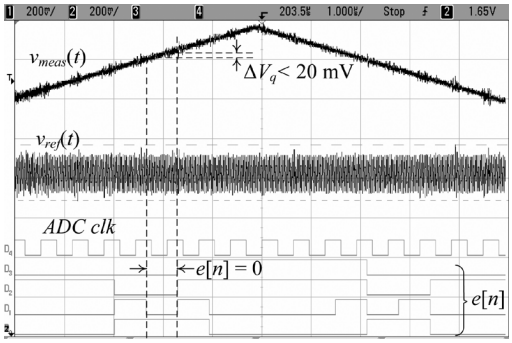

Fig. 8. Stand-alone operation of the ADC around 3.3 V for a triangular input signal; Ch.1: reference $v_{\rm ref}(t)$; Ch.2: input $v_{\rm meas}(t)$; $d_0 - d_3$: 4-b error $e[n]$.

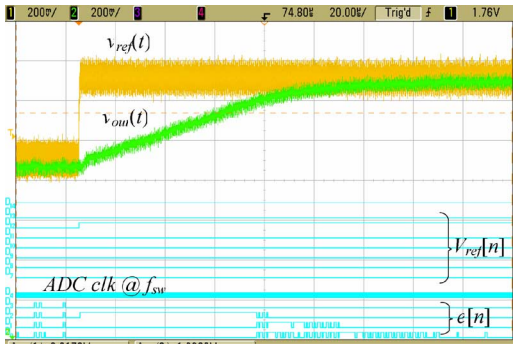

Fig. 9. Change of the voltage reference (1.6 V to 2 V) Ch.1: reference $v_{\rm ref}(t)$; Ch.2: output voltage $v_{\rm out}(t)$; $d_0 - d_3$: $e[n]$; d_4: ADC clock; $d_7 - d_{14}$ 8 MSBs of $V_{\rm ref}[n]$.

band-gap that requires insignificant power and area can be designed using new technologies.

The results of Fig. 7, showing closed-loop operation of the buck converter for two load transients, demonstrate fast conversion of the ADC and the filtering effect of its delay line. It can be seen that in steady state, the output voltage error is zero, even though the filter capacitor ripple is as high as 160 mV. The results also show that the ADC reacts quickly to the output voltage changes and completes conversion in less than 200 ns after the clock signal occurs. Fig. 8 shows stand-alone operation of the ADC with a triangular input $v_{\rm meas}(t)$ whose frequency is lower and amplitude is similar to that of the filter capacitor ripple. A high sensitivity to this input signal that provides tight output voltage regulation can be seen. Fig. 9 verifies the functionality of the Σ–Δ DAC. It shows operation of the SMPS when the reference changes. The DAC changes $V_{\rm ref}$ in a few μs, allowing ADC use in systems where a quick change of the reference is required, such as predictive DVS [21].

V. Conclusion

This paper introduces a new application-specific ADC for low-power SMPS that has programmable voltage reference, conversion time, accuracy of the output voltage regulation, low power consumption and small silicon area. It consists of a modified windowed delay-line based ADC and a Σ–Δ DAC. To reduce power consumption and allow on-chip DAC implementation in the latest CMOS technologies, the natural averaging effect of the delay line is utilized. Then, slow and digitally programmable current-starved delay cells are combined to both improve the accuracy of output voltage regulation of delay-line based ADC and reduce its size to a fraction of the original value. The programmable voltage regulation and conversion time allow further controller optimization in terms of size and power consumption. The ADC was implemented on a prototype chip and its characteristics were experimentally verified.

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