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Programmable Resistive-Switch Nanowire Transistor Logic Circuits

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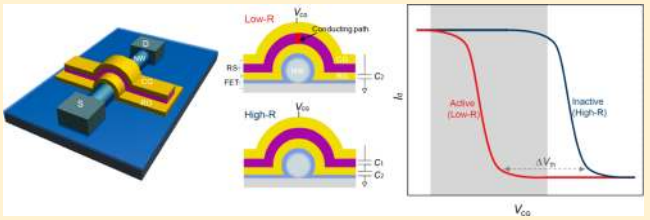
Supporting Information

ABSTRACT: Programmable logic arrays (PLA) constitute a promising architecture for developing increasingly complex and functional circuits through nanocomputers from nanoscale building blocks. Here we report a novel one-dimensional PLA element that incorporates resistive switch gate structures on a semiconductor nanowire and show that multiple elements can be integrated to realize functional PLAs. In our PLA element, the gate coupling to the nanowire transistor can be modulated by the memory state of the resistive switch to yield programmable active (transistor) or inactive (resistor) states within a well-defined logic window. Multiple PLA nanowire elements were integrated and programmed to yield a working 2-to-4 demultiplexer with long-term retention. The well-defined, controllable logic window and long-term retention of our new one-dimensional PLA element provide a promising route for building increasingly complex circuits with nanoscale building blocks.



KEYWORDS: *Nanoprocessor, nanocomputing, nanoelectronics, programmable logic arrays, crossbar arrays, memory*

Significant effort in the nanoelectronics field has been placed on the efficient integration of nanoscale device elements for improved density and functionality.[1,2] Crossbar array-based architectures have been proposed for achieving efficient large-scale integration as well as compatibility with bottom-up assembly and fabrication using nanoscale building blocks.[3−5] Following this direction, logic circuits in the crossed-array form were demonstrated, using different means such as molecular functionalizations,[6] synthetic encoding,[7] or dielectric decoupling[8,9] for cross-point differentiation to realize functional differentiation. These efforts have provided data supporting the importance of crossbar array-based architectures, although cross-point differentiation, which is central to "programming" specific logic circuits, was predetermined by fabrication thus precluding the realization of a highly defect-tolerant and universal architecture.[3]

Alternatively, hybrid structures consisting of simple two-terminal crossbar nanoswitch arrays with conventional CMOS transistor circuits, where the nanoswitch array is used for peripheral routing to form programmable architectures, have been studied.[10−13] While taking advantage of the power of conventional logic circuits, this approach does not address the long-standing goal[3] of building programmable circuits that could function as nanoprocessors from assembled nanowire or carbon nanotube semiconductor components. Therefore, efforts have also been placed on searching for programmable logic elements,[14−18] where the bistable function enables the integration of logic function and differentiation at the device element level. Still, up to date few studies have proceeded beyond single-device demonstration and toward the further integration into functional logic circuits.

To realize this goal in which common crossbar circuits can be tiled or linked together and programmed to yield complex functional logic gates for nanoprocessors requires that individual nodes within crossbar circuits be programmable following assembly and fabrication.[3−5,19,20] To this end, we recently introduced a dielectric charge-trapping shell structure on nanowire transistor elements and showed that by modulating the charge state in the dielectric layers the transistor could be programmed as "active" or "inactive" within a specific logic window. Integration of these nanowire device elements into a crossbar array[19,20] further yielded a basic module or tile that could be used for proposed array-based architecture.[1,3−5]

There are several important features critical to a programmable crossbar circuit. First, once programmed the circuit logic should be stable until it is reprogrammed. This requires that the programmed states of individual device nodes in the crossbar are nonvolatile. Second, the state nonvolatility should be maintained as the device node size is reduced to enable increasing density of nodes within the crossbar. Third, rapid programming of the active/inactive nodes within a crossbar can be important to viable reconfiguration/programming as well as when crossbar elements would be used for memory,[21−23] for example, in a nanoprocessor.

Here we report a new and powerful approach for achieving programmable active/inactive transistor nodes in crossbar arrays based on the incorporation of a resistive switch gate

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structure on semiconductor nanowire, where the gate coupling to the nanowire transistor can be modulated by the memory state of the resistive switch. Compared to charge-based programming of active/inactive nodes,[19,20] which has analogies to flash memory,[24] resistive switch elements provide potential advantages in terms of nonvolatility or retention, scaling, and programming speed and endurance.[21−23] First, in the resistive switch the state change is largely due to a local structural/composition change in the material between switch electrodes, and the retention is often projected to be beyond years.[21,22] Second, because the process is highly localized, there is potential for aggressive device scaling[23] without sacrificing retention, which contrasts charge-based systems.[24] Third, the programming speed can be below the microsecond region achieved in conventional charge-based systems.[22,23] Below we first describe the working mechanism and performance of the resistive-switch nanowire transistor device and then demonstrate the integration of this element into a crossbar architecture for programmable logic circuits.

A single input (or node) resistive-switch nanowire transistor device consists of a conventional top-gated nanowire transistor structure with a layer of dielectric (dielectric-1, blue) and metal (yellow) deposited sequentially on the nanowire (Figure 1a). Layers of resistive switching material (dielectric-2, purple) and metal (yellow) are then deposited sequentially on top of the conventional gate to yield a metal−insulator−metal (M-I-M) sandwich structure characteristic of a resistive switch.[21−23] We term the lower metal layer as resistive-switch gate (RG) and the upper metal layer as the control gate (CG).

We utilize the two memory states in the resistive switch to achieve nonvolatile programming of the device (Figure 1b). When the resistive switch is set to the low-resistance (low-R) state (top, Figure 1b), the metallic conducting filament effectively shorts RG and CG and, thus, there will be a strong gate coupling between CG and the nanowire transistor channel (upper panel). On the other hand, when the switch is set to the high-resistance (high-R) state, the dielectric switching layer reduces the gate coupling between CG and nanowire transistor channel (bottom panel). The differences in gate coupling for the two resistive switch states will produce a threshold voltage (V_{th}) change for CG (Supporting Information, Figure S1), where the threshold voltage shift, ΔV_{th}, can be analyzed in terms of the different capacitances.[25] Specifically, the effective voltage on RG will be reduced from V_{CG} in the low-R state (upper panel) to $[C_1/(C_1 + C_2)]V_{CG}$ in the high-R state (bottom panel) (see below for quantitative analysis and comparison with device experiments). The different thresholds associated with the two resistive switch states yield a hysteresis loop for transistor drain current versus V_{CG} (Figure 1c) such that we can define a programmable logic window (gray region, Figure 1c),[1,19,20] where the resistive-switch nanowire transistor can serve as a typical transistor (red curve, "active") or as a passive resistor (blue curve, "inactive").

Qualitatively, there are several factors contributing to the threshold difference between active and inactive states. First, a high high-R/low-R ratio is important such that the low-R state fully shorts CG and RG, and the high-R state is dominated by capacitive coupling between CG and RG. Second, a low dielectric constant (low-k) resistive switching material (versus high-k for dielectric-1) should be used to reduce the capacitive coupling in the high-R state for a given thickness layer. These two challenges were met in our studies using the standard low-k dielectric, SiO_2, as the switching material between the RG and

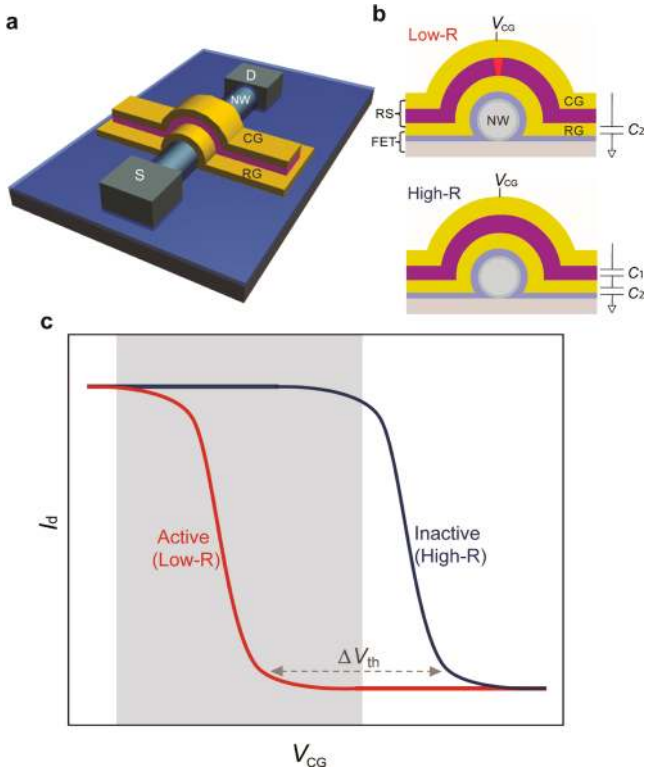

Figure 1. Structure and mechanism of resistive-switch nanowire transistor. (a) Schematic of the resistive-switch nanowire transistor device. (b) Cross-section schematics of the programmed states of the device with the equivalent capacitive coupling between the CG and transistor channel shown on the right. Here RS denotes resistive switch formed by the CG/dielectric-2 (purple)/RG layers, with C_1 denoting its capacitance; FET denotes the nanowire (NW)/dielectric-1 (blue)/RG components that form the conventional field-effect transistor structure, with C_2 denoting its capacitance. The red column in the upper panel indicates the conducting filament that forms in the low-R state. (c) Schematic of the programmable logic window resulted from the threshold voltage shift ΔV_{th} induced by the change of CG coupling to the transistor channel. The red and blue curves correspond to the programmed states in upper and bottom panels in (b), respectively.

CG electrodes. Previous studies have shown that a M-I-M structure with I = SiO_2 yields a robust resistive switch[26−29] in which a conducting filament leads to a metallic ON state. In addition, studies have shown that the switching property is independent of a range of metallic electrode materials[30] and thus compatible with standard fabrication technology.

Figure 2a shows a representative false-color scanning electron microscopic (SEM) image of a test device in which two resistive-switch elements or nodes were fabricated on a single nanowire. Briefly, Ge/Si core/shell nanowires[31−33] with defined source and drain contacts were used as p-type transistor channels. A 7 nm ZrO_2 layer grown by atomic layer deposition serves as the dielectric-1 for the RG (30 nm Au), and then SiO_2 (30 nm) and CG layers (50 nm Au) were defined on top of the RGs by standard lithography, deposition, and lift-off processes.[34] In addition, other high dielectric constant materials such as Al_2O_3 or HfO_2 may as well serve as dielectric-1. In this manner, we fabricate and test resistive-switch elements with different RG/CG widths (W_{RG}/W_{CG}) on the same nanowire device as in Figure 2a, where the widths are 750/500 nm and 500/250 nm for the two elements.

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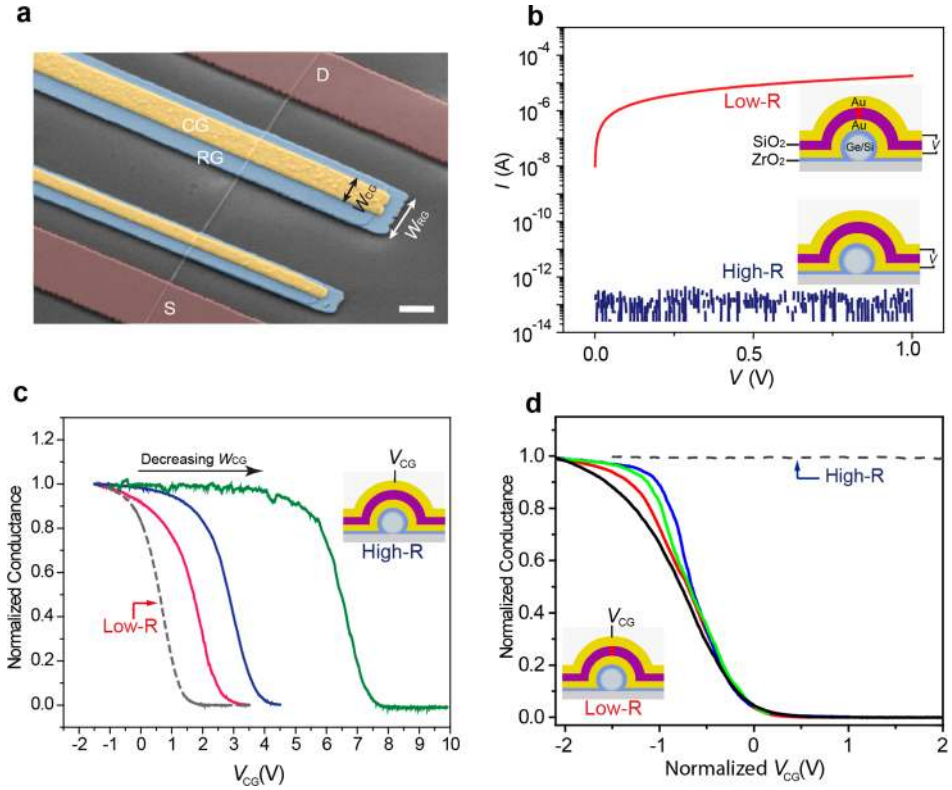

Figure 2. Characterizations of resistive-switch nanowire transistor devices. (a) An SEM (false color) image of two fabricated resistive-switch nanowire transistor device elements with different W_{CG} and W_{RG} dimensions. Scale bar, 500 nm. (b) Characteristic conduction curves in the low-R and high-R states in the resistive switch. For typical devices fabricated in our studies, the high-R/low-R ratios were ~10^7. (c) Transport properties of the inactive states, high-R state (color curves) for devices with different W_{CG} (V_{ds} = 1 V, W_{RG} = 500 nm). The red, blue, and green curves correspond to W_{CG} values of 500, 250, and 30 nm, respectively. The dashed gray curve corresponds to the active, low-R state in the resistive-switch nanowire transistor, which is independent of W_{CG}. (d) Transport properties of the active states (color curves) in devices with different W_{RG} (V_{ds} = 1 V, W_{CG} = 30 nm). Offset is applied to align all curves to V_{th} = 0 to enable direct comparison of transconductance versus W_{RG}. The black, red, blue, and green curves correspond to W_{RG} values of 500, 300, 100, and 50 nm, respectively. The dashed gray curve corresponds to the inactive state with W_{RG} = 50 nm.

We first investigated the switching properties in the CG/SiO_2/RG resistive switch at room temperature in vacuum (10^{-5} Torr). Following a typical electroforming process[26] the resistive switch elements exhibited well-defined low- and high-R states. For example, a CG/SiO_2/RG element (Figure 2b) exhibited high-R/low-R ratio of ~10^7 (at 1 V) using set/reset voltages of 5/20 V, respectively. The typical measured low-R state resistance values were in the range of 10^4–10^5 Ω, similar to those observed in previous studies.[26−30] The typical high-R state resistance measured for the switch elements achieved for reset voltages >15 V, 10^{12} Ω (near our measurement limit) ensures that CG is decoupled from RG in the high-R state and thus maximizes the threshold difference and logic window. Indeed, we found that a high resistance is necessary to produce capacitive coupling to yield the logic window (Supporting Information, Figure S2). Note that RG is floating during device logic characterization and circuit operation once the resistance state in the CG/SiO_2/RG switch element has been programmed.

We have investigated the effect of the resistive switch electrode widths, W_{CG} and W_{RG}, to both test our model and examine size scaling for a transistor node. First, we investigated how decreasing W_{CG} for fixed W_{RG} affects the nanowire transistor inactive state (high-R switch state), where capacitive coupling of CG to RG should describe the effective gate voltage (Figure 1b, Supporting Information, Figure S3, inset). Figure 2c shows that the inactive state V_{th} increased from 3.1 ± 0.5 (red curve) to 4.2 ± 0.5 (blue curve) to 7.7 ± 0.8 V (green curve) for W_{CG} values of 500, 250, and 30 nm, respectively, for a fixed W_{RG} of 500 nm. The active state of the devices (i.e., low-R state of the switch) had a V_{th} of 1.6 ± 0.3 V (dashed gray curve, Figure 2c) independent of W_{CG}, which is consistent with the localized conduction in the SiO_2 dielectric layer.[26,29] Importantly, the shift of V_{th} in the inactive state with decreasing W_{CG} is consistent with capacitive coupling between CG and RG, where the gate capacitance and gate coupling decrease with decreasing W_{CG}. We have explicitly modeled the effect of W_{CG} on V_{th} with two serial capacitors (Supporting Information, Figure S3) and found reasonably good agreement with the observed experimental results. The ability to control the inactive state V_{th} and logic window size through W_{CG}, and in particular increase the threshold at smaller widths, is distinct from previous studies where the value was fixed[6−9,14,19,20] and can provide flexibility for realizing successful logic operations.

Second, we characterized how decreasing W_{RG} for fixed W_{CG} of 30 nm affects V_{th} for the nanowire transistor active state (low-R switch state). The active-state conductance versus V_{CG} adjusted such that V_{th} = 0 V for all data (Figure 2d) shows that transistor ON/OFF behavior is relatively insensitive to W_{RG} as the width is reduced from 500 to 50 nm. The absolute values of V_{th} for W_{RG} values of 500, 300, 100, and 50 nm were 1.3, 1.9, 2.7, and 3.5 V, respectively. The increase in V_{th} with decreasing

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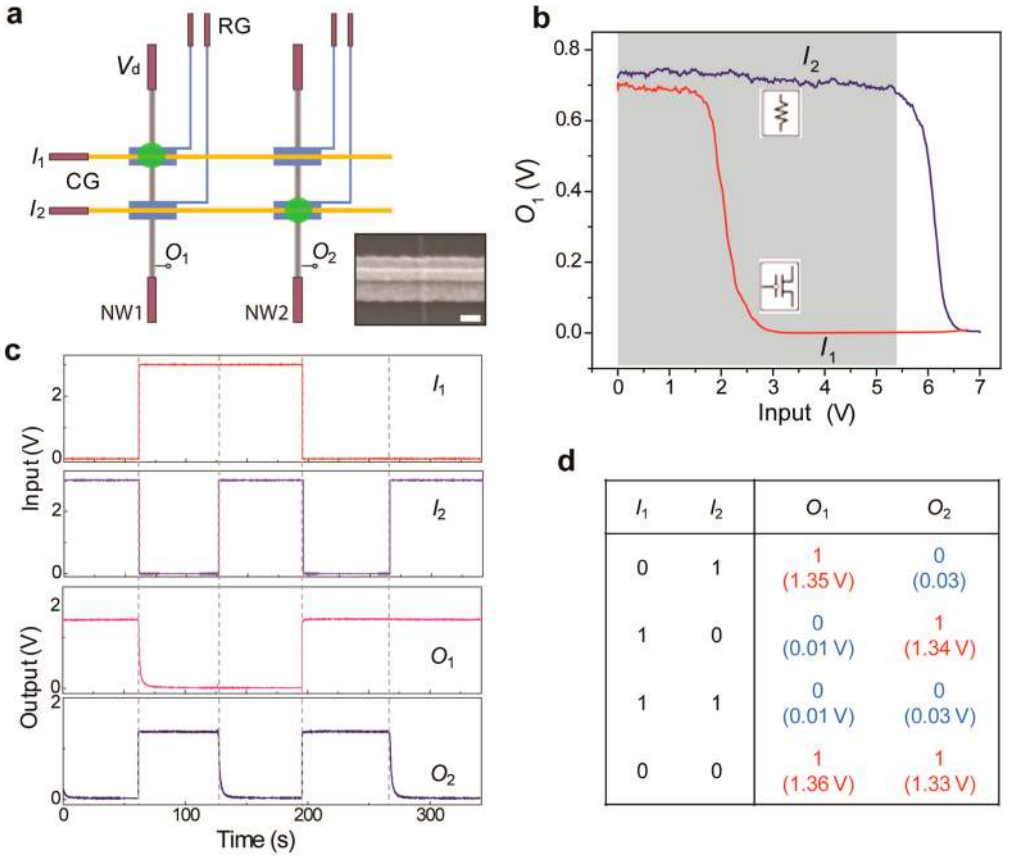

Figure 3. Resistive-switch nanowire transistor logic circuit. (a) Schematic of a 2 × 2 crossbar circuit. The horizontal yellow lines (CG) indicate the logic input (I_1, I_2), and the blue lines are the RGs. The vertical gray lines indicate the nanowires, each connected with a load resistor (not shown here) close to the source. Together, they form an inverter configuration for each output (O_1, O_2) with respect to either I_1 or I_2. The green dots indicate device nodes programmed to the active, low-R state. The inset shows the SEM image of the actual device node with W_{CG} = 100 nm, W_{RG} = 500 nm. Scale bar, 100 nm. (b) Characteristic output O_1 versus inputs I_1, I_2 for the first nanowire; V_d = 1 V. The gray region indicates the programmable logic window. (c) Logic flow of the output (O_1 and O_2) with respect to inputs (I_1 and I_2) from the programmed 2 × 2 circuit. (d) Corresponding truth table of the 2 × 2 circuit. The measured voltage outputs are in brackets and corresponding logic states, low or high, indicated by 0 or 1.

W_{RG} is expected given that the effectiveness of a gate electrode (RG in our device) in turning off a transistor channel reduces at reduced dimensions.[35,36] The observed threshold shift could be compensated for by using a lower work-function metal,[32] although even without such optimization the inactive state V_{th} (dashed gray curve, Figure 2d) remains sufficiently large at the smallest dimensions to provide a flexible logic window. In addition, we note that the overlap of RG/CG lines affects the device "length" dimension relevant to total area per element and has not yet been optimized (but should have similar size limit as width). Consequently, the filament formed in the low-R state for the 30 nm minimum lateral feature demonstrated in our devices could occur anywhere along the "length" dimension. Given that the resistive switch is ultimately limited only by a nanometer-scale filament,[21−23,26,29,37] the further reduction in the W_{CG}/W_{RG} below the current 30/50 nm as well as similar reduction in the "length" dimension is possible.

We initially investigated the potential of programmable resistive-switch nanowire transistors for building integrated circuits using a 2 × 2 crossbar array model. In our resistive-switch nanowire transistor implementation of the 2 × 2 circuit (Figure 3a), the active/inactive nodes are defined at the cross-points between the two nanowires, NW1 and NW2, and common input CG lines, I_1 and I_2, with independently addressable RGs for the four nodes. To test[38] this 2 × 2 circuit the (1,1) and (2,2) nodes were programmed to the active (green dot, low-R) state and the off-diagonal nodes were set in the inactive (high-R) state. The programmed active and inactive states in the devices were characterized by measuring the voltage output with respect to I_1 and I_2. For example, measurement of output O_1 (NW1) versus inputs I_1, I_2 (Figure 3b) demonstrates inverter behavior (i.e., low output for high input) for both nodes, although the minimum voltage values of a logic input 1 to output logic 0 differ substantially for the active and inactive states: threshold input voltages of 2.6 ± 0.3 V and 6.6 ± 1.0 V were required for a logic output 0 (defined as 1/10 V_d) for the active (red curve) and inactive (blue curve) states, respectively. This difference provides a wide logic window (gray region, Figure 3b) within which the inverter logic can be utilized for active-state nodes, while the inactive state shows approximately no change as the input voltage is varied.

Figure 3c shows the measured outputs from NW1 (O_1) and NW2 (O_2) for the programmed 2 × 2 circuit (Figure 3a) as input voltages I_1 and I_2 are varied, and highlights several key points. First, the output of the 2 × 2 circuit is consistent with that measured individually as single nanowire devices without cross-talk. Second, two outputs have very close high ("1") and low ("0") values (see also, Figure 3d), and moreover, these values are stable during time evolution after each I_1 and I_2 change. This stability is important for logic circuits. Third, the

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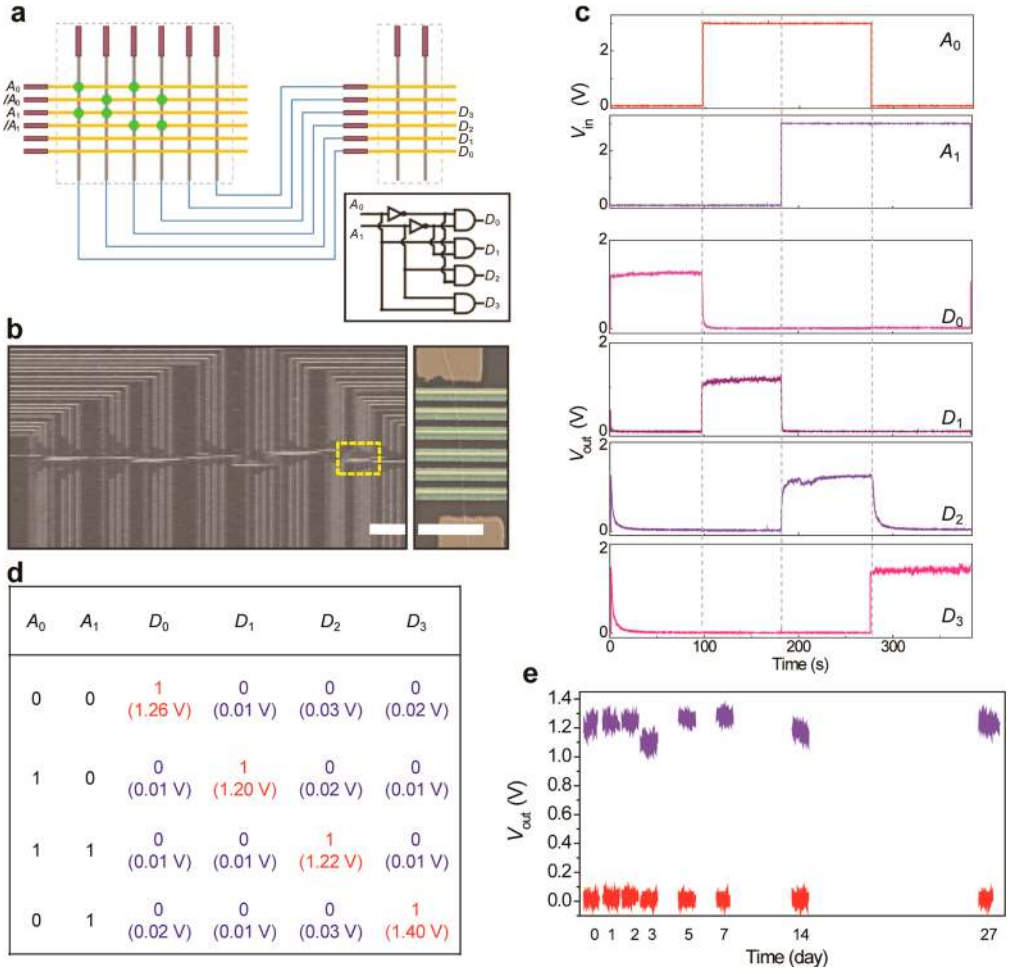

A_0	A_1	D_0	D_1	D_2	D_3
0	0	1 (1.26 V)	0 (0.01 V)	0 (0.03 V)	0 (0.02 V)
1	0	0 (0.01 V)	1 (1.20 V)	0 (0.02 V)	0 (0.01 V)
1	1	0 (0.01 V)	0 (0.01 V)	1 (1.22 V)	0 (0.01 V)
0	1	0 (0.02 V)	0 (0.01 V)	0 (0.03 V)	1 (1.40 V)

Figure 4. The 2-to-4 demultiplexer circuit. (a) Schematic of logic circuit achieved by interconnecting crossbar arrays. For simplicity, the RGs, source ends, and load resistors are not shown. The green dots show the specific programming pattern (active device nodes) for a 2-to-4 demultiplexer with A_0, A_1 indicating the 2-bit inputs and D_0–D_3 indicating the 4-bit outputs. The inset shows the equivalent[19] standard CMOS circuit for the 2-to-4 multiplexer. (b) SEM images of the resistive-switch nanowire transistor matrix formed by a nanowire array (left panel) with each nanowire in the array having six device nodes (right panel). Scale bars, 20 μm (left) and 2 μm (right). (c) Logic flow of the output (D_0–D_3) with respect to inputs (A_0A_1) from the programmed demultiplexer circuit. (d) Corresponding truth table. The measured voltage outputs are summarized in brackets with low or high logic states indicated with 0 or 1. (e) Output D_2 (both 1 and 0) measured at different time intervals for the programmed circuit in ambient environment.

low values are less than <0.1 V, and thus close to logic "0". Last, summarizing the input–output results in a truth table (Figure 3d) shows that programmed 2 × 2 circuit yields the correct logic of a 2-bit inverter: $O_1 = \overline{I}_1$ and $O_2 = \overline{I}_2$.

We have also explored the potential of the resistive-switch nanowire transistor element to realize substantially more complex and functional crossbar circuits. As shown schematically in Figure 4a, we considered a 8 × 6 array consisting of 6 × 6 and 2 × 6 crossbars. Each crossbar array functions as a NOR logic gate unit, and in combination can yield complete logic functions dependent only on programming and the ultimate array sizes.[3,19,20] For our demonstration, we have considered a 2-to-4 demultiplexer with active resistive switch nodes indicated by green dots; an equivalent circuit is also shown for comparison (inset, Figure 4a). For inputs A_0, /A_0, A_1, /A_1, and outputs D_0, D_1, D_2, D_3, demultiplexer output relationships are $D_0 = \overline{A}_0 \bullet \overline{A}_1$, $D_1 = A_0 \bullet \overline{A}_1$, $D_2 = A_0 \bullet A_1$, and $D_3 = \overline{A}_0 \bullet A_1$, where "•" represents the logical AND.

We fabricated the 2-to-4 demultiplexer resistive-switch nanowire transistor crossbar circuit by assembling aligned Ge/Si nanowires using nanocombing[20,39] followed by conventional lithography.[34] Figure 4b (left panel) shows a SEM image of one of the fabricated arrays consisting of 10 nanowires with 6 device nodes on each nanowire. The crossbar array features a resistive-switch pitch of ~800 nm, and W_{CG} and W_{RG} at 100 and 500 nm, respectively; a higher resolution image of one nanowire in the array (right panel, Figure 4b) highlights the resistive switch structure. A total of 60 programmable resistive-switch nanowire transistor device nodes were integrated in the array, although only a subset were selected for the demultiplexer.

Figure 4c shows representative input/output data for the consecutive input combinations of A_0A_1 (00→10→11→01). The D_0, D_1, D_2, and D_3 outputs for different A_0A_1 input combinations showed that the output voltage levels for logic states 0 and 1 are distinctly separated and each has similar absolute values, consistent with our results for the smaller 2 × 2 circuit described above. These output values, which are summarized in a truth table (Figure 4d) demonstrate the narrow distribution of the voltages for both the 0 state (0.01–0.03 V) and 1 state (1.20–1.40 V). The fact that similar output circuit values of logic 0/1 statues are maintained in the larger 2-

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to-4 demultiplexer circuit suggest that further integration should be possible with this approach.

Last, we characterized the robustness of the nonvolatility of the programmable resistive-switch nanowire transistors in the 2-to-4 demultiplexer logic circuit. Significantly, measurements showed that the circuit maintained its full function beyond the testing time of 4 weeks, (Supporting Information, Figure S4), which is considerably longer than demonstrated in charge-based programmable circuits.[20,21] Explicit comparison of the output values of both logic 1 and 0 states (Figure 4e) shows no obvious degradation over the four week period. More generally, we suggest that much longer stability is possible given the reported robustness in programmed states of SiO_2-based resistive switch[40] and the general expectation of greater than a year stability in resistive switching materials.[21]

The above studies demonstrate that resistive switch elements combined with nanowire transistors yield programmable transistor devices and that these devices can be further integrated into crossbar arrays for functional logic circuits, thus providing a new approach for realizing PLAs. Compared to charge-based nonvolatile programmable transistor elements,[14,19,20] the resistive switch elements provide a greater robustness in retention of the active/inactive transistor state[21−23,40] and thereby allow longer-term stability of the programmed circuits. The functionality and stability of a crossbar resistive switch nanowire transistor circuit was demonstrated with a programmed 2-to-4 demultiplexer with no obvious degradation in performance during the testing time span of 4 weeks in ambient environment. This level of robustness is substantially greater than the retention of hours in charge-based systems.[14,19,20] In addition, the stacked resistive switch elements (nodes in crossbar) are attractive for minimizing the area per node compared with charge-based nanowire programmable device elements.[19,20] Specifically, this study demonstrates that programming capability is maintained for a gate length of 50 nm with a 30 nm width switch element, as opposed to a >200 nm feature demonstrated in charge-based nanowire crossbar structures.[19,20] The resistive switch element does have a disadvantage compared to charge-based switches because of the additional independent RG gates required for each node. However, we note that this constraint in circuit integration and scaling may be addressed[1] by adding peripheral addressing demultiplexer to reduce the selection inputs to $[2 \log_2 N]$ versus N, where N is the number of nodes in the crossbar. The long-term stability, potential for device size scaling, along with the advantage of a simple SiO_2 material for the switch component suggest substantial promise for our approach for constructing high-density PLAs in the future.

■ ASSOCIATED CONTENT

Supporting Information

Additional information and figures. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

‖W.S. and J.Y. contributed equally to this work.

Notes

The authors declare no competing financial interest.

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SiO_2/Si) dispersed with gold nanoparticles (10 nm, Ted Pella) was placed in a quartz-tube reactor system. The Ge core was synthesized at 255 °C and 450 Torr with 30 sccm germane (GeH_4, 10% in H_2) and 200 sccm H_2 as the reactant and carrier gas, respectively. The growth time was 80 min, yielding an average length of ~80 μm. The epitaxial Si shell was grown immediately after the growth of Ge core at 460 °C and 5 Torr for 2 min with 5 sccm silane (SiH_4) as the reactant gas and yielded nanowires with an overall diameter of 15 nm.

(34) The Ge/Si nanowires were first assembled by nanocombing. The assembled nanowires were then trimmed to ordered array with uniform length (~8 μm) by reactive ion etching (SF_6 as reactant gas) using resist layer (PMMA 950 C5) as sacrificial mask. The source and drain contacts of the nanowires were defined by electron-beam lithography followed by the thermal evaporation of metal contacts (Cr/Ni, 1/40 nm) and lift-off process. The dielectric-1 layer (ZrO_2, 7 nm thick) were deposited by atomic-layer deposition at 200 °C using $Zr[N(CH_3)_2]_4$ as precursor gas. The first gate line (RG) was defined by electron-beam lithography, thermal evaporation of metal (Cr/Au, 1/30 nm) and lift-off process. The resistive switching material of SiO_2 (30 nm) and top metal layer (CG) were defined by a second electron-beam lithography, consecutive electron-beam evaporations of SiO_2 and metal (Cr/Au, 1/50 nm), and lift-off process.

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(38) The programming of the resistive-switch nanowire transistor devices, that is, the electroforming, set, and reset of the RG/SiO_2/CG resistive switch was done in vacuum (10^{-5} Torr) in a probe station (Lake Shore) connected to a 4156C semiconductor analyzer parameter (HP-Agilent, Inc.). Its transport properties (e.g., CG gate response with respect to the nanowire transistor channel) after the programming were then measured in ambient environment. For resistive-switch nanowire transistor circuits, the chip was first programmed in the vacuum and then transferred to another probe station (Model 12561B, Cascade Microtech) in ambient environment for logic characterizations. Specifically, a custom-designed 204-pin probe card (Accuprobe) with BNC interface was used to electrically access the device arrays. A computer-controlled analog I/O system (2 × PXI-6723, 2 × PXIe-6358 in a PXIe-1065 chassis, National Instruments), featuring 64 analog-voltage output channels and 24 analog-voltage input channels, was used for the electrical characterization. For each nanowire, an external resistor (10−30 MΩ, Vishay) was used as load resistor. The resistance value of the load resistor was chosen to be at least 1 order of magnitude larger than the ON state resistance of the nanowire transistor (<1 MΩ). Simplified circuit schemes without showing the load resistors are presented in Figure 4a. For the logic outputs, drain voltages of 1.5−1.9 V were used with the source grounded. The input gate voltages were 0 V for logic 0 and 3 V for logic 1, unless otherwise specified.

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