Review Article

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# Progress and challenges in p-type oxide-based thin film transistors

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**Abstract:** Transparent electronics has attracted much attention and been widely studied for next-generation high-performance flat-panel display application in the past few years, because of its excellent electrical properties. In display application, thin film transistors (TFTs) play an important role as the basic units by controlling the pixels. Among them, oxide-based TFTs have become promising candidates and gradually replaced the conventional amorphous and polycrystalline silicon TFTs, due to high mobility, good transparency, excellent uniformity and low processing temperature. Even though n-type oxide TFTs have shown high device performance and been used in commercial display application, p-type oxide TFTs with the equal performance have been rarely reported. Hence, in this paper, recent progress and challenges in p-type oxide-based TFTs are reviewed. After a short introduction, the TFT device structure and operation are presented. Then, recent developments in p-type oxide TFTs are discussed in detail, with the emphasis on the potential p-type oxide candidates as copper oxide, tin oxide and nickel oxide. Moreover, miscellaneous applications of p-type oxide TFTs are also presented. Despite this, the performance of p-type oxide TFTs still lags behind, as compared with that of n-type counterparts. Thus, the current issues and challenges of p-type oxide TFTs are briefly discussed.

**Keywords:** thin film transistors (TFTs); copper oxide; tin oxide; nickel oxide

## 1 Introduction

Transparent oxide semiconductors have great potential applications, such as solar cells, solid-state sensors, flat-panel displays, smart windows, electrochromics, transparent flexible electronic devices [1–3]. By using high-performance transparent oxide semiconductors, transparent displays with higher pixel density (higher resolution) and higher refresh frequencies can be realized [1, 2]. In addition, energy-efficient displays can be constructed by using transparent oxide semiconductors, which enables a person to look right through the panel like glass, and it also consumes 90% less electricity due to the removal of backlight [2]. Therefore, oxide electronics is a promising alternative to amorphous silicon and organic semiconductors to build more reliable thin film transistors (TFTs) and more complex electronic circuits, addressing the challenges of ultra-high resolution, ultra-large size, low cost and environmentally friendly electronics.

However, the current use of transparent oxide semiconductors is mostly limited to unipolar devices (based on n-type semiconductors). Many of the potential transparent electronic applications are limited by the lack of the availability of high-performance p-type oxide semiconductors. For example, complementary metal oxide semiconductor (CMOS), a key component in analog and digital electronic systems thanks to its low power consumption, cannot be realized due to the lack of p-type oxide transistor that with a performance similar to n-type because of low hole mobility. As a result, transparent devices and circuits with higher energy efficiency and more complex structures cannot be manufactured.

For a long time, domestic and foreign academia and industry have been committed to discovering p-type semiconducting oxides to fabricating high-performance p-type oxide TFTs. One option is organic p-type TFTs, but most devices show poor stability and low mobility ($< 2\,cm^2\,V^{-1}\,s^{-1}$) [3]. An alternative to this is the inorganic p-type oxide TFTs, which have already attracted widespread attention. So far, a lot of progress has been made in p-type metal-oxide TFTs. Much attention has been given to copper oxide and tin oxide as potential p-type oxides. The simple binary oxide

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based on nickel oxide has also been studied as a promising p-type oxide. If high-performance p-type oxide TFTs can be realized through these efforts, it would usher in an era of transparent electronics that could affect many facets of our daily lives.

This paper reviews the recent progress and challenges in p-type oxide-based TFTs and it is organized in six sections, including the current introduction section numbered section 1. The TFT device structure and operation are discussed in section 2. Recent progress of p-type oxide TFTs are presented in section 3. Later on, miscellaneous applications of p-type oxide TFTs are given in section 4, while current issues and challenges of p-type oxide TFTs are presented in section 5. Finally, necessary conclusions are summarized in section 6.

# 2 TFT device structures and operation

## 2.1 TFT device structures

TFTs are three-terminal field-effect devices, whose working principle is quite similar to other field-effect devices in terms of operation and composing layers, such as the well-known MOSFETs. The three terminals are respectively named source, drain and gate. When a voltage is applied on the gate electrode of a MOSFET, carriers are injected near the dielectric/semiconductor interface, forming a parallel-plate capacitor structure along with the gate dielectric and semiconductor. Then the current between two electrodes (source and drain) is controlled by modulating the semiconductor channel, called as field-effect. Different from the MOSFETs, there is no p-n junction in the source and drain regions of TFTs, and the modulation is achieved by an accumulation layer, while in MOSFETs an inversion region has to be formed close to the dielectric/semiconductor interface. In addition, the substrate materials and manufacturing temperatures of these two devices are also quite different [1, 2, 4].

### 2.1.1 Top-gate and bottom-gate structures

The typical structures of TFTs can be divided into top-gate (TG) and bottom-gate (BG) types, depending on the position of the gate electrode (on the top or bottom of the structure). For each type, it can be further subdivided into coplanar (C) and staggered (S) types according to the relative locations of the three electrodes to the semiconductor layer. For the C-TG and C-BG TFT structures, the semiconductor/dielectric interface directly contacts the source and drain, indicating that the current flows horizontally in a single plane. In contrast, for the S-TG and S-BG structures, the source and drain contact the opposite side of the semiconductor/dielectric interface, indicating that the current flows in two planes: first vertically to the channel then horizontally from source to drain [4, 5]. The schematics of these structures are shown in Figure 1.

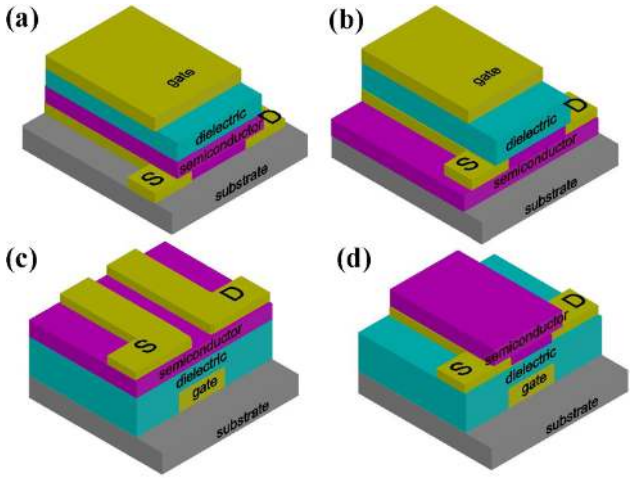


**Figure 1:** Schematics of typical TFT structures: (a) S-TG, (b) C-TG, (c) S-BG, (d) C-BG

Each structure has advantages and disadvantages, depending on the manufacturing material and the working conditions of the TFT devices. For TG structures, there is no overlap between the gate and the source/drain electrode, and consequently, it does not create a signal delay from the parasitic capacitance [4–6]. Meanwhile, the TG structure is preferred not only when a semiconductor material requires high processing temperatures that may damage the previously deposited layers, but also when a semiconductor with a high-quality crystal structure is desired or the semiconductor is a flat and continuous film without any layers beneath it. In addition, in this structure the top gate insulator and electrode may act as a passivation layer, which protects the semiconductor layer from external damage, also saving cost and reducing process steps. However, this structure is not suitable for liquid crystal display (LCD) application, because light from the backlight unit reaches the semiconductors without being shielded by the metal gate electrode, the stability of oxide semiconductor for light illumination should be strengthened. For BG structures, they are widely used for the fabrication of TFTs, mostly due to the simple fabrication process and en-

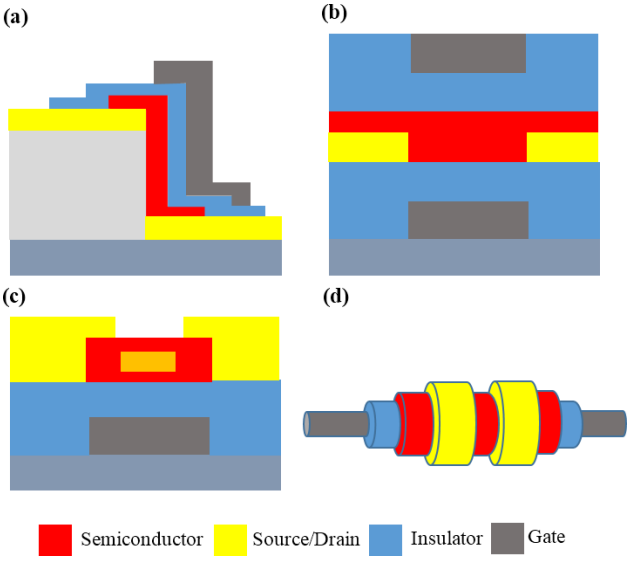


**Figure 2:** Schematics of improved TFT structures: (a) V-TFT, (b) DG-TFT, (c) BL-TFT, (d) CG-TFT

hanced electrical properties. It can also block the backlight by the metal gate electrodes on TFTs. It is worth noting that the semiconductor layer in this structure is directly exposed to air, which can be a simple way to modify its properties, but can also lead to instability effects. In addition, the back channel surfaces can suffer damage from subsequent source/drain patterning or back channel etch processes [5, 6]. In order to overcome these problems, the back channel etched (BCE) structure or the etch stopper (ES) structure are applied to the TFTs [7, 8].

### 2.1.2 Improved structures

To improve the characteristics of TFT devices, some improved structures of TFT devices have been reported, as shown in Figure 2. For most TFTs, the channel length is determined by photolithographic patterning step rather than the thickness of a device layer. It is difficult to satisfy the recent demand for small device footprint and nanoscaled channel lengths [9, 10]. However, it is imperative to reduce the driving voltage without compromising the output driving capability that can be achieved by reducing the channel length [11]. To fill this gap, the vertical TFT (V-TFT) was developed and it demonstrated good potential for fabricating smaller length devices. In V-TFT structure, the channel is formed on a multi-layer stack of source-dielectric-drain. To improve the electrical characteristics, double-gate TFT (DG-TFT) structures can be employed. In DG-TFT structure, an additional gate can effectively control a larger portion of the semiconductor channel. Therefore, the dual gate device performs better than the single gate mainly in terms of mobility, on/off current ratio and sub-threshold swing [12, 13]. Also, DG-TFTs have been reported to exhibit excellent device stability [14]. Besides, the buried-layer TFT (BL-TFT) structure with a highly doped additional active layer buried at the interface between the active channel layer and the dielectric has been reported with the stability and the mobility improvements, since the suggested instability mechanism is the oxygen adsorption and carrier trapping/detrapping on the back interface and the gate-interface between channel layer and gate-insulator [15]. Recently, the cylindrical gate TFT (CG-TFT) structure has been reported and it has the potential to be applied to smart textiles (wearable electronics for example) due to the unique combination of electrical and mechanical properties. In addition, the cylindrical structure is designed to reduce size to achieve higher packing density [16–19]. The CG-TFT used a metal core of yarn as the gate electrode, then casing it with a thin insulating layer. The semiconductor layer was later deposited and source-drain contacts were formed finally.

## 2.2 TFT device operation

The most important static characteristics of p-type TFTs can be extracted from their output and transfer characteristics, as shown in Figure 3. The output characteristics of p-type TFTs can be divided into two main operating regions according to the value of the drain-source voltage ($V_{DS}$), namely, linear region and saturation region.

In the linear region, the $V_{DS}$ value is small, and the channel resistance is basically controlled by the gate-source voltage ($V_{GS}$), the accumulated charges are uniformly distributed throughout the channel. The field effect between drain and source is equivalent to a variable resistor controlled by the $V_{GS}$, with a linear increment in the current with respect to $V_{DS}$ [20, 21]. The drain-source current ($I_{DS}$) can be described as:

$$I_{DS} = -\mu_{FE} C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (1)$$

where $\mu_{FE}$ is the field-effect mobility, $C_{ox}$ is the gate dielectric capacitance per unit area, and W and L are the channel width and length.

In the saturation region, the $V_{DS}$ is higher than the $V_{GS}$, when $V_{GS}$ is constant, the $I_{DS}$ hardly changes with the $V_{DS}$ and presents constant current characteristic. Near the drain electrode, a lack of channel region results from the depletion of the charges in the accumulation layer near this electrode, and is defined as the pinch-off [22, 23]. The

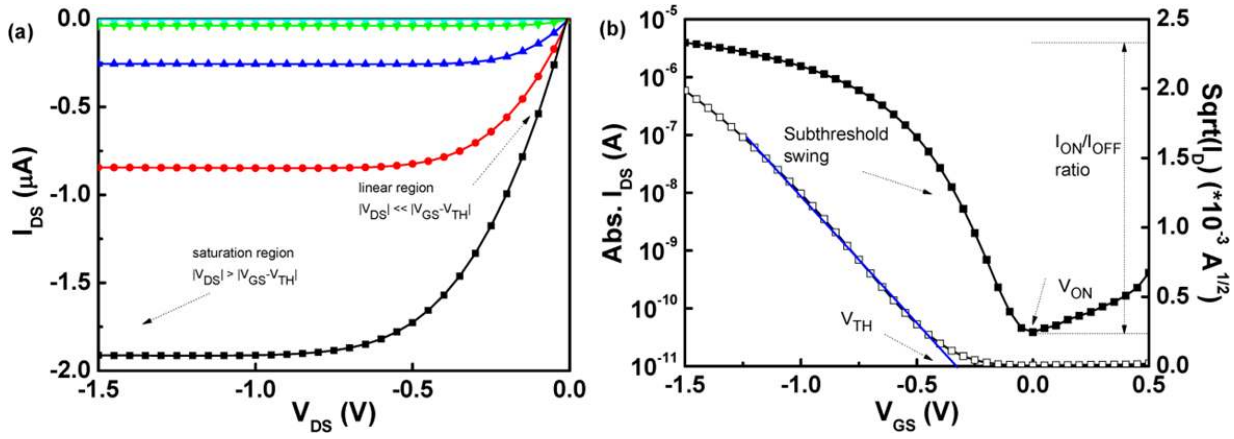


**Figure 3:** Typical output and transfer characteristics of p-type TFTs

$I_{DS}$ can be approximately given by:

$$I_{DS} = -\mu_{sat} C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2 \quad (2)$$

where $\mu_{sat}$ is the saturation mobility.

The performances of the TFT device can be judged by the transfer and output characteristics. However, this method is inefficient. Thus, we evaluated the device characteristics by defining some important parameters, including on/off current ratio, threshold voltage, turn-on voltage, sub-threshold swing and mobility, which can be extracted from the transfer characteristic. These important parameters of the TFTs are introduced below.

(i) On/off current ratio. The on/off current ratio ($I_{ON}/I_{OFF}$) is usually defined as the ratio of the maximum $I_{DS}$ to the minimum $I_{DS}$ (typically in saturation region) [24], which can be extracted from the transfer characteristic curve. Normally, this value is greater than $10^6$ or more for digital circuits [25], but the value of $10^4$ is sufficient for analog circuits [26].

(ii) Threshold voltage. Threshold voltage ($V_{TH}$) is the value of $V_{GS}$ when the accumulation layer or conductive channel formed near the dielectric layer/active layer interface in TFTs. In p-type TFTs, if $V_{TH}$ is negative/positive, the devices are designated to operate in enhancement/depletion mode. Both enhanced and depleted devices can be used in the circuit, but the enhancement-mode is preferred because there is no need for additional $V_{GS}$ to turn off the transistor, which simplifies circuit design and reduces power consumption. There are several methods used to extract $V_{TH}$, such as linear extrapolation of the $I_{DS}$-$V_{GS}$ plot (linear region) or of the $I_{DS}^{1/2}$-$V_G$ plot (saturation region), $V_{GS}$ corresponding to a specific $I_{DS}$ [27]. The most employed methodology is the second method, which defines the intersection point between the reverse extension line of the linear region in the $I_{DS}^{1/2}$-$V_G$ curve as the $V_{TH}$. It is noted that even if you choose one method to define $V_{TH}$, $V_{TH}$ also has a large ambiguity.

(iii) Turn-on voltage. Turn-on voltage ($V_{ON}$) is simply defined as the $V_{GS}$ for the onset of drain current conduction, simply corresponding to the $V_{GS}$ at which the $I_{DS}$ starts to increase as seen in a log $I_{DS}$-$V_{GS}$ plot or the $V_{GS}$ at which the TFT is turned off completely.

(iv) Sub-threshold swing. The sub-threshold swing (SS) is an important parameter that indicates the switching efficiency of a transistor. The SS is directly related to the quality of the dielectric/semiconductor interface [24, 28], and defined as the inverse of the maximum slope of the transfer characteristic and reflected by the $V_{GS}$ needed to increase the $I_{DS}$ by one decade in the sub-threshold region. The lower the SS value is, the faster the operation speed is and the lower the power consumption is. The SS value can be given by:

$$SS = \left( \frac{\partial log I_{DS}}{\partial V_{GS}} |_{max} \right)^{-1} \quad (3)$$

The characteristics of TFTs are well known to be strongly influenced by the interface trap states at the dielectric/semiconductor interface because the field-induced carriers are confined in a very thin region close to the interface. The interface defects can produce trapping or scattering effects, leading to SS degradation. Therefore, the interface trap density ($D_{it}$) can be evaluated according to the SS equation by:

$$D_{it} = \frac{1}{q} \left( \frac{qSS}{2.3kT} - 1 \right) C_{ox} \quad (4)$$

where $k$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the charge quantity of an electron.

(v) Mobility. Mobility is a parameter related to the efficiency of carrier transport in the material, which directly affects the maximum $I_{DS}$ and the operating frequency of devices [29]. Mobility is affected by several scattering mechanisms, including lattice vibrations, ionized impurities, grain boundaries, interface surface roughness, lattice strain and other structural defects, velocity saturation, and electron trapping [30]. As a result, the channel mobility may not be constant and can vary with $V_{DS}$ and $V_{GS}$. In a real TFT, mobility varied with voltage requires the definition of several types: effective mobility, field-effect mobility and saturation mobility.

Effective mobility ($\mu_{eff}$) can be obtained by the output conductance ($g_d$) in the linear region (at low $V_{DS}$) according to the equation:

$$\mu_{eff} = \frac{g_d L}{WC_{ox}(V_{GS} - V_{TH})} \tag{5}$$

Field-effect mobility ($\mu_{FE}$) can be obtained by the transconductance ($g_m$) in the linear region (at low $V_{DS}$) according to the equation:

$$\mu_{FE} = \frac{g_m L}{WC_{ox} V_{DS}} \tag{6}$$

Saturation mobility ($\mu_{sat}$) can be obtained using the transconductance in the saturation region (at high $V_{DS}$) according to the equation:

$$\mu_{sat} = \frac{2L}{WC_{ox}} \left( \frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}} \right)^2 \tag{7}$$

It is noted that the $\mu_{eff}$ requires $V_{TH}$ to be determined, and the L used to calculate $\mu_{sat}$ is larger than the actual length due to $\mu_{sat}$ describing a situation where the channel is pinched off. Therefore, the $\mu_{FE}$ is the most widely used parameter to evaluate the performance of the TFTs because of its simple calculation.

# 3 Recent progress of p-type oxide TFTs

## 3.1 Historical perspective

With the great success of n-type oxide semiconductor and its application in oxide-based TFTs, researchers are eager to fabricate p-type oxide TFTs with performances similar to their n-type counterparts, so that more energy-efficient and more complex transparent devices and circuits can be fabricated, such as CMOS, a key component in analog and digital electronic systems. The main difficulty in achieving p-type oxide TFTs is the low hole mobility due to the unique electronic configuration of oxide materials. The majority of metal oxide semiconductors are characterized by the conduction band minimum (CBM) with spatially spread metal orbitals (s) and the valence band maximum (VBM) with rather localized oxygen orbitals (2p). Thus, the mobility of valence band derived carriers is generally lower than that of conduction band derived carriers, namely, high electron mobility and low hole mobility. Even when a certain concentration of holes is available, the VBM consists mainly of anisotropic and localized oxygen 2p orbitals, resulting in a large hole effective mass and low mobility due to hopping conduction [31–34].

Therefore, in order to obtain high-performance p-type oxide TFTs, the best strategy is to find a material in which the VBM is formed by hybridized orbitals of O 2p and appropriate orbitals of neighboring metal cations [32, 35]. According to this principle, a series of p-type oxide semiconductors was discovered through the use of hybridized orbitals between O 2p and Cu 3d, namely $CuAO_2$ (A=B, Al, Ga and In), $SrCu_2O_2$, and LaCuOCh (Ch=S and Se). Similar electronic structures were also found in $Cu_2O$ and $Ag_2O$ [32, 36, 37]. However, except for $Cu_2O$, other materials exhibit either very low mobility or very high hole density, suggesting that they are not suitable for TFTs [38]. $Cu_2O$ also has an electronic structure, in which the VBM is composed of O 2p and Cu 3d hybridized orbitals, and its hole density can be well controlled [35, 39]. Thus, $Cu_2O$ has become a promising p-type oxide semiconductor with high mobility, and the first p-type $Cu_2O$ TFT was demonstrated by Matsuzaki *et al.* in 2008 [40]. An alternative approach to attain high-performance p-type oxides TFTs is to find an oxide in which the VBM is made of spatially spread s orbitals. Such electronic structures were found in oxides of heavy metal cations, such as PbO, $Bi_2O_3$ and SnO. Among them, it has been reported that PbO is n-type semiconductor, while $Bi_2O_3$ is p-type semiconductor with low mobility [41, 42]. In particular, $SnO_x$ has a unique electronic structure, in which the VBM is formed by hybridized orbitals of localized oxygen (2p) and spatially spread Sn metal (5s) [35]. The first p-type SnO TFT was introduced by Ogo *et al.* in 2008 [43]. In addition, NiO has a structure that the VBM is formed by hybridized orbitals of localized oxygen (2p) and partially filled metal d orbitals [44–46], and the spontaneously formed Ni vacancies resulted in the stable p-type character of NiO [47]. Therefore, the simple binary oxide

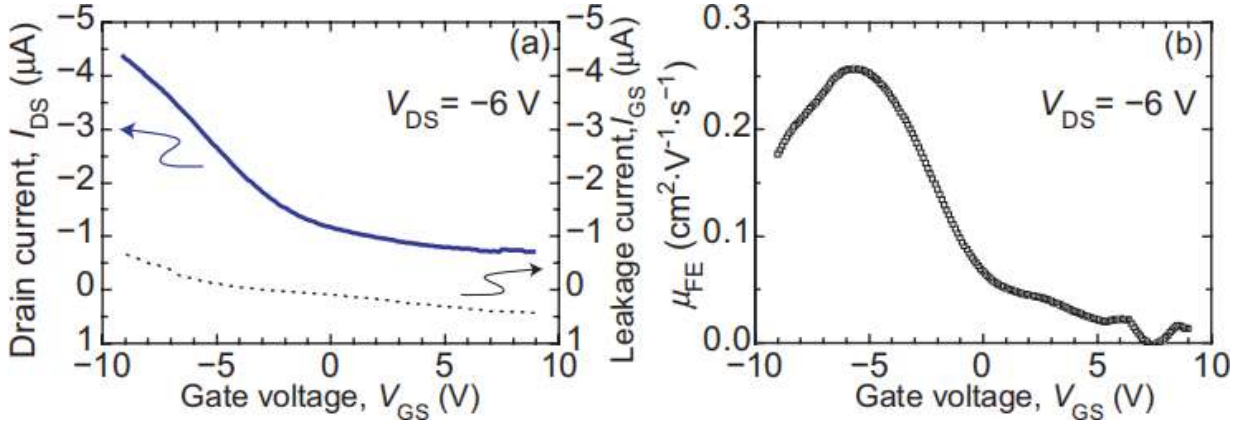


**Figure 4:** Characteristics of the first p-type $Cu_2O$ TFT [40]

based on NiO has also been utilized to realize p-type oxide TFTs.

Furthermore, the growth of the potential p-type oxide materials is always of the great importance for the fabrication of p-type oxide TFTs. Since different thin film growth techniques have different advantages in processing materials, we must choose the appropriate technique according to different materials and applications. Reactive magnetron sputtering is very advantageous to control the stoichiometry of the deposited film, oxygen content for example, and the power source of sputtering target can be direct current or radio frequency for conductive target and insulated target, respectively. Atomic layer deposition is commonly used to accurately control the film thickness and composition, thus suitable for growing uniform and high-quality films in large-area electronics. Thermal oxidation is a conventional approach for preparing high-quality oxides because of its simplicity and low cost. The solution-based fabrication provides a simpler and more cost-effective route with very high throughput.

In the following subsections, the discussion will focus on recent research progress of the emergent and promising p-type oxide TFTs based on copper oxide, tin oxide and nickel oxide with different film growth techniques.

## 3.2 Copper oxide TFTs

In 2008, the first p-type $Cu_2O$ TFTs were reported by Matsuzaki *et al.* [40], which were grown by pulsed laser deposition (PLD) at 700°C on MgO substrates. It is a coplanar top-gate TFT with a 150-nm-thick amorphous $Al_2O_x$ gate insulator deposited by PLD at room temperature (RT) with $P_{O2} = 1\times10^{-3}$ Pa. The Au source/drain/gate electrodes were formed by e-beam evaporation. The TFT exhibited a high Hall mobility (90 $cm^2\ V^{-1}\ s^{-1}$), but the $\mu_{FE}$ was low at 0.26 $cm^2\ V^{-1}\ s^{-1}$ and the $I_{on}/I_{off}$ was just 6 which was not enough for practical circuits. The main reason for the low $\mu_{FE}$ was the subgap traps formed by the extra defects, which were mainly oxygen vacancies or secondary CuO phase. The characteristics of this TFT are presented in Figure 4.

Two years later in 2010, Fortunato *et al.* reported the first low temperature bottom-gate p-type $Cu_2O$ TFT [39, 48]. The $Cu_2O$ films were deposited by reactive rf magnetron sputtering (RFMS) at RT and annealed in air at 200°C. An engineered insulator consisting of a superlattice of $Al_2O_3$ and $TiO_2$ (ATO) with a thickness of 220 nm was used as the gate dielectric. After annealing in air at 200°C for 10 hours, the Hall mobility was improved from 0.65 to 18.5 $cm^2\ V^{-1}\ s^{-1}$, which was associated with an increase of the grain size from 8.30 to 15.72 nm. And a $\mu_{FE}$ of $1.2\times10^{-3}$ $cm^2\ V^{-1}\ s^{-1}$ and an $I_{on}/I_{off}$ of $2\times10^2$ were obtained. This study was very important due to the successful fabrication of p-type oxide TFTs using an industry-compatible method at low temperature. In the same year, the bottom-gate structured p-type TFTs using CuO active layers were demonstrated by Sung *et al.* [49]. The $Cu_2O$ thin films deposited at RT using RFMS were transformed to a CuO phase with optical bandgap of 1.41 eV after an annealing treatment in air above 200°C. The TFT device exhibited an $I_{on}/I_{off}$ of $10^4$ and a $\mu_{FE}$ of 0.4 $cm^2\ V^{-1}\ s^{-1}$.

In order to improve the performance of $Cu_2O$-based TFTs, in 2010 Zou *et al.* used the top-gate configuration together with a very thin layer (20 nm) of high-$\kappa$ HfON as a gate dielectric [50]. As compared to the conventional $SiO_2$ gate dielectric, high-$\kappa$ material with high dielectric constant such as $Al_2O_3$, $Ta_2O_5$, and $HfO_2$ has been often employed as the gate dielectric, since it can effectively improve the device performance due to the high gate capacitance density. The films were grown on $SiO_2$/Si substrate

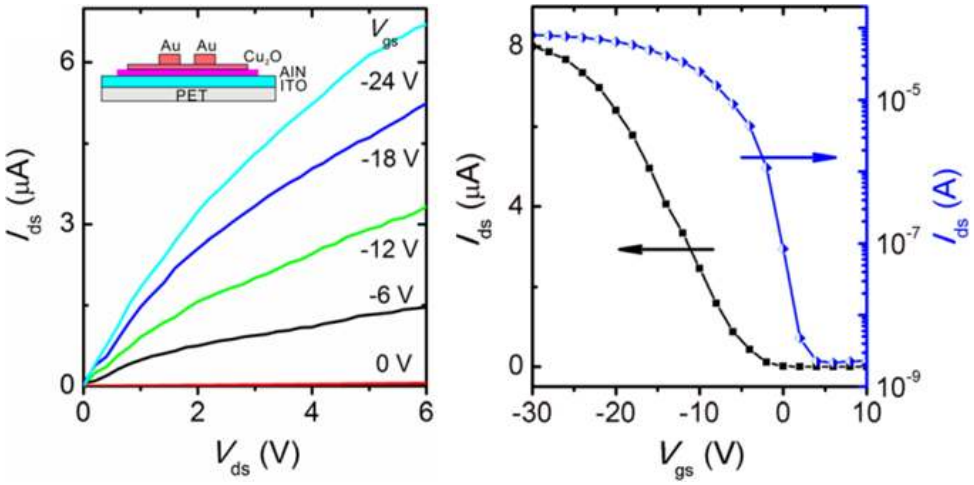


**Figure 5:** Characteristics of the first flexible p-type $Cu_2O$ TFT [52]

by PLD under different substrate temperature and the optimal condition was obtained at 500°C. The TFT showed a high $I_{on}/I_{off}$ of $3\times10^6$, a SS of 0.18 V/decade and a large $\mu_{sat}$ of 4.3 $cm^2\ V^{-1}\ s^{-1}$ at low operation voltages. The optimal performance of the p-type $Cu_2O$ TFTs were ascribed to the increased Hall mobility resulting from the decreased scattering of both the ionized defects and the grain boundary for $Cu_2O$ channel films, and the superior property of the $Cu_2O$/HfON interface.

In 2011, Zou *et al.* further reported another bottom-gate p-type $Cu_2O$ TFTs with the $HfO_2/SiO_2$ stacked gate dielectric [51], which exhibited superior performances with a $\mu_{sat}$ value of 2.7 $cm^2\ V^{-1}\ s^{-1}$, an $I_{on}/I_{off}$ of $1.5\times10^6$ and a SS of 137 mV/decade. The $Cu_2O$ thin film and $HfO_2$ high-$\kappa$ gate dielectric were deposited by pulsed laser ablation. The $Cu_2O$ TFT with the $HfO_2/SiO_2$-stacked gate dielectric exhibited good output and transfer properties, yielding six-fold mobility improvement as compared with that with the $SiO_2$ gate dielectric. This study revealed the bilayer dielectric could effectively improve interface properties and decrease gate-leakage current and then increase the mobility, reduce the SS and enhance the stability of the gate-bias-voltage stressing.

Different from the restriction of high processing temperature (200–700°C) for the above works, in 2012, Yao *et al.* reported the fabrication of the first flexible bottom-gate p-type $Cu_2O$ TFT magnetron sputtered (MS) at RT without any post-annealing [52]. Figure 5 shows the output and transfer characteristics of the first flexible p-type $Cu_2O$ TFT with the schematic structure in the inset. The TFT device showed a high $\mu_{FE}$ of 2.4 $cm^2\ V^{-1}\ s^{-1}$ and an $I_{on}/I_{off}$ of ~$4\times10^4$. The device consists of nano-crystalline $Cu_2O$ films as the active channel, a high-$\kappa$ AlN as the gate dielectric, and ITO films as the electrodes on PET substrates at RT. The superior transfer performance suggested the good potential for applications in high-throughput and low-cost electronics.

Thermal oxidation is one of the conventional methods for preparing high-quality oxides because of its simplicity and low cost [53]. In 2013, Figueiredo *et al.* first prepared copper oxide thin films by thermal oxidation (TO) of metallic copper (Cu) at different temperatures (150–450°C). The TFT devices were produced successfully by TO of a 20 nm Cu film, obtaining p-type $Cu_2O$ TFT (at 200°C) with an $I_{on}/I_{off}$ of 60 and CuO (at 250°C) TFT with an $I_{on}/I_{off}$ of $10^2$, and the $\mu_{FE}$ is $1.56\times10^{-3}$ $cm^2\ V^{-1}\ s^{-1}$ and $1.16\times10^{-3}$ $cm^2\ V^{-1}\ s^{-1}$, respectively.

In 2013, Kim *et al.* presented the potential of using the solution process to fabricate p-type $Cu_2O$ TFT for the first time [54]. The $Cu_2O$ thin films were grown by sol-gel spin coating (SC) and annealed at 400°C in $N_2$ atmosphere for 30 min then at 700°C for 30 min in $O_2$ atmosphere to improve surface uniformity. A staggered bottom-gate TFT was fabricated on Si substrate with $SiO_2$ as the dielectric layer, and Ni/Au was chosen as the source and drain electrodes. The p-type operation with a $\mu_{FE}$ of ~0.16 $cm^2\ V^{-1}\ s^{-1}$ and an $I_{on}/I_{off}$ of ~$1\times10^2$ was obtained, paving the way for the development of solution-based p-type TFTs.

In 2014, Chen *et al.* reported a p-type CuO TFT fabricated by dc reactive sputtering (DCMS) of copper at RT instead of PLD and RFMS [55], which may be applied to large-scale production with low cost. The TFT device used the bottom-gate configuration together with a very thin layer (60 nm) of $HfO_2$ as the gate dielectric. The post-annealed CuO TFT with the oxygen partial pressure ($O_{pp}$) of 30% exhibited p-type characteristics with a $\mu_{FE}$ of ~$5\times10^{-3}$ $cm^{-2}\ V^{-1}\ s^{-1}$ and an $I_{on}/I_{off}$ of ~$10^2$.

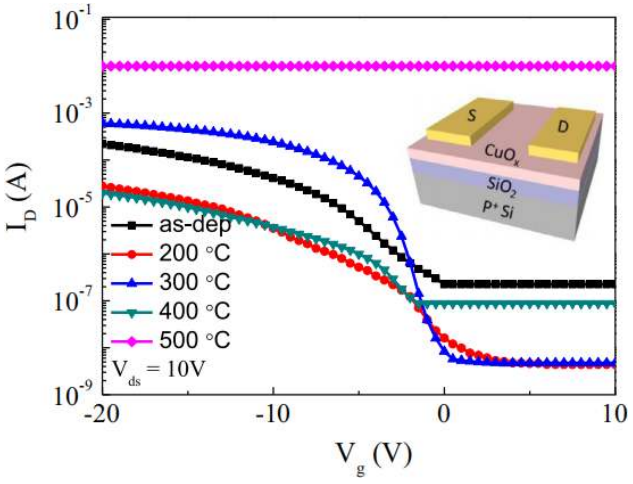


**Figure 6:** Transfer characteristics of the $CuO_x$ TFTs with various annealing temperatures [56]

An alternative deposition method of the active channel layer is atomic layer deposition (ALD), which provides accurate control of the film thickness and composition, thus suitable for growing uniform and high-quality films in large-area electronics. In 2015, Maeng *et al.* reported the TFT device incorporating the ALD-grown $CuO_x$ semiconductor [56], attained an unusually high-performance p-type device with a $\mu_{FE}$ of ~5.6 $cm^2\ V^{-1}\ s^{-1}$ and a high $I_{on}/I_{off}$ of ~$1.8\times10^5$ after annealing at 300°C. The p-type $CuO_x$ films were grown by ALD at a relatively low temperature of 100°C. The transfer characteristics of the $CuO_x$ TFTs with various annealing temperatures were shown in Figure 6. The high performance after annealing at 300°C could be attributed to the optimized distribution of CuO and $Cu_2O$ phases in the film and the preservation of an amorphous microstructure.

Also in 2015, Liu *et al.* fabricated Cu-based oxide TFTs at low-temperature by a solution-processed method with a mobility of ~0.78 $cm^2\ V^{-1}\ s^{-1}$ and an $I_{on}/I_{off}$ of ~$10^5$ [57]. It is worth noting that the novel $ScO_x$ dielectric thin films were prepared by water-inducement route for the first time. Due to the organic-free water inducement precursor solution, it can effectively reduce the formation of volatile gases, which may generate nanopores in the resultant dielectric films and become an obstacle for high-performance electronic devices.

In 2017, Liu *et al.* further reported a simple one-step synthetic method to fabricate a p-type $Cu_xO$ thin film via in-situ reaction of a CuI film in aqueous NaOH solution at RT [58]. Figure 7 shows the fabrication process of the solution-processed $Cu_xO$ TFTs. A bottom-gated TFT with an $Al_2O_3$ high-$\kappa$ dielectric was constructed and examined. The hole mobility of the optimized device was calculated to be 0.32 $cm^2\ V^{-1}\ s^{-1}$, along with an $I_{on}/I_{off}$ of 5($10^4$ and a SS of 1.1 V/decade. It is referred that the large area capacitance of $Al_2O_3$ gate dielectric leads to the increase of hole mobility and the decrease of operating voltage. This study demonstrated a simple and efficient route to fabricate high-quality p-type $Cu_xO$ thin films.

It's worth noting that in 2018 Jung *et al.* explored the effects of hypochlorous acid (HClO) oxidation on p-type oxide semiconductors [59]. With the treatment of HClO-based oxidation, oxygen radicals changed the film composition, simply reducing the $V_{cu}$ levels in the $CuO_x$ thin films, thus improving the switching characteristics of the p-type TFT. In the modified $CuO_x$ TFT, the SS was 0.70 V/decade, the $I_{on}/I_{off}$ was ~$4.9\times10^4$, and the $\mu_{FE}$ was ~2.8 $\times\ 10^{-3}$ $cm^2\ V^{-1}\ s^{-1}$. Figure 8 shows the transfer characteristics of the $CuO_x$ TFT with HClO treatment.

In 2019, Reker *et al.* reported p-channel TFTs formed by CuO nanoparticles with a diameter of 25-55 nm dispersed in a water-based solution [60]. The semiconductor layer with CuO nanoparticles was deposited by doctor-blade process (DBP) under ambient conditions, showing encouraging electrical performance. The gate dielectric using a high-$\kappa$ organic-inorganic nanocomposite was deposited by spin-coating. The effects of gold and nickel electrodes with the treatment of 2,3,4,5,6 Pentafluorothiophenol, respectively, were investigated. It was demonstrated that the electrode treatment reduced the contact resistance between metal contacts and semiconductor CuO nanoparticles and then improved the operating voltage.

Details of the described studies on p-type copper oxide TFTs were summarized in Table 1.

## 3.3 Tin oxide TFTs

In 2008, Ogo *et al.* reported the first p-type TFT based on SnO grown epitaxially on (001) yttria-stabilized zirconia (YSZ) substrate by PLD at 575°C [43]. The $V_{th}$, $\mu_{FE}$ and $I_{on}/I_{off}$ were determined to be 4.8 V, 1.3 $cm^2\ V^{-1}\ s^{-1}$ and ~$10^2$, respectively. The TFT device was operated in depletion mode. The small $I_{on}/I_{off}$ was attributed to the high off-state current, which was associated with the large hole density (>$10^{17}$ $cm^{-3}$) in the SnO channel. Figure 9 shows the structure and characteristics of the first p-type SnO TFT.

Unlike the PLD that required high temperature, in 2010, Fortunato *et al.* reported high-performance p-type $SnO_x$ TFT by RFMS, followed by annealing at 200°C in air atmosphere [61]. The as-deposited films were amorphous but changed to polycrystalline comprising a mixture of tetragonal $\beta$-Sn and $\alpha$-$SnO_x$ phases after post-annealing.

**Table 1:** Short-review of the reported p-type copper oxide TFTs

| Channel layer | Structure (Technique) | Substrate/Dielectric | $V_{th}$ (V) | $\mu$ ($cm^2 V^{-1} s^{-1}$) | $I_{on}/I_{off}$ | SS (V/dec) | Ref. | Year |
|---|---|---|---|---|---|---|---|---|
| $Cu_2O$ | C-TG(PLD) | $MgO/Al_2O_x$ | / | 0.26 | 6 | / | [40] | 2008 |
| $Cu_2O$ | S-BG(RFMS) | Glass/ATO | −12 | $1.2(10^{-3}$ | $2\times10^2$ | / | [39, 48] | 2010 |
| CuO | S-BG(RFMS) | $Si/SiO_2$ | / | 0.4 | $10^4$ | / | [49] | 2010 |
| $Cu_2O$ | C-TG(PLD) | Si/HfON | −0.8 | / | $3\times10^6$ | 0.18 | [50] | 2010 |
| $Cu_2O$ | S-BG(PLD) | $Si/SiO_2/HfO_2$ | 0.3 | 2.7 | $1.5\times10^6$ | 0.137 | [51] | 2011 |
| $Cu_2O$ | S-BG(MS) | PET/AlN | / | 2.4 | $4\times10^4$ | / | [52] | 2012 |
| $Cu_2O$ | S-BG(TO) | Glass/ATO | / | $1.56\times10^{-3}$ | 60 | / | [53] | 2013 |
| $Cu_2O$ | S-BG(SC) | $Si/SiO_2$ | / | 0.16 | $10^2$ | / | [54] | 2013 |
| $Cu_2O$ | S-BG(DCMS) | $Glass/HfO_2$ | / | $5\times10^{-3}$ | $10^2$ | / | [55] | 2014 |
| $Cu_xO$ | S-BG(ALD) | $Si/SiO_x$ | −1.9 | 5.6 | $1.8\times10^5$ | 0.75 | [56] | 2015 |
| CuO | S-BG(SC) | $Si/ScO_x$ | −0.6 | 0.78 | $10^5$ | 0.4 | [57] | 2015 |
| $Cu_xO$ | S-BG(SC) | $Si/Al_2O_3$ | 26 | 0.32 | $5\times10^4$ | 1.1 | [58] | 2017 |
| $CuO_x$ | S-BG(SC) | $Si/SiO_2$ | / | $2.8\times10^{-3}$ | $4.9\times10^4$ | 0.7 | [59] | 2018 |
| CuO | C-BG(DBP) | Si/nanocomposite | / | 0.01 | $10^5$ | 1.2 | [60] | 2019 |

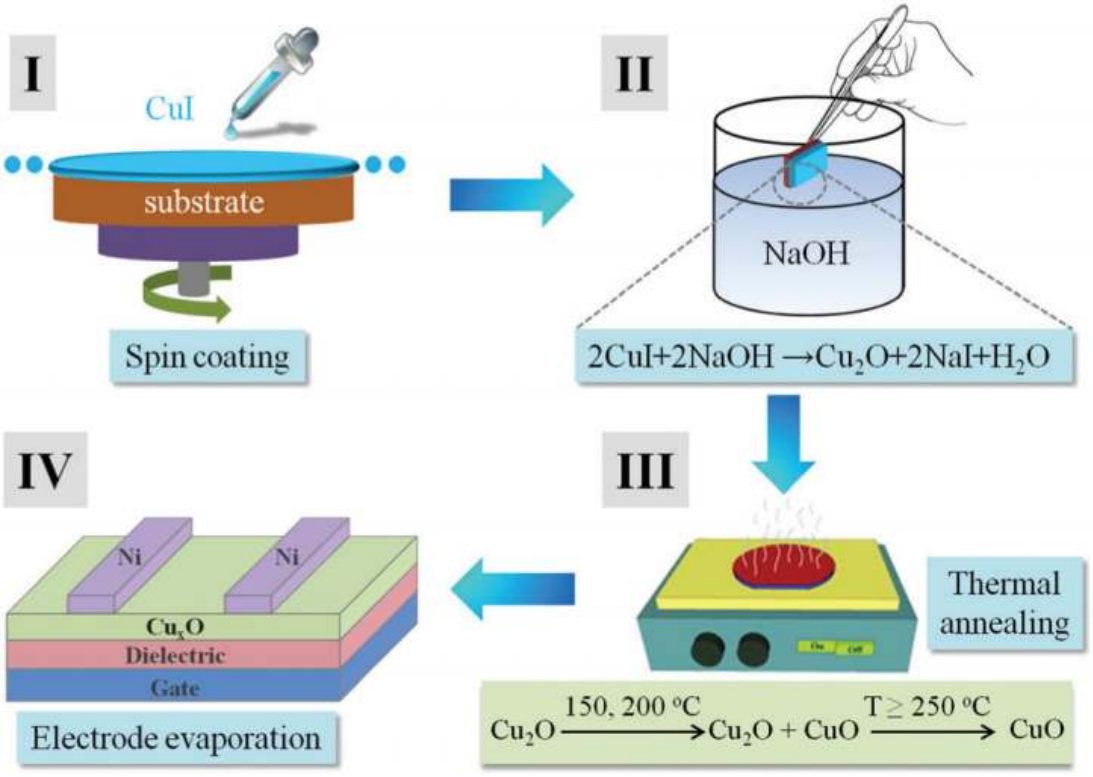


**Figure 7:** Fabrication process of the solution-processed $Cu_xO$ TFTs [58]

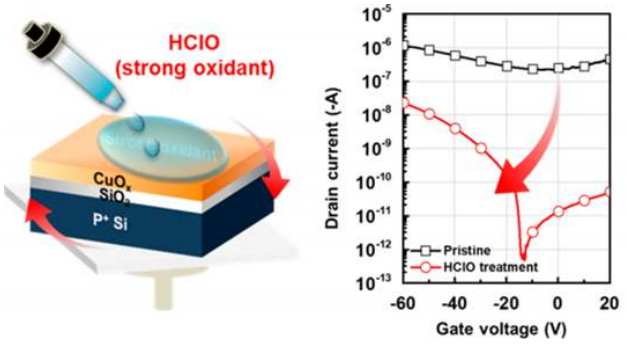


**Figure 8:** Transfer characteristics of the $CuO_x$ TFT with HClO treatment [59]

Metallic behavior was observed for $O_{pp}$ < 5%, but converted into n-type semiconductor behavior for $O_{pp}$ > 15%. The $SnO_x$ films with p-type conductivity was obtained for a narrow $O_{pp}$ range from 5% to 15%, and the fabricated $SnO_x$ TFT device exhibited the $V_{th}$, $\mu_{FE}$ and $I_{on}/I_{off}$ values of −5 V, 1.2 $cm^2\ V^{-1}\ s^{-1}$ and ~$10^3$, respectively. Furthermore, a year later, in 2011 the same group further reported a high mobility of 4.6 $cm^2\ V^{-1}\ s^{-1}$ and a high $I_{on}/I_{off}$ of 7($10^4$ by controlling the Sn oxidation state, where Ni/Au source and drain contacts were applied [62].

In 2010, Yabuta *et al.* reported p-type TFTs using polycrystalline SnO–$SnO_2$ channels grown by a conventional sputtering method and subsequent annealing treatments [63]. Figure 10 shows the schematic phase classification of SnO-$SnO_2$ films deposited with different sputtering, annealing and capping conditions. It was found that the oxidation of the SnO films decreased hole density and finally produced n-type $SnO_2$, thus proposing a simple method for selective formation of p- and n-channel TFTs by a single annealing step for producing oxide TFT complimentary circuits. In 2011, Nomura *et al.* first reported SnO TFT with ambipolar operation by PLD and its application to a complementary-like inverter [64]. The ambipolar operation could be attributed to the reduction of trap states caused by reducing the channel thickness. The $\mu_{sat}$ values of ~0.81 $cm^2\ V^{-1}\ s^{-1}$ and ~5($10^{-4}$ $cm^2\ V^{-1}\ s^{-1}$, respectively, for p- and n-channel operation were obtained. A CMOS-like inverter was built by combining two ambipolar SnO TFTs, showing voltage gain value of ~2.5.

In 2012, Okamura *et al.* demonstrated the first solution-processd p-type SnO TFT [65]. The SnO thin film was fabricated by spin-coating a precursor solution followed by post annealing. The TFT showed a $\mu_{FE}$ of 0.13 $cm^2\ V^{-1}\ s^{-1}$, a $V_{th}$ of −1.9 V and an $I_{on}/I_{off}$ of 85. The successful fabrication of solution-processed p-type SnO and functional devices significantly expands the variety of solution-processed applications. In 2013, Caraveo-Frescas *et al.* demonstrated nanoscale fully transparent p-type SnO TFTs at temperature as low as 180°C with a record $\mu_{FE}$ of 6.75 and 5.87 $cm^2\ V^{-1}\ s^{-1}$ for transparent rigid and translucent flexible substrates, respectively [66]. The $O_{pp}$ and deposition pressure were optimized during the deposition process. A detailed phase map for nanoscale physical vapor deposition of SnO has been developed for the first time, as shown in Figure 11. The results showed that the device performance was greatly improved by the control of SnO phase formation. The mix phase with small traces of $\beta$-Sn in a matrix of SnO exhibited better Hall mobility as compared to pure phase SnO. However, the high SS ranged from 7.63 to 10 V/decade indicated a high density of trap states in the semiconductor and/or at the interface with the dielectric, which needed to be optimized for further performance enhancements.

In 2014, Lee *et al.* developed a p-type SnO TFT using low-cost vacuum thermal evaporation (VTE) method combined with thermal annealing and oxygen plasma treatment [67]. An uncommonly high $\mu_{FE}$ of 5.59 $cm^2\ V^{-1}\ s^{-1}$ was achieved in this p-type SnO TFT by optimization of post-deposition treatment, providing a solution for low-cost high-performance TFT technology. However, the $I_{on}/I_{off}$ was just ~50, which was still needed improvement for practical application.

To evaluate the reliability of p-type SnO TFTs, in 2014, Chiu *et al.* investigated the gate-bias stress stability of p-type SnO TFTs [68]. The TFT device showed a $\mu_{FE}$ of 0.24 $cm^2\ V^{-1}\ s^{-1}$, a $V_{th}$ of 2.5 V, a SS of 2 V/decade and an $I_{on}/I_{off}$ of $10^3$. It was found that the $V_{th}$ was shifted with the same polarity as the stress voltage under gate-bias stress, while the $\mu_{FE}$ and SS remained almost unchanged. This phenomenon could be ascribed to charge trapping at the interface between the active layer and the gate dielectric or at the gate dielectric near the interface, which was the dominant factor for the instability of the SnO TFTs.

In 2015, Zhong *et al.* proposed p-type SnO DG-TFTs with double-gated structure, achieving excellent performances under the DG mode, including a high $\mu_{FE}$ of 6.54 $cm^2\ V^{-1}\ s^{-1}$, a low SS of 143 mV/decade and a high $I_{on}/I_{off}$ of >$10^5$ [69]. The top and bottom gates can be biased independently (single-gated mode) or jointly to switch the device (DG mode). The TFT device under the operation of DG mode exhibited great improvements in the on-state current and mobility as compared to that under the operation of BG and TG modes, which could be attributed to the accumulated carriers in the middle of the channel induced under the DG mode of operation, thus suffering less surface scattering. Besides, it was demonstrated that the transfer characteristics of the SnO TFT under single-gated mode were tunable with the bias applied to the opposite gate.

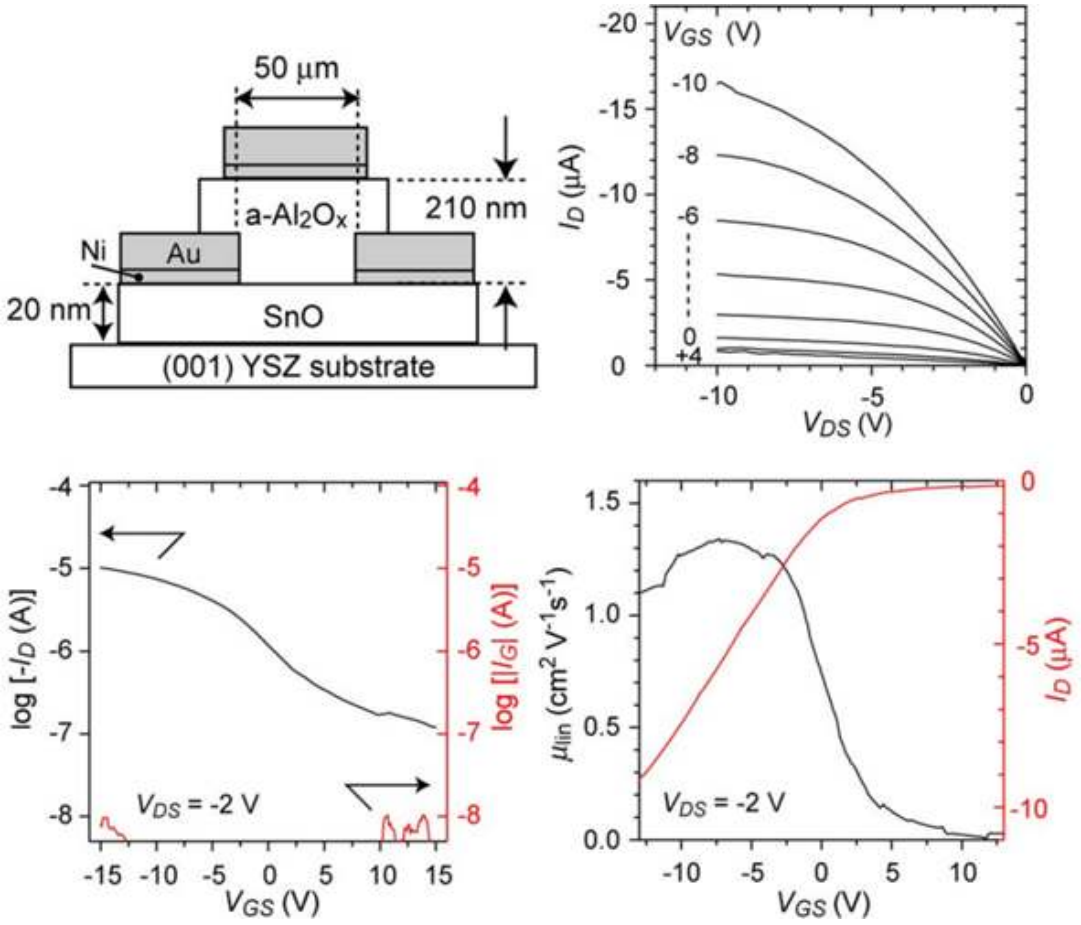


**Figure 9:** Structure and characteristics of the first p-type SnO TFT [43]

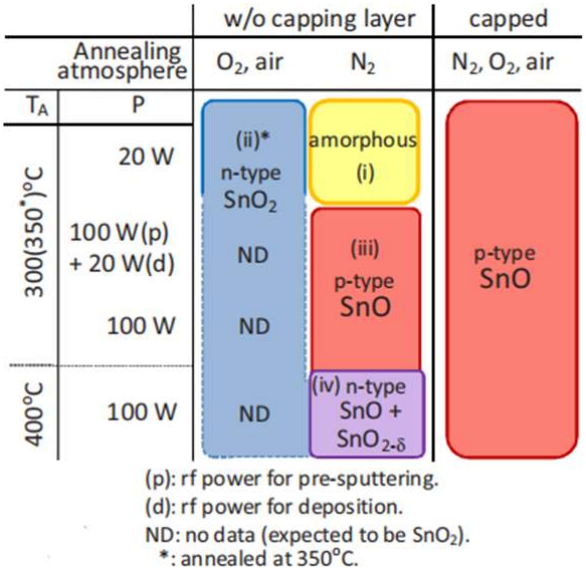


**Figure 10:** Schematic phase classification of SnO-$SnO_2$ films deposited with different sputtering, annealing and capping conditions [63]

In 2016, Chen *et al.* reported a highly sensitive p-type SnO TFT device for the application of the blue-light detection [70]. The p-type SnO TFT device exhibited a high $I_{on}/I_{off}$ of 4.47($10^4$, a low SS of 142 mV/decade and a $\mu_{FE}$ of 5.56 $cm^2$ $V^{-1}$ $s^{-1}$ in dark condition. It was observed that the TFT device exhibited a light/dark read current ratio ($I_{light}/I_{dark}$) of 18 for the red-light illumination, an $I_{light}/I_{dark}$ of $7.8\times10^2$ for the green-light illumination, and an $I_{light}/I_{dark}$ of $8.2\times10^3$ for the blue-light illumination. Figure 12 shows the transfer characteristics of the p-type SnO TFT in the dark and under light illumination at red/green/blue (RGB) wavelengths. Additionally, $\mu_{FE}$ decreased from 5.6 to 3.9 $cm^2$ $V^{-1}$ $s^{-1}$, when decreasing the wavelength of the illumination from the red-light to the blue-light. The results showed the proposed p-type SnO TFT device was very beneficial for the detection of the blue-light radiation hazard.

Furthermore, in 2016, Chen *et al.* proposed an easy approach of a channel surface treatment by oxygen plasma to achieve the bipolar conduction mechanism in SnO TFTs [71]. With increasing the exposure time of oxygen

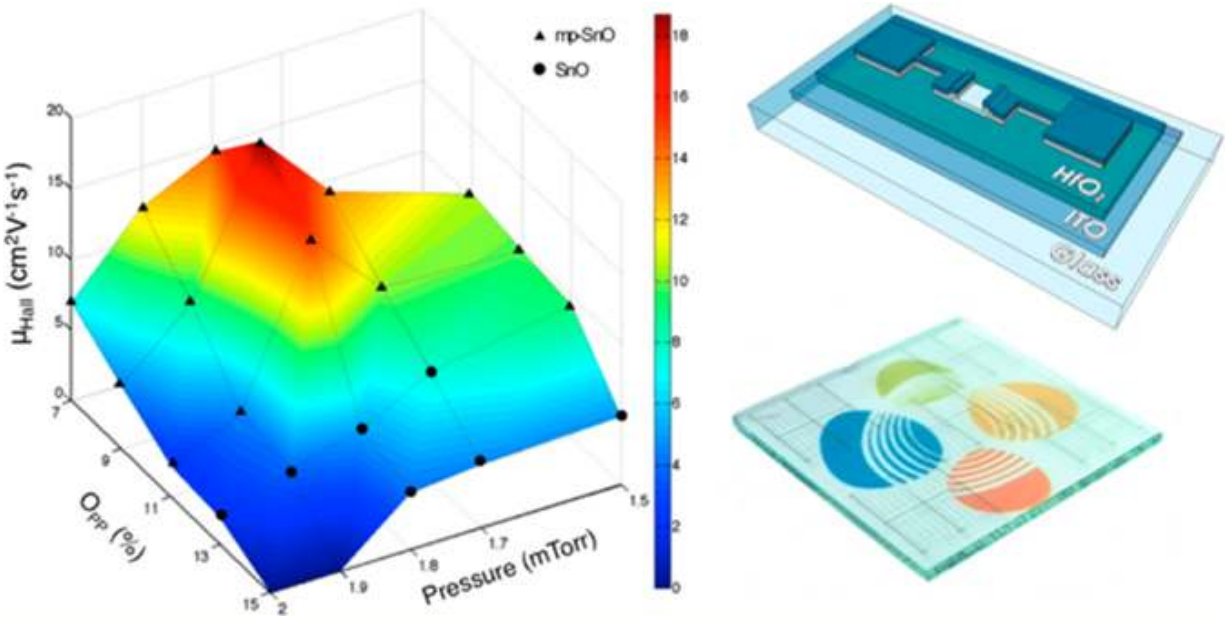


**Figure 11:** Phase map for nanoscale physical vapor deposition of SnO [66]

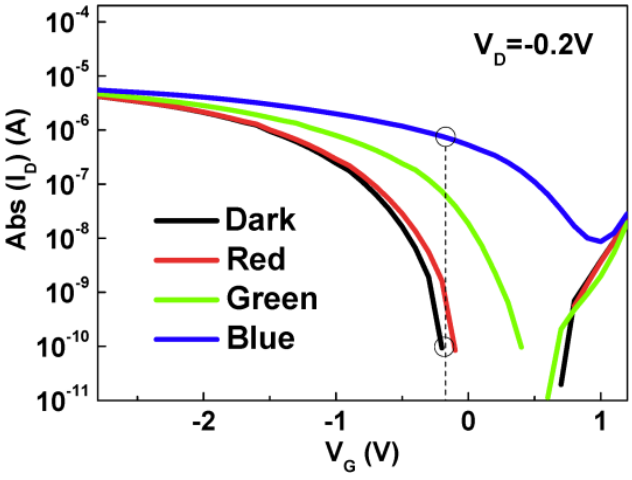


**Figure 12:** Transfer characteristics of the p-type SnO TFT in the dark and under light illumination at RGB wavelengths [70]

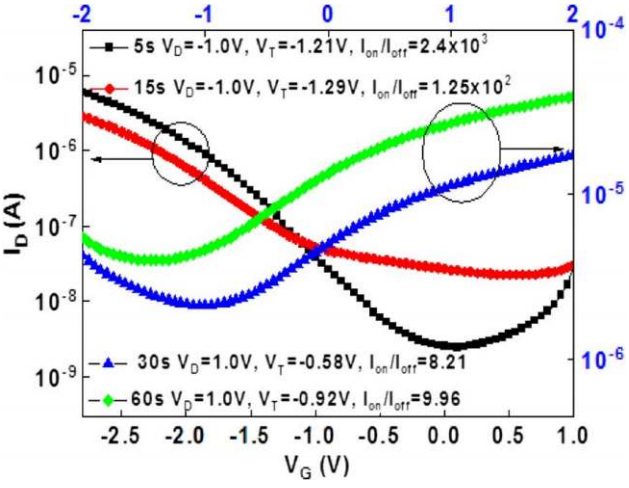


**Figure 13:** Transfer characteristics of SnO TFTs with bipolar conduction under oxygen plasma treatment on the channel with different exposure time [71]

plasma, excess oxygen was incorporated to the channel layer and converted oxygen-deficient $SnO_x$ to oxygen-rich $SnO_{2-x}$, which in turn caused the device operation from p-type to n-type. Figure 13 shows the transfer characteristics of SnO TFTs with bipolar conduction under oxygen plasma treatment on the channel layer with different exposure time. The optimal p-type SnO TFT with the oxygen plasma treated on the channel layer at 100 W for 15 s showed an $I_{on}/I_{off}$ of >$10^4$, a $\mu_{FE}$ of 2.14 cm$^2$ V$^{-1}$ s$^{-1}$ and a $V_{th}$ of –1.05 V. To investigate the mechanism, the effects of oxygen plasma treatment on band structure, density of states and electron density difference of the $SnO_x$ channel layer were performed by the first-principles calculation using density functional theory by Chiu *et al.* in 2017 [72]. The p-type $SnO_x$ TFT without the oxygen plasma treatment exhibited an $I_{on}/I_{off}$ of 4.25×$10^3$, a $\mu_{FE}$ of 6.11 cm$^2$ V$^{-1}$ s$^{-1}$ and a $V_{th}$ of –0.32 V. With the oxygen plasma treatment on the $SnO_x$ channel layer, excess reacted oxygen was incorporated to the channel, leading to n-type operation. For the SnO, the energy proximity of the Sn 5s and O 2p states results in equal contributions to the VB edge. However, for the $SnO_2$, the CB is predominated by the Sn 5s orbitals and the VB by the O 2p orbitals. The first-principles calculation

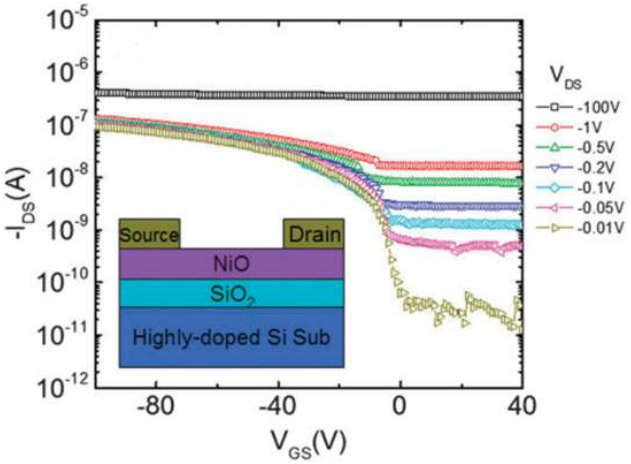


**Figure 14:** Transfer characteristics of p-type NiO TFT [82]

revealed that the oxygen plasma treatment changed the inner energy of $SnO_x$ crystal. In the same year, Chen *et al.* also demonstrated p-type and n-type SnO TFTs on flexible polyimide (PI) substrate by using simple one-mask channel pattern process and low-temperature oxygen plasma treatment on the channel layer [73]. For the flexible p-type SnO TFT device, a high $I_{on}/I_{off}$ of $5.7\times10^5$ and a high $\mu_{FE}$ of 10.7 $cm^2\ V^{-1}\ s^{-1}$ were achieved simultaneously. It showed high potential for achieving n-type and p-type TFTs under the same simple device process, which is of great importance for process simplification of CMOS devices.

Apart from oxygen plasma treatment, in 2017, Chen *et al.* proposed another approach of fluorine plasma treatment on the SnO channel layer to improve the performances of p-type SnO TFTs [74]. The fabricated p-type SnO TFT with the channel layer treated by the fluorine plasma exhibited a very high $I_{on}/I_{off}$ of 9.6($10^6$, a $\mu_{FE}$ of 2.13 $cm^2\ V^{-1}\ s^{-1}$, a very low SS of 106 mV/decade and an extremely low off-state current of 1 pA, with a $V_{th}$ of −0.92 V. These good properties could be ascribed to the fluorine plasma treatment on p-type SnO channel that reduced crystallized channel roughness and passivated oxygen vacancies and interface traps. Recently, the effects of plasma fluorination in p-type SnO TFTs were modeled and simulated by Rajshekar *et al.* [75]. The model and simulation indicated that the significant improvement in device performance could be attributed to fluorine plasma that suppressed the interface trap density and reduced the acceptor-like Gaussian states. Moreover, in 2017, Chen *et al.* also demonstrated an Al-doped SnO TFT with p-type conduction due to the substitution reactions of $Al^{3+}$-$Sn^{4+}$, which produces hole carriers in the Al-doped SnO channel layer [76]. The fluorine plasma was also treated on the Al-doped SnO channel layer with different conditions. The optimal TFT device exhibited a very high $I_{on}/I_{off}$ of 2.58($10^6$ and a low SS of 174 mV/decade, which can be ascribed to the passivation effect of the plasma fluorination on the dominant donor-like traps at the channel/dielectric interface. In addition, in 2017, Bae *et al.* demonstrated a high-performance p-type SnO TFT using argon plasma surface treatment [77]. As compared to the device without argon plasma surface treatment, the device with argon plasma treated on the channel layer for 20 s exhibited a very high $I_{on}/I_{off}$ of $5.2\times10^6$, a very low off-state current of $1.2\times10^{-12}$ A and a low SS of 0.99 V/decade.

Different from the MS and PLD methods mentioned above, which are commonly used for the deposition of the SnO channel layer, ALD is another thin film growth technique based on a self-limiting mechanism, which can keep the physical and chemical properties unchanged. In 2017, Kim *et al.* demonstrated a p-type TFT with the SnO channel deposited by ALD at 210°C and annealed at 250°C to increase the crystal quality [78]. The back-channel surface of the SnO active layer was passivated by an $Al_2O_3$ layer, which effectively reuded the defect states and hole carriers near the surface. This p-type SnO TFT exhibited a high $I_{on}/I_{off}$ of $2\times10^6$, a SS of 1.8 V/decade and a $\mu_{FE}$ of ~1 $cm^2\ V^{-1}\ s^{-1}$.

In 2018, Guan *et al.* proposed the first p-type phototransistor based on SnO thin film [79]. A layer of hybrid perovskite $CH_3NH_3PBI_3$ ($MAPbI_3$) was deposited on the SnO channel layer to enhance the device performances. As a result, the phototransistor behavior was notably changed. The $I_{on}/I_{off}$ increased from 519 to $2.7\times10^3$ and the $\mu_{FE}$ increased from 3.46 to 5.53 $cm^2\ V^{-1}\ s^{-1}$. These significant improvements were achieved due to the favorable band alignment and charge transfer between the photoactive $MAPbI_3$ and the SnO channel. In 2019, Barros *et al.* investigated the role of structure and composition on the performances of p-type $SnO_x$ TFT processed at low temperature up to 200°C [80], which was very beneficial for fully transparent CMOS either on rigid or flexible substrates. The TFTs exhibited an $I_{on}/I_{off}$ of $7\times10^4$ and a $\mu_{sat}$ of 4.6 $cm^2\ V^{-1}\ s^{-1}$.

Details of the described studies on p-type tin oxide TFTs were summarized in Table 2.

## 3.4 Nickel oxide TFTs

In 2008, Shimotani *et al.* demonstrated the first p-type electric double-layer (EDL) field-effect transistor using NiO single-crystal as the channel [81]. The transistor showed a $\mu_{FE}$ of $1.6\times10^{-4}$ $cm^2\ V^{-1}\ s^{-1}$ and an $I_{on}/I_{off}$ of 130, suggesting that the ability of EDL transistor to accumulate a high carrier density might be useful in future investiga-

**Table 2:** Short-review of the reported p-type tin oxide TFTs

| Channel layer | Structure (Technique) | Substrate/Dielectric | $V_{th}$ (V) | $\mu$ ($cm^2\ V^{-1}\ s^{-1}$) | $I_{on}/I_{off}$ | SS (V/dec) | Ref. | Year |
|---|---|---|---|---|---|---|---|---|
| SnO | C-TG(PLD) | YSZ/$Al_2O_x$ | 4.8 | 1.3 | $10^2$ | / | [43] | 2008 |
| $SnO_x$ | S-BG(RFMS) | Glass/ATO | −5 | 1.2 | $10^3$ | / | [61] | 2010 |
| SnO | S-BG(RFMS) | Si/$SiN_x$ | 30 | 0.24 | $10^2$ | / | [63] | 2010 |
| $SnO_x$ | S-BG(RFMS) | Glass/ATO | / | 4.6 | $7\times10^4$ | / | [62] | 2011 |
| SnO | S-BG(PLD) | Si/$SiO_2$ | −3 | 0.8 | $10^4$ | 1.9 | [64] | 2011 |
| SnO | S-BG(SC) | Si/$SiO_2$ | −1.9 | 0.13 | 85 | / | [65] | 2012 |
| SnO | S-BG(DCMS) | Glass/$HfO_2$ | −1 | 6.75 | $64\times10^3$ | 7.63 | [66] | 2013 |
| SnO | BG(VTE) | Si/$SiO_2$ | −4.8 | 5.59 | 50 | 28.6 | [67] | 2014 |
| SnO | S-BG(RFMS) | Glass/$HfO_2$ | 2.5 | 0.24 | $10^3$ | 2 | [68] | 2014 |
| SnO | DG(DCMS) | Si/$SiO_2$ | −0.7 | 6.54 | $>10^5$ | 0.143 | [69] | 2015 |
| SnO | S-BG(DCMS) | Si/$HfO_2$ | / | 5.56 | $4.5\times10^4$ | 0.142 | [70] | 2016 |
| SnO | S-BG(DCMS) | Si/$HfO_2$ | −1.05 | 2.14 | $>10^4$ | / | [71] | 2016 |
| $SnO_x$ | S-BG(DCMS) | Si/$HfO_2$ | −0.32 | 6.11 | $4.3\times10^3$ | / | [72] | 2017 |
| SnO | S-BG(DCMS) | PI/$HfO_2$ | −0.92 | 10.7 | $5.7\times10^5$ | 0.113 | [73] | 2017 |
| SnO | S-BG(DCMS) | Si/$HfO_2$ | −0.92 | 2.13 | $9.6\times10^6$ | 0.106 | [74] | 2017 |
| Al:SnO | S-BG(DCMS) | Si/$HfO_2$ | / | / | $2.6\times10^6$ | 0.174 | [76] | 2017 |
| SnO | S-BG(RFMS) | Si/$SiO_2$ | / | 0.63 | $5.2\times10^6$ | 0.99 | [77] | 2017 |
| SnO | S-BG(ALD) | Si/$SiO_2$ | / | 1 | $2\times10^6$ | 1.8 | [78] | 2017 |
| SnO | S-BG(DCMS) | Glass/$HfO_2$ | | 5.53 | $2.7\times10^3$ | / | [79] | 2018 |
| $SnO_x$ | S-BG(RFMS) | Glass/ATO | −10 | 4.6 | $7\times10^4$ | / | [80] | 2019 |

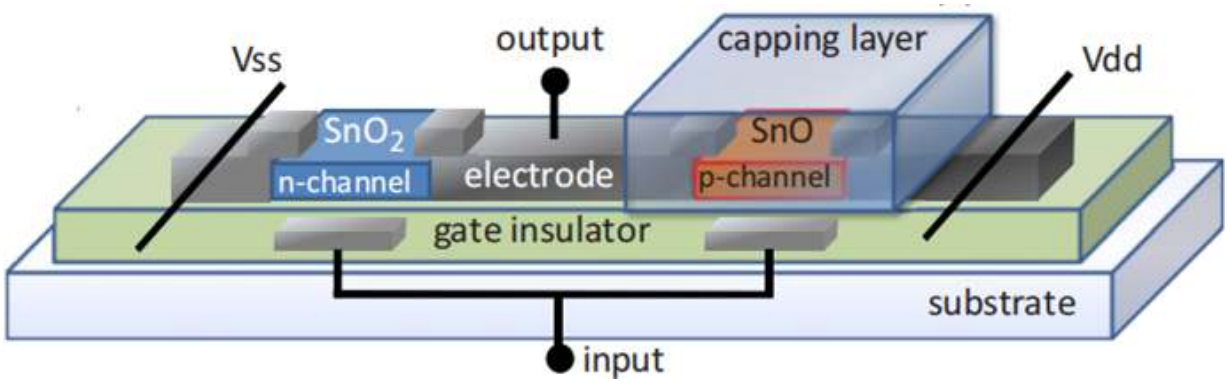


**Figure 15:** A conceptual design of a SnO-based CMOS inverter [63]

tions of Mott insulators. In 2013, Jiang *et al.* reported a p-type nanocrystal NiO-based TFT fabricated by simply thermally oxidizing (TO) the electron-beam evaporated Ni thin films at 400°C in air [82], which exhibited a $\mu_{FE}$ of 5.2 $cm^2\ V^{-1}\ s^{-1}$, an $I_{on}/I_{off}$ of $2.2\times10^3$ and a SS of 3.91 V/decade. Figure 14 shows the transfer characteristics of the p-type NiO TFT. By controlling the annealing time, the upper parts of the Ni films were clearly oxidized and the lower parts in contact with the gate dielectric were partially oxidized to form a quasi-discontinuous Ni layer, which contributed to the high mobility of this TFT.

In 2014, Liu *et al.* reported a solution-processed p-type $NiO_x$ TFT. The $NiO_x$ film was formed via spin-coating the precursor solution onto the substrate, followed by annealing at 275°C for 1 h [83]. However, the p-type $NiO_x$ TFT only exhibited a $\mu_{FE}$ of 0.141 $cm^2\ V^{-1}\ s^{-1}$. In 2015, Chen *et al.* investigated the effects of the growth temperature and gas flow ratio on the electrical properties of sputtered NiO films and fabricated the corresponding p-type NiO TFTs [84]. It was found that the p-type NiO TFT showed a $\mu_{sat}$ of 0.05 $cm^2\ V^{-1}\ s^{-1}$, a $V_{th}$ of −8.6 V, a SS of 2.6 V/decade and an $I_{on}/I_{off}$ of $10^3$. It should be noted

**Table 3:** Short-review of the reported p-type nickel oxide TFTs

| Channel layer | Structure (Technique) | Substrate/Dielectric | $V_{th}$ (V) | $\mu$ ($cm^2\ V^{-1}\ s^{-1}$) | $I_{on}/I_{off}$ | SS (V/dec) | Ref. | Year |
|---|---|---|---|---|---|---|---|---|
| NiO | TG(/) | NiO/EDL | / | $1.6\times10^{-4}$ | 130 | / | [81] | 2008 |
| NiO | S-BG(TO) | $Si/SiO_2$ | −11.4 | 5.2 | $2.2\times10^3$ | 3.91 | [82] | 2013 |
| $NiO_x$ | S-BG(SC) | $Si/SiO_2$ | / | 0.14 | / | / | [83] | 2014 |
| NiO | C-BG(RFMS) | $Glass/Al_2O_3$ | −8.6 | 0.05 | $10^3$ | 2.6 | [84] | 2015 |
| Sn:$NiO_x$ | C-BG(SC) | $Glass/AlO_x$ | −1.44 | 0.97 | $10^6$ | 0.24 | [85] | 2016 |
| Cu:$NiO_x$ | S-BG(SCS) | $Glass/ZrO_2$ | 0.45 | 1.53 | $3\times10^4$ | 0.13 | [86] | 2017 |
| $NiO_x$ | S-BG(IJP) | $Si/Al_2O_3$ | −0.6 | 0.78 | $5.3\times10^4$ | 1.37 | [87] | 2018 |

that the performances of the p-type NiO TFTs were subsequently improved through doping technique. In 2016, Lin *et al.* reported a p-type solution-processed $NiO_x$ TFT with a significant performance enhancement by introducing Sn dopant [85]. The fabricated p-type Sn-doped $NiO_x$ TFT exhibited an $I_{on}/I_{off}$ of ~$10^6$ and a $\mu_{FE}$ of 0.97 $cm^2\ V^{-1}\ s^{-1}$. With Sn doping, Sn atoms tended to substitute Ni sites and induce more amorphous phase. The improvements in TFT performances could be attributed to the decrease in density of states in the gap of $NiO_x$ by Sn doping and the shift of Fermi level into the midgap. Soon afterwards, in 2017, Liu *et al.* demonstrated a p-type TFT based on Cu-doped NiO thin films [86]. The films were fabricated by using solution combustion synthesis (SCS) at a temperature lower than 150°C. The optimized p-type Cu-doped NiO TFT exhibited outstanding electrical performances, including a $\mu_{FE}$ of 1.53 $cm^2\ V^{-1}\ s^{-1}$, an $I_{on}/I_{off}$ of $3\times10^4$ and a SS of 130 mV/decade. The enhanced p-type conductivity could be due to the light Cu doping that substituted the Ni site and dispersed the valence band of the NiO matrix. In 2018, a p-type NiOx TFT with 50-nm-thick $Al_2O_3$ as the gate dielectric was demonstrated by inkjet printing (IJP) technique [87], achieving a hole mobility of 0.78 $cm^2\ V^{-1}\ s^{-1}$, a $V_{th}$ of −0.6 V, a SS of 1.37 V/decade and an $I_{on}/I_{off}$ of $5.3\times10^4$.

Details of the described studies on p-type nickel oxide TFTs were summarized in Table 3.

# 4 Miscellaneous applications of p-type oxide TFTs

## 4.1 Displays

The most significant application of oxide TFTs is on displays, including liquid crystal displays (LCDs) and organic light-emitting diodes (OLEDs). Both LCDs and OLEDs require a backplane drive to control light to form patterns in a controlled manner [88]. The driving mode can be divided into passive-matrix (PM) driving and active-matrix (AM) driving. Active-matrix driven display is the main driving technology for high-performance display at present, which uses TFT devices as the pixel switches. Currently, many companies and teams are working on oxide TFTs for demonstrating flexible and transparent displays. However, the driven oxide TFTs are almost n-type, since the high-performance n-type oxide TFTs have been achieved. Developing high-performance p-type oxide TFTs comparable with n-type oxide TFTs will definitely promote a new era for flat-panel display, because p-type oxide TFTs have the advantage over n-type ones, supplying hole current for the anodes of OLEDs without affecting the drain current in saturation mode [62].

## 4.2 Oxide CMOS

CMOS technology has been widely applied to integrated circuits due to its low power consumption, low waste-heat generation, high noise margin, high logic swing output, high circuit-integration density and simple architecture [89]. A basic CMOS inverter requires both n-type and p-type field-effect transistors. In the past few years, oxide-based TFTs have attracted much attention, due to high carrier mobility, high optical transparency, low temperature process and CMOS compatibility, and become potential candidates for the new-generation high-performance transparent and flexible electronics applications. Although n-type oxide-based TFTs, such as indium-gallium-zinc-oxide (IGZO) TFTs, have been widely researched and even some of them have been commercialized, p-type oxide-based TFTs are still far behind. Therefore, due to the lack of high-performance p-type oxide TFTs, most reported oxide logic inverters were based on pure n-type or p-type oxide TFT technology or hybrid tech-

nology with the incorporation of p-type organic TFT [90–92]. Recently, with the development of p-type oxide TFTs, a few fully oxide CMOS inverters, based on n-type oxides such as $In_2O_3$ [93], $SnO_x$ [64, 94], ZnO [95, 96], IGZO [97–103], and p-type $CuO_x$ [97], SnO [95, 96, 98–104], have been demonstrated. Among these p-type oxides, SnO has been considered as the most promising p-type oxide due to its high stability in air, good uniformity for large-scale fabrication and high $\mu_{FE}$ in comparison to $CuO_x$. Besides inverters, various oxide-based CMOS circuits, including NAND, NOR, XOR and transmission gates and ring oscillators, have been also reported.

In 2008, Dhananjay *et al.* reported the first fully oxide-based CMOS inverters by combining a p-type $SnO_2$ TFT and an n-type $In_2O_3$ TFT with the channels formed by reactive evaporation (EVA) process [93]. This inverter operated fairly at high operating voltages and exhibited an output gain of ~11.

In 2010, Yabuta *et al.* reported the sputtering formation of both p-type SnO and n-type $SnO_2$ TFTs on the same substrate by employing $SiO_x$ capping layers and post thermal annealing to control the oxidation [63]. The oxidation of SnO film decreased the hole density and thus produced n-type $SnO_2$, while the capping layer suppressed oxygen penetration during the annealing and thus protected p-type SnO. A conceptual design of a CMOS inverter based on this simple method for selective formation of p-type and n-type TFTs by a single annealing step was presented, as shown in Figure 15. The similar conceptual design of $SnO_x$-based CMOS inverter using simple one-mask channel pattern process was also proposed by Chen *et al.* in 2017 [73]. With the one-mask channel pattern process, the uncovered p-type SnO film could be converted to n-type $SnO_2$ by oxygen plasma treatment, achieving an inverter consisting of both p-type SnO and n-type $SnO_2$ TFTs on the same substrate.

In 2011, the first ambipolar oxide TFT using a SnO channel was proposed and an oxide CMOS inverter configured by two amipolar SnO TFTs were demonstrated by Nomura *et al.* [64]. The p-type and n-type SnO TFTs exhibited the mobilties of 0.8 and $5\times10^{-4}$ $cm^2$ $V^{-1}$ $s^{-1}$, respectively, and the inverter showed a maximum output gain of 2.5. It was the first demonstration of a CMOS circuit using a single oxide semiconductor channel, providing an important step toward practical oxide electronics.

Similarly, in 2014, Nayak *et al.* reported an oxide CMOS inverter using a single-step deposition of the SnO channel layer [94]. The p-type SnO and n-type $SnO_2$ films were simultaneously achieved by using ALD-$Al_2O_3$ and solution-derived (SD)-$Al_2O_3$ as the dielectrics. The formation of $SnO_2$ could be due to the large number of hydroxyl groups in the SD-$Al_2O_3$, which acted as an additional oxygen source. In the following year, Wang *et al.* from the same group reported another approach of converting SnO to $SnO_2$ phase with low-temperature annealing by using a dual active layer of $Cu_2O$/SnO [104]. The use of the $Cu_2O$ capping layer regulated the oxidation of the exposed surface of SnO and controlled oxygen diffusion into the underlying $SnO_x$ film. The CMOS inverter based on this approach achieved a maximum gain of ~4.

Since oxide semiconductors have been regarded as one of the most promising candidates for flexible electronics, a few fully oxide-based CMOS inverters have been successfully demonstrated on flexible substrates. In 2011, Dindar *et al.* reported a vertically stacked inverter comprised of a p-type $CuO_x$ TFT and an n-type IGZO TFT on a flexible polyethersulfone (PES) substrate [97], as shown in Figure 16. This vertical structure yielded a high gain value of 120. In the same year, Martins *et al.* reported a CMOS inverter using paper as both substrate and dielectric [103]. This paper inverter used $SnO_x$ (x<2) and IGZO as p-type and n-type channels, respectively. Although the CMOS device showed a high leakage current, it was not surprising given the advance from a rigid substrate to paper. This oxide-based paper-CMOS creates an opportunity for light weight, low cost and green electronics applications. The details of this paper-CMOS can be found in the paper presented in 2013 [98]. In 2016, Li *et al.* demonstrated another oxide-based CMOS inverter employing p-type SnO and n-type ZnO TFTs on a flexible PI substrate [96], achieving a voltage gain of ~12. These results demonstrated the feasibility of realizing flexible oxide-based CMOS circuits.

Besides CMOS inverters, oxide-based CMOS ring oscillators, as well as various logic gates (NAND, NOR, XOR and transmission gates, etc.) [95, 96, 98–100, 102], have been reported so far. In 2014, Chiu *et al.* demonstrated the first fully oxide-TFT-based CMOS ring oscillators us-

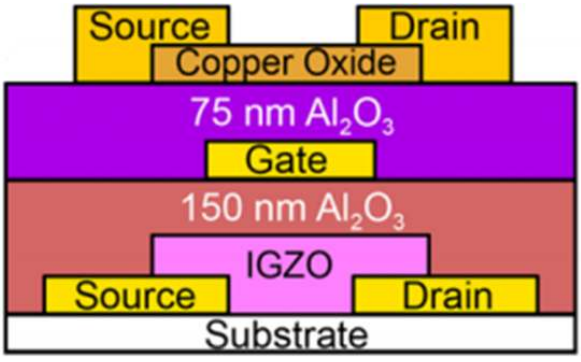


**Figure 16:** Schematic of a vertically stacked p-type $CuO_x$ TFT fabricated on top of an n-type IGZO TFT on a flexible PES substrate [97]

**Table 4:** Short-review of the reported oxide CMOS inverters

| P-type channel | N-type channel | Substrate/Dielectric | Dep. Tech. | $\mu_p$ ($cm^2\ V^{-1}\ s^{-1}$) | $\mu_n$ ($cm^2\ V^{-1}\ s^{-1}$) | Inverter gain | Ref. | Year |
|---|---|---|---|---|---|---|---|---|
| $SnO_2$ | $In_2O_3$ | $Si/SiO_2$ | EVA | 0.0047 | 0.054 | 11 | [93] | 2008 |
| $SnO_x$ | $SnO_x$ | $Si/SiO_2$ | PLD | 0.81 | $5\times10^{-4}$ | 2.5 | [64] | 2011 |
| $CuO_x$ | IGZO | $PES/Al_2O_3$ | RFMS | 0.0022 | 1.58 | 120 | [97] | 2011 |
| $SnO_x$ | IGZO | Paper/Paper | RFMS | 1.3 | 23 | 4.2 | [98] | 2013 |
| $SnO_x$ | $SnO_x$ | $Si/Al_2O_3$ | DCMS | 0.42 | 0.52 | 3 | [94] | 2014 |
| SnO | ZnO | $Glass/HfO_2$ | RFMS | 0.33 | 3.5 | 17 | [95] | 2014 |
| SnO | $Cu_2O/SnO$ | Glass/ATO | DCMS | 2.39 | 0.23 | 4 | [104] | 2015 |
| SnO | ZnO | $PI/HfO_2$ | RFMS | 0.03 | 1.6 | 12 | [96] | 2016 |
| SnO | IGZO | $Si/SiO_2$ | RFMS | 0.51 | 11.9 | 24 | [99] | 2017 |
| SnO | IGZO | $Si/Al_2O_3$ | RFMS | 1.19 | 10.05 | 112 | [100] | 2018 |
| SnO | IGZO | $Si/Al_2O_3$ | RFMS | 0.7 | 8.2 | 142 | [101] | 2018 |
| SnO | IGZO | $Si/Al_2O_3$ | RFMS | 10.2 | 0.87 | 132 | [102] | 2019 |

ing large-area-compatible sputtering process [95]. The five-stage ring oscillator using p-type SnO and n-type ZnO TFTs exhibited an oscillation frequency of ~2 kHz at $V_{DD}$ of 14 V. In 2018 and 2019, Li and Yang *et al.* from the same group successively reported oxide CMOS inverters using p-type SnO and n-type IGZO TFTs with extremely high voltage gain [100–102]. A record voltage gain of 142 was achieved [101], which was very crucial for integrated circuits. Based on the oxide inverters, various oxide CMOS circuits, including NAND, NOR, XOR and transmission gates and ring oscillators were demonstrated and analyzed. These results indicate that fully oxide-based CMOS technology has great potential in future applications of large-scale flexible and transparent integrated circuits.

Table 4 summarized the performances of the reported oxide CMOS inverters.

### 4.3 Sensing

With the development of TFT technology, oxide-based TFTs, whether n-type or p-type, have found their usage in numerous new emerging applications, such as X-ray detection [105, 106], blue-light radiation hazard detection [70], memory devices [107], chemical sensing [108, 109], biochemical sensing [110] and biological sensing [111]. For most of sensing applications, the TFT array substrate is integrated with a sensor layer, which produces an electrical signal correspondingly and in turn transmits to TFTs. So far, many studies of TFT-based sensors have been performed in the field of physical, chemical and biochemical sensing. For example, flat-panel X-ray detectors for medical diagnoses [105], resistive pressure sensors for TFT touch screens [112], uncooled infrared sensors for infrared radiation sensing [113, 114], gas sensors related to the environment [108, 115–117] have been developed and realized. Recently, the possibility of TFT array substrates as new tools for electrical experiments on biological cells has been investigated [111, 118]. Although most TFT biosensors are based on organic TFT technology, the TFTs using oxide semiconductors with high mobility for biological applications are also under investigation.

## 5 Current issues and challenges of p-type oxide TFTs

In the past decades, enormous progress has been achieved in the research field of p-type oxide-based TFTs. However, there are still some issues and challenges as follows:

(i) The process temperature is an important factor for the mass-production of TFTs, especially for those on flexible plastic substrates. Although several low-temperature approaches have been successfully employed to fabricate n-type oxide films, they remain difficult to be applied in p-type oxides.

(ii) In order to realize novel large-area and cost-effective applications, such as foldable and printable displays, disposable smart labels and smart packaging, vacuum processing technology needs to be replaced by continuous processes with higher throughput.

(iii) Even though significant progress has been made, the p-type TFT devices can still hardly yield performance levels similar to their n-type counterparts,

which have entered volume production in the display market. In terms of future research directions, several key areas need to be addressed, including high off-state current, high interfacial defect/states and low mobility.

(iv) Although some computer-based material design simulations have been performed and reported [119–124], more computational studies should be carried out to find potential p-type oxide materials with intrinsically higher hole mobility and the ease of p-type doping. In addition, by combining TCAD models with experimental data of the TFT devices [75, 125–129], we can better understand the mechanisms of electrical performance improvement in TFT devices, such as defects, doping and band dispersion. The computer simulations can also make the design process more efficiently and economically.

# 6 Conclusions

To summarize, the last decade has witnessed enormous progress in p-type oxide-based semiconductors and related opto/electronic devices. In this review, we have illustrated and discussed the material performances of Cu-based oxides, Sn-based oxides and Ni-based oxides for p-type TFT applications. These oxide TFTs, in principle, have significant potential in many applications that were discussed, including low-power electronics, transparent/flexible electronics, high-performance display applications, etc.

Concerning the work developed so far, in the three promising candidates for p-type oxide TFTs, the copper oxide and tin oxide based semiconductors show moderate mobility values, clearly suggesting that there is further room to optimize their $\mu_{FE}$. This means that better materials design strategies and deposition processes are needed to improve the performances of these two p-type oxide semiconductors. In contrast, the $\mu_{FE}$ of most nickel oxide based TFTs is lower than expected due to the special electronic structure. However, it has been proposed that the hole transport limitation can be effectively improved by intentionally doping extrinsic atoms. So far, for the p-type $Cu_2O$ TFTs, the best results obtained are with the $\mu_{FE}$ of 5.6 $cm^2\ V^{-1}\ s^{-1}$ and $I_{on}/I_{off}$ of the order of $10^6$, and for the p-type SnO TFTs with the $\mu_{FE}$ of 10.7 $cm^2\ V^{-1}\ s^{-1}$ and $I_{on}/I_{off}$ of the order of $10^7$.

Although the performance of SnO and CuO based TFTs is very promising among the p-type oxide TFTs, there are still some important issues needed to be solved for further performance improvement. Firstly, higher mobility can be achieved by optimizing the semiconductor/dielectric interface to reduce the density of defective traps. Secondly, more appropriate and better processing techniques for different high-quality layers can be adopted to control the material growth process accurately. Last but not least, the investigation of bipolar semiconductors should be given more research attention. It is of great significance to realize compact CMOS devices and power-efficient transparent circuits through a simple fabrication process.

Even though there is still much work to be done, the speed of developments in this field has undergone in the last years, which indicates that p-type oxide-based TFT technology will play a key role in future's electronic scenario. It would usher in an era of transparent electronics that could affect many facets of our daily lives, probably faster than you can imagine.

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