Progress in the development and understanding of advanced low k and ultralow k dielectrics for very large-scale integrated interconnects—State of the art

Cite as: Appl. Phys. Rev. **1**, 011306 (2014); https://doi.org/10.1063/1.4861876
Submitted: 11 October 2013 • Accepted: 13 November 2013 • Published Online: 15 January 2014

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APPLIED PHYSICS REVIEWS

Progress in the development and understanding of advanced low k and ultralow k dielectrics for very large-scale integrated interconnects—State of the art

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(Received 11 October 2013; accepted 13 November 2013; published online 15 January 2014)

The improved performance of the semiconductor microprocessors was achieved for several decades by continuous scaling of the device dimensions while using the same materials for all device generations. At the 0.25 μm technology node, the interconnect of the integrated circuit (IC) became the bottleneck to the improvement of IC performance. One solution was introduction of new materials to reduce the interconnect resistance-capacitance. After the replacement of Al with Cu in 1997, the inter- and intralevel dielectric insulator of the interconnect (ILD), SiO_2, was replaced about 7 years later with the low dielectric constant (low-k) SiCOH at the 90 nm node. The subsequent scaling of the devices required the development of ultralow-k porous pSiCOH to maintain the capacitance of the interconnect as low as possible. The composition and porosity of pSiCOH dielectrics affected, among others, the resistance of the dielectrics to damage during integration processing and reduced their mechanical strength, thereby affecting the reliability of the VLSI microprocessor. New ILDs had to be developed to overcome such problems and enable the fabrication of reliable high performance devices. The capacitance of the interconnect is also affected by the dielectric caps separating the Cu conductor from the ILD. This effect has increasing impact as interconnect dimensions shrink further with each technology node. New caps with lower k values and smaller thickness have been developed to reduce the impact of the caps to the capacitance of the interconnect and enable fabrication of devices of high reliability. This paper reviews the development of advanced ultralow-k (ULK) ILD dielectrics and caps with reduced capacitance contributions and presents the state of the art of these interconnect dielectrics. [http://dx.doi.org/10.1063/1.4861876]

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I. INTRODUCTION—HISTORICAL BACKGROUND

Five decades ago, the semiconductor industry started to integrate various electronic components onto the same Si

chip creating the integrated circuits (ICs) and using the same materials in its structures for many generations. Today, the industry is integrating also various materials in the same chip, after extensive and prolonged development efforts to accomplish successful integration of the required new materials. Among these new materials are the dielectric insulators of the interconnects of VLSI chips.

For several decades, the performance of the VLSI integrated circuits was progressing following Moore's law,[1] by shrinking the dimensions of the individual devices and packing more devices in the same area. The decreasing dimensions of the devices made them faster with each new technology generation.

Figure 1 shows a diagram of a cross-section of a VLSI circuit and illustrates the fact that most of the cross-section's real estate is occupied by the interconnect (or back end of the line, BEOL) structures. These structures connect between individual active devices and between the devices and the outside of the VLSI chip. The RC (R = resistance; C = capacitance) of the interconnect controls the signal delay between the active devices and between the devices and the external world and affects the cross-talk between devices. Until the 0.25 μm generation, the interconnect was composed of the elements Si, O, Al, and N. At this technology node, the RC of the BEOL became a bottleneck to the improvement of the performance of the VLSI devices.

The BEOL consists of multiple hierarchical metallization levels consisting of conductors separated by dielectric insulators and the RC of a metallization level in the interconnect can be defined by[2]

$$RC = 2\rho k\left(4L^2/P^2 + L^2/T^2\right),$$

where

L = line length, P = metal pitch, T = thickness of metal line, ρ = metal resistivity, and k = dielectric constant.

The shrunken dimensions of the devices noted above resulted in the increase of both R and C to the extent that, while the active devices became faster, the RC of the BEOL slowed down the performance of the chip. With device scaling, the need for reducing BEOL RC delay became increasingly important.[3,4] New materials had to be introduced in the interconnect of the VLSI chip to reduce its RC and in 1997 IBM[5] and then Motorola[6] replaced the Al with Cu as the conductor material of the interconnect. Cu, having a 40% lower resistivity than Al, enabled the scaling of thin wire levels, thereby reducing their capacitance and the interconnect's RC delay.[7] The next "new" material to be successfully integrated in a microprocessor was fluorinated silicon glass (FSG or SiOF), introduced in 2000 as the intra- and inter-level (ILD) dielectric at the 0.18 μm technology node.[8,9] The fluorination of the silicon dioxide reduced its dielectric constant from 4.1 to 3.6, thereby reducing the capacitance of the interconnect.

Further reduction of the dielectric constant of the interconnect dielectrics became problematic. Over the years, the academia and industry have invested many efforts in developing and trying to integrate a large number ($\sim$150) of organic or hybrid dielectrics with lower dielectric constants than that of FSG;[10] however, all failed the integration in VLSI chips. These failures were, among other factors, a result of the lower mechanical strength and reduced chemical robustness of the new dielectrics as compared to SiO_2. The developers of the ITRS roadmap ignored initially the diminished properties of the new dielectric materials. The targets set for dielectric constants were unrealistic forcing repeated revisions of the ITRS roadmap since 1997, as illustrated in Figure 2.

The first successful non-SiOx low-dielectric constant material was the organosilicate glass, SiCOH, deposited by plasma enhanced chemical vapor deposition (PECVD).[11] SiCOH with a dielectric constant k = 3.0 was successfully integrated in some 130 nm and 90 nm products starting in 2001[12–14] and then in almost all the 90 nm products since 2004.[15–17]

Continuous shrinking of the interconnect dimensions with each technology node required further reduction of the dielectric constant in order to prevent or limit an increase in the BEOL capacitance. The reduction of k of SiCOH dielectrics could be achieved only by introducing porosity in the

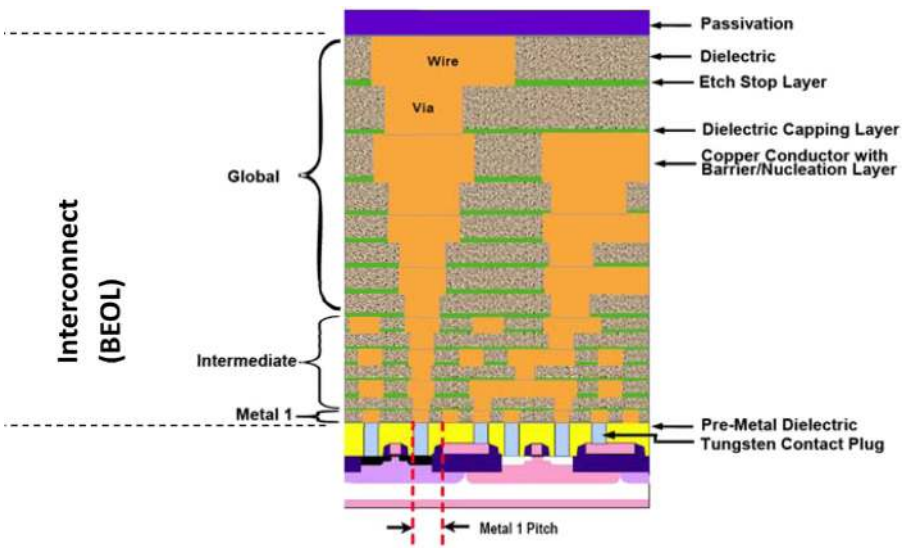

FIG. 1. Diagram of a cross-section of a VLSI circuit. Etch stop layers are not used in double-damascene structures. Reprinted with permission from ITRS 2005, http://www.itrs.net/Links/2005itrs/home2005.htm.[58]

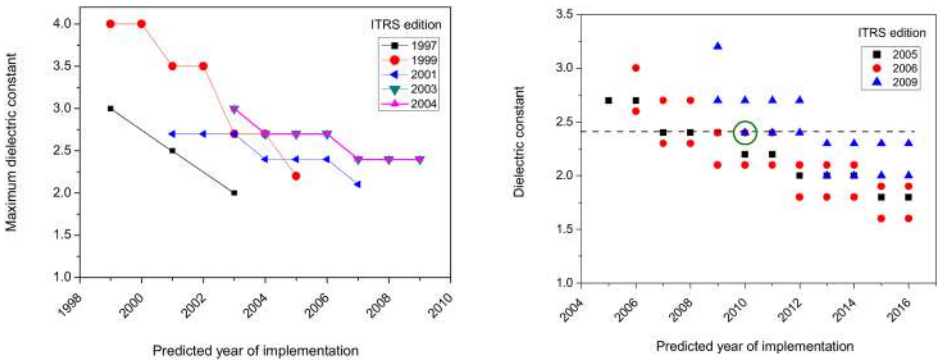

FIG. 2. Changes in ITRS roadmap. The circle in the right plot indicates the implementation by IBM of pSiCOH with k = 2.4 in P7 microprocessor.

films. While the prevailing wisdom by 1998-9 was that "porosity can be created in dielectric films only by polymerization techniques; porous films cannot be fabricated by PECVD," we have demonstrated the fabrication of porous pSiCOH dielectrics by the PECVD technique[18,19] enabling their integration in VLSI chips.[20]

In addition to affecting the speed of the microprocessor through the RC product, the capacitance affects directly the power used by the chip through the relation[2]

$$\text{Power} = CV^2f,$$

where

V = operating voltage, f = operating frequency.

As one of today's major goals of the semiconductor technology is the increase of the power efficiency, i.e., the reduction of the power consumption of the semiconductor chips, the reduction of the interconnect capacitance is especially important. If dielectrics of same k are used, the power consumption increases with decreasing technology node; therefore, the integration of dielectrics with lower and lower k values would be of great benefit.

The Cu present in VLSI interconnect structures has low electrical resistivity and high resistance to electromigration. But, a robust dielectric barrier film is required in high performance CMOS ICs to prevent inter and intra level Cu diffusion. As illustrated in Fig. 1 and shown in Fig. 3, the dielectric caps are an integral component of BEOL and are contributing to the capacitance of the interconnect. To reduce the contribution of the caps, the historical SiN cap ($k \sim 7$) was replaced at the 90 nm node with SiCH and SiCNH ($k \leq 5.3$) caps.[21] The contribution of the caps to the total capacitance was relatively small at this and a few subsequent technology nodes; however, their contribution to the capacitance increased at the 22 nm node and beyond because the caps do not scale with the ILD dielectrics. While the thickness of the ILD decreases with each new node, we shall see later that the thickness of the caps cannot decrease at the same rate without degradation of the cap properties. Furthermore, with the decrease in the thickness of low k dielectric stack, the impact of dielectric barrier on effective k value has become even more important.[22]

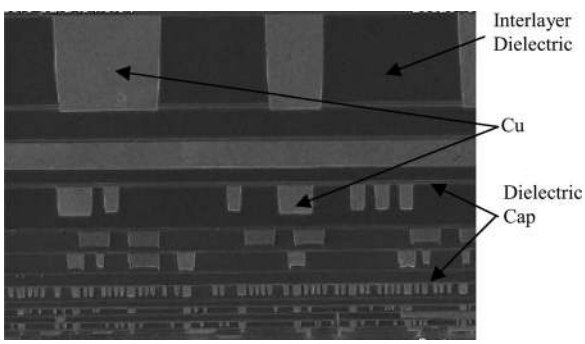

FIG. 3. Cross-section of an IBM 32 nm Cu low k interconnect showing the dielectric caps deposited on top of copper.

A review of the development and properties of SiCOH and the initial development of porous pSiCOH dielectrics can be found elsewhere[2] and of the early development and characterization of pSiCOH in Ref. 23. Since the publications of these papers, the BEOL ILD and cap dielectrics have continued to be developed to further improve their properties for successful integration with improved reliability in the VLSI microprocessors. The present paper reviews the latest developments of the PECVD ILD and cap dielectrics and discusses the state of the art of these materials and their implementation in VLSI microprocessors.

II. EXPERIMENTAL

The films discussed in this paper were deposited on 300 mm Si (100) wafers in commercial, parallel plate, PECVD deposition systems. The tool used for the deposition of the ILD films contained a second chamber for UV curing the porous pSiCOH films. The UV curing was performed with wideband UV lamps (for details, see Ref. 23). The pSiCOH films have been deposited either from a mixture of a SiCOH skeleton precursor with an organic porogen precursor or using single precursor molecules of skeleton with embedded porogen.[24] For the deposition of some of the discussed films, a second skeleton precursor was added to either of the two options above. The specific fabrication details of the different films will be discussed later in the corresponding sections.

Prior to the deposition of the caps, chemical mechanical polishing (CMP) of Cu is performed to planarize the electroplated metal. Since CMP and cap deposition are performed in different tools, a surface clean (pre-clean) is performed before the deposition of the cap to remove any copper oxide. For the fabrication of the caps discussed in this review, a NH_3 plasma pre-clean was performed *in-situ* in the same chamber used for the deposition of the caps.

The structure, composition, and elastic modulus of the dielectrics were determined by Fourier Transform Infrared (FTIR) spectroscopy, X-ray photoelectron spectroscopy (XPS) with depth profiling, and nanoindentation (NI), correspondingly. The elastic modulus was calculated taking into consideration the contribution of the substrate to the nanoindentation measurements, and as an additional precaution, NI was performed on films of identical thickness of 400 nm. The degree of porosity of the films and their pore size was generally determined using ellipsometric porosimetry (EP).[25] In some cases, positron annihilation spectroscopy (PAS) was used to determine interconnectivity of the pores.[25]

The dielectric constant, leakage properties, and breakdown voltage of the dielectrics were measured on blanket films using metal-insulator-semiconductor (MIS) structures built with Al dots on top of the dielectric films and Al metallization of the back of the Si wafers.

Plasma damage to ULK films was measured using the dT method, which has been described previously.[26] Briefly, we expose a blanket ULK film to a reference plasma and measure the thickness after the plasma exposure. The plasma removes carbon from the ULK to some depth into the film, forming a damaged layer. Next, we selectively etch off the damaged layer using diluted HF ($HF:H_2O = 1:300$), which gives an equivalent SiO_2 removal of 7 A/min; measure again the thickness. The diluted HF rapidly removes the carbon-lean damaged layer but has a slow etch rate in the undamaged portion of the film. Thus, the thickness change (delta thickness, dT) is a measure of the thickness of the damaged layer.

To compare different ULK films, we calculate a degree of damage for each sample film. The degree of damage is the ratio of dT of the sample film to the dT of a reference film, V1.c (see Table I). The reference film is a highly porous film with $k = 2.2$ prepared with the V1 chemistry and is damaged more than all other ILD dielectrics reported here. The degree of damage for the reference dielectric V1.c is defined as 1, and all other dielectrics have a lower degree of damage.

The performance of the caps as oxidation barriers was evaluated on blanket structures of Cu covered with the desired thickness of cap. The oxidation barrier test was performed by exposing the structure to a temperature of 310 °C for 24 h in air with ~70% relative humidity. These conditions are more drastic that the actual conditions to which these films will be exposed. However, testing under these extreme conditions provides more reliable information about the oxidation barrier properties of the caps.

The UV cure used to remove the porogen incorporated in the pSiCOH films during deposition exposes also the underlying cap to UV radiation, which can modify the properties of the cap. Properties of the dielectric caps were therefore characterized after deposition and some after exposure to UV.

III. ULTRALOW-k POROUS pSiCOH ILD DIELECTRICS

A. pSiCOH ILDs

The reduction of the dielectric constant of the SiCOH films required the introduction of porosity in the low-k SiCOH dielectrics. Porous pSiCOH films can be fabricated either by the *structural* or the *subtractive* method. One approach of the structural method is based on using the same precursor as for the dense SiCOH films ($k = 3.0$) and adjusting the plasma deposition conditions to obtain films with lower k values of $k = 2.7$.[27,28] The lowest k values obtainable by this method are relatively high, $k > 2.55$. The second structural approach is to use a precursor with unsaturated bonds and deposit pSiCOH films by plasma polymerization.[29] Again, the lowest k achieved by the polymerization approach was about 2.55.

The subtractive method for fabricating pSiCOH films is much more flexible and dielectrics with $k < 2.0$ have been achieved using this method.[23,30] In this technique, the films are deposited as a dual phase material, SiCOH-CHx, using a mixture of a SiCOH skeleton precursor with an organic porogen precursor. The skeleton precursor could in principle be one of those shown in Figure 4, while an organic molecule with sufficient volatility could be used as a porogen.

The as-deposited SiCOH-CxHy films have to be cured to remove the labile organic fraction CxHy and form a porous film. The curing can be done thermally[18,19,30] or using electron beam or ultraviolet (UV) irradiation.[23] The thermal cure has to be done for several hours at temperatures limited at about 400 °C and produces films of low mechanical strength. The industry has adopted instead broadband UV curing for the fabrication of pSiCOH dielectrics. The UV curing is done in a few minutes, breaks a fraction of mainly the $Si\text{-}CH_3$ (Si-Me) bonds and rearranges and enhances the

TABLE I. Selected properties of ILD dielectrics.

Dielectric	V1.a	V1.b	V1.c	V2.a	V2.b	V2.c	V3	V4.a	V4.b
Precursor	DEMS + BCHD			DEMS + BCHD + TDDMS			Embedded porogen	Embedded porogen + carbosilane	
k (at 150C)	2.53	2.4	2.2	2.56	2.35	2.2	2.46	2.53	2.42
Breakdown voltage (MV/cm)	>7.3	>6.0		>6.5	>6.0		>7	7	
E (GPa)	7.2	4.9	4.7	6.5	4.73	3.04	6.64	10.2	6.64
Adhesion (J/cm^2)	4.5	4.4					3.9	4.4	3.9
C%	15.7	15.5		20.6	23.2	35.0	21.1	16.3	17.4
Porosity (%)	16.3	24.5	29	19	22	26.5	14.4	17.9	19.7
Pore diameter (nm)	1.2	1.2	2.4	1.2	1.2	1.32	1	1.1	1.3
PID (ratio to control)[a]	0.67	0.9	1	0.57	0.55	~0.5	0.57	0.49	0.65

[a]Control = V1.c.

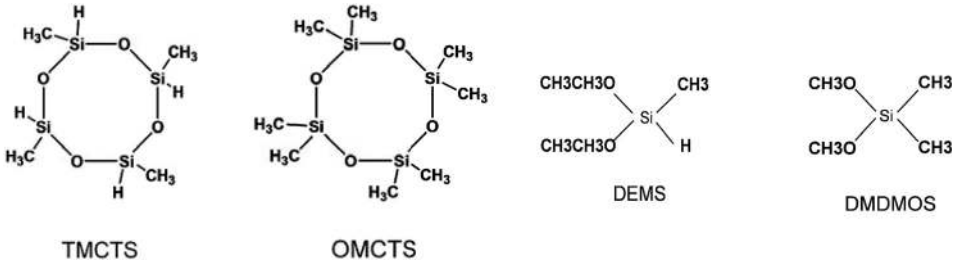

FIG. 4. SiCOH skeleton (matrix, backbone) precursors.

cross-linking of the skeleton, resulting in films with improved mechanical strength (bigger elastic modulus and hardness). The value of the modulus increases with longer UV cure; however, over-cure can cause loss of too many Si-Me bonds and pore collapse, resulting in films of higher k values.

An alternative to the use of a mixture of skeleton with porogen precursor for the fabrication of porous films by the subtractive method is the deposition of the SiCOH-CxHy using a single precursor molecule consisting of skeleton with embedded (or grafted) porogen precursor.[24] An example of such a pSiCOH is Applied Materials' Black Diamond 3 (BD3) dielectric.[31] After deposition, the films are cured by UV to create porosity and improve their mechanical properties.

The semiconductor industry has adopted the subtractive method for fabrication of pSiCOH dielectrics implemented in VLSI devices.

1. pSiCOH version V1

We will discuss next the first generation of pSiCOH films deposited by the subtractive method using mixtures of skeleton and porogen precursors. When depositing such films, the plasma power has to be adjusted to be sufficiently high to dissociate the porogen precursor and incorporate labile CxHy fragments in the deposited film but should not be too high to over-dissociate the skeleton precursor causing the formation of an oxide type skeleton. Preferred skeleton precursors are siloxanes containing alkyl Si-methyl (Si-CH_3 or Si-Me) or Si-ethyl (Si-Et) bonds together with alkoxy SiO-Me or SiO-Et bonds. It was established empirically that the difficulty of dissociation in the plasma of the different bonds of such precursors is SiO-Me or SiO-Et < Si-H < Si-Me < SiO. As a result, it was found that it is difficult to incorporate porogen fractions in films deposited with the cyclic skeleton (matrix) precursors, tetramethylcyclotetrasiloxane (TMCTS) octamethylcyclotetrasiloxane (OMCTS) in Fig.4, used for the fabrication of the dense SiCOH films, and large porogen to skeleton flow ratios had to be used to fabricate such pSiCOH films.[30] Much lower flow ratios have to be used with the non-cyclic skeleton precursors,[23] and the branched diethoxymethylsilane (DEMS) (Fig. 4) has been adopted by most of the industry as the skeleton precursor.

It has also been established empirically that an efficient incorporation of the CxHy porogen fractions in the deposited films requires the use of porogen molecules with at least two reactive bonds, such as double C=C bonds or strained bonds. While many such precursors have been investigated,[23] the industry has adopted bicycloheptadiene (BCHD) or α-terpinene (ATRP) (Figure 5) as the porogens used with DEMS. The pSiCOH V1 dielectrics discussed next were prepared from mixtures of DEMS with BCHD.

The V1 films were initially developed with a dielectric constant k = 2.4 (V1.b in Table I) for integration in the BEOL of the 45 nm technology node.[20,32] V1.c films with k = 2.2 have also been developed but have been found difficult to integrate in the BEOL structure. The decreasing dimensions at the 32/28 nm node required the further optimization of the ILD dielectric and the development of a pSiCOH V1.a with k = 2.55[33] to maintain the reliability of the BEOL. Some properties of the V1 films are shown in Table I.

The different versions of the V1 dielectrics have similar bonding structures which have been studied using FTIR analysis. Figure 6 shows a FTIR spectrum of pSiCOH V1 with k = 2.55. The spectrum is similar for V1 films with k = 2.4. The spectrum is characterized by several typical absorption bands. The strong SiO band at 1250-950 cm^{-1} can be deconvoluted into 3 peaks corresponding to absorption from the different oxide structures composing the skeleton, i.e., SiO network, SiO cage, and suboxide.[34] The peak at 1274 cm^{-1} and the absorption band at 950–650 cm^{-1} correspond to absorptions from Si-Me, and Si-Me_n (n = 1–3) and H-SiO, respectively. The spectrum in Fig. 6 contains additional small peaks at 2972 cm^{-1} and 2916 cm^{-1}, corresponding to sp^3 C-H_3 and sp^3 C-H_2 stretching oscillations, and at 2239 cm^{-1} and 2178 cm^{-1}, corresponding to Si-H stretching absorptions in H-SiO_3 and H-SiO_2Si.[34]

Figure 6 also shows the spectrum of a V3 film deposited from a single precursor with embedded porogen, and it can be seen that this film is characterized by similar FTIR absorption bands as that of the V1.a film, thereby indicating that the two types of dielectrics have essentially similar bonding structures. This similarity can also be seen in Table II which summarizes the ratios of the intensities of the different absorption peaks to that of the SiO peak. V1.a and V3 films have similar ratios indicating that they have very similar boding structures. According to the discussed above,

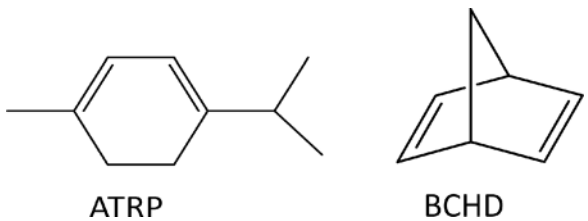

FIG. 5. Porogen precursors.

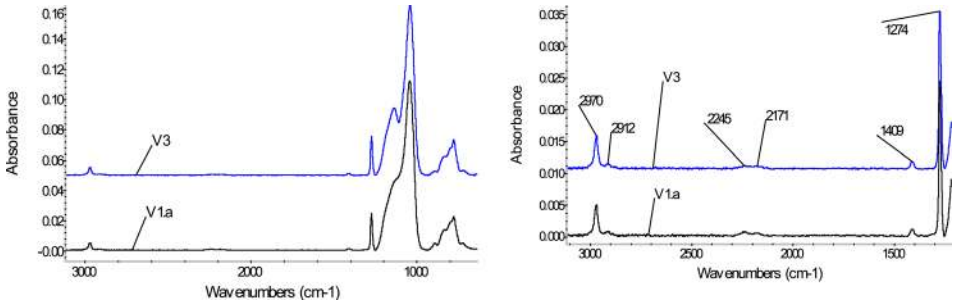

FIG. 6. FTIR of V1.a and V3 type pSiCOH. Right plot shows expanded section of left plot.

the structures of both pSiCOH V1.a and V3 are comprised of a 3-dimensional skeleton of randomly oriented SiO bonds to which are connected terminal bonds of Si-Me groups and Si-H bonds. These bonds terminate into the pores of pSiCOH and reduce the average coordination number of O to Si, thereby reducing the mechanical strength of the materials.

2. Integration challenges

The basic properties of the pSiCOH V1.b dielectrics with k = 2.4 are summarized in Table I. These properties made the material a candidate BEOL insulator at the 45 nm node. However for successful integration of the dielectric in a VLSI device, the material had to satisfy additional critical requirements, among them:

1. High interfacial strength (adhesion) to dielectric caps. Strong adhesion between different layers is required for enabling the integration of the interconnect structure and maintaining the reliability of the VLSI chip in packaging.
2. Resistance to processing-induced damage during integration. Processing-induced damage includes damage to the ULK caused by CMP, Physical Vapor Deposition (PVD) metal deposition, but especially problematic is plasma-induced damage (PID) during dielectric etching and photoresist removal by ashing. PID can cause excessive damage to the ILD dielectric leading to increased capacitance, while removal of the damaged dielectric layer from the sidewalls of the etched pattern by wet etching can lead to re-entrant feature profiles and metal fill problems. Good resistance to PID is required in order to enable control of critical dimensions (CDs) and to preserve the value of k.
3. Sufficiently high mechanical properties, i.e., high elastic modulus, especially for chip packaging (or chip-package-interaction, CPI), and high hardness for CMP. The weakened mechanical properties of SiCOH, caused by the reduction of the coordination number due to the replacement of some O with C, are further exacerbated by the porosity of the pSiCOH films.
4. Minimal pore size with minimal interconnectivity to prevent penetration of liners or Cu and humidity in the dielectrics and maintain the values of k and reliability of the chip.
5. Hydrophobicity to maintain k values. Ingress of humidity in the dielectric will increase its dielectric constant.

TABLE II. Comparison of relative intensities of FTIR peaks of several pSiCOH dielectrics with k = 2.55.

	Ratio to SiO peak (%)			
Dielectric	CH	SiH	Si-CH_2-Si	SiMe
V1.a	0.013	0.0054	0.0000	0.029
V3	0.015	0.0049	0.0000	0.032
V2.a	0.023	0.0060	0.0007	0.036
V4.a	0.013	0.0085	0.0011	0.026

Additional details regarding critical integration related characteristics can be found in Ref. 2.

The introduction of porosity in SiCOH and replacement of some Si-O bonds with Si-Me bonds degraded the properties of the dielectric, and the integration processes had to be adapted to enable the reliable integration of the V1 pSiCOH dielectrics in a VLSI device. As we shall see later, improvement of the characteristics listed above, especially item 2 could be achieved by developing new versions of ULK pSiCOH dielectrics, replacing some Si-O-Si skeleton bonds with carbosilane bonds (Si-CH_2-Si). Next, we will address topic 1 of the above list of requirements, while topic 2 will be discussed in detail in Sec. III B.

3. Interface engineering for improved adhesion

The BEOL (interconnect) structure of a VLSI device is composed of many layers of various conducting and insulating materials, and the integrity of the final product depends on strong adhesion between the different layers in contact. During the integration of the original dense SiCOH in a BEOL structure, it was discovered that the interface strength between the SiCOH ILD layer and the underlying dielectric cap was weak. The BEOL structure of the microprocessor chip could be fabricated without delamination; however, delaminations occurred between the ILD and cap layers during packaging.[35]

Different treatments were tried to modify the surface of the cap to enhance the adhesion of the SiCOH deposited on top of it. However, only some of these treatments, especially those which oxidized the cap surface, improved partially, yet insufficiently the interfacial strength of the ILD to the cap. The analysis of the delaminations revealed that they occurred in the initial layer of the deposited SiCOH ILD. This initial layer was characterized by a low cohesive strength caused by a spike (higher concentration) of carbon at the start of the deposition of the SiCOH. As explained elsewhere,[35] the carbon spike was caused by the complex chemistry used with the typical deposition process, wherein the plasma is

activated after the precursor gases are equilibrated in the PECVD reactor, and by the fact that the RF power that sustains the plasma, activated after the equilibration of the gases reaches its value gradually (though in a very short time).

Based on this understanding, the interface strength between the SiCOH ILD and the cap was enhanced by developing a process where the precursors for the fabrication of the ILD were introduced gradually into the PECVD reactor while an oxygen containing plasma was already active in the chamber.[35] The oxygen flow was then reduced and the precursor flow adjusted to the deposition of the bulk of the ILD. This process created an initial oxide layer in contact with the dielectric cap, followed by a smooth graded layer where the C concentration increased from almost 0% to its concentration in the bulk ILD. Such an improved structure, whose composition profile is illustrated in Figure 7, provided strong interface strength between the cap and the ILD, achieving interface strength close to the cohesive strength of the bulk[35] and enabled the successful integration of the low-k SiCOH and ultralow-k pSiCOH in reliable semiconductor devices.

The fabrication of the transition layer is a relatively simple process for SiCOH, but it becomes more complex for pSiCOH which is fabricated from a mixture of skeleton precursor with porogen precursor. Details of the later process can be found elsewhere.[36] Typical interface strengths obtained for different dielectrics are shown as the *Adhesion* in Table I.

B. Development of advanced pSiCOH with improved properties

1. PID

The Sec. III A 3 has shown how the first item of the integration issues (see Sec. III A 2) has been solved. In this section, we will address the second item of the integration challenges, PID. PID has become a major obstacle in the scaling of the dielectric constant below k = 2.55. The V1.b pSiCOH with k = 2.45 was used in production at the 45 nm technology node. However, this film could not be used at the smaller dimensions of the 32 nm node because the PID layer created by integration processing became a larger fraction of the dielectric between the lines. The PID layer is depleted of carbon, is hydrophilic and absorbs water, and is typically denser than the pristine ULK film. All these factors contribute to an increased line to line capacitance (increased k_{eff}) and can eliminate the advantage of using an ILD with an ultralow k. The effect of PID on the value of k_{eff} increases with decreasing interline spacing.

The increased capacitance resulting from PID was such that the k_{eff} obtained with V1.b film had no benefit over a k = 2.7 film. This motivated an effort to develop pSiCOH materials that were more resistant to PID and thus more compatible with damaging integration steps. As described below, PID resistance was improved by fabrication of dielectrics with a combination of optimized porosity, raised carbon content, and a carbon structure that has better resistance to plasma damage.

2. pSiCOH V2 and V4

At the 32 nm node, the V1.b pSiCOH with k = 2.4 was replaced by V.1a pSiCOH dielectrics with k = 2.55 having a lower porosity than V1.b (see Table I), and these type of dielectrics became widely used in the semiconductor industry for several subsequent technology nodes. Efforts to integrate V1 dielectrics of lower k values showed two major issues as porosity increased with reduced k. One of these issues was higher PID associated with relatively high porosity and a Si-methyl content that is too low to protect the skeleton from plasma damage. The second issue was the reduction in mechanical strength as k decreased.

To improve PID and other forms of integration damage, V2 type of dielectrics were fabricated by adding a third precursor, [trimethylsilylmethyl]dimethoxymethylsilane, or TDMMS, to the DEMS and BCHD precursors. Figure 8 shows a schematic structure of TDMMS and of a generic carbosilane precursor. The V2 films contained a higher carbon content and a favorable pore structure compared to V1 films of same k. Both the carbon and pore structure contributed to the much lower degree of damage (PID) for the V2 dielectrics (see Table I), rendering the material more compatible with integration. The V2 pSiCOH dielectrics were described generally in Ref. 37 and a detailed comparison of the pore structure in the V2 and V1 materials in Ref. 38.

Figure 9 shows an FTIR spectrum of a V2.a dielectric. The spectrum has features similar to that of V1.a dielectric (see Figure 6) but with distinct changes. Common to both V1 and V2 dielectrics is the intense band from 1000 cm^{-1} to 1250 cm^{-1} assigned to O-Si-O vibrations, and the narrow

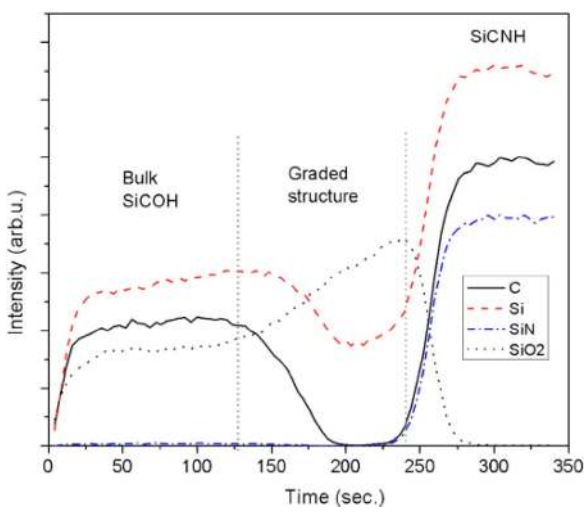

FIG. 7. SIMS profile through a cap/graded layer/SiCOH structure fabricated with an improved transition layer process. Reprinted with permission from J. Appl. Phys. **103**, 054104 (2008). Copyright 2008 AIP Publishing LLC.[35]

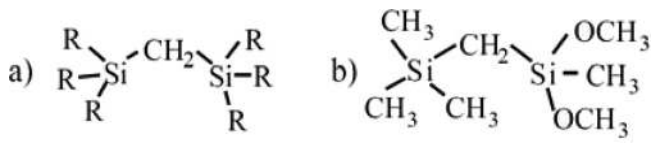

FIG. 8. Schematic structure of (a) a general carbosilane precursor and (b) TDMMS used to prepare V2 type dielectrics. The groups R can be the same or different from each other. TDMMS is [trimethylsilylmethyl] dimethoxymethylsilane.

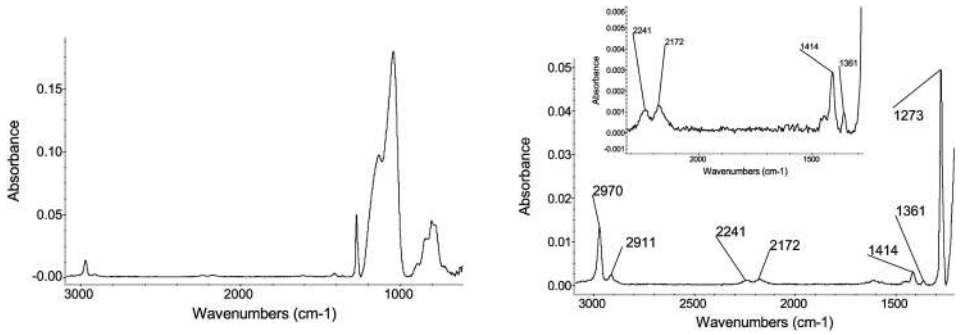

FIG. 9. FTIR of V2 type pSiCOH. The plot at right shows expanded sections of left plot.

Si-CH_3 peak at 1274 cm^{-1}. The ratio of these peaks (Si-CH_3 to O-Si-O) can be used to easily compare the relative carbon content in these materials. As shown in Table II, this ratio is larger for V2.a (Figure 9) than for V1.a (Figure 6), consistent with the higher C content in V2.a measured by XPS (Table I). The expanded scale in the right panel of Figure 9 shows a new peak at the 1360 cm^{-1} associated with Si-CH_2-Si bonds.[38] This absorption peak indicates the existence of a new C structure not found in V1 or V3 films: the "methylene bridge" bonds within the network.

As was shown in detail elsewhere,[38] carbon exists in the V2 dielectrics in 3 structures: Si-CH_3 (Si-Me), Si dimethyl (Si-Me_2), and Si-CH_2-Si. The FTIR peaks of methyl and dimethyl Si are not resolved but overlap. These structures reduce the mechanical strength of the material because the Si atoms in the dimethyl structure have only 2 bond connections to the network. Si atoms with 3 and 4 network bond connections contribute to a high mechanical strength or elastic modulus. The replacement of Si-O-Si bonds with the methylene bridge Si-CH_2-Si maintains a high average Si coordination number and thus can potentially help provide a high mechanical strength of the dielectric. The C in the methylene bridge, illustrated in Figure 8, also improves PID resistance, and therefore, the methylene bridge structures are essential to the fabrication of optimized pSiCOH dielectrics with a balance of desired properties.

A detailed picture of the pore structure in the V1 and V2 pSiCOH was obtained by combining data from three techniques: Positron Annihilation Lifetime Spectroscopy (PALS), EP, and N_2 adsorption porosimetry.[38] The combined analysis showed the presence of small ultramicropores (ULM) (diameter < 0.7 nm) and larger supermicropores (SMP) (diameter > 0.7 nm) in these materials. The pore connectivity measured by PALS for V2 materials was smaller than for the V1 materials. The methyl-rich V2.b ($k = 2.4$) had about half the pore interconnection length of the corresponding V1 pSiCOH.[38] The difference was even more pronounced for films with $k = 2.2$. The trends in PALS connectivity correlated with the fraction of the porosity present as the larger SMP, a greater fraction of SPM leading to higher PALS connectivity.

TABLE III. The porous volume detected by N_2 adsorption and EP and the difference (Delta) between the 2 volumes. Reproduced by permission from Gates *et al.*, J. Electrochem. Soc. **156**, G156 (2009). Copyright 2009 by The Electrochemical Society.[38]

Film	k	V N_2 (cm^3 g^{-1})	V EP (cm^3 g^{-1})	Delta (N_2 − EP) (cm^3 g^{-1})
V1.b	2.4	0.245	0.201	0.044
V2.b	2.4	0.279	0.193	0.086
V1.c	2.2	0.361	0.294	0.067
V2.c	2.2	0.320	0.237	0.083

Using the adsorption of toluene in one measurement (EP) and of N_2 in a second measurement (N_2 adsorption porosimetry), we then calculated the difference, Delta, between the porous volumes from the two measurements, as shown in Table III. Delta reflects the porous volume present as the smallest ultramicropores.[38] Delta can be used as a figure of merit to predict integration compatibility. For the same k values, dielectrics with larger Delta values are expected to have better resistance to PID, as illustrated by the comparison of the data of V2 and V1 dielectrics in Table I and III.

Another major integration issue of the pSiCOH dielectrics that required a solution was the reduced mechanical strength of the V1 materials as porosity increased. This effect is illustrated in Table I by the elastic modulus, E, in V1.a through V1.c. Mechanical strength could be enhanced at a given k by making the skeleton more oxide like, but this would result in an increased PID. We addressed this issue by developing the V4 version of pSiCOH dielectrics. These films were deposited using a mixture of a carbosilane precursor of the type illustrated in Figure 8(a) with an embedded-porogen precursor and were subsequently UV cured to remove the porogen.

The network structure of V4 dielectrics contains the methylene bridge Si-CH_2-Si similar to the V2 materials, as revealed in the FTIR spectra. Figure 10 shows the spectral region 1305 cm^{-1} to 1455 cm^{-1}, for the $k = 2.55$ materials V2.a and V4.a. The absorbance peak at 1360 cm^{-1} is due to

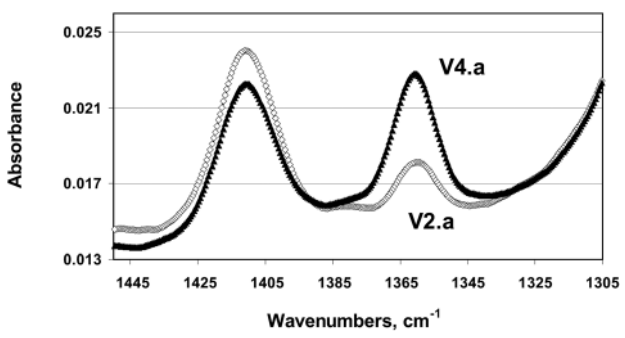

FIG. 10. Expanded FTIR spectrum of V2.a (open symbols) and V4.a (solid triangles), detected using the Brewster angle of incidence.

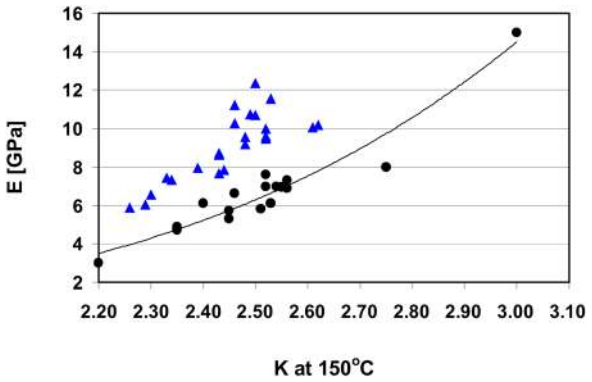

FIG. 11. Plot of Young's Modulus, E, versus k value for V1 (black circles) and for V4 (blue triangles) type dielectrics.

Si-CH_2-Si bonding. This figure shows that a high concentration of the Si-CH_2-Si bonds was incorporated into the V4 dielectrics, the V4.a spectrum showing a 1360 cm^{-1} peak that is 2 to 3 times more intense than that of the V2.a spectrum.

The elastic modulus measured by nanoindentation was used to guide the development of the V4 materials. Figure 11 presents the elastic modulus, E, as a function of k for a variety of dielectrics. Data points shown by circles correspond to V1 type dielectrics. The two data points with k values of 2.75 and 3.0 were measured from V1 materials made with no porogen, using OMCTS. Triangles show the modulus measured for different V4 pSiCOH materials produced using different deposition conditions. Consistently, at all k values, the modulus is higher for V4 compared to the V1 materials. The V4 materials have a network with high average coordination number, in part because of the high concentration of the Si-CH_2-Si bonds noted above.

As seen in Table I, the V4 materials have a high elastic modulus and in the same time a lower PID than the V1 dielectrics at any given k value. At the same time, the V2 films have lower modulus than V1 due to the higher C content in terminal -CH_3 groups. The V4 pSiCOH dielectrics are a significant improvement over the V1 and V2 materials. For example, V4.a with k 2.55 stands out in Table I with a high elastic modulus (about 10 GPa) and simultaneously the lowest PID value of about 0.5 among the k 2.55 materials.

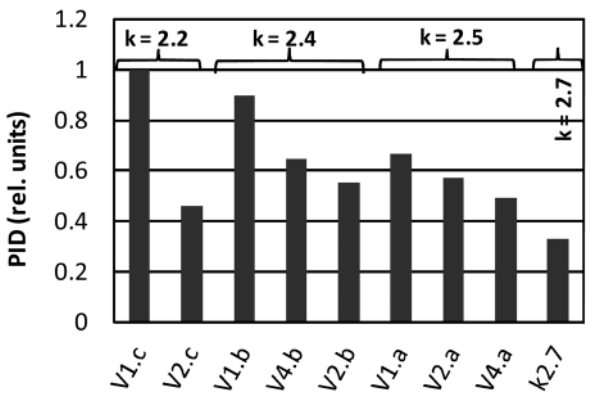

FIG. 12. The degree of damage for several SiCOH and pSiCOH films as measured by the dT test. The degree of damage is normalized to the V1.c control film.

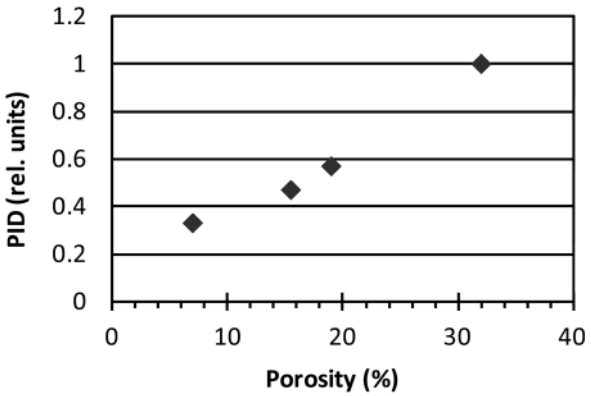

FIG. 13. The degree of damage as measured by the dT test as a function of pSiCOH porosity. Each sample had a carbon content of 19%–22%.

Figure 12 shows the degree of plasma induced damage, PID, for a number of SiCOH and pSiCOH films with varying k values, whose properties are summarized in Table I. As mentioned in Sec. II, V1.c, with k = 2.2, was used as the reference film for defining PID. V1.b was used in production at the 45 nm node, but it could not be used at smaller technology nodes because plasma damage increased its k. For subsequent nodes, V1.a was used because it suffered less plasma damage due to its lower porosity. Since V1.a has a degree of damage equal to 0.67, we tried to develop new dielectrics for advanced nodes with a PID < 0.67. For example, PID at lower k value was nearly cut in half with the V2 pSiCOH compared to V1 as shown in Figure 12.

Figure 13 shows how the degree of damage increases with increasing porosity in films over a short range of carbon content of 19%–22%. Higher porosity makes the film more permeable to the reactive species from the plasma, creating deeper damage. Therefore, minimizing porosity at a target k is critical.[39–41] Figure 14 shows how the degree of damage decreases as the %C in the film increases. This is illustrated with two sets of films: one set has high porosity (24%–27%) and the other has low porosity (16%–19%). Higher carbon content makes the film less susceptible to plasma damage for at least two reasons.

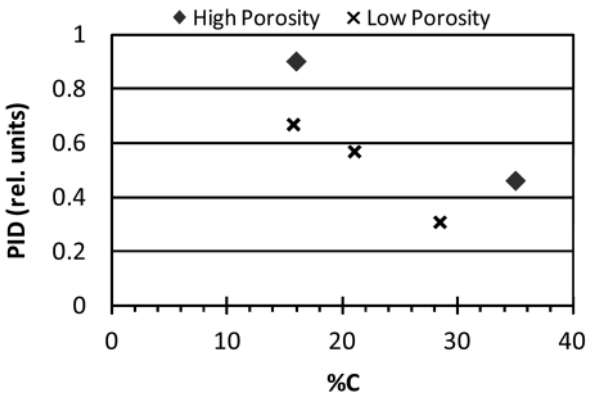

FIG. 14. The degree of damage as measured by the dT test as a function of pSiCOH carbon content (%C). The porosity was in the range of 16%–19% for the low porosity sample set, while the high porosity set had 24%–27% porosity.

First, if the film has higher carbon content before plasma exposure, then it will have more carbon left after the plasma exposure. The high residual carbon in the damage layer keeps the film relatively hydrophobic, which helps minimize the k increase due to plasma damage. Higher residual carbon also reduces the HF wet etch rate, which minimizes wet etch induced profile changes to trenches etched into ULK films. Second, the carbon acts to getter the reactive species from the plasma, which limits the depth of plasma damage.[26] The reactive species from the plasma are depleted by reactions with carbon in the film. More carbon in the film will deplete these species sooner, thus limiting the depth of damage. At $k = 2.2$, the degree of damage of the V1.c dielectric became a major integration problem, and PID had to be dramatically reduced by adding carbon to the films and improving the pore structure.

All the films with PID < 0.67 were fabricated with lower porosity, higher carbon content, or a combination of the two. Using PID as a guide, we successfully developed improved ULK dielectrics at $k = 2.5$, $k = 2.4$, and $k = 2.2$ that were optimized for minimum PID, as illustrated in Figure 12.

C. Implementation of SiCOH and pSiCOH in VLSI products

A critical property of a SiCOH or pSiCOH dielectric for enabling its implementation in reliable semiconductor devices is the time dependent dielectric breakdown (TDDB). The TDDB typically degrades with shrinking technology nodes, where the spacing between adjacent metallization lines decreases from node to node, especially for sub-80 nm pitch lines, and this degradation is further aggravated by the introduction of porosity in the dielectrics.[42] While it is beyond the scope of this review to discuss the TDDB reliability of the different ILD dielectrics, it should be noted that the TDDB lifetime generally decreases with decreasing k values, i.e., increasing porosity, and with decreasing carbon content and is affected by the pore structure as well.[42] This is illustrated by comparing the plots in Figure 15 with the properties of the corresponding dielectrics in Table I. The TDDB properties of the specific ILD dielectrics have determined their implementation in existing products and their implementation in future technology nodes.

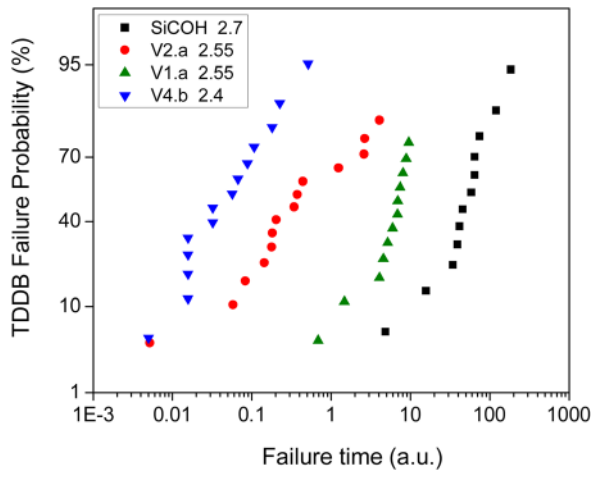

FIG. 15. TDDB lifetime of several ILD dielectrics. The numbers in the legend indicate the k values of the plotted dielectrics.

TABLE IV. Available low-k and ultralow-k SiCOH ILD dielectrics.

k	Precursors
Porogenless	
3.00	OMCTS
2.75	OMCTS
With porogen	
2.55–2.2	DEMS + BCHD (V1)
2.55–2.2	DEMS + BCHD + TDMMS (V2)
2.55	Embedded porogen (V3)
2.55–2.3	Embedded porogen + carbosilane (V4)

Table IV summarizes the types of currently available low-k and ultralow-k ILD dielectrics and the type of precursors used for their fabrications. As mentioned in the Introduction, the SiCOH films with $k = 3.0$ have become industry's standard interconnect insulator from the 90 nm technology node.[15–17] The porogenless SiCOH with $k = 2.7$ has been introduced by IBM and its partners in products at the 45 nm node.[20] At the same technology node, IBM and its partners have introduced for the first time the pSiCOH dielectric V1.b, with $k = 2.4$ in products (e.g., IBM's P7 microprocessor).

While some 32 nm chips continued to use a V1.b type ILD, most of the manufacturers replaced it with V1.a type ILD[33] ($k = 2.55$) for improved reliability at the lower dimensions. The other types of pSiCOH dielectrics are being considered for introduction at 22 nm and lower nodes based on easier manufacturability, e.g.,V3, or better mechanical properties, e.g., V4. The implementation and potential implementation of the low-k and ULK dielectrics described above is further illustrated in Figure 16.

IV. CAPS

A. Cap contribution to interconnect capacitance

Figure 17 shows the results of modeling of the total capacitance vs. cap dielectric constant and thickness for 14 nm node BEOL M2 inter-level metal structures with a fixed inter

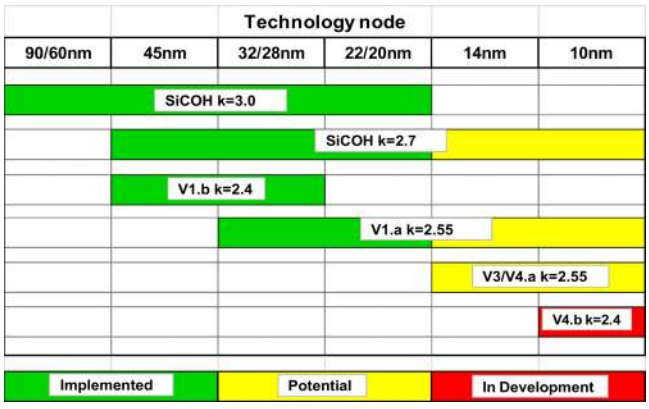

FIG. 16. Implementation of SiCOH and pSiCOH by IBM and its Alliance partners.

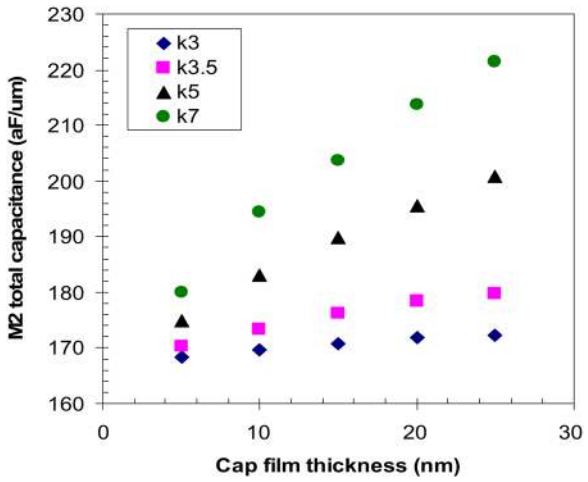

FIG. 17. Total capacitance as a function of dielectric cap film thickness and dielectric constant. Modeling shows reduction in capacitance with thinner, lower k dielectric cap film. Courtesy of James Chen, IBM Research.

level dielectric pSiCOH ($k \sim 2.55$) and constant Cu line dimensions. The modeling shows that both the dielectric constant of the cap film and its thickness determine the capacitance increase of the interconnect.

At a fixed cap thickness of 20 nm, a ~20% decrease in total capacitance can be obtained when the k of the dielectric cap is lowered from 7 to 3. The decrease in capacitance with the reduction of cap thickness is much more significant for higher k caps (e.g., $k = 5$ or 7) as compared to lower k caps (e.g., $k = 3$ or 3.5). The modeling shows that the difference in capacitance is significant for thicker cap films (~3% at 20 nm) even for small differences in dielectric constant (e.g., $k = 3$ and $k = 3.5$ curve). Figure 17 thus shows that thinner caps with lower dielectric constant are required to reduce the total capacitance of the device. However, a robust dielectric barrier film is required for fabrication of reliable device structures and; as we will see later, thinning of the cap is limited by the requirements that it must satisfy. Therefore, the first approach used by industry to address the contribution of the cap to the RC delay of the BEOL was the reduction of the dielectric constant, k, of the cap.

B. SiN and SiCNH caps

The first generation of dielectric cap that was integrated successfully with Cu metallization was SiN ($k \sim 7$) at 0.22 and 0.18 μm technology nodes.[43,44] Conventional SiN film was a robust Cu cap but with a relatively high dielectric constant.

The second generation cap with lower k value was SiCNH ($k \sim 5.3$) obtained by incorporation of carbon into the SiN. SiCNH cap was initially introduced at 130 and 90 nm technology nodes and has been used since for several technology generations.[21,45] The significant decrease of the dielectric constant from 7 to 5.3 reduced the cap's contribution to the total capacitance of the interconnect and the RC delay. Other properties of the SiCNH cap film are shown in Table V.

1. Key requirements for dielectric caps

While it is desirable to reduce the thickness of the dielectric cap as much as possible, this reduction is limited by the key requirements that a cap has to satisfy. The cap has to

1. be a barrier to Cu diffusion into the dielectric;
2. protect the Cu lines from corrosion during patterning steps in the fabrication of the device;
3. act as an etch stop layer for via build and, in some cases, as stopping layer for planarization by CMP, balancing the stress at copper-low k interface;[46]
4. protect the Cu from oxidation; during the fabrication process, the Cu lines covered by the cap are exposed to oxidizing plasmas during the deposition of SiCOH or pSiCOH ILD and the cap has to prevent the oxidation of the Cu;
5. provide a hermetic seal and prevent humidity ingress to the Cu in the final device;
6. the breakdown voltage and current leakage of the cap should be maintained above minimal values and the mechanical properties of the cap should be maintained in order to withstand subsequent processing steps.[46]

The requirements described above that have to be satisfied by a dielectric cap induce challenges in the thinning of existing caps or the development of new ones. This is illustrated next by the description of the oxidation barrier test.

2. Effects of reduction of SiCNH thickness on oxidation barrier properties

SiCNH caps in the thickness range of 35–40 nm were implemented at 90 to 45 nm technology nodes.[47] The thickness of the SiCNH cap film needs to be scaled down further for sub-30 nm devices in order to minimize the overall device capacitance. Various barrier performance tests along with evaluation of electrical properties were performed to

TABLE V. Selected properties of dielectric caps.

Cap	Description	Minimal thickness (nm)	k	Breakdown voltage (MV/cm)	Modulus (GPa)	Stress after UV
SiCNH	SiCNH	20	5.3	5	100	Tensile
Bilayer low k	SiCNxH/C-rich SiCNyH	25–30	3.8	4.2	104	Low tensile
Bilayer nitride	SiNx/SiNy	10	6.8	7.5	150	Compressive
Trilayer	SiNx/SiNy/SiCNyH	25–30	4.2	5	150	Compressive
Cyclic SiN	Multilayer SiN	12–20	6.1	8	160	Compressive
Co/SiN	*In-situ* clean/selective CVD Co/multilayer SiN	Co (1.8–2.4)/SiN (12–20)				Compressive

evaluate the lower limit of acceptable cap thickness that will satisfy the requirements described above and it was found, as illustrated next, that material modifications are required to further scale the thickness of the SiCNH cap film below 20 nm.[47]

An oxidation barrier test was performed on SiCNH films, 5 nm to 35 nm thick, and the results are shown in Figure 18. The figure shows optical images of as deposited SiCNH over Cu and after exposing the Cu covered by the SiCNH to the oxidation test[23] (see Sec. II). The first panel in Fig. 18(a) shows an optical image of the as-deposited SiCNH cap film on top of blanket Cu, while the other panels (Figs. 18(b)–18(f)) show images of SiCNH cap films of different thickness on Cu after the oxidation anneal. The black dots visible in the optical images corresponding to 5, 10, and 15 nm caps indicate partially oxidized copper (CuOx) after the oxidation test. The amount of oxidized copper (density of black dots) decreases with the increase in cap thickness, and for 25 and 35 nm thick caps, no sign of copper oxidation was detected after the oxidation test. These results indicate that a thickness bigger than 15 nm is required for SiCNH to act as an oxidation barrier.

The scaling down of the cap thickness for reducing the RC delay is also limited by the cap's performance as a barrier to Cu diffusion. It was shown elsewhere[47] that the thickness range of SiCNH caps showing good oxidation barrier performance is also the thickness range satisfying the requirement for robust copper diffusion barrier. Auger analysis has shown that, while the oxygen penetrates in the SiCNH cap to about 10 nm below the surface and the Cu diffuses into the cap by less than 10 nm during the oxidation test, the formation of Cu hillocks under thin caps is another factor imposing a lower limit on the thickness of a reliable SiCNH cap.[47]

The breakdown and leakage of SiCNH also showed degradation with reduction of cap thickness from 35 nm to 20 nm and were further affected by exposure to UV. These observations indicate that minimum SiCNH thickness required for reliable device performance is about 20 nm–25 nm.[47] Other properties of SiCNH caps such as modulus, breakdown voltage, and stress are summarized in Table V.

C. Advanced caps with reduced k and/or reduced thickness

1. Bilayer low-k dielectric cap (SiCNxH/SiCNyH)

The results discussed in Sec. IV B indicate that new cap materials are required for further reduction of the BEOL capacitance. As shown in Fig.17, one way to achieve the capacitance reduction is to decrease the k value of the cap. A new PECVD bilayer SiCNxH/SiCNyH dielectric cap film was developed to achieve this goal.[22,48] The two layers have different properties and the combined bilayer stack retains the benefits of both films. The first layer (SiCNxH) interfacing the copper has high nitrogen content and robust barrier properties, while the second layer (SiCNyH) is a film of lower nitrogen content, lower dielectric constant, and good plasma etch selectivity. The difference in nitrogen content of the layers was obtained by changing the precursor chemistry used for depositing them. Silane + ammonia or trimethyl silane + ammonia mixtures were used to deposit the first, nitrogen rich layer. The chamber was then purged prior to introduction of a carbon rich organosilicon precursor (dimethyl silacyclopentane) and ammonia for the deposition of the second, carbon rich layer.[48]

The thickness of the two layers in the bilayer film can be adjusted to obtain robust cap performance at a low effective dielectric constant. The range of k values of the bilayer film obtained by varying the precursor flow rates and the thickness of the individual layers has been discussed elsewhere.[48] The two layers can be combined to obtain a reliable cap with a dielectric constant of the bilayer film of ~3.8, significantly lower than that of the SiCNH film discussed in Sec. IV B 2 (see bilayer low k cap in Table V). The barrier performance, electrical properties, and electromigration (EM) performance of this bilayer film have been found to be comparable with that of the single layer SiCNH, indicating that this capacitance reduction strategy has minimal impact on reliability.[22] A scanning electron micrograph (X-STEM) of a cross-section of a bilayer cap of total thickness of 26 nm is shown in the left panel in Fig. 19(a).

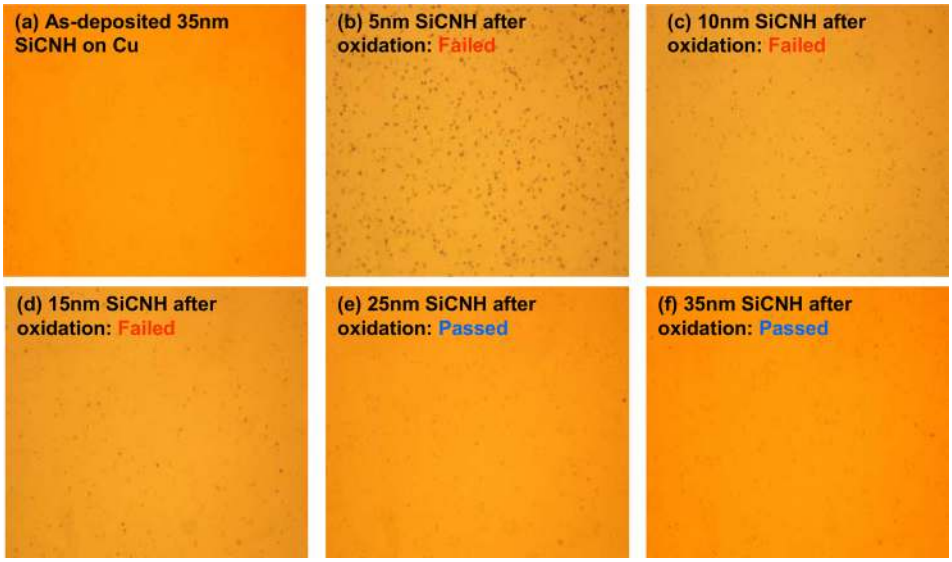

FIG. 18. Top-view optical image of (a) as-deposited SiCNH on Cu, (b)–(f) 5 nm–35 nm SiCNH on Cu post oxidation test (310 °C, 24 h, ambient air). Dark spots represent oxidized copper. Reproduced by permission from Nguyen *et al.*, ECS Trans. **33**, 137 (2010). Copyright 2010 by The Electrochemical Society.[47]

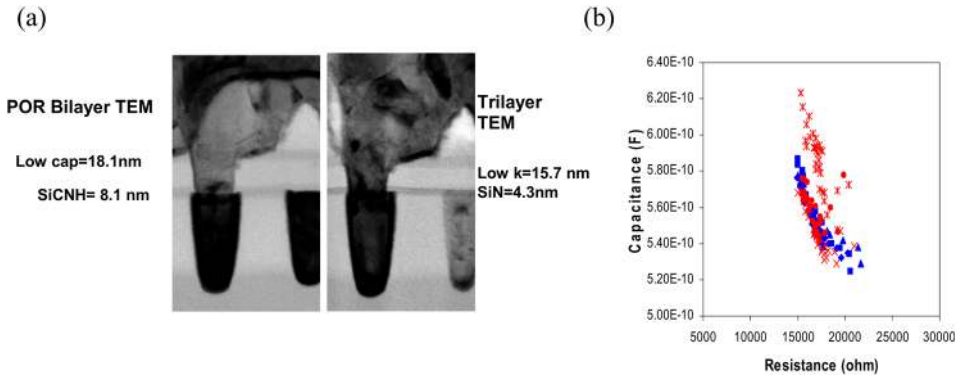

FIG. 19. Typical 20–26 nm thick low-k bilayer and trilayer caps on 32 nm Cu-low k interconnect structure. (a) Cross section micrographs of bilayer (left) and trilayer (right) caps; (b) capacitance vs. resistance of ~20 nm trilayer cap (blue) and ~26.2 nm bilayer cap (red). A ~4% capacitance reduction was obtained with thinner trilayer cap as compared to the bilayer cap. Reproduced by permission from Nguyen *et al.*, ECS Trans. **41**(43), 3 (2012). Copyright 2012 by The Electrochemical Society.[49]

2. Bilayer ultra-thin dielectric cap (SiNx/SiNy)

With each technology node, the layers of the metallization stack become thinner and the thickness of the cap needs to be reduced, especially in the thin wire levels. In this section, an alternate ultra-thin bilayer cap film will be discussed. Reduction of the cap's thickness require better intrinsic cap properties compared to that of SiCNH and this bilayer cap is therefore based on SiN.

The new bilayer cap film is deposited using silane and ammonia as precursors. The two layers in the bilayer film offer different properties and the combination of the two layers in a single stack offers additional advantages. In the SiNx/SiNy bilayer stack, the first silicon nitride, SiNx, layer is deposited at a low plasma power to minimize the damage to the pSiCOH ULK film. The second silicon nitride, SiNy, layer is a denser film deposited using same precursors but at a high RF power. This second layer is characterized by relatively high compressive stress and hence the film stack retains compressive stress post exposure to UV cure.[49]

The first layer interfacing the Cu is less dense and may not be a robust copper barrier. But this film protects the ULK surface from damage that could be created during the deposition of the dense second layer. Since the purpose of the first layer is to protect the ULK surface, an ultra-thin (1–1.5 nm) first layer is sufficient to form a continuous film. The second layer provides the barrier properties and a film thickness in range of 8–10 nm is required. This combined bilayer stack can provide robust barrier performance in the thickness range of 9 nm–12 nm.[49] The modulus of this bilayer SiN film (bilayer nitride cap in Table V) is higher than that of the carbon containing SiCNH or the bilayer SiCNxH/SiCNyH cap films discussed in Sec. IV C 1.

3. Trilayer low k ultra-thin dielectric cap (SiNx/SiNy/SiCNyH)

The bilayer SiCNxH/SiCNyH described above is a low k dielectric cap showing robust barrier performance. However, upon exposure to UV used for the cure of the pSiCOH ILD, the bilayer cap film changes its stress from compressive to tensile. The stress of the as deposited bilayer SiCNxH/SiCNyH is lower than the SiCNH film (Table V), but both films become tensile after exposure to UV. This can lead to potential cracking in the BEOL structure, impacting the device reliability. The SiNx/SiNy bilayer film discussed above overcomes the stress change problem because this retains compressive stress post UV exposure. But this bilayer film is a silicon nitride cap; hence, the dielectric constant of the cap is relatively high. In order to overcome these issues, a robust trilayer cap film, which retains compressive stress post UV cure of the pSiCOH, was developed with a dielectric constant of ~4 (see trilayer cap in Table V).

PECVD was used to deposit the three layers of the trilayer cap films in a sequential manner. Silane + ammonia were used for depositing the first two SiNx and SiNy layers of a total thickness of ~4 nm. These layers were deposited at low and high RF plasma power to form a film with high, as-deposited, compressive stress (~1200 MPa compressive). The third layer was deposited using trimethyl silane + ammonia + ethylene as precursors. This is a carbon rich layer with k ~ 3.3 and reduces the effective k value of the trilayer stack. The presence of first two nitride layers provides high modulus to the composite cap.

The trilayer film provides excellent cracking resistance in BEOL ULK structures. The initial low power SiNx layer prevents damage to the pSiCOH surface. The right panel in Figure 19(a) shows a cross-section scanning electron micrograph (X-STEM) of typical 20 nm trilayer cap. The trilayer cap has low leakage and provides ~4% decrease in capacitance as compared to the low k bilayer SiCNxH/SiCNyH cap (Fig. 19(b)).[49]

4. Conformal cyclic SiN

Dielectric films with high conformality are required for various applications for sub-20 nm technology nodes.[50] In the case of copper interconnects, the interface between copper and the cap plays a critical role in EM lifetime. Often, recesses can be seen in Cu lines near the corners after CMP, and such recesses can result in voids in the BEOL structure and affect EM lifetime. With increasing density of the interconnect structure, such recesses are expected to be more frequent. Thus, a newer conformal dielectric cap film is required to cover the copper lines without leaving any voids. In contrast to changing the deposition technique from PECVD to ALD or PEALD[50] as discussed by many in the industry, we describe a new cyclic conformal SiN cap prepared by PECVD. Such films can be deposited in existing PECVD cap tools without requiring significant investment in tool upgrades.

The new conformal SiN film is formed by using a cyclic deposition-plasma treatment process. The multi-layer SiN

film is formed by depositing ultra thin (∼2 nm) layers using mixtures of silane and ammonia. Each layer is deposited using a low-power RF plasma to improve the film's conformality and reduce damage to the pSiCOH ILD. After the deposition of each layer, a mild plasma nitridation is performed to densify the film. The process is repeated until the desired film thickness is achieved. The multilayer SiN is a highly conformal film that provides good step coverage with conformality of ∼70% or greater, as illustrated in Figure 20.

The multilayer, cyclic SiN film has high breakdown voltage and low leakage currents, and ultra-thin (12–14 nm) caps show robust copper oxidation barrier performance. The as deposited films are compressive and remain compressive after exposure to UV irradiation. Other properties of this cap are summarized in Table V. The conformal cyclic SiN shows higher modulus and breakdown in comparison to previously discussed dielectric caps and retains compressive stress post UV curing.

5. Selective Co/dielectric cap

As the spacing between the Cu lines decrease with each technology node, there is significant drop in EM reliability because of potential fast diffusion paths between the lines. This problem became critical for sub-32 nm nodes. The interface between Cu and the dielectric cap plays a critical role in the EM performance. Weak adhesion between Cu and the dielectric cap makes the structure susceptible to EM induced mass flow.[51,52] It was shown that the void growth rate under EM testing increases with decreasing interface debond energy between the copper and cap.[52,53] The post-CMP recess observed in copper lines can aggravate this issue.

Metal capping layers have better adhesion to Cu, but any metal deposited on top of the ILD dielectric can cause the degradation of the TDDB. Furthermore, metal caps could interact with Cu and increase its resistivity, an issue that should be avoided to prevent an increase in RC. Different selective deposition methods have emerged to provide a selective metal cap solution for EM enhancement without TDDB degradation. One of the methods for selective metal capping is to use electroless deposition of Co cap.[54] The major issue with this approach is the contamination of the ILD from the plating bath, which can cause degradation in yield and potential impact on capacitance. In addition, the electroless plating approach adds processing steps and increases wafer cost.

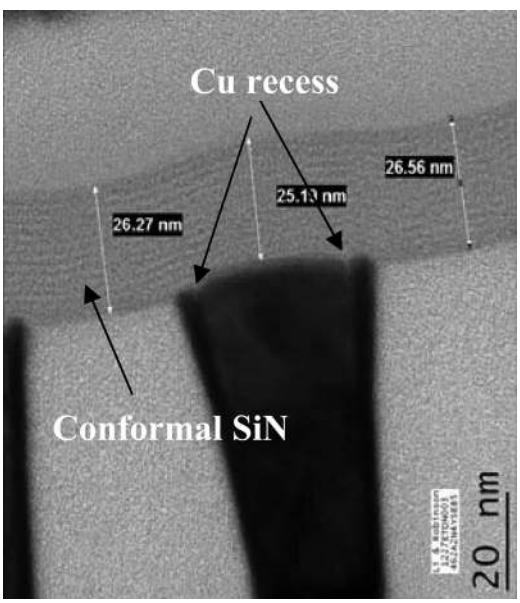

FIG. 20. Conformal cyclic SiN copper barrier cap. The multilayer film has good conformality over copper recess.

An alternate method for fabrication of a selective metal cap is to use alloy (doped) Cu seed layers.[55,56] Mn or Al are the preferred doping components. These metals have higher affinity for oxygen than copper and therefore segregate readily to the copper surface. The segregated metals reduce the copper oxide and form a metal layer on top of the copper lines. These self-forming barrier layers have strong adhesion to Cu and suppress copper diffusion. The issue with this approach is its strong dependence on the segregation behavior of a metal layer to the top of the Cu lines, and it may not provide uniform dopant-metal coverage on top of wider Cu lines. In addition, the dopant may not segregate completely to the surface, and the un-segregated dopant atoms may remain in solid solution in the copper lines, leading to increased line resistivity.

A more robust approach for improving EM is the use of a metal cap layer, e.g., Co, deposited on top of the metal lines using selective chemical vapor deposition (CVD). The deposition should be highly selective to enable the deposition of a sufficiently thick cap on Cu without metal deposition on the ILD dielectric. Such a process is described next.

A carbonyl based precursor is used in the current selective CVD Co process.[57] Prior to the deposition of Co, the copper surface is cleaned to remove any copper oxide and carbon residues. Co is deposited selectively only on Cu using a cyclic process where in each cycle the deposition of a thin Co layer is followed by a plasma treatment. The deposition rate drops with time in each cycle and the plasma treatment generates a fresh metal surface to restore the deposition rate. Co is not deposited on top of the oxygen rich pSiCOH. Figure 21 illustrates the selectivity of the Co process after the deposition of a 3 nm Co film.

Figures 21(a)–21(c) show the EDX scans of Co liner and Co cap selectively deposited on top of Cu lines, TaN/Ta liner, and the conformal cyclic SiN cap (described in Sec. IV C 4), respectively. Co is identified only on top of the Cu but not outside it on the dielectric.

A similar but non-selective PECVD process was used to fabricate Co liners along the walls of the Cu lines and vias. Electromigration reliability was then evaluated for structures using a ultralow $k \leq 2.55$ pSiCOH ILD and either dielectric caps, or selective Co plus dielectric cap, or a wrap-around Co structure, where the Cu is encapsulated between Co cap and Co liner. The EM lifetime distribution for these structures is shown in Figure 22. Electromigration testing was performed under a constant DC current density. In order to get any substantial fails on samples with Co cap, the testing temperature was increased to 340 °C, i.e., 25–50 °C higher than the regular testing temperature. As shown in Figure 22, the use of the CVD Co cap film improved the EM lifetime

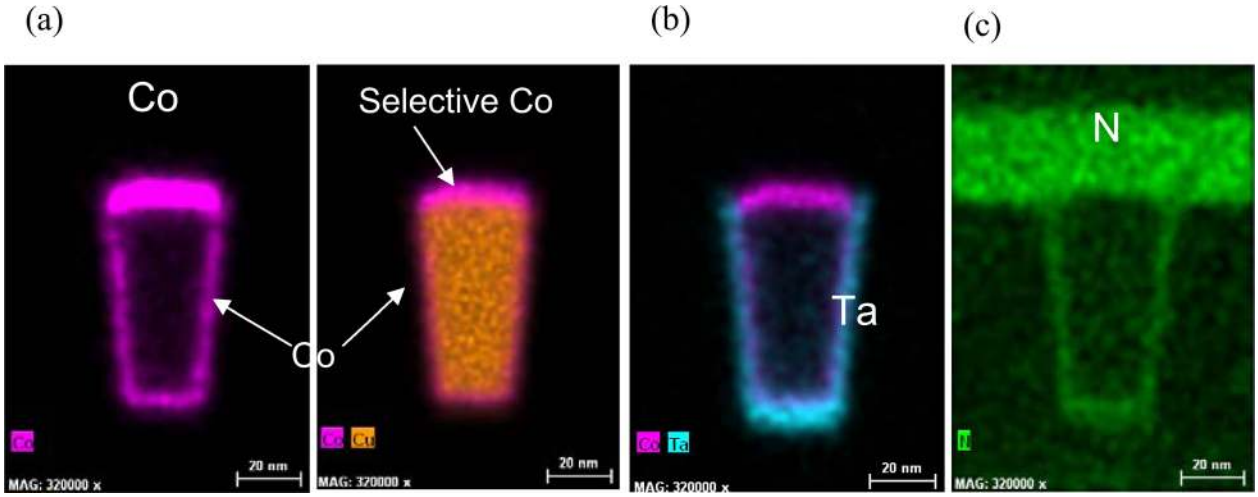

FIG. 21. EDX signal of (a) Co from selective cap and liner, Cu in the trench, (b) Ta from the barrier layer and Co from the selective cap and liner, and (c) N from dielectric cap and liner layer. Co selectively deposits on top of Cu and not on ILD or the Ta liner layers. A complete wrap around structure is achieved by using a Co cap and Co liner.

by ~10×, while the Co wrap-around structure increased the EM lifetime by ~1000× compared to the structure with only dielectric cap.

Thin Co at the edges of Cu lines, with Cu recess at the corners, is weak points for Cu migration. As shown in Fig. 21(b), Co cap aligns well with the Co liner but does not deposit on top of TaN/Ta liner. Thus, a preferred approach for obtaining the maximum EM benefit is to use a combination of Co liner with selective Co cap.

The results discussed above show a considerable improvement in device reliability with the selective metal cap process. It is important to understand the impact of any other parameters on device performance, especially if the selective Co cap deposition was followed with an *in-situ* vs. an *ex-situ* dielectric capping process.[57] After the Cu lines are selectively capped with Co, there is still a need to deposit a dielectric barrier cap layer before depositing the ILD pSiCOH film. The dielectric barrier cap prevents the selective Co from oxidizing during the pSiCOH deposition. The dielectric cap can be deposited without a vacuum-break after the deposition of the Co, in a chamber sharing the same platform as the CVD Co chamber (*in-situ*), or can be deposited in a stand-alone tool, whereby the Co cap is exposed to air before the deposition of the dielectric cap (*ex-situ*). In the *ex-situ* process, the Co surface will be partially oxidized, and it will be difficult to reduce the Co oxide prior to dielectric cap deposition. Furthermore, a thicker Co cap film is required for an *ex-situ* process to prevent the oxidation of Cu underlying the Co layer. In contrast, with an *in-situ* process, the dielectric cap is deposited on Co without any intermediate oxidation of the Co or Cu. In this case, a thin continuous Co layer is sufficient to get the required EM benefits. A ~10× improvement in EM was observed with an *in situ* capping process[57] vs. the *ex-situ* process.

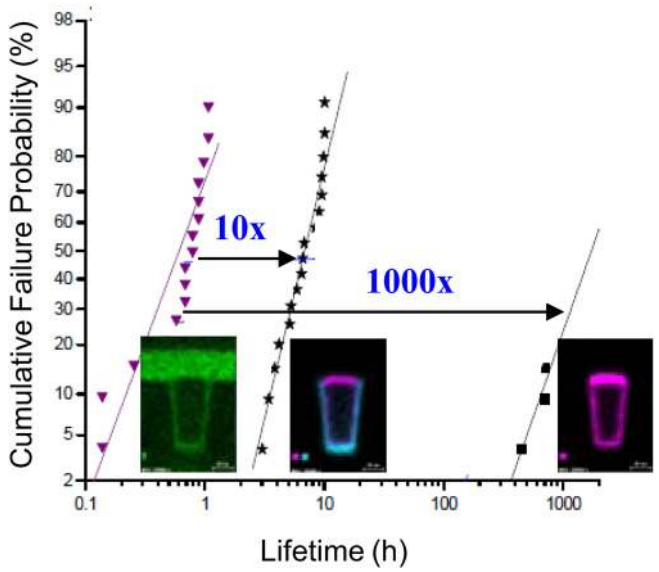

FIG. 22. Electromigration lifetime distribution with (a) conformal cyclic SiN dielectric cap, (b) selective Co/conformal cyclic SiN cap, and (c) Co liner along with selective Co/conformal cyclic SiN cap. 10× improvement in lifetime was achieved with a metal only cap layer and ~1000× improvement was obtained with a Co cap and Co liner complete wrap-around structure as compared to dielectric only cap structure. Courtesy of C.-K. Hu, IBM Research.

V. SUMMARY

Manufacturable ILD SiCOH and pSiCOH V1 dielectrics have been developed with k values from 3.0 to 2.2. Of those, SiCOH and pSiCOH dielectrics with k = 3.0, 2.7, and 2.4 have already been implemented in 45 nm and 32 nm products. ILD dielectrics with k = 2.7 and 2.55 are being currently integrated at the 22 nm node and evaluated for next technology nodes.

Advanced versions of pSiCOH dielectrics with high-C content, containing Si-CH_2-Si skeleton bonds, have been developed with improved resistance to plasma induced damage and improved mechanical properties. These materials provide better control of critical dimensions and improved reliability of the interconnect structure, including packaging interactions. These advanced ILD dielectrics are being evaluated for integration and reliability at current and future technology nodes.

SiCNH and SiNx dielectrics have been used as cap materials for Cu/low-k interconnects in many device generations. The SiCNH cap has minimum thickness limit for performing as an oxidation barrier. Reduction in RC with aggressive interconnect scaling therefore required development of new, thinner, lower-k dielectric barrier films. This led to development of several multi-layer caps with $k < 4$ and thinner 10–25 nm caps. Conformal dielectric cap film was developed to provide good coverage of recesses in copper lines. In addition, a selective Co cap process was developed to further improve the device reliability leading to significant enhancements in EM without degradation in TDDB.

ACKNOWLEDGMENTS

The authors are thankful to S. Cohen, Y. Ostrovski, E. Adams, A. Madan, N. Klymko, S. Molis, K. Virwani, T. Shaw, H. Shobha, E. Liniger, J. Chen, and C. K. Hu for their contributions to the characterization of the interconnect dielectrics. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

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