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Prolonged silicon carbide integrated circuit operation in Venus surface atmospheric conditions

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The prolonged operation of semiconductor integrated circuits (ICs) needed for long-duration exploration of the surface of Venus has proven insurmountably challenging to date due to the ~ 460 °C, ~ 9.4 MPa caustic environment. Past and planned Venus landers have been limited to a few hours of surface operation, even when IC electronics needed for basic lander operation are protected with heavily cumbersome pressure vessels and cooling measures. Here we demonstrate vastly longer (weeks) electrical operation of two silicon carbide (4H-SiC) junction field effect transistor (JFET) ring oscillator ICs tested with chips directly exposed (no cooling and no protective chip packaging) to a high-fidelity physical and chemical reproduction of Venus' surface atmosphere. This represents more than 100-fold extension of demonstrated Venus environment electronics durability. With further technology maturation, such SiC IC electronics could drastically improve Venus lander designs and mission concepts, fundamentally enabling long-duration enhanced missions to the surface of Venus. [http://dx.doi.org/10.1063/1.4973429]

Authoritative expert panel reports have described why improved understanding of Venus and its greenhouse effect atmosphere and geology has relevance to a better understanding of the Earth and solar system formation.[1–4] Towards this end, these reports call for surface observations that will require prolonged-mission Venus landers, including long-term atmospheric and seismic activity data.

While long-term operation of silicon-based ICs has enabled years of useful Mars lander mission duration,[1,5,6] achieving similar mission duration on the surface of Venus has proven an insurmountable challenge to date.[5–8] Venus' thick CO_2-based atmosphere supports massive greenhouse warming and extreme physical conditions (~460 °C, ~ 94 MPa, above CO_2's critical point).[7,9] Adding to the challenge is a caustic atmospheric chemistry containing enough SO_2 (around ~180 ppm at the surface) to form sulfuric acid cloud-decks many tens of kilometers thick.[9] As these conditions fall well beyond the operating realm of silicon-based ICs,[10,11] prior Venus landers and modern designs for future landers have employed pressure vessels and/or cooling systems to protect mission-critical IC electronics. These protection measures add substantial mass and mission expense, and are only effective for a few hours (2 hours, 7 minutes is the surface operation record set by Venera 13) before the surrounding Venus environment overcomes the protection and thermally fails the electronics with silicon ICs bringing end of mission.[3,5–8]

Other groups have reported short term (i.e., far less than 500 hours) T ≥ 460 °C Earth-atmosphere operation of SiC and III-N integrated circuits with single-level interconnect.[12–23] Recently our group at NASA Glenn reported the fabrication and demonstration of 4H-SiC JFET integrated circuits (up to 24 transistors, with two levels of metal interconnect) and ceramic packaging that have consistently

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functioned for more than 1000 hours (41.7 days) at 500 °C in Earth-atmosphere oven-testing.[24–26] Given these promising results, we decided to subject other chips diced from the same prototype IC wafer to electrical testing in simulated Venus surface atmospheric conditions inside the NASA Glenn Extreme Environments Rig (GEER).[27] Ring oscillator chips were selected for the first such test, as these ICs can be operated using the fewest number of wires (one signal output in addition to $+V_{DD}$, GND, and $-V_{SS}$ chip DC power inputs), are a recognized standard for logic IC demonstration, and provide harmonic output signals that can be detected in frequency spectrum even in the presence of substantial expected electrical noise and output signal path attenuation. Two NASA Glenn fabricated SiC JFET ring oscillator ICs residing on separate chips were selected for testing in GEER: a 3-stage ring oscillator and an 11-stage ring oscillator that are further described in the supplementary material and elsewhere.[24–26,28]

Two electrical feedthrough probe assemblies that are further described in the supplementary material were custom-built to enable operational testing of these chips exposed to simulated Venus surface atmosphere in GEER. Each probe assembly nominally provided four outside-chamber electrical connections to the SiC IC chip inside the chamber. The limited number of available test ports on

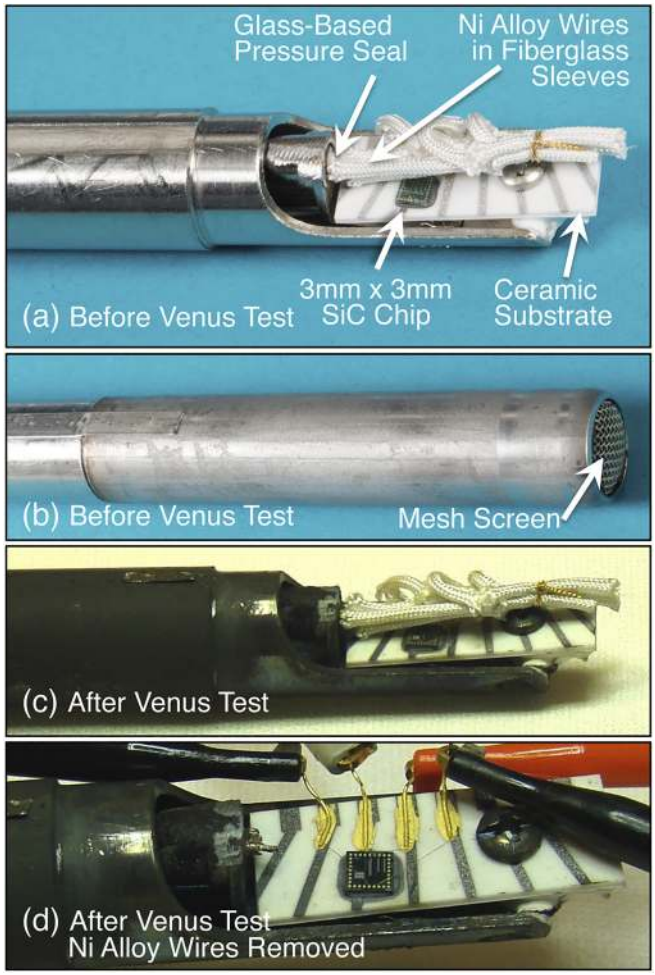

FIG. 1. Annotated photographs documenting the chip-containing end of the 11-stage ring oscillator feedthrough probe assembly at various stages of this study. (a) Nearly-completed assembly showing the 3 mm x 3 mm 11-stage SiC ring oscillator chip attached to ceramic substrate and fiberglass-sleeved wiring bundle prior to any heated testing. (b) Completed assembly prior to heated testing showing the mesh screen cap that permits chip immersion in simulated Venus atmosphere during the test. (c) After 21.7 days of simulated Venus surface conditions testing following removal of the mesh screen cap. (d) During clip-lead electrical testing conducted with the chip disconnected/isolated from the short-circuited feedthrough by removal of the nickel alloy wires.

the GEER chamber, limited space and number wires in the first custom feedthrough probe design, and lengthy processes of probe construction, pressure qualification, and safety approval were all factors that combined to restrict the sample size for this first feasibility test to just two SiC ICs. Figure 1 shows the inside-chamber end of one such probe assembly at various stages of the experiment. Fig. 1(a) shows the mounting and wiring of the 3 mm x 3 mm 11-stage SiC JFET ring oscillator IC chip almost ready for testing. Electrical signals were routed through mineral insulated cable comprised of four Nickel 201 (alloy) wires separated by crushed magnesium oxide ceramic insulation material inside an Inconel 600 jacket, sealed at both ends by multiple cycles of manually applying and curing Ferro 1180A high temperature glass. The subsequently installed cover with wire-mesh screen seen in Fig. 1(b) permitted simulated Venus atmosphere immersion of the chip, wire bonds, die attach, and ceramic substrate during the test, whilst protecting these from physical damage during feedthrough probe handling and mounting. Prior to simulated Venus surface conditions testing, both feedthrough probes with chips were operationally qualified 1) in Earth-atmosphere 460 °C to 480 °C tube oven for over 47 hours, and 2) installed in GEER under nitrogen atmosphere of 460 °C and 9.0 MPa for 56 hours.

Two 4-conductor cables (more than 14 m long) routed through safety wall bulkheads electrically connected each chip/probe assembly to computer-controlled instruments. As discussed in the supplementary material, the setup greatly attenuates measured oscillator IC output signals to varying degree that depends upon a number of experimental factors, including oscilloscope probe loading, cable parasitics and length, IC output signal frequency and impedance, and electrical parasitics of the custom-built feedthroughs. However, since the IC output buffers largely isolate the critical feedback ring circuit loop, oscillator output frequencies are much less affected by these varying off-chip signal path conduction factors. A dual-output supply provided V_{DD} = +24 V and V_{SS} = −24 V DC power to both chips for all the testing in GEER. Two computer-controlled relays, each residing between

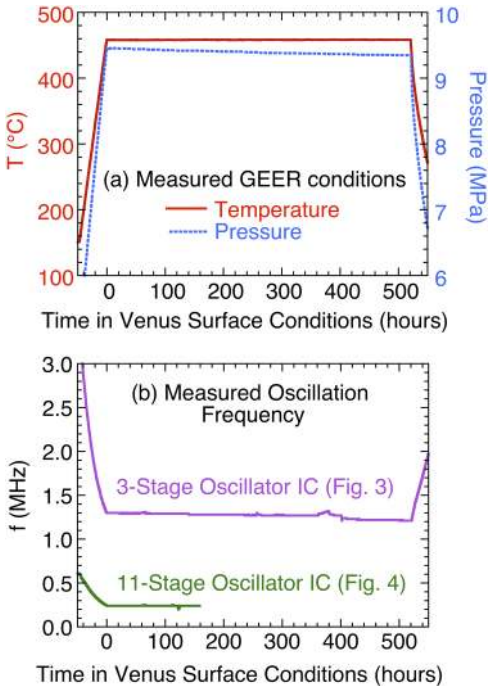

FIG. 2. SiC ring oscillator IC testing data summary as a function of time in Venus surface atmospheric conditions. (a) Recorded GEER vessel temperature (red, solid) and pressure (blue, dashed). (b) Measured SiC ring oscillator IC output signal frequencies. The 3-stage SiC JFET ring oscillator IC (top trace, purple) functioned at 1.26 ± 0.05 MHz over the entire 521 hours (21.7 days) it was exposed to Venus surface atmospheric conditions. The 11-stage ring oscillator IC (bottom trace, green) functioned at 245 ± 5 kHz for 109 hours, after which output signal degraded and was lost at 161 hours; however, as shown in Fig. 4(b), this IC was later verified fully functional following post-test disconnection from its electrical feedthrough that short-circuited during Venus conditions testing. Data from some of the pre-test heat-up and post-test cool-down is also shown.

respective feedthrough probe V_{DD} cable wire inputs and the V_{DD} power supply output terminal, were inserted to facilitate independent powering and measurement of each oscillator as well as measurement of "power-off" background noise waveforms. More information on the GEER vessel and experimental procedures is in the supplementary material.

Figure 2 summarizes the experimental test results as a function of time in simulated Venus surface atmospheric conditions. Figure 2(a) shows the measured GEER chamber pressure and temperature. The reference time t = 0 hours corresponds to GEER arriving at 460 °C and 9.4 MPa pressure with the simulated Venus surface atmospheric composition. 521 hours (21.7 days) of simulated Venus surface conditions testing time were accumulated before facility scheduling forced test conclusion. Measurements for some of the pre-testing ramp-up and post-testing cool-down are included in Fig. 2 plots, showing expected oscillation frequency dependence on temperature.[29] The oscillation frequency ratio between the two ICs differs somewhat from the 11 to 3 ratio that would be expected based solely on number of signal feedback loop gates/stages, but further study is required to firmly ascertain the reasons behind this discrepancy.

Figure 2(b) shows the measured oscillation frequencies of the two ICs throughout the Venus conditions testing. As seen in Fig. 2(b) and Fig. 3, the 3-stage ring oscillator IC functioned at 1.26 ± 0.06 MHz for the entire 521 hour (21.7 days) duration in simulated Venus surface conditions. This time of IC operation in Venus surface atmospheric conditions is more than 100-fold longer than what has been previously demonstrated 1) without a protective enclosure or cooling and 2) on actual Venus landers with heavily cumbersome electronics-protection measures.[5,7] "Power off" control waveforms recorded throughout the testing confirmed that no oscillation signal was present

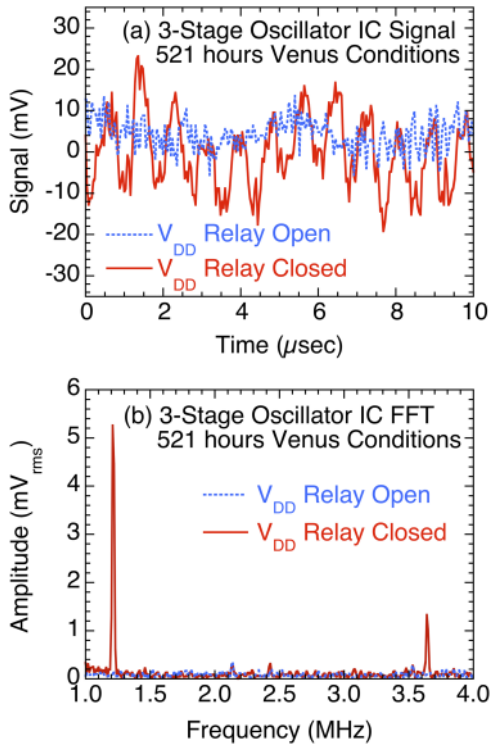

FIG. 3. Three-stage ring oscillator IC output signal recorded at 521 hours of simulated Venus surface conditions operation. (a) 10 μsec window of waveform data measured with 3-stage oscillator V_{DD} powered (V_{DD} relay closed, solid red) and unpowered (V_{DD} relay open, dashed blue). (b) Fast Fourier Transform (FFT) magnitude spectra calculated from full recorded waveforms, illustrating that fundamental (1.21 MHz) and third-order harmonic (3.63 MHz) FFT peaks are present only when the 3-stage SiC ring oscillator is properly powered with the V_{DD} relay closed (solid red) and not present when the V_{DD} relay is open (dashed blue). The IC output signal amplitude is substantially attenuated by feedthrough and cabling between the chip and the measurement oscilloscope, but the amount of attenuation could not be independently quantified during the Venus conditions testing.

unless the corresponding V_{DD} relay was closed to properly power the IC, as illustrated by the example waveforms shown in Fig. 3(a) and resulting Fast Fourier Transform (FFT) magnitude spectra shown in Fig. 3(b). The measured amplitude of the 3-stage ring oscillator signal, impacted by substantial signal path attenuation, varied from 2.4 mV_{rms} to 6.2 mV_{rms} over the course of the test.

The 11-stage ring oscillator IC functioned with excellent frequency and amplitude stability at 240 ± 10 kHz and 36 ± 2 mV_{rms} for the first 109 hours of simulated Venus surface atmosphere testing. As shown in Fig. 4(a), there is negligible difference between measured oscillator output waveforms at t = 0 hours and t = 109 hours. However, starting at t = 111 hours, 11-stage oscillator output began to erratically exhibit significant instability superimposed on oscillation signals, and by t = 161 hours loss of 11-stage IC oscillation signal occurred. Over this same time period V_{SS} power supply current increased from ~ 0.7 mA at t = 109 hours to ~ 4 mA at t = 161 hours. By t = 379 hours, the 200 mA power supply current limit was reached, even when the 11-stage V_{DD} relay was open, which affected V_{SS} supplied to the 3-stage oscillator by the same instrument. Therefore, all three power wires (V_{DD}, GND, and V_{SS}) leading to the 11-stage probe cable were removed and 11-stage probe data collection suspended for the remainder of testing in GEER.

Although the 11-stage ring oscillator IC functioned in Venus surface atmospheric conditions far longer than any ICs reported prior to this work, it is important to understand why this chip did not function as long as the 3-stage ring oscillator IC. Following post-test temperature and pressure ramp down, the feedthrough probe assemblies were removed from GEER for further study. Fig. 1(c) shows the post-test appearance of the chip end of the 11-stage probe following mesh cap removal. While significant discoloration is apparent compared to Fig. 1(a) pre-test appearance, the SiC IC chip, ceramic substrate, wire bonds, wiring, and fiberglass insulation sleeves appeared intact. Current-voltage (I-V) measurements, conducted prior to this feedthrough's removal from GEER and repeated following Fig. 1(c) mesh cap removal, revealed that all four 11-stage probe

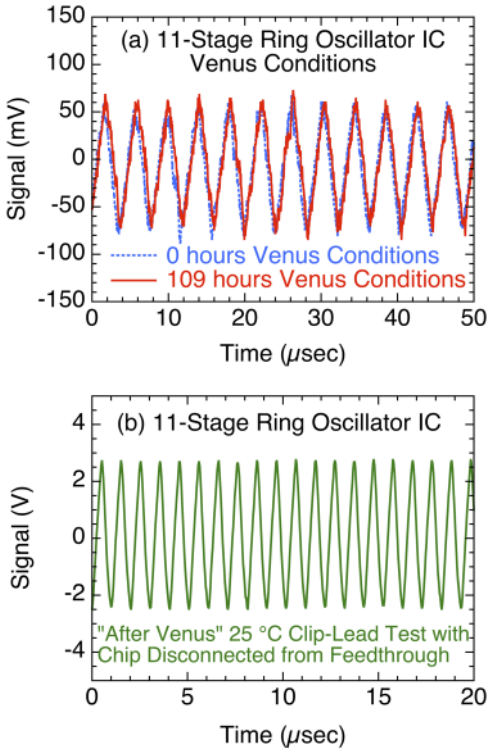

FIG. 4. Measured 11-stage ring oscillator IC output waveforms. (a) 50 μs window of waveform data recorded at the start (0 hours, blue dashed) and at 109 hours (red solid) of simulated Venus surface conditions testing in GEER. (b) 20 μs window of 25 °C clip-lead test waveform data (i.e., with chip disconnected from its short-circuited feedthrough as shown in Fig. 1(d)) recorded after the conclusion of 521 hours of Venus surface conditions testing in GEER.

electrical input/output connections were short-circuited to each other with less than 5 Ω resistance. The four nickel alloy feedthrough wires emerging from the glass seal were then removed as seen in Fig. 1(d), electrically disconnecting the 11-stage ring oscillator from the rest of the feedthrough probe assembly. However, additional I-V measurements after nickel wire removal showed the feedthrough input/output connections remained short-circuited, proving that short-circuits resided in the feedthrough electrical path prior to the ceramic substrate and 11-stage oscillator chip.

As shown in Fig. 1(d), electrical test leads were then clipped to remaining gold substrate wires to facilitate independent measurement of the 11-stage oscillator IC following its disconnection from the short-circuited feedthrough. The resulting Fig. 4(b) measured oscillator waveform proved that the 11-stage oscillator IC remained functional following the 521 hour exposure to simulated Venus surface conditions. The 980 kHz oscillation frequency was 14% from the 860 kHz pre-test oscillation signal recorded prior to first heating on GEER. Thus, it is understood that for both SiC ICs tested in GEER, the ring oscillator circuits themselves remained in full working order as of the conclusion of the 21.7 day test in Venus surface atmospheric conditions.

The post-test measurements independently verified that substantial changes to some feedthrough electrical connection properties occurred during the Venus atmospheric testing. The feedthroughs are undergoing further study to understand the degradation. Feedthroughs with consistent immunity to Venus atmospheric exposure and ability to handle more electrical connections with higher signal fidelity are desired for future IC tests in GEER.

This study marks the first reported demonstration of multi-day/week semiconductor IC functionality in Venus surface atmospheric conditions without pressure vessel, cooling, or other means protecting chips from the scorching caustic environment. We are presently striving to upscale the Venus-durable SiC JFET IC technology towards hundreds of transistors per chip circuit complexity. Such level of integration would be comparable to the complexity of IC chips used in mankind's first wave of solar system exploration launched prior to 1978, including the highly successful NASA Viking Mars landers.[30] Elimination of heavily cumbersome electronics sheltering measures (e.g., pressure vessels and cooling systems) while simultaneously extending IC surface operating time to weeks or months should drastically alter the hardware and approach to Venus surface exploration and fundamentally change what can be considered in future Venus mission concepts. With concurrent maturation of other Venus-lander technologies, we believe that further-developed SiC JFET ICs will play a mission-enabling role in the first landers to return weeks of important science data from the surface of Venus.

SUPPLEMENTARY MATERIAL

See supplementary material for additional experimental information on the SiC JFET ring oscillator ICs, chip mounting and connections, electrical measurements, and Venus environment chamber (GEER).

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