Properties and Synthesis of Passive Lossless Soft-Switching PWM Converters

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Abstract— This paper derives general topological and electrical properties common to all lossless passive soft-switching converters with defined characteristics and proposes a synthesis procedure for the creation of new converters. The synthesis procedure uses the properties to determine all possible locations for the resonant inductors and capacitors added to achieve soft switching. Then a set of circuit cells is used to recover the energy stored in these resonant elements. This paper also explains the operation of the circuit cells and the many new passive lossless soft-switching converters. A family of soft-switching boost converters is given as an example of the synthesis procedure. Experimental waveforms are shown for a new soft-switching Cuk converter.

Index Terms— Lossless snubber, soft switching, zero-current turn on, zero-voltage turn off.

I. INTRODUCTION

HIGHER switching frequencies allow reduction of the magnetic component sizes with pulsewidth-modulated (PWM) switching converters. Unfortunately, increased switching frequencies cause higher switching losses and greater electromagnetic interference (EMI). The switching loss mechanisms include the current and voltage overlap loss during the switching interval and the capacitance loss during turn on. The diode reverse recovery also causes an additional conduction loss and further contributes to the current and voltage overlap loss. Active or passive soft-switching methods have been reported to reduce these switching losses. Recently, passive soft switching has received renewed inspection as a better alternative to active methods, because they do not require an extra switch or additional control circuitry. Consequently, they are less expensive, have higher reliability, and have been reported to achieve higher performance/price ratios than active methods [1], [2]. For PWM converters, passive soft switching reduces switching losses by lowering the active switch's di/dt and dv/dt to achieve zero-current turn on and zero-voltage turn off. Furthermore, by controlling the di/dt of the active switch, the reverse recovery currents of the diodes are also controlled. The only loss mechanism not recovered with the passive technique is the energy in the internal capacitance of the switch. However, this loss is much smaller than the other switching losses and may be smaller than the loss incurred by using an auxiliary switch in an active method [1]–[3]. Historically, passive soft-switching techniques were used to

reduce spikes in the switching circuits and were lossy by dissipating the recovered switching energy in resisters [4]. More recently, many lossless and partially lossless techniques have been proposed [1], [5]–[21].

The two necessary components that must be added to the circuit to achieve passive zero-current turn on and zero-voltage turn off are a small inductor and capacitor. The inductor provides zero-current turn on of the active switch and limits the recovery current of the diodes while the capacitor provides zero-voltage turn off of the active switch. Traditionally, the inductor and capacitor have been placed in series and parallel with the active switch, respectively. However, many other locations are possible and can lower the component count and reduce switch stress. Furthermore, additional circuitry accompanying the capacitor and inductor is used to recover their energy to either the load or the input. There are many different proposed circuits to accomplish this. The objective of this paper is to find general topological and electrical properties that describe these recovery circuits and the placements of the resonant inductor and capacitor to facilitate the creation of new circuits. Furthermore, circuit cells are constructed that simplify the creation of new soft-switching circuits.

This paper derives general topological and electrical properties common to all lossless passive soft-switching converters with defined characteristics and proposes a procedure for the synthesis of new converters. The synthesis procedure uses the properties to determine all possible locations of the inductor and capacitor added to achieve soft switching. Then a set of circuit cells is used to easily add circuitry that recovers the energy stored in these elements. The properties also explain the operation of the circuit cells and the many new passive lossless soft-switching converters that can be synthesized. Section II introduces the topological and electrical properties. Section III presents the synthesis procedure and gives examples. Section IV describes the operation of a new Cuk converter created by the synthesis procedure with reference to the properties. Then the experimental waveforms of the circuit are shown to verify operation. Section V concludes this paper.

II. TOPOLOGICAL AND ELECTRICAL PROPERTIES OF LOSSLESS PASSIVE SOFT-SWITCHING CONVERTERS

A. Definition of Lossless Passive Soft-Switching PWM Converters

The definitions below first list the components that describe the underlying hard-switched PWM converter and then follow with additional components that are added to allow

lossless passive soft switching. An essential element of isolated topologies, transformers, have been left out of the underlying PWM converter components. Although not addressed in this paper, they can be seen as an extension to the properties that follow. Additionally, the properties assume that there is only one active switch in the PWM converter. Multiswitch implementations are addressed in [22]. For the assumptions and many of the proofs that follow, the PWM converter consisting of the elements described below is viewed as a graph G and uses terms from graph theory [23].

1) The Underlying PWM Converter:

a) A set of dc voltage sources $V_g = (V_{g_i}, i = 1, \ldots, n_g)$.

b) A set of linear time-invariant (LTI) resistors $R = (R_i, i = 1, \ldots, n_r)$.

c) A set of LTI inductors $L = (L_i, i = 1, \ldots, n_l)$.

d) A set of LTI capacitors $C = (C_i, i = 1, \ldots, n_c)$.

e) An active switch S.

f) A set of diodes $D = (D_i, i = 1, \ldots, n_d)$.

2) The Passive Elements for Lossless Soft Switching:

a) A set of zero-current inductors $Lr = (Lr_i, i = 1, \ldots, n_{lr})$. Lr provides zero-current turn on of active switch S.

b) A set of snubber inductors $Ls = (Ls_i, i = 1, \ldots, n_{ls})$.

c) A set of zero-voltage capacitors $Cr = (Cr_i, i = 1, \ldots, n_{cr})$. Cr provides zero-voltage turn off of the active switch.

d) A set of snubber capacitors $Cs = (Cs_i, i = 1, \ldots, n_{cs})$.

e) A set of snubber transformers $Ts = (Ts_i, i = 1, \ldots, n_{ts})$.

f) A set of snubber diodes $Ds = (Ds_i, i = 1, \ldots, n_{ds})$.

3) Voltage Storage Device (VSD): A VSD is a device or subcircuit that stores energy in the form of voltage (e.g., capacitor, voltage supply, and transformer-coupled voltage supply).

4) Passive Turn-On and Turn-Off Snubbers: Sets of passive elements for soft switching that are added to the underlying hard-switched converter to limit the switch current and voltage during switch turn-on and turn-off intervals, respectively.

Assumption A1: Each load R forms a loop with a subset of elements in $(C \cup V_g)$.

Assumption A2: In the graph G and each of the-switched subgraphs created by turning on groups of switches, there are neither loops consisting only of elements in $C \cup V_g$ nor cutsets consisting only of elements in L.

Assumption A3: The active switch in the PWM converter is current bidirectional.

Assumption A4: The underlying PWM converter graph will not be modified by the snubber components except by the insertion of a set of Lr. In addition, the set of Lr will not break the loop formed by R and the subset of elements $(C \cup V_g)$.

Notation Convention: Constants f_x, f_x^T are single-valued or row vectors containing either 0, 1, -1 depending on the placement of the element x within the cutset or loop and the chosen current or voltage polarity convention for that element.

The definition of the underlying PWM converter and Assumptions A1 and A2 follow closely with [24]–[28]. The differences are due to the treatment of active and passive switches. In the definitions above, the distinction is made between active and passive switches since it is assumed that the underlying PWM topology and switch implementation has already been identified.

Most practical PWM converters today use current bidirectional switches and so is the driving purpose for Assumption A3. MOSFET switches are already current bidirectional because of the inherent body diode. Additionally, many insulated gate bipolar transistors (IGBT's) have antiparallel diodes built-in so they can be used for a wider variety of applications. Furthermore, it will be shown later that PWM converters which need voltage bidirectional switches cannot passively recover energy from the Lr inductors.

Assumption A4 describes the basic nature of how the passive soft-switching elements are added to the underlying PWM converter.

B. Lossless Passive Turn-On and Turn-Off Snubber Requirements

A lossless passive turn-on and turn-off snubber not only should slow the di/dt and dv/dt of the active switch respectively, but also losslessly recover the zero-current inductor (ZCL) and zero-voltage capacitor (ZVC) energy and maintain a manageable voltage stress across the switch and diodes. All these functions are executed during the switch-transition interval, a small resonant interval during the switch turn-on and turn-off transitions. The length of the switch-transition interval is dependent on the switch speed, converter characteristics, and size of the soft-switching components. The rest of the time, the converter is operating in the normal PWM converter mode. It is assumed that the snubbers do not change the PWM converter operation except during the small switch-transition intervals at turn on and turn off.

The main requirement of the turn-on snubber is to slow the switch current rise time. This is done by the insertion of ZCL's, Lr, into proper locations of the circuit. However, these ZCL's will store energy that must be recovered ultimately to the load R or the voltage source V_g to maintain lossless operation. This stored energy comes from two sources, the reverse recovery current of diodes D, and the PWM converter current from filter and/or energy transfer inductors L. In both cases, the snubber circuit must provide a conduction path when a diode D_i or a switch S turns off. If no path is provided, either device may be destroyed by a voltage spike. Since an inductor stores its energy in the form of current, which can increase converter conduction losses, it is desirable to transfer the ZCL's energy to a VSD as soon as possible. Therefore, the energy recovery from the reverse recovery current of the diode should be performed as soon as the diode recovers. The recovery circuitry should also maintain a manageable voltage stress across the switch and diodes.

The main task of the turn-off snubber is to slow the switch voltage rise. This is done by the insertion of ZVC's Cr into the circuit. These capacitors will accumulate energy that must transfer to the load or the voltage source before the next turn-off interval. Because it is a passive circuit, this energy must be recovered when the switch S is turned on.

C. Zero-Current Turn On of the Active Switch

The following property first describes that inductors need to be placed in every loop containing the switch of a hard-switching PWM converter so that the active switch current is forced to rise slowly at turn on. As mentioned before and detailed later, additional components are added to manage the ZCL's energy and provide soft turn off of the switch. However, these components must not disrupt the zero current turn-on characteristic. Therefore, the second part of the property describes the topological and operating characteristics of the passive soft-switching converter so that zero current turn on is ensured.

Property 1: Zero-Current Inductor Placement: From the underlying PWM converter, a set of Lr is placed in all loops with S that do not contain an inductor. From the formed soft-switching topology, there exists a cutset which contains the switch S, a nonempty subset of Lr, and a subset of $(L \cup Ls \cup Ds)$, such that in the vicinity of the time that switch S is turned on, the current through any diodes in the cutset is zero.

Proof: The switch S current can be found by applying Kirchhoff's current law to the cutsets defined above

$$i_S = f_{Lr}^T i_{Lr} + f_L^T I_L + f_{Ls}^T i_{Ls} + f_{Ds}^T i_{Ds} \qquad (1)$$

where terms $f_L^T I_L$ are for the hard-switching PWM elements with the rest representing soft-switching elements.

Then, since the diode currents are also zero as given, the switch current S at turn on is given by

$$i_S(0^-) = f_{Lr}^T i_{Lr} + f_L^T I_L + f_{Ls}^T i_{Ls} = 0. \qquad (2)$$

Since $I_S(0^-) = 0$, then $I_S(0^+) = 0$ because the switch current is solely dependent on inductor currents and zero current turn on is achieved. This completes the proof. □

There are several reasons for the inclusion of the following corollary that describes the elements in the loops that Lr are inserted. Using this corollary, the voltage imposed across Lr when the switch turns on is described and later used to prove Property 2. Additionally, this corollary is used in the synthesis procedure given in Section III to determining the minimum number of ZCL's needed for soft switching.

Corollary 1: Zero-Current Inductor Loops: Each Lr_i makes a loop with S, a nonempty subset of D, and a nonempty subset of $(V_g \cup C)$.

Proof: From Property 1 and Assumption A4, Lr can be inserted in loops that contain switch S and any other hard-switching elements except L and R. This completes the proof. □

As a result of Corollary 1, Kirchhoff's voltage law is used to give the voltage relationship between the switch S and the other elements in the ZCL loop

$$V_S = f_g^T V_g + f_C^T V_C + f_D^T V_D + f_{Lr_i}^T V_{Lr_i}. \qquad (3)$$

Although other loops are possible, it is assumed that the diodes in the chosen loop are conducting at the moment that S turns on. Consequently, the voltage across the diodes $f_D^T V_D$ are zero and because the switch voltage is also zero (3) becomes

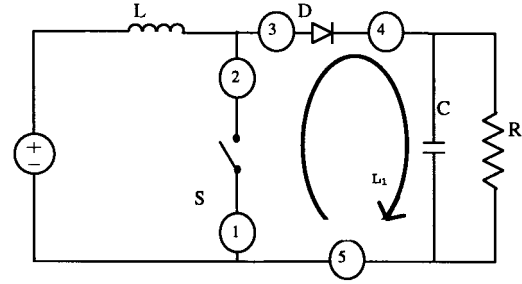$$0 = f_g^T V_g + f_C^T V_C + f_{Lr_i}^T V_{Lr_i}. \qquad (4)$$

Fig. 1.   ZCL locations for boost converter.

The inductor voltage can be solved as follows:

$$f_{Lr_i}^T V_{Lr_i} = -\left[f_g^T V_g + f_C^T V_C \right] = -V_{\mathrm{dc}}. \qquad (5)$$

This is the voltage imposed across the ZCL during zero current turn on of the switch. For hard-switching converters, V_{dc} represents the off-voltage stress of the switch as given in [28].

Using Property 1, the possible placements of the ZCL can be found for a given hard-switched topology. For example, Fig. 1 shows a boost converter with possible locations of the ZCL's shown in circles. Until now, only locations 2 and 3 have been proposed for lossless passive soft-switching boost converters [1], [5]–[9]. However, locations 1 and 4 are viable new placements of the resonant inductor. Although location 5 is new and will provide zero-current turn on of S, it will adversely affect the load voltage and feedback control circuitry. Therefore, only locations 1–4 are proper. In any case, one can see the ease of locating possible inductor locations by following Property 1.

D. Energy Management for Zero-Current Inductors

When the diode turns off, to minimize conduction losses, energy collected in the ZCL from the reverse recovery current of a diode should be discharged.

When the active switch turns off, the ZCL energy has several transition variations depending on the inductor's topological location. The most obvious case is when the ZCL is inserted in a branch containing a switch. In this case, when the switch turns off, the inductor energy (i.e., current) must return to zero to minimize conduction losses. When the inductor is inserted in a diode branch that conducts complementary to the switch, the inductor must be charged at switch turn off. Finally, if the inductor is inserted in a nonswitch or nondiode branch (e.g., next to the energy transfer capacitor in a Cuk converter), the inductor will be discharged and then charged at switch turn off. In all these cases, an alternative conduction path must be provided to control (i.e., charge or discharge) the ZCL energy and eliminate large voltage spikes. The following property describes how this energy is controlled.

Property 2: Management of Inductor Energy at Either Switch or Diode Turn Off: A nonempty subset of Ds and a VSD is placed to form a loop with Lr_i. The polarity of the VSD is such that when Ds is conducting, it imposes an opposite voltage polarity across Lr_i with respect to $-V_{\mathrm{dc}}$. The polarity of Ds blocks the VSD voltage when $V_{Lr_i} < V_{\mathrm{VSD}}$.
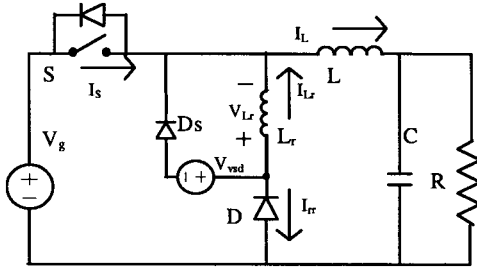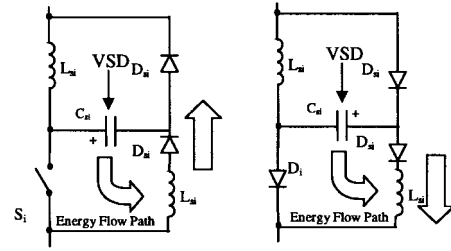
Fig. 2. Conceptual energy management example.

Fig. 3. Examples of recovering Cs_i energy.

Proof: Because the VSD imposes an opposite voltage polarity across the inductor with respect to $-V_{dc}$, the inductor voltage is clamped to either $-V_{dc}$ or V_{VSD} during the switch-transition interval and is zero during the normal PWM period. This allows "voltage second balance" and manages its energy. From Assumption A3, in one voltage polarity, the magnitude of the inductor voltage cannot be larger than V_{dc}. Since the switch in the loop can only block voltage in one direction, if $|V_{Lr_i}|$ equals V_{dc}, the diodes D and the switch's antiparallel diode around this loop will conduct and clamp V_{Lr_i}'s voltage. By the same reasoning, for the opposing voltage polarity, Ds will conduct and V_{VSD} will clamp the V_{Lr_i}'s voltage when its voltage equals V_{VSD}. This completes the proof. □

Fig. 2 gives a conceptual example of Property 2 with a buck converter, and it will be used to describe how the inductor voltages are clamped during the switch transition intervals. When S is turned off, diode Ds will conduct and the inductor voltage V_{Lr} will be clamped to V_{VDS}. Diode Ds will continue to conduct until the I_{Lr} current is charged above I_L (Ds will have some recovery current). When diode Ds recovers, since I_{Lr} is greater than I_L, it must flow through the antiparallel diode of switch S and diode D. V_{Lr} is then clamped to $-V_{dc}$ (i.e., $-V_g$). When S turns on, $V_{Lr} = -V_{dc}$ and the I_{Lr} current will decrease to $-I_{rr}$ where the diode D recovers. At this point, Diode Ds conducts and once again clamps V_{Lr} to V_{VDS}. Diode Ds and the VSD ensure that both the inductor energy is managed and the voltage stress across the switch and diode are controlled.

Two important results from Property 2 deal with switch implementation and switch voltage stress. The first observation is that converters which need bidirectional voltage switches cannot passively recover the inductor energy. These converters have loops defined by Corollary 1 where the voltage around the loop changes polarity under different operating conditions (i.e., different duty ratios). Therefore, the VSD polarity cannot oppose $-V_{dc}$ under all conditions and consequently no longer can guarantee control of the inductor current. Another observation comes from (3), which shows that the voltage stress of the switch will be increased by V_{Lr_i} ($V_{Lr_i} \leq V_{VSD}$). This is often a tradeoff with passive soft-switching converters. They provide zero current turn on, but may increase the magnitude voltage stress of the converter. An exception of this observation will be shown with Property 4.

As inferred from Property 2, one management loop is needed for each inductor. However, more than one energy management loop may be provided and it may contain a subset of $(S \cup D)$. In this case, these loops are only effective for the turn off of diodes and switches not in the subset of $(S \cup D)$. The following more general treatment of Property 2 summarizes this observation.

1) Generalization of Property 2: Loops comprised of Lr, the nonempty subset of Ds, a subset of $(S \cup D)$, and a VSD can manage the inductor energy for the turn off of switches and diodes not in the subset of $(S \cup D)$. The polarity of the VSD is such that when Ds is conducting, it imposes an opposite voltage polarity across Lr_i with respect to $-V_{dc}$. Furthermore, the polarity of Ds blocks the VSD voltage when $V_{Lr_i} < V_{VSD}$.

Circuits that do not have a loop described by Property 2 are theoretically lossy but may still reduce a converter's overall losses. For example, [7] and [8] reduce the losses in the active switch, but contain no loops satisfying Property 2. Consequently, the reverse recovery current of the main diode will not be recovered and the voltage spike across this diode can be very large. If large or saturable inductors are used in these circuits then the amount of reverse recovery current may be small enough so that the energy lost is negligible.

For Property 2, the VSD may be a relatively *stiff* voltage device where the voltage does not change much from cycle to cycle. Under these conditions, the next two subsections describe how this can be achieved.

2) Realization of VSD by a Capacitor: Because the inclusion of an additional power source is inconvenient for most applications, VSD can be realized by a relatively large capacitor from the set $(Cs \cup C)$. This capacitor will accumulate energy from the ZCL each cycle. The energy accumulating in the capacitor also needs partial recovery each cycle to reach an equilibrium voltage. If the VSD is from the set C only, then as shown in [9] this capacitor can be a filter capacitor for some PWM converter topologies (modified buck, Cuk, modified Zeta). For these selected topologies, the capacitor energy transfers directly to the load resistor. Otherwise the energy can be recovered by inserting a second inductor and diode so that an L–C–D circuit is in parallel with the an active switch or diode as shown in Fig. 3. With this arrangement, when the active switch (diode) is conducting the capacitor is transferring the energy to the inductor. When the active switch (diode) turns off the inductor will transfer this energy to the input source, load or energy transfer capacitors. The size of the additional inductor should be valued so that the additional conduction loss of the switch or diode is small. However, as the inductor value is increased, the switch voltage stress becomes larger. In [9], an inductor is placed similar to Fig. 3(b) without the additional diode. Without this diode,
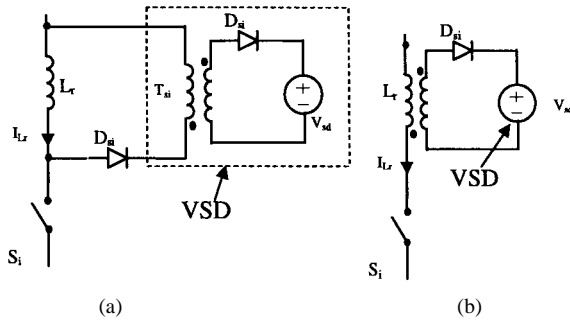
Fig. 4. Realization of VSD by transformer coupling: (a) forward transformer and (b) flyback transformer.

Fig. 5. Possible loops to achieve zero-voltage turn off of switch S.

current can reverse direction in the inductor and increase the capacitor voltage, rising the voltage stress of the switch and diode.

3) Realization of VSD by a Transformer Coupling: A forward or flyback transformer coupling can be used to realize a VSD as shown in Fig. 4(a) and (b) for a switch. The advantage of transformer coupling is that the ZCL energy transfers each cycle directly to the bus voltage or other voltage storage element in the converter. The forward transformer method has been used for many proposed converters [12]–[19]. The flyback transformer was suggested in [4] and [11]. For either transformer coupling methods, the transformer leakage inductance can cause large voltage spikes when the switch or diode is turned off. Therefore, all proposed circuits also use some additional voltage clamping action (either lossy or lossless) to control this leakage inductance energy. References [5], [7] and [10] show how the transformer can be coupled to the energy transfer inductor to realize a VSD.

E. Zero-Voltage Turn Off of Active Switches

The following property describes how a set of Cr along with snubber diodes Ds are added to the converter to achieve zero voltage turn off of the active switch. In addition, the property also describes what voltage must be across the Cr capacitors when the active switch is turned off.

Property 3: Zero-Voltage Capacitor Placement: A set of Cr is placed so S makes a loop with a nonempty subset of Cr, a subset of $(V_g \cup C \cup Cs)$, and a nonempty subset of Ds. The diodes Ds must be in the direction to conduct the switch current when S turns off. The electrical requirement of this loop is that when the switch S is opened, the voltage around the loop must still be zero volts the moment after turn off.

Proof: Kirchhoff's voltage law can be written in terms of elements in the loop defined in the property

$$V_S + f_g^T V_g + f_C^T V_C + f_{Cr}^T V_{Cr} + f_{CS}^T V_{CS} + f_{Ds}^T V_{Ds} = 0. \tag{6}$$

When the switch is turned off, $f_{Ds}^T V_{Ds}$ is zero because the diodes must conduct. For zero voltage turn off of s, the voltage stored in Cr_i must equal to the following equation and it completes the proof: □

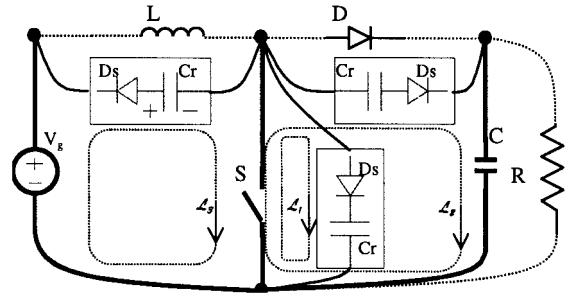$$f_{Cr}^T V_{Cr} = -\lfloor f_g^T V_g + f_C^T V_C + f_{CS}^T V_{CS} \rfloor. \tag{7}$$

The snubber components (Cr, Cs, and Ds) that make up the loop satisfying Property 3 are defined as the *ZVC subcircuit*. The diodes Ds are necessary to prevent the energy in Cr from dissipating in the switch when it is turned on. The other elements in the loop are part of the underlying hard-switching topology. The following corollary aids in locating the possible placements of the ZVC subcircuit locations for the synthesis procedure described later.

Corollary 2: Zero-Voltage Capacitor Subcircuit Placement: Every zero-voltage capacitor subcircuit represents a element that creates a loop from the largest connected subgraph that contains the switch S and a subset of $(C \cup V_g)$

As an example of Property 3, the boost converter in Fig. 5 shows the three different loops possible for the active switch S and the *ZVC subcircuits* shown in boxes. The subgraph as described in Corollary 2 is shown in bold, with each *ZVC subcircuit* creating a loop. Take loop $\mathcal{L}_3$ as an example and assume the switch has negligible parasitic capacitance. When the switch S turns off, the voltage across the capacitor Cr must equal the input voltage V_g so that the voltage around the loop equals zero volts. This ensures that the voltage across the switch increases from zero at the rate determine by the inductor current I_L and the value of capacitor Cr.

For passive soft-switching converters, the ZVC must be reset to a voltage satisfying the electrical requirement of Property 3. The reset occurs when the active switch turns on. Furthermore, the energy in Cr must ultimately transfer to the input voltage source or the load of the converter to ensure lossless operation. An L–C resonance is the most practical way to losslessly transfer this energy. Fig. 6 shows for a boost converter several different variations of L–C resonance that can be used. The reset circuits transfer the energy in Cr either to the input source or to another capacitor which completely or partially discharges to the load during each switching cycle (the additional circuitry is not shown). The active switch is on when the reset period starts and assume that the inductor current is zero. The Fig. 6 caption describes how the energy transfer occurs for each reset circuit. For the reset circuit shown in Fig. 6(a), the ZVC voltage V_{cr} initially equals the output voltage V_o. The circuit resets V_{cr} to zero voltage by transferring all of the energy to the snubber inductor Lr. At this moment, the energy in Lr transfers back to Cr until V_{cr} equals $-V_{cs}$. Then the energy is transferred to the parallel combination of Cs and Cr. Additional circuitry must transfer the energy in Cs to the load or the input. For the reset
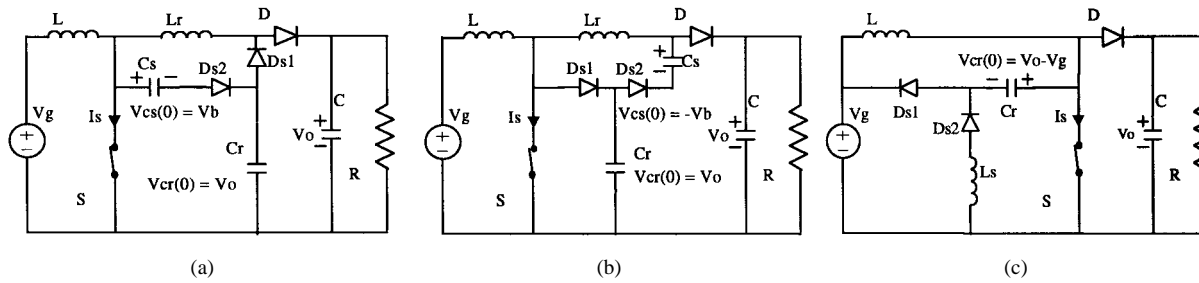
Fig. 6. Possible reset circuits for Cr. [Additional circuitry to recovery Cs energy not shown. To see the complete circuitry for (a), see Fig. 8(c) and for (b) see Fig. 9(c).] (a) Energy flow $Cr \Rightarrow Lr \Rightarrow Cr$ while $(V_{cr} > -V_{cs})$, and then $Lr \Rightarrow Cr$ and Cs. (b) Energy flow $Cr \Rightarrow Lr$ and $Cs \Rightarrow Cs$. (c) Energy flow $Cr \Rightarrow Ls \Rightarrow Cr$ while $(V_{cs} > -V_g)$, and then $Ls \Rightarrow V_g$ $(V_{cs} = -V_g)$.

circuit shown in Fig. 6(b), the circuit operates very similarly except the inductor energy continuously transfers to Cs as V_{cr} discharges to zero. For the reset circuit shown in Fig. 6(c), the energy in the capacitor transfers to the inductor, then back to the capacitor, but with a different voltage polarity. Once the voltage across the capacitor equals $-V_g$, it is completely reset and the rest of the energy in the inductor transfers to the voltage supply V_g. Fig. 6(c) will not completely reset unless the initial capacitor voltage is greater than V_g. This limits the operating range of the circuit.

These reset circuits add additional current stress to the active switch. The smaller the resonant interval is, the lower the conduction losses. The drawback is that to lower the resonant interval times, the size of the ZCL and ZVC are made smaller, which in turn increases switching losses. This tradeoff must be accounted for in a proper design. References [29] and [30] outline a simple method to minimize these additional conduction losses while ensuring soft switching.

F. Minimal Active Switch Voltage Stress

Property 4: Minimum Active Switch Voltage Stress: Minimum active switch voltage stress can be achieved in the case when all Lr are inserted adjacent to diodes D. In this case, a set of Ds can be inserted to provide the same current path from the active switch to the subset $(C \cup V_g)$ as the underlying PWM topology diodes D did. Additional circuitry ensures that the additional diodes Ds stop conducting before the active switch is turned on, so that zero-current turn on is realized.

Proof: The diode Ds ensures the voltage across the switch can be no larger than the stress for the underlying hard-switched PWM converter. ☐

In this property, the word *adjacent* means an connection exists between Lr_i and D_i that contains no other elements and the node between them has only two branches. The ZCL inserted into the circuit using Property 1 no longer allows the turn-off transition of the active switch to be clamped to a voltage supply through the diodes D. Therefore, to maintain the minimal voltage stress across the active switch, a separate snubber diode current conduction path must reproduce the original conduction path that the diode D allowed before inserting the inductor Lr. Although the switch stress is minimized, the voltage stress of the diodes D will still be higher with this method.

III. SYNTHESIS OF PASSIVE LOSSLESS SOFT-SWITCHING CONVERTERS

The topological and electrical properties from Section II simplify the synthesis of lossless passive soft-switching PWM converters. The synthesis process is described for a group of single active switch dc–dc converters and may be extended to converters with more than one active switch [22]. As can be derived from Properties 1 and 3, since there is one active switch, only one ZCL and ZVC can provide zero-current turn on and zero-voltage turn off of the active switch respectively. The locations of the turn-on inductor Lr and the turn-off capacitor Cr are described as the basic soft-switching topologies for a given underlying PWM converter. These basic topologies describe all passive soft-switching circuits with defined characteristics originating from a given underlying PWM converter. Additional lossless passive components need to be included to ensure the energy from the ZCL and ZVC is recovered. The number of additional components and their interconnections are virtually limitless. This paper proposes several circuit cells that can take each basic topology and realize a lossless soft-switching converter. The steps in the synthesis procedure are as follows.
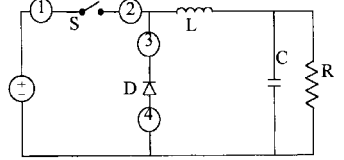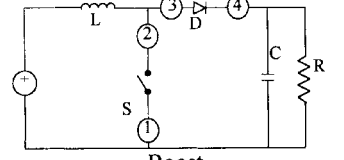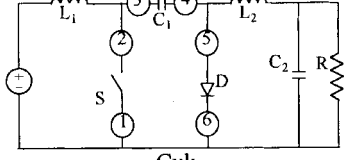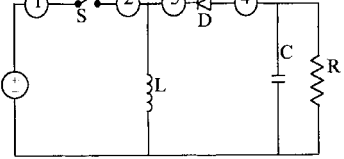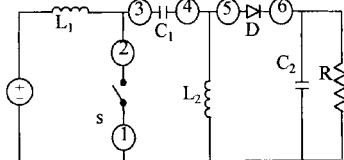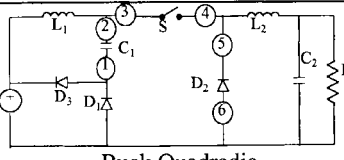
Step 1: Find the possible inductor locations satisfying Property 1. To use a minimum number of ZCL's, take the element intersection of all loops satisfying Corollary 1. The resulting set of elements is where the ZCL can be inserted to make a cutset with that element. The ZCL is not inserted into a branch with a supply V_{g_i} such that the common node between the supply and load capacitor is eliminated.

Step 2: For each inductor location of Step 1, identify the locations of the zero-voltage capacitor subcircuit using Property 3. Using the subgraph defined in Corollary 2, the number of locations can be found by defining the number of nodes in the subgraph on either side of switch S as N_1 and N_2, respectively. The number of capacitor subcircuit locations for one ZCL location is as follows:

$$C_{\text{loc}} = (N_1)(N_2). \tag{8}$$

These inductor and capacitor subcircuit locations make up the <u>basic</u> soft-switching topologies.

Step 3: For each <u>basic</u> topology, match one or more of the given circuit cells to the ZCL and ZVC subcircuit

TABLE I
BASIC SOFT-SWITCHING TOPOLOGIES FOR A GROUP OF DC–DC CONVERTERS

L_r locations	C_r Locations	Total
Buck	L1-1 L2-3 L3-3 L4-3	10
Boost	L1-1 L2-3 L3-3 L4-3	10
Cuk	L1-2 L2-3 L3-3 L4-6 L5-6 L6-6	26
Buck-Boost	L1-1 L2-3 L3-3 L4-3	10
Sepic	L1-2 L2-3 L3-3 L4-6 L5-6 L6-6	26
Buck Quadradic	L1-2 L2-1 L3-1 L4-2 L5-2 L6-2	10

locations to ensure the rest of the topological and electrical properties are satisfied.

Table I describes the basic topologies for a group of single switch dc–dc converters using Steps 1 and 2 of the synthesis procedure. For each hard-switching converter, the reasonable ZCL locations are shown. For each ZCL location, the number of possible ZVC subcircuits is listed. For example, ZCL location one of the boost converter, labeled L1, has only one ZVC subcircuit placement. Therefore, the table entry for this location is L1-1. The total number of basic topologies is also listed for each converter.

Once a basic topology is identified, one or more circuit cells are used to provide the additional circuitry to satisfy all the properties. Fig. 7 shows two circuit cells that satisfy the pertinent turn-on and turn-off properties and provides minimum voltage stress across the active switches (Property 4). Among
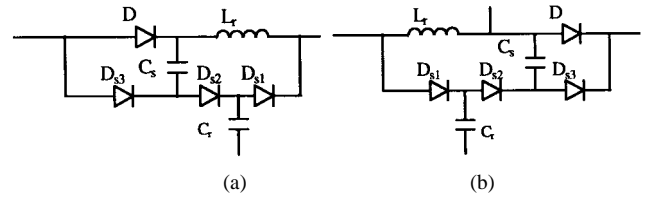

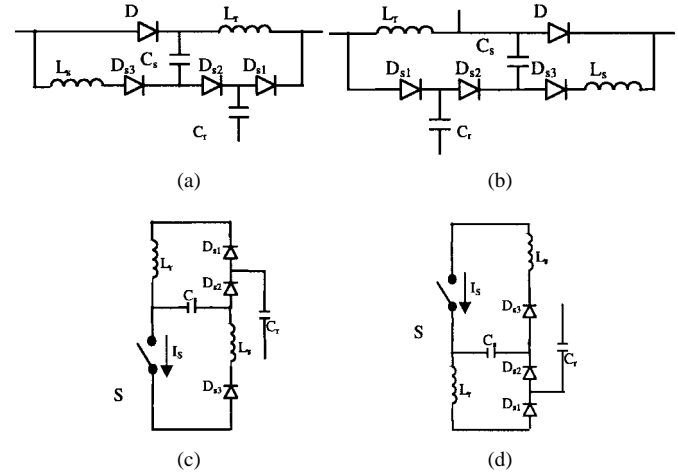Fig. 7. Minimum voltage stress circuit cell. These cells satisfying Property 4. (a) Cells I and (b) II.

Fig. 8. Nonminimum voltage stress circuit cells. These cells use a capacitor to reset inductor Lr. (a) Cell III. (b) Cell IV. (c) Cell V. (d) Cell VI.

them, cell I is new and cell II can be used to create a soft-switching boost converter shown in [6]. In the circuit cells, Lr and Cr are the ZCL and ZVC to satisfy Properties 1 and 3. Ds_1 and Cr make up the ZVC subcircuit. Lr also transfers the energy in Cr to Cs. Cs recovers the energy in Lr (Property 2) and Cr (Property 3). Diodes Ds_1, Ds_2, and Ds_3 transfer the energy in Cs to the load or energy transfer capacitor each switching period and satisfy Property 4. Fig. 8 shows four circuit cells (i.e., cells III–VI) that satisfy the pertinent turn-on and turn-off snubber properties, but do not maintain the minimum voltage stress across the switch (Property 4 not satisfied). For these cells, Cs is a relatively large capacitor and stores the inductor Lr and capacitor Cr energy from cycle to cycle. Elements Cr, Cs, and Ds_2 comprise the *ZVC subcircuit*. Ls is relatively large and transfers the energy in Cs to a subset of $(C \cup V_g)$. Cells III and IV can be used to create converters similar to ones presented in [9], however, cells V and VI are new. All cells in Figs. 7 and 8 become just turn-on snubbers by removing the capacitor Cr and a diode Ds_1. Cells V and VI become just turn-off snubbers by not placing inductor Lr into a loop satisfying Property 1.

Since Cells I and III (also Cells II and IV) can be used in identical locations, different applications will determine which cells are more suitable. Cells I and II minimize voltage stress across the main switch, however, their soft-switching range can be limited compared to the other circuit cells (III–VI). The nonminimum voltage stress circuit cells, Cells III–VI add stress to the main switch. The benefit to these cells is that, in comparison to Cells I and II, with the same size Lr and Cr their soft-switching range is substantially extended. Detailed
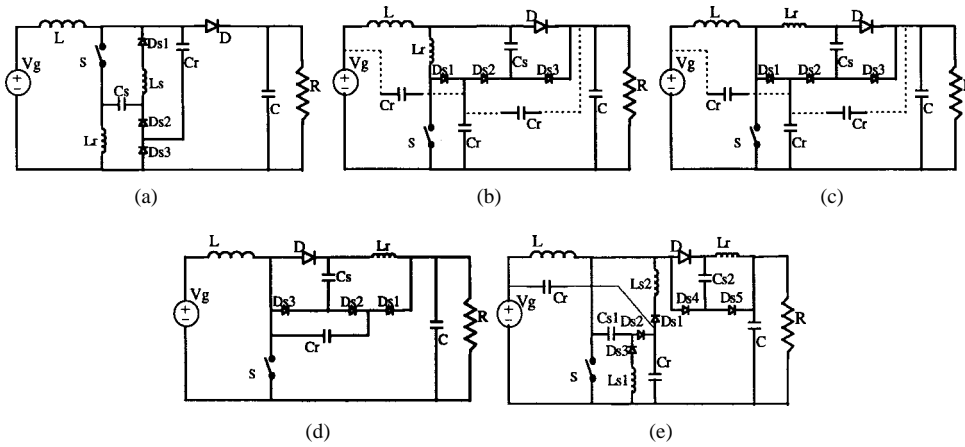
Fig. 9.   Synthesis results for the boost converter. Locations (a) L1-1, (b) L2-3, (c) L3-3, (d) L4-1, and (e) L4-2.

operating stages and simple design procedures for the choice of the resonant elements in these cells are shown in [29] and [30].

Most basic topologies require only one circuit to provide complete soft switching. However, a few basic topologies must use two circuit cells, one for a turn-on snubber and one for a turn-off snubber. Cell V needs a slight modification to work as a turn-off snubber when realizing two basic topologies of the Cuk and Sepic converters and one basic topology of the buck quadratic converter. For these topologies, the energy transfer capacitor C is inserted into the branch containing Cs so it makes a cutset with Cs.

Fig. 9 shows the synthesis procedure results for the boost converter. It shows a set of soft-switching circuits, one for each basic topology. Each circuit provides both zero-current turn on and zero-voltage turn off of the active switch. Seven of the ten circuits provide the active switch with the same voltage stress as the underlying PWM converter (Property 4). Fig. 9(a) shows the circuit created using inductor location L1 and the circuit cell VI. Fig. 9(b) shows three circuits created using inductor location L2 and the circuit cell II. Each different capacitor Cr connection creates a different ZVC subcircuit location. Fig. 9(c) shows three circuits created using inductor location L3 and uses circuit cell II. Here, the circuit cell is inserted into the converter slightly differently to adjust for the different inductor location. Fig. 9(d) shows one circuit created using inductor location L4 and cell I. No other placements of the capacitor subcircuit are possible with this circuit cell. Therefore, Fig. 9(e) shows the additional two ZVC subcircuit locations for inductor location L4. These locations require two circuit cells. The turn-on snubber uses a modified version of Cell I (no Cr and Ds_1) and the turn-off snubber uses Cell V.

IV. A NEW SOFT-SWITCHING CUK CONVERTER

From the synthesis procedure, a new soft-switching Cuk converter shown in Fig. 10 was derived. This circuit has the ZCL in location 6 and uses cell I. The operation of the circuit can be understood with the aid of the properties and the theoretical waveforms in Fig. 11. Assume that diode D is conducting and the MOSFET switch is turned on at t_0. Because of Property 1, the inductor current I_{Lr} will decrease
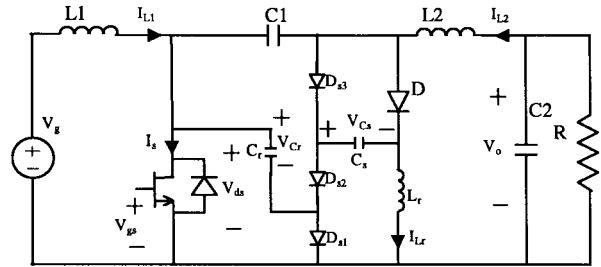

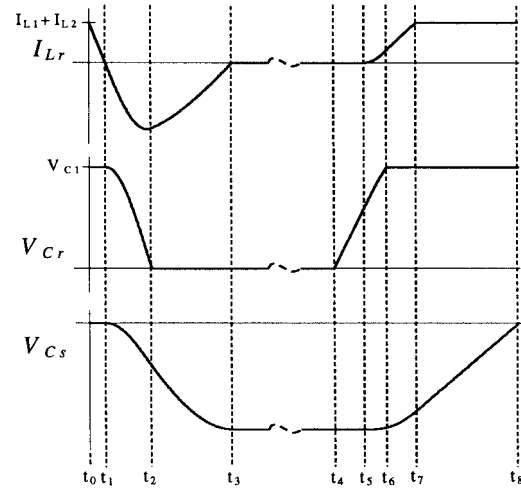Fig. 10.   A new lossless passive soft-switching Cuk converter.

Fig. 11.   Theoretical Cuk converter waveforms.

allowing the switch current to rise slowly until it reaches the sum of the currents in L1 and L2

$$I_S(t) = \frac{V_{C1}}{Lr}t. \qquad (9)$$

When I_{Lr} equals zero, the diode D will start to recover. Then the diode D recovers and turns off at t_1 (an ideal diode is assumed in Fig. 11). Without capacitor Cr, when the diode D turns off, the energy stored in Lr from the reverse recovery current would be controlled by the loop containing diodes Ds_1 and Ds_2 and capacitor Cs (Property 2) until it returns to zero. However, as it is, inductor Lr resonates with Cr and Cs through Ds_2 until Cr resets to zero volts at t_2. This ZVC
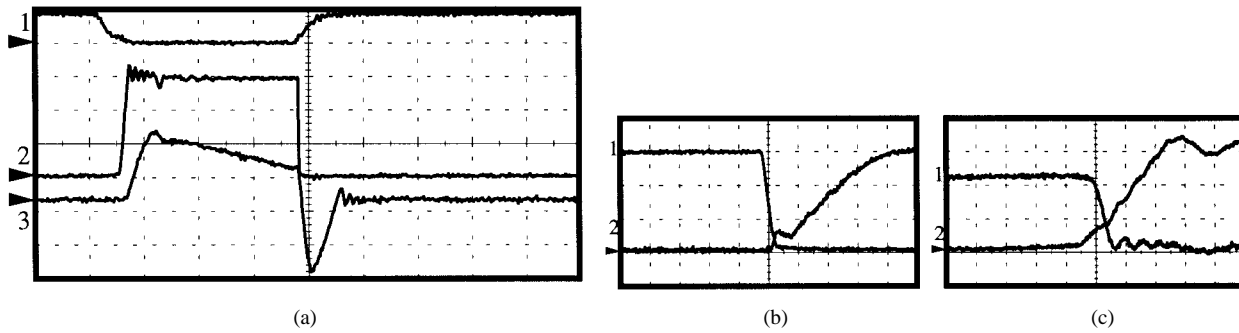
Fig. 12. Experimental waveforms for Cuk Converter. (a) Switching cycle. 1: V_{gs} 20 v/div; 2: V_{ds} 50 v/div; 3: I_{Lr} 2 amp/div; horizontal scale: 1 us/div. (b) Switch turn on. 1: V_{ds} 50 v/div; 2: I_S 2 amp/div; horizontal scale: 50 ns/div. (c) Switch turn off. 1: I_S 2 amp/div; 2: V_{ds} 50 v/div; horizontal scale: 50 ns/div.

reset has the same resonant characteristics as the circuit shown in Fig. 6(b) and satisfies the electrical requirement of Property 3. Then the energy in Lr is controlled by the loop defined by diodes Ds_1 and Ds_2 and capacitor Cs until it returns to zero at t_3. When the switch turns off at time t_4, the ZVC subcircuit (Cr and Ds_1) will allow the switch to turn off with a slowed voltage rise (Property 3) until it reaches V_{C1}-V_{Cs} at t_5. Then both diodes Ds_1 and Ds_3 start conducting, and the current in Lr will increase slowly. This stage is usually very short and ends when V_{Cr} reaches V_{C1} at t_6. At this point, Ds_1, Ds_2, and Ds_3 start conducting, clamping the switch voltage to V_{C1} (Property 4), and the Lr inductor current is controlled by the loop defined by Cs and diodes Ds_1 and Ds_2 (Property 2). Once the inductor current reaches the sum of L1 and L2 currents at t_7, diodes Ds_1 and Ds_2 stop conducting. Diode Ds_3 will continue to conduct until the Cs voltage returns to zero and then diode D will conduct at t_8. To ensure diodes Ds_1, Ds_2, and Ds_3 completely turn off, there must be enough energy stored in Cs at t_3. This energy comes from the resonant reset of Cr and the reverse recovery current of D. These design parameters are beyond to scope of this paper and are addressed in [29].

Experimental waveforms of the new soft-switching Cuk converter are shown in Fig. 12 and verified theoretical operations. The experimental circuit operated with the following parameters: $Fs = 100$ kHz, $V_g = 50$ V, $V_o = 100$ V, $P_{out} = 100$ W, $Lr = 4$ uH, $Cr = 5$ nF, and $Cs = 30$ nF. Fig. 12 shows the experimental waveforms. Fig. 12(a) shows the switch voltage and the I_{Lr} current. Notice that the voltage stress across the switch is still 150 V, the same as the underlying PWM converter. When the switch turns on, the inductor Lr resets the Cr capacitor voltage to provide zero-voltage turn off. Fig. 12(b) shows how Lr slows the switch current at turn on. The small current hump at the start is attributed to parasitic diode Ds_1 capacitance that must be charged. Fig. 12(c) shows how Cr slows the switch voltage rise at turn off.

V. CONCLUSION

This paper studies properties common to all lossless passive soft-switching converters that use components listed in Section II-A and requirements cited in Section II-B. These properties ease the development of a synthesis procedure for the creation of new converters. For a number of ZCL

and ZVC subcircuits, a complete set of basic soft-switching topologies are defined for a given underlying hard-switched PWM converter. This set of basic topologies describes all passive soft-switching converters with defined characteristics for a given underlying hard-switched PWM converter. Additional circuitry then needs to ensure the energy stored in these passive elements is recovered. The possible number of circuits to achieve this result is almost limitless, however, they also have many common configurations. A set of circuit cells are then presented that can be used to synthesize families of soft-switching converters. As an example, ten soft-switching boost converters are given and one soft-switching Cuk converter was shown with experimental results.

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