Protection Circuit for High Power Amplifiers Operating Under Mismatch Conditions

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***Abstract* — A protection circuit is developed which protects transistors in the output stage of a High Power Amplifier against voltage breakdown as a result of mismatch. The circuit is applied in an S-band and X-band High Power Amplifier and measured under various mismatch conditions. The devices have been developed in the 6-inch 0.5 µm GaAs power pHEMT process (PP50-11) of WIN Semiconductors.**

***Index Terms*— MMICs, Power amplifiers, Protection.**

I. INTRODUCTION

In several applications High Power Amplifiers (HPA) are directly connected to antenna elements. The input impedance of such an antenna element depends on the environment and will not always be equal to the impedance for which the HPA was designed. This causes load-pulling of the HPA. Besides the reduced performance this load pulling could also damage the HPA or reduce the lifetime. An important source of power performance degradation in GaAs pHEMT devices is voltage breakdown [1]. This paper describes a protection circuit which protects the transistors in the output stage of an HPA against voltage breakdown. In the first place two test circuits were designed and analyzed. The first circuit was a DC test circuit, on which the operating principle was verified. The second test circuit consisted of the protection circuit connected to a single transistor. Finally the protection circuit was applied in an S-band and X-band HPA.

Protection circuits have been reported for silicon bipolar processes [2],[3] and GaAs HBT processes [4]. The application in a GaAs pHEMT process has not been seen before.

II. OPERATING PRINCIPLE

The operating principle of the protection mechanism is illustrated in Fig. 1. At the output transistors the maximum voltage is measured with a peak detector. The output voltage of this detector is compared against a reference voltage. If the measured peak voltage exceeds the reference level, the gain of the input stage is reduced. This reduces the drive level of the output stage. The output of the comparator is an error signal which represents the difference between the measured peak voltage and the reference voltage. The gain reduction of the first stage is a function of this error signal. This results in a continuous control loop that is stable at the level where the peak voltage equals the reference voltage. By applying the correct reference voltage the maximum peak voltage at the output transistors is controlled.

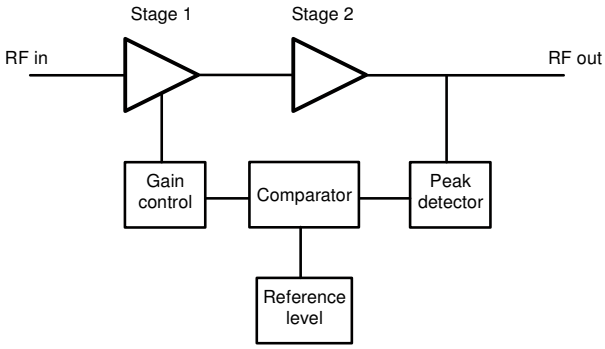

Fig. 1 Schematic representation of HPA with additional protection circuit.

The gain of the first stage is controlled by adjusting the bias level of the transistors. A more detailed schematic is given in Fig. 2. The peak voltage on the drain of one of the transistor in the output stage is measured by the peak detector which consists of diode D7, capacitor C1 and resistor R4. This resistor together with diode D1 through D6 and current source I2 also provide level shifting of the signal, such that it falls within the input voltage range of differential pair Q1 and Q2. When the measured peak drain voltage is low, the voltage on the gate of Q2 will be lower than the voltage on the gate of Q1, generated by resistive divider R1 and R2. In this case no current flows through Q2 and R3 and the output first stage bias voltage equals the nominal bias. At a certain peak drain voltage level the gate voltage of Q2 exceeds the gate voltage of Q1 and current will start to flow through R3. The voltage drop over this resistor causes the output first stage bias voltage to be lower than the nominal bias, resulting in a lower gain for the first stage.

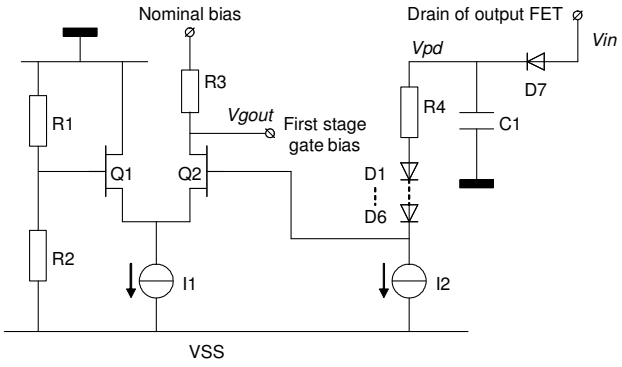

Fig. 2 Implementation of protection circuitry.

III. Measurement Results DC Test Circuit

The DC test circuit consisted of the protection circuit with a DC input at the peak detector. From this circuit the DC transfer function is measured. The result is given in Fig. 3. The input voltage Vin is the voltage at the input of the peak detector, which mimics a peaks drain voltage. The output voltage is a bias voltage that is adjusted for high measured voltages. It can be seen that the output bias voltage remains constant for an input voltage up to 16 V. Between 16 V and 18 V a transition is seen from -0.9 V to -2.7 V. At higher input voltages the output voltage remains constant.

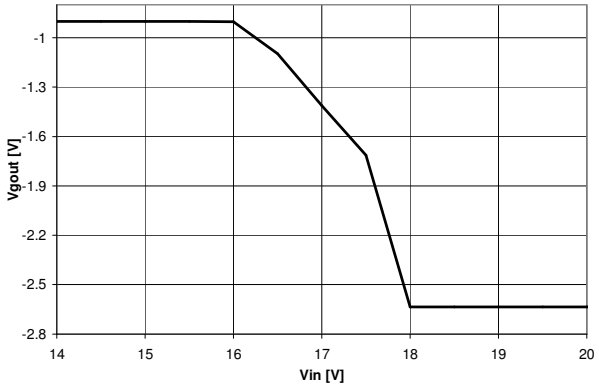

Fig. 3 Measured response of DC test circuit.

IV. Measurement Results RF Test Circuit

An RF test circuit consisting of an 8x175 µm pHEMT with a protection circuit connected to the drain was measured at different output loads. The measurements are performed at a source power of 19 dBm which correspond to a compression level of approximately 2.5 dB at the nominal output load. Fig. 4 gives the output voltage of the protection circuit as a function of measured output voltage of the peak detector for all applied loads. It is seen that the measurement point are all on a smooth line, which indicates that the response is driven by the drain voltage: the input and output power at which the circuit is activated is different for each load, however the peak voltage is equal.

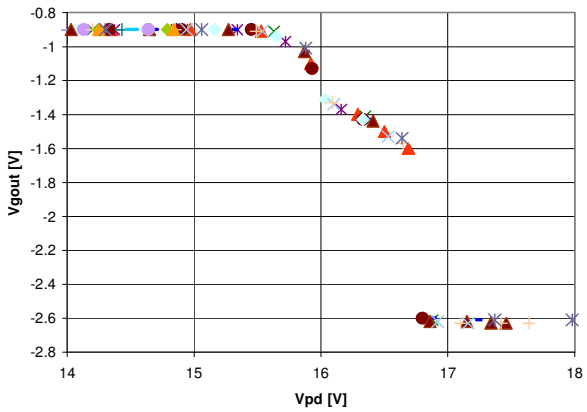

Fig. 4 Measured output voltage vs. measured peak voltage of RF test circuit, for different loads, Vd=8 V, Vg=-0.9 V, Ps=19 dBm, TA=25°C.

V. Measurement Results in S-band HPA

The clamp circuit was applied in a two stage S-band HPA. This HPA as well as an equal HPA without the protection circuit were measured at a VSWR of 1.5:1 with different phases. For these measurements the HPAs were mounted on Copper-Molybdenum carriers. The nominal bias voltages of the HPAs are generated by an active gate bias circuit which compensates for the threshold voltage variation. The measurements were performed under pulsed conditions at a source power which gives a gain compression of approximately 2.5 dB at a VSWR of 1:1. Fig. 5 shows the output power variation referred to the nominal output power of each amplifier at a VSWR of 1:1. From the results of the HPA without protection it can be seen that for certain load angles the output power is higher than at the nominal load. This can be explained by the fact the design was not optimized for output power, but a compromise between output power and efficiency was chosen. Furthermore the compression level may vary, something that cannot be observed from this plot. To interpret the measured results on the HPA with protection circuit, it is necessary to look at other measured parameters. However from this plot it is already seen that the maximum decrease with respect to the nominal output power is 1.2 dB, while no power increase is observed.

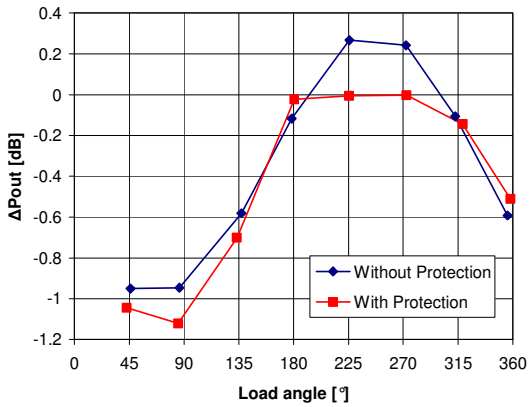

Fig. 5 Measured output power variation of S-band HPA vs. load angle, measured at Vd=8 V, T_A=25°C, VSWR=1.5:1, PRF=5 kHz, PW=10 µs.

In Fig. 6 for both HPAs the measured gate voltage variation of the first stage referred to the small signal gate voltage of each HPA is given. For the HPA without protection the gate voltage is higher than the small signal value for all load angles. This is caused by the negative gate current drawn by the output stage. This current flows through the internal resistance of the bias circuit, increasing the bias voltage of both stages, as illustrated in Fig. 7 in which the gate bias circuit is represented by an ideal voltage source with a series resistance. The negative gate current is caused by breakdown of the drain to gate junction of the output FETs and is higher as the drain voltage peaks are higher. This means that from the maximum gate voltage at load angles of 45° to 135° it can be concluded that the peak drain voltages are maximal at these load angles.

For the HPA with protection circuit an increased gate voltage is observed at phase angles between 180° and 360°. The reason is the same as for the HPA without protection. At phase angles between 45° and 135° a significant reduction of gate voltage is observed. This reduction is caused by the protection circuit, triggered by the measured peak drain voltage on the output stage which as found before is maximal for these load angles. This implies that the protection circuit effectively reduces the drain voltage peaks.

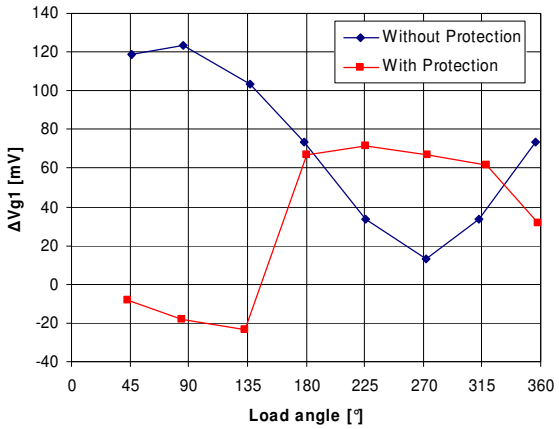

Fig. 6 Measured gate voltage variation with respect to small signal voltage of input stage S-band HPA vs. load angle, measured at Vd=8 V, T_A=25°C, VSWR=1.5:1, PRF=5 kHz, PW=10 µs.

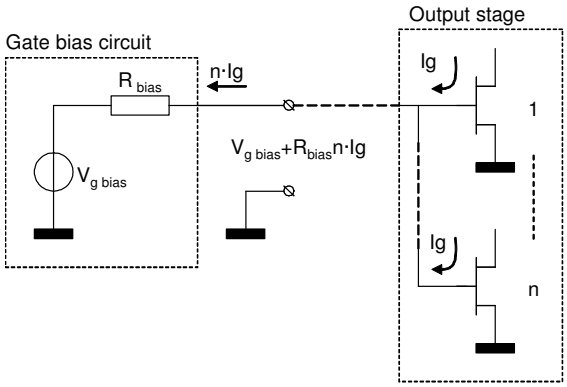

Fig. 7 Simplified representation of gate biasing showing that gate currents drawn by transistors in output stage affect output voltage of gate bias circuit.

The gate voltage of the first stage is reflected by the measured drain current of this stage, as shown in Fig. 8. This figure gives the drain current of the first stage, normalized to the small signal drain current.

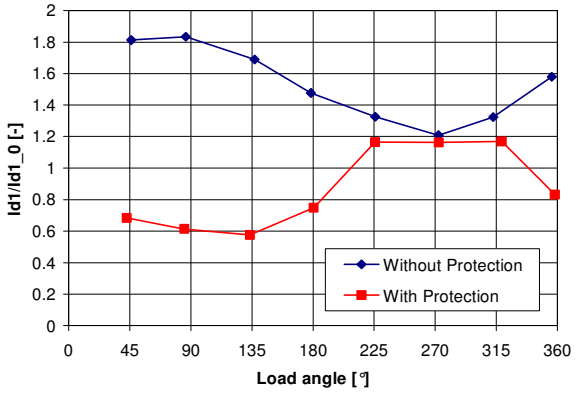

Fig. 8 Measured current increase with respect to small signal current of input stage S-band HPA vs. load angle, measured at Vd=8 V, T_A=25°C, VSWR=1.5:1, PRF=5 kHz, PW=10 µs.

In Fig. 9 the measured drain current of the output stage, normalized to the small signal drain current is shown. It is seen that the drain current has a global minimum at load angles between 45° and 90°. Since load variation results in a varying load line of the transistors in the output stage, drain current and maximum drain voltage are more or less exchangeable. A steeper load line will result in a higher drain current. A load which is less steep will result in higher peak voltages. This confirms that at load angles between 45° and 90° the voltage swing will have a maximum and the protection circuit has the largest effect in this region.

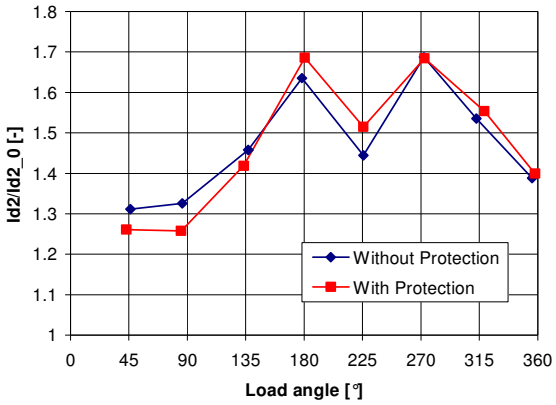

Fig. 9 Measured current increase output stage S-band HPA vs. load angle, measured at Vd=8 V, T_A=25°C, VSWR=1.5:1, PRF=5 kHz, PW=10 µs.

VI. Measurement Results in X-band HPA

A two stage X-band amplifier containing the protection circuit has been measured for VSWR values up to 3:1. The internal gate voltage of this X-band HPA is generated by use of a gate bias circuit similar to that in the S-band HPA. The measurements were performed on a device mounted on a Copper-Molybdenum carrier under pulsed conditions. The source power corresponds to the 1 dB compression power at VSWR=1:1. The first stage drain current referred to the current at VSWR=1:1 is shown in Fig. 10 for different VSWR values and load angles.

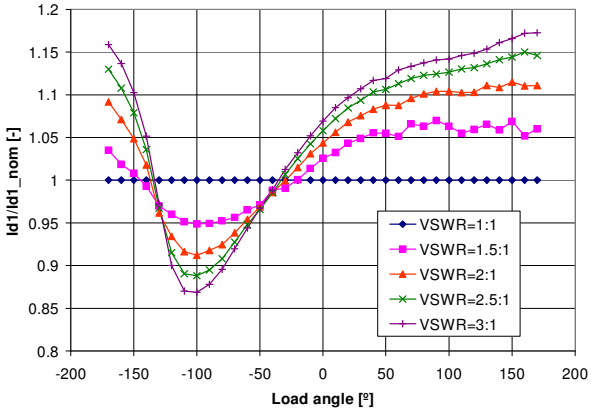

Fig. 10 Measured current increase input stage X-band HPA vs. load angle, measured at Vd=8 V, T_A=25°C, PRF=10 kHz, PW=10 µs.

For load angles between 20° and 170° the first stage drain current is limited by the protection circuit. It is within this range that the voltage swing in the output stage is maximal. This can be concluded from the second stage drain current as show in Fig. 11, which is minimal at these load angles.

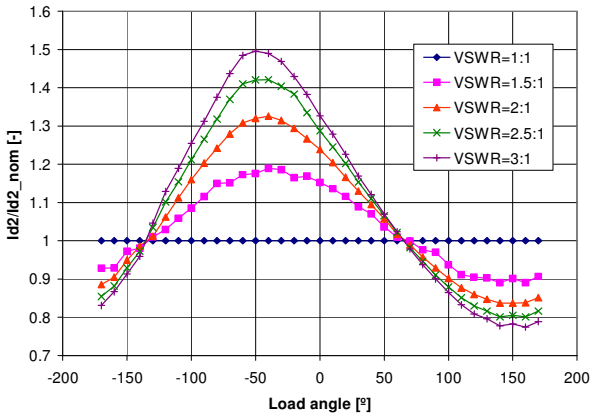

Fig. 11 Measured current increase output stage X-band HPA vs. load angle, measured at Vd=8 V, T_A=25°C, PRF=10 kHz, PW=10 µs.

VII. Conclusion

A circuit providing protection against voltage breakdown due to mismatch was designed and applied in an S-band and X-band HPA. The measurement results on the S-band HPA show that the effect on output power is small, while the measured internal gate voltage and drain currents indicate that the peak voltage on the transistors in the output stage is reduced. Also a significant decrease of first stage drain current is obtained which results in a higher efficiency and lower temperature. The measured drain currents in the X-band HPA confirms the operation in this device.

References

[1] Y. C. Chou *et al*, "Hot Carrier Effect in Power Performance in GaAs PHEMT MMIC Power Amplifiers", *Proc. IEEE IMS2005*, Long Beach, 12-17 June 2005.

[2] A. Scuderi *et al*., "A VSWR-Protected Silicon Bipolar RF Power Amplifier With Soft-Slope Power Control", *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 911–921, March 2005.

[3] A. Bezooijen *et al*., "Over-Temperature Protection by Adaptive Output Power Control", *Proceedings of the 36th European Microwave Conference*, Manchester, September 2006.

[4] K. Yamamoto *et al.*, "A 3.2-V operation single-chip dual-band Al-GaAs/GaAs HBT MMIC power amplifier with active feedback circuit technique," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1109–1120, Aug. 2000.