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Protection of insulated gate bipolar transistors against short circuit

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Abstract

Insulated gate bipolar transistors (IGBTs) are widely used in power electronic converters. Two IGBT gate drive circuits, capable of protecting the devices against short circuit by sensing their collector–emitter voltage, have been developed for low-voltage devices. One uses discrete components, while the other uses an IC drive MC33153. These circuits are simple, reliable and useful for practising engineers. Both the circuits are tested thoroughly for their ability to protect the devices against both types of faults, namely, hard switched fault (HSF) and fault under load (FUL), under different circuit conditions. The test results bring out the influence of DC bus voltage and fault inductance on the short-circuit transients. From this, a method can be arrived at for estimating fault inductance using device current and device voltage under fault. The overvoltage spikes due to shut down following fault detection are quite low. This vindicates the design of the low stray inductance bus-bar used. A simple gate drive circuit capable of short-circuit protection and a sandwich bus-bar with low parasitic inductance hold the key to improve the reliability of IGBT-based converters.

Keywords: Insulated gate bipolar transistors, short-circuit currents.

1. Introduction

Insulated gate bipolar transistors (IGBTs) are widely used in power electronic systems like uninterruptible power supplies (UPS), motor drives and active power filters. To make these systems rugged, the power devices used in them must be protected against short circuit. A fault may occur when a particular device is in conduction. This is termed as 'fault under load' (FUL). Alternatively, the device may turn on into a fault. This is called 'hard switched fault' (HSF). The device has to be protected against both kinds of faults. Fast switching devices like IGBTs cannot be protected by fuses, circuit breakers, etc. They can only be protected by timely fault detection, followed by quick shut down of the gate drive.[1–10] This must be done within the short-circuit withstand time (t_{SC}) of the IGBT, which is 10 µs for most devices.[11–15] Also, it must be ensured that no further drive is provided till the fault is cleared.

Any solution provided to improve the reliability of power converters must itself be simple and effective to be of any practical use. Hence different issues concerning short-circuit protection of IGBTs are discussed, and the ones of relatively higher significance are identified. Two simple IGBT gate drive circuits, having only the essential features of a fault protection scheme, are developed for low-voltage devices. These are tested thoroughly to check their effectiveness in protecting devices from both types of faults over a range of bus voltages and fault inductances.

2. Issues in short-circuit protection of IGBTs

The major aspects of the short-circuit protection of IGBTs are discussed in this section. Also, the essential features of a simple gate drive circuit are shown.

2.1. *Fault-sensing*

Sensing a fault is the primary step in short-circuit protection of a device. This can either be based on the device current[9–10, 16] or on the voltage drop across the device.[1–10, 16]

2.1.1. *Based on device current*

The drop across a resistor in series with the device is a good measure of the device current. However, the use of an external resistor makes the power-circuit layout clumsy. Certain new devices are becoming available with in-built series resistors.[16] Irrespective of the resistor used, either internal or external, the drop across it is quite low (a few 10s of mV). This low-magnitude signal is prone to noise problems. The protection scheme is very much sensitive to the layout of the drive circuit and its connection to the power circuit. Alternatively, a defined fraction of the device current is made to flow through a large resistance, internal to the power device or the device driver. The drop across this resistance is used for fault-sensing as in intelligent power modules and a few device drivers.[17–18]

A very recent technique for fault detection uses drop across the inductor between the emitter power terminal and its semiconductor contact inside the casing. The Kelvin emitter terminal (drive side emitter terminal) can be regarded as the semiconductor contact point itself. Thus the voltage drop between the power and Kelvin emitter terminals gives a measure of di/dt. This is integrated to get an estimate of the collector current, which is then used for protection.[9, 10] As this inductance is very low (only a few nanohenries), the voltage across it is also low. This makes fault-sensing prone to noise problems as earlier. Further, the use of integrator complicates the gate drive circuitry.

2.1.2. *Based on device voltage*

The on-state drop across an IGBT is low under normal conditions. In case of a fault, the device comes out of saturation, and the drop across it increases. This can be used to detect a fault. This method, using the collector–emitter voltage of the device, is known as 'desaturation technique'.

The collector–emitter voltage (v_{CE}) is convenient to use as far as the magnitude is concerned. The device current and the on-state drop are not proportional in case of an IGBT unlike in the case of a MOSFET. Besides, the drop also depends on the rate of rise of the device current. Doubts have been expressed in the literature regarding the detection of faults, especially soft faults with low di/dt, using this technique.[9–10] Hence, its effectiveness in fault detection must be determined by thorough testing.

2.2. *Fault current limiting*

To reduce the current in the event of a fault, the gate emitter voltage can be adjusted dynamically. It can be reduced below the normal level, but still above the threshold voltage to control

the fault current. Once reduced suitably, it must remain clamped at the same level till the gate drive is shut down. Several circuits have been reported in the literature for such a limiting of fault current.[2-6, 9, 10] Incorporation of fault current limiting increases the component count and the complexity of the gate drive circuitry. The performance of the drive circuit is quite sensitive to certain parameters in the fault current-limiting circuit.

2.3. *Shut down*

The gate pulse is shut down in the case of a fault. The shutdown leads to an overvoltage due to the large d*i*/d*t* and the parasitic inductance in the bus-bar. If in excess, this overvoltage can damage the device. Hence either the d*i*/d*t* or the parasitic inductance or both have to be reduced for this.

2.4. *Nondegradation of the normal operation*

The short-circuit protection mechanism, incorporated in the gate drive circuit, must not deteriorate the normal performance of the drive. There must be no nuisance trip. Also, conduction and switching losses of the device must not increase appreciably.

2.5. *Features of a simple short-circuit protection scheme*

While fault detection, safe shut down and nondegradation of normal performance are absolutely essential for any fault protection scheme, fault current limiting and gate clamping can be done away with for simplicity. From the discussion in Section 2.1, fault detection based on v_{CE} sensing is the simplest for the purpose. Such a simple short-circuit protection scheme is considered in this work. Two gate drive circuits with these features are developed. One of them uses discrete components, while the other uses an IC driver Motorola MC33153. These are presented in the next section.

3. Proposed IGBT gate drive circuits

The gate drive circuit-I uses discrete components for fault detection and protective action (Fig. 1). The gate drive signal, generated by the controller, first passes through an HP3101 optocoupler[19] for galvanic isolation, and then through a drive stage. The drive stage provides adequate drive for proper switching of the device. This stage consists of buffers and a transistor bridge. The on- and off-state gate-emitter voltages are $V_{GE(ON)} = +15$ V and $V_{GE(OFF)} = -15$ V, respectively. The gate resistances are $R_{G(ON)} = R_{G(OFF)} = 22\ \Omega$ for Semikron SKM50GB-123D as prescribed in the device data sheet.[11]

A fast recovery diode (MUR1100E) and an LM339 comparator are used for fault-sensing. A reference (desaturation voltage) of 6.2 V is provided to the comparator. Whenever the drop across the device is greater than 6.2 V, the comparator output goes low.

The output of the comparator and the isolated gate drive signal are used to generate status signal. This signal is high under normal condition, and is low under fault. The status signal is held high as long as the gate drive is low, and also for t_{BLANK} seconds (blanking time) after the low-to-high transition of the drive signal to allow for the normal turn-on operation. The

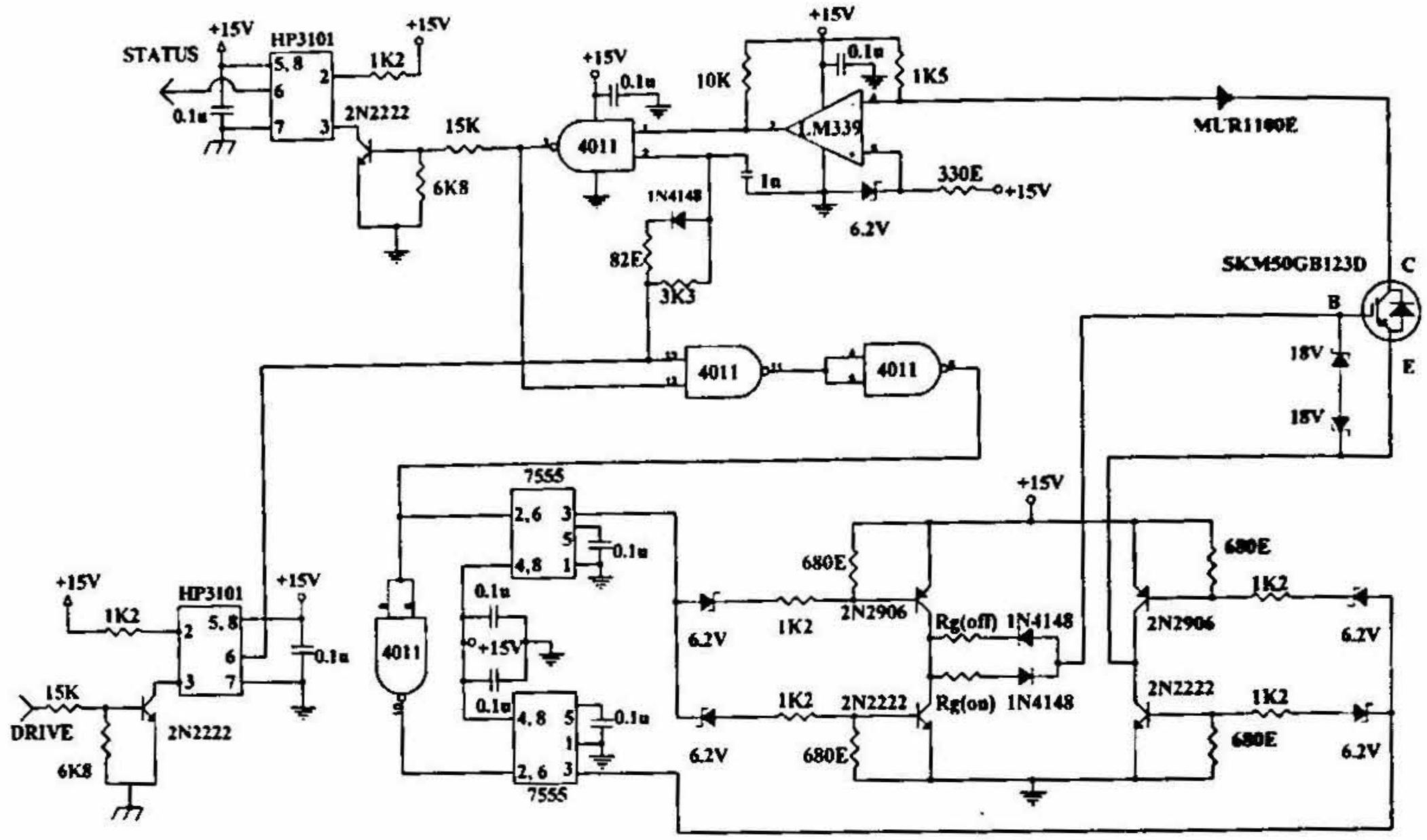


FIG. 1. IGBT gate drive circuit-I: discrete component version.

blanking time must be sufficiently larger than the worst case turn-on time to avoid nuisance trip. When the gate drive is high, the status signal goes low whenever the comparator output goes low after the end of blanking time. This status signal is ANDed with the drive signal on the isolated side. Thus, a fault is detected and the drive is shut in the case of a fault. The status signal is fed back to the central protection card or the controller through another HP3101 opto-coupler. This signal is useful to prevent gate pulses from being fed further to the device till the clearance of the fault.

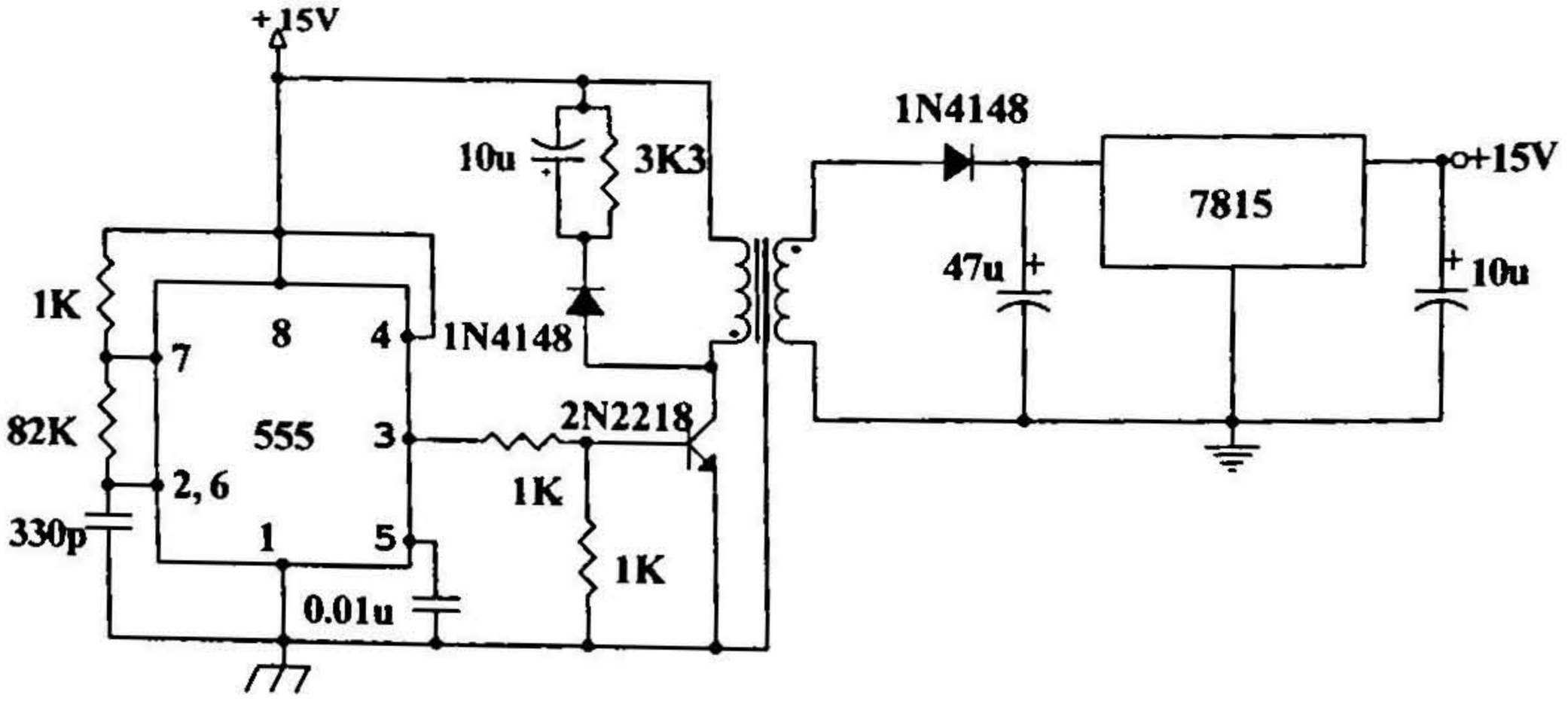


FIG. 2. Isolated power supply for gate drive circuit-I.

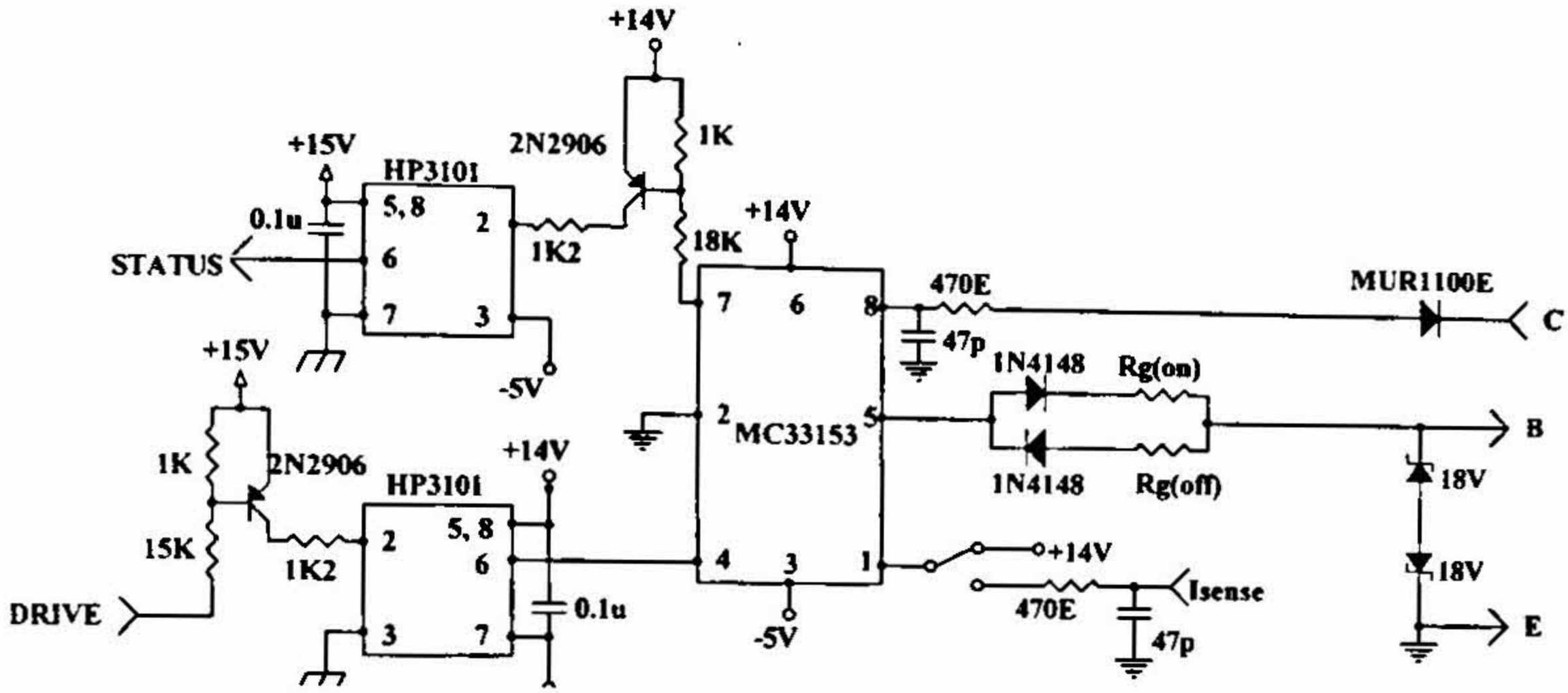


FIG. 3. IGBT gate drive circuit-II: MC33153 version.

The power supply for the isolated side shown in Fig. 2 consists of a flyback converter[20–21] with a linear regulator at the output for voltage regulation. The gate drive circuit-II, shown in Fig. 3, uses HP3101 for isolating the gate drive. However, instead of discrete components, this circuit uses an IC driver MC33153 for fault-sensing, providing blanking time, and shutting down the gate pulse and generating a suitable status signal in the event of a fault. The status signal is also isolated using HP3101 as in the earlier case. The IC driver MC33153 has an absolute maximum voltage swing of 20 V. Hence, the swing between $V_{GE(ON)}$ and $V_{GE(OFF)}$ must be less than 20 V. Therefore, $V_{GE(ON)} = +14$ V and $V_{GE(OFF)} = -5$ V are used in this circuit.

The isolated side of circuit-II requires a bipolar supply. The power supply consists of a flyback converter with bipolar output and two linear regulators (Fig. 4).

4. Testing for protection against short circuit

Both the gate drive circuits are tested for protection against HSF and FUL (Figs 5a, 5b). The IGBT used is SEMIKRON SKM50GB123D, which is a 50 A, 1200 V, half-bridge module.

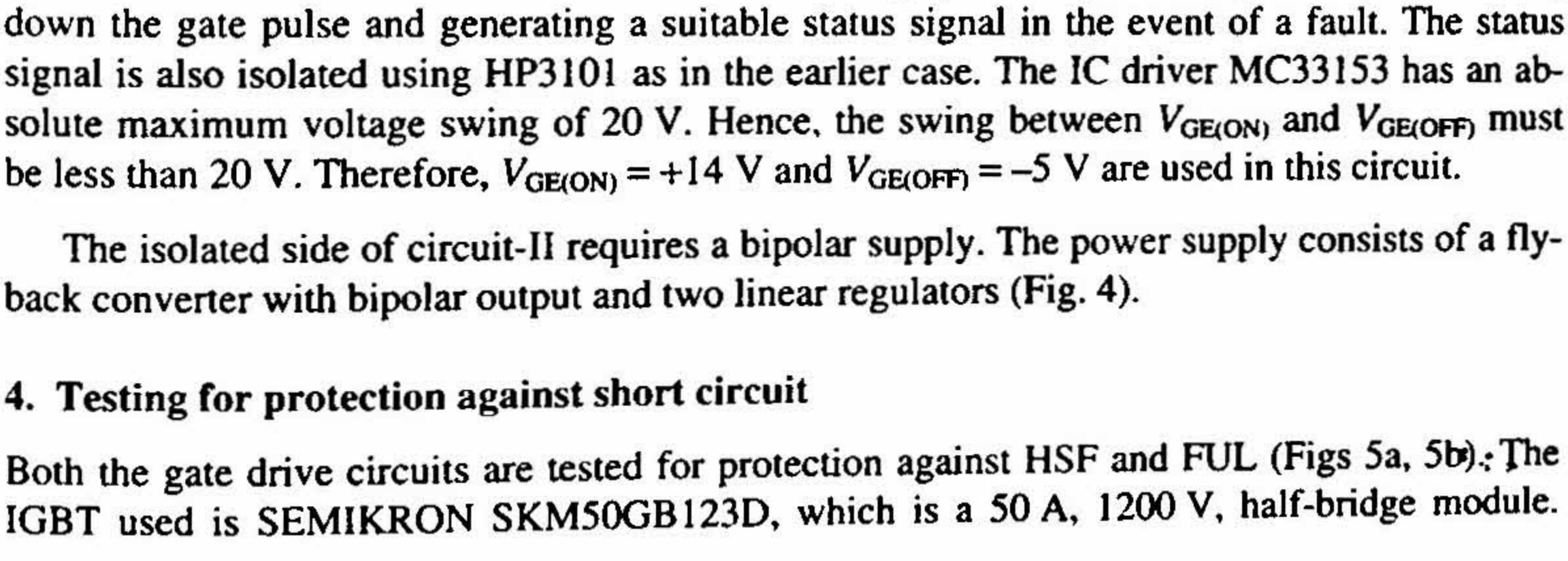
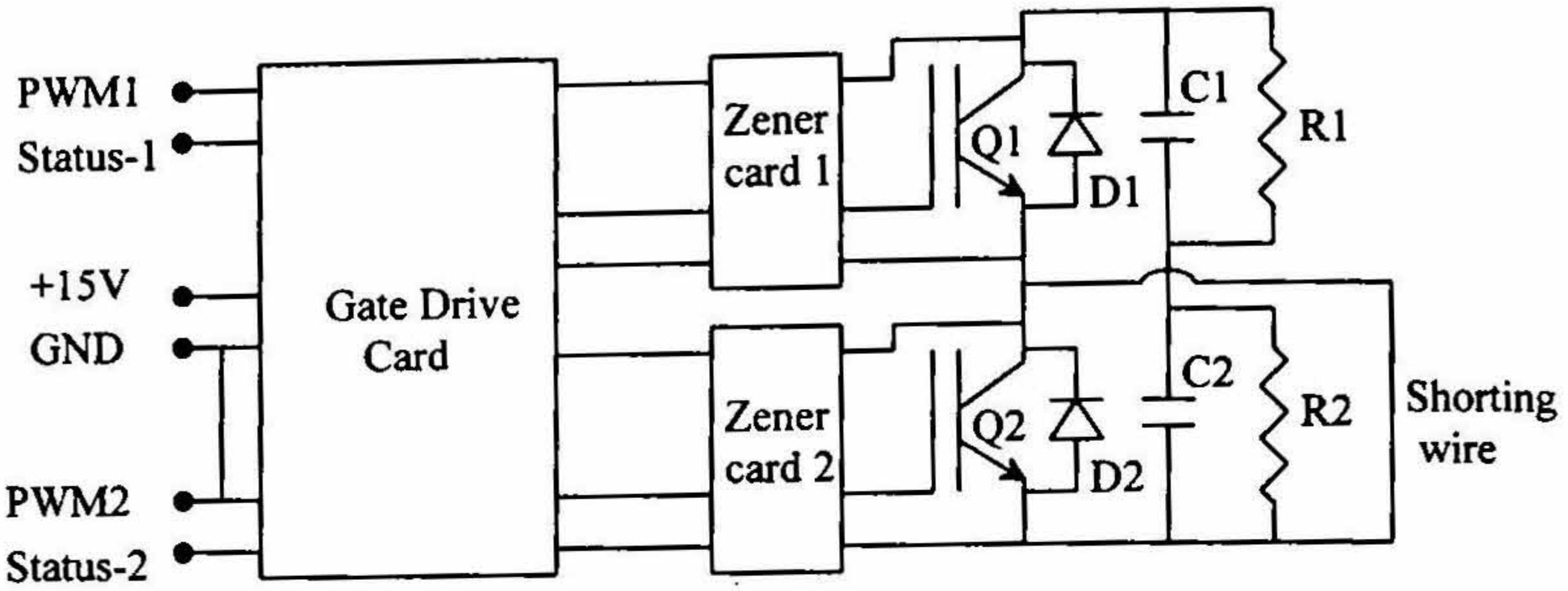
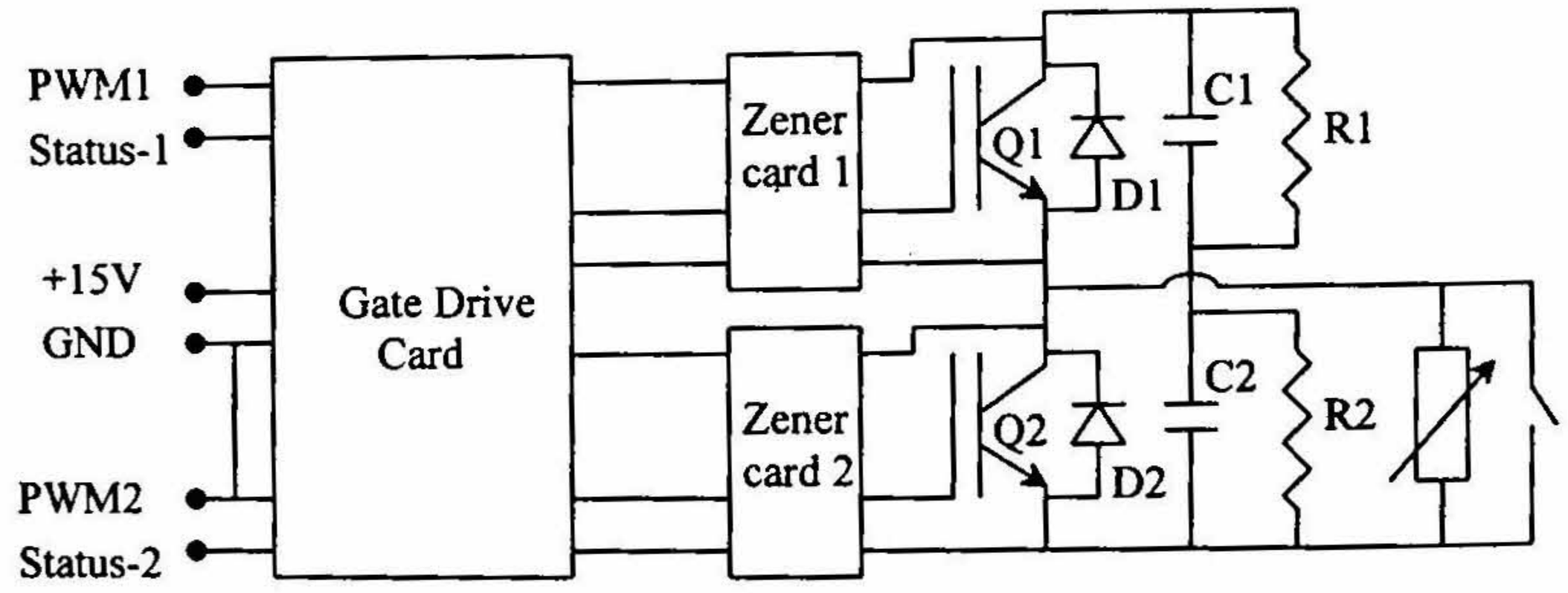


FIG. 4. Isolated bipolar power supply for gate drive circuit-II.



(a)



(b)

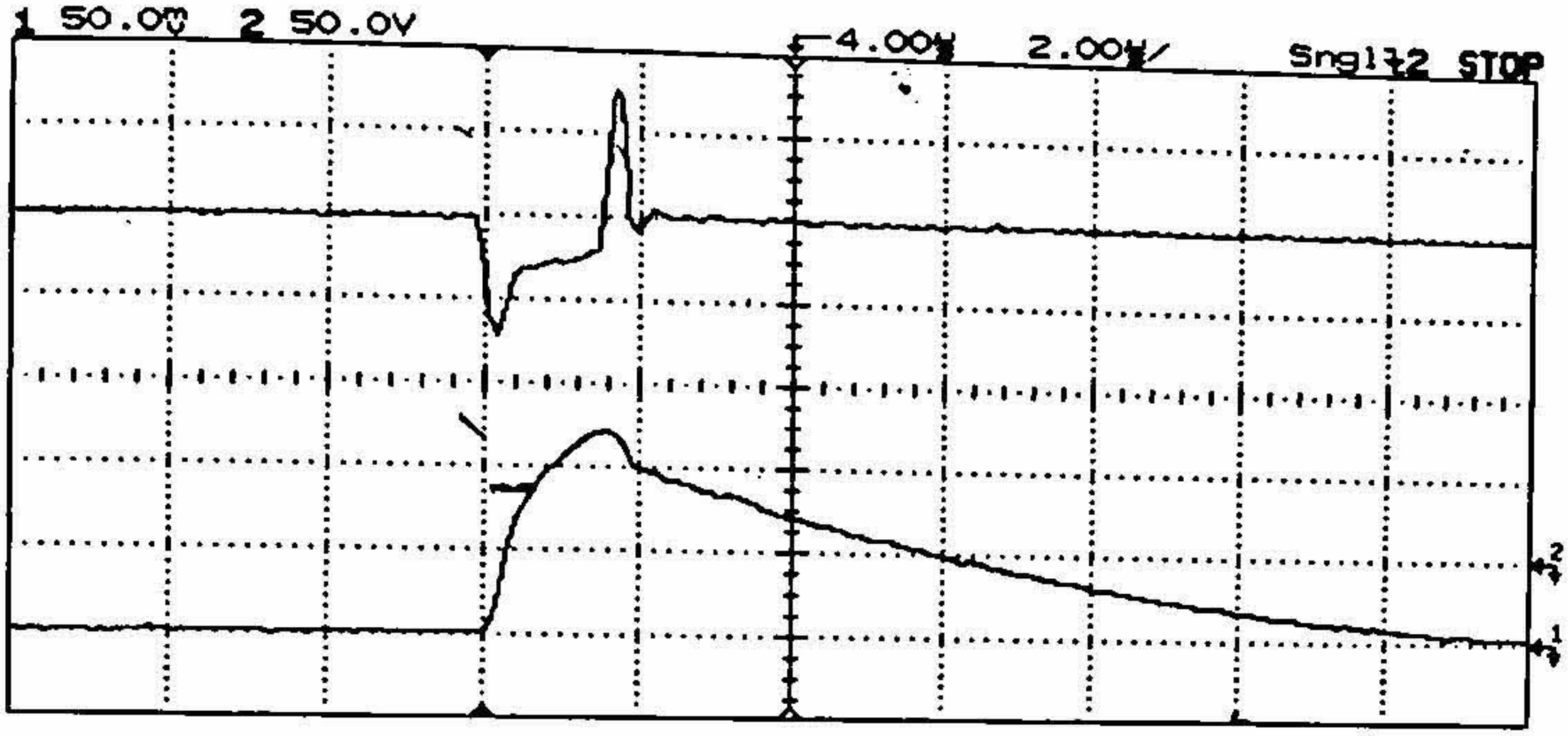
FIG. 5. Experimental setup to test for protection against a) Hard-switched fault (HSF) and b) Fault under load (FUL). C1, C2: 3300 μF, 400 V electrolytic capacitors; Q1, D1, Q2, D2: SEMIKRON SKM50GB123D IGBT half-bridge module; R1, R2: 10 K, 25 W wire wound resistors (for voltage balancing).

The connections between the DC bus capacitors and the device are made using a sandwich bus-bar with low parasitic inductance.[22–23] The tests are carried out over a range of DC bus voltages and also a range of fault inductance. The test procedure and the results are presented in this section.

4.1. *Hard-switched faults (HSF)*

The testing circuit for protection against HSF is as shown in Fig. 5a. The test device is turned on with its complementary device shorted. The DC bus voltage is set at the required level. Gate drive is applied to the test device. The gate drive circuit must shut down the drive after the blanking period (t_{BLANK}). The fault current and the voltage across the device are recorded using a storage oscilloscope.

a)



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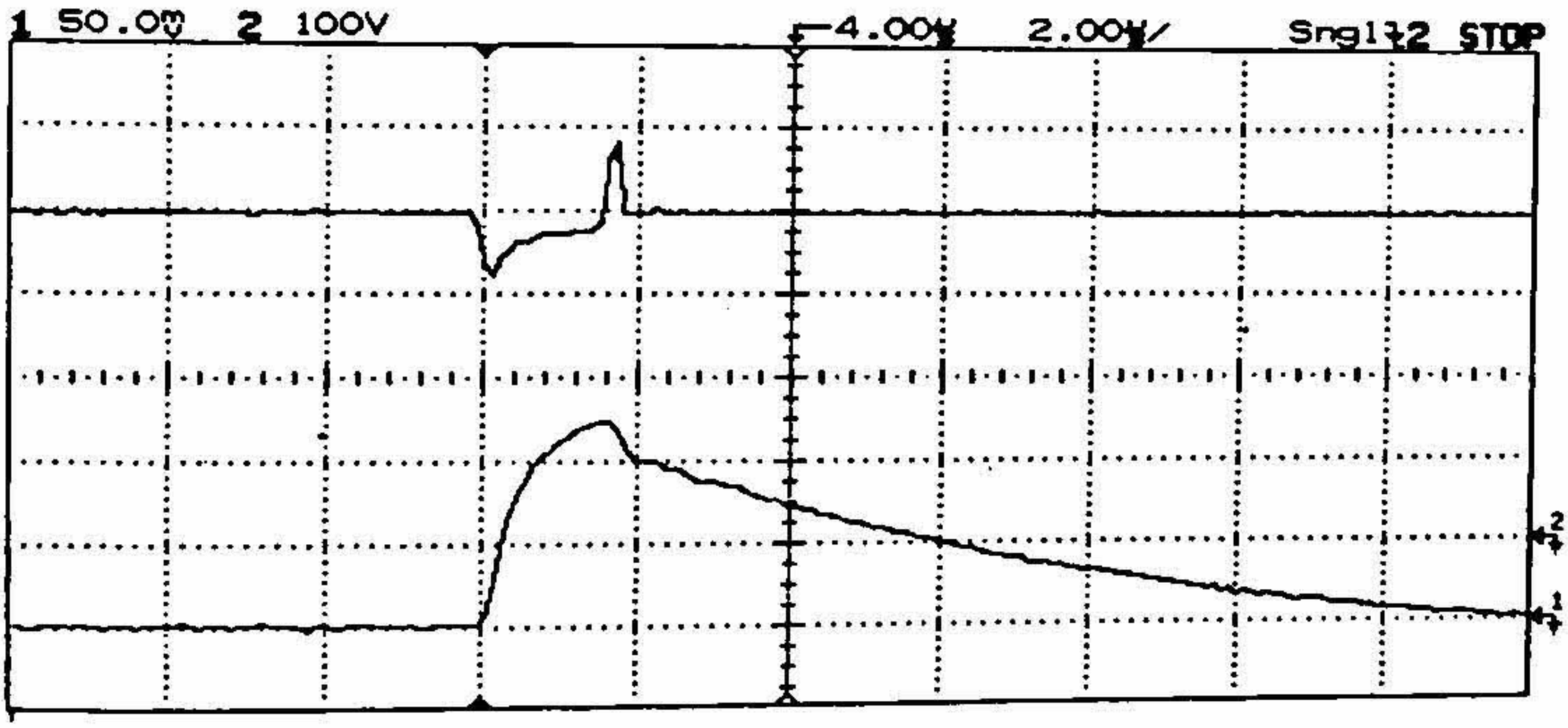

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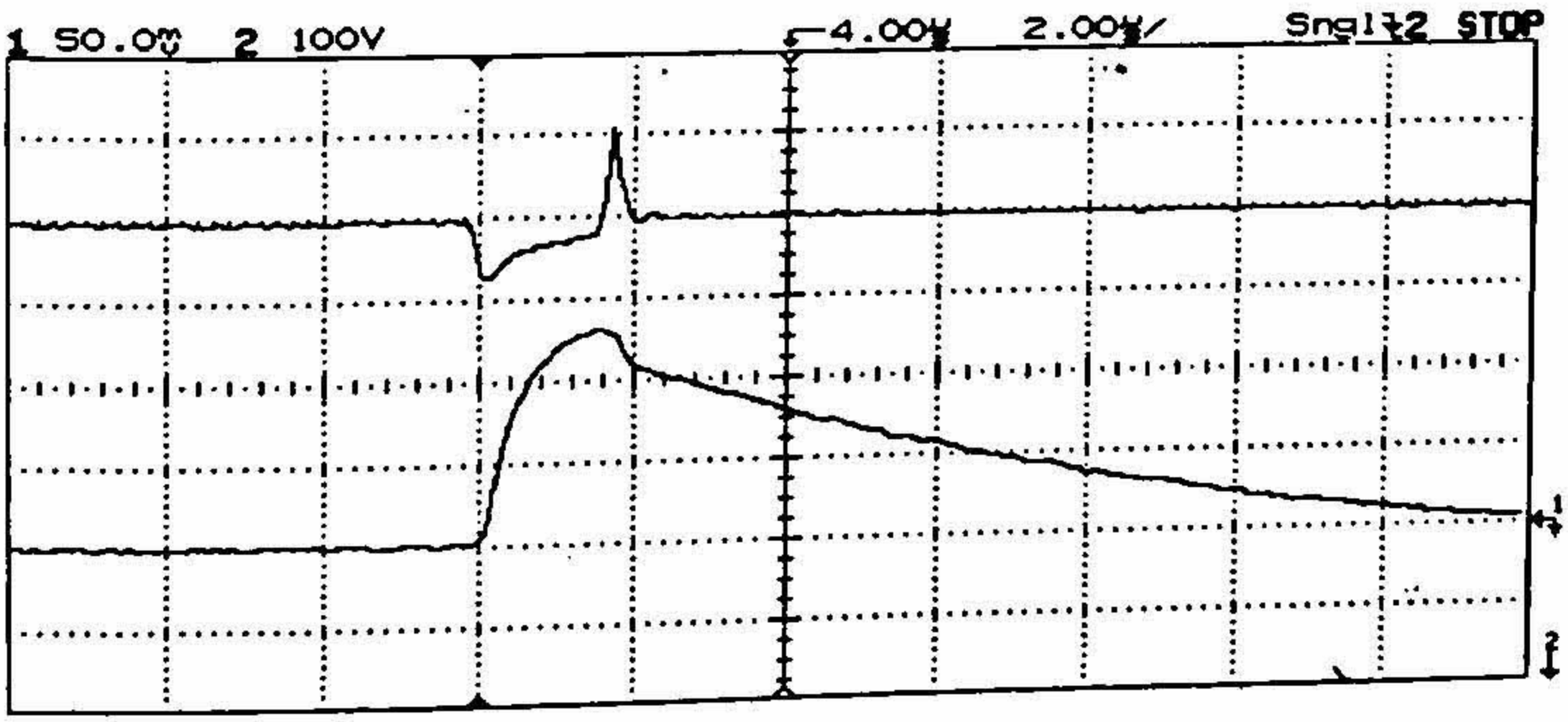
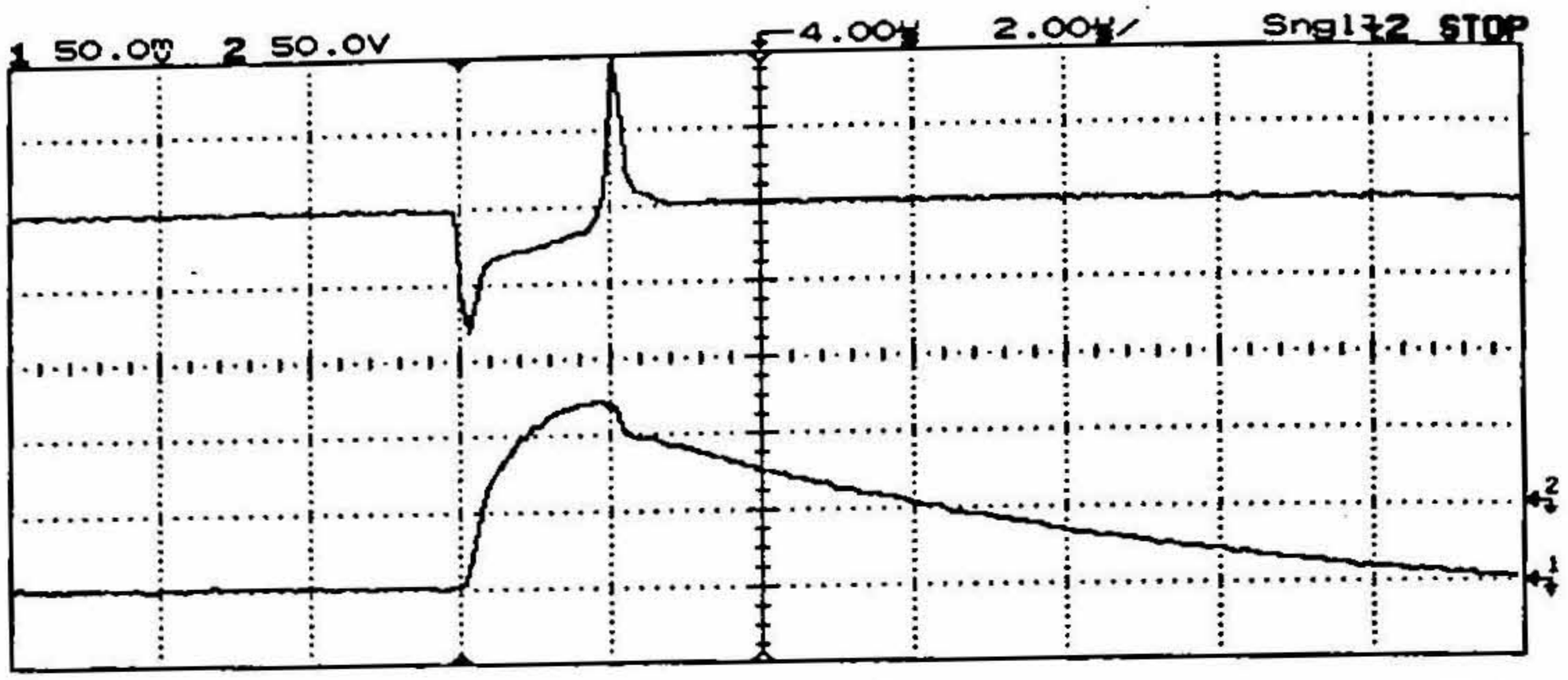


FIG. 6. Testing of drive circuit-I for protection against HSF at different bus voltages with $L = 200$ nH at a) $V_{DC} = 200$ V, b) $V_{DC} = 400$ V and c) $V_{DC} = 600$ V. Channel 1: Fault current (1 division or 50 mV corresponds to 100 A) Channel 2: Device voltage.

a)



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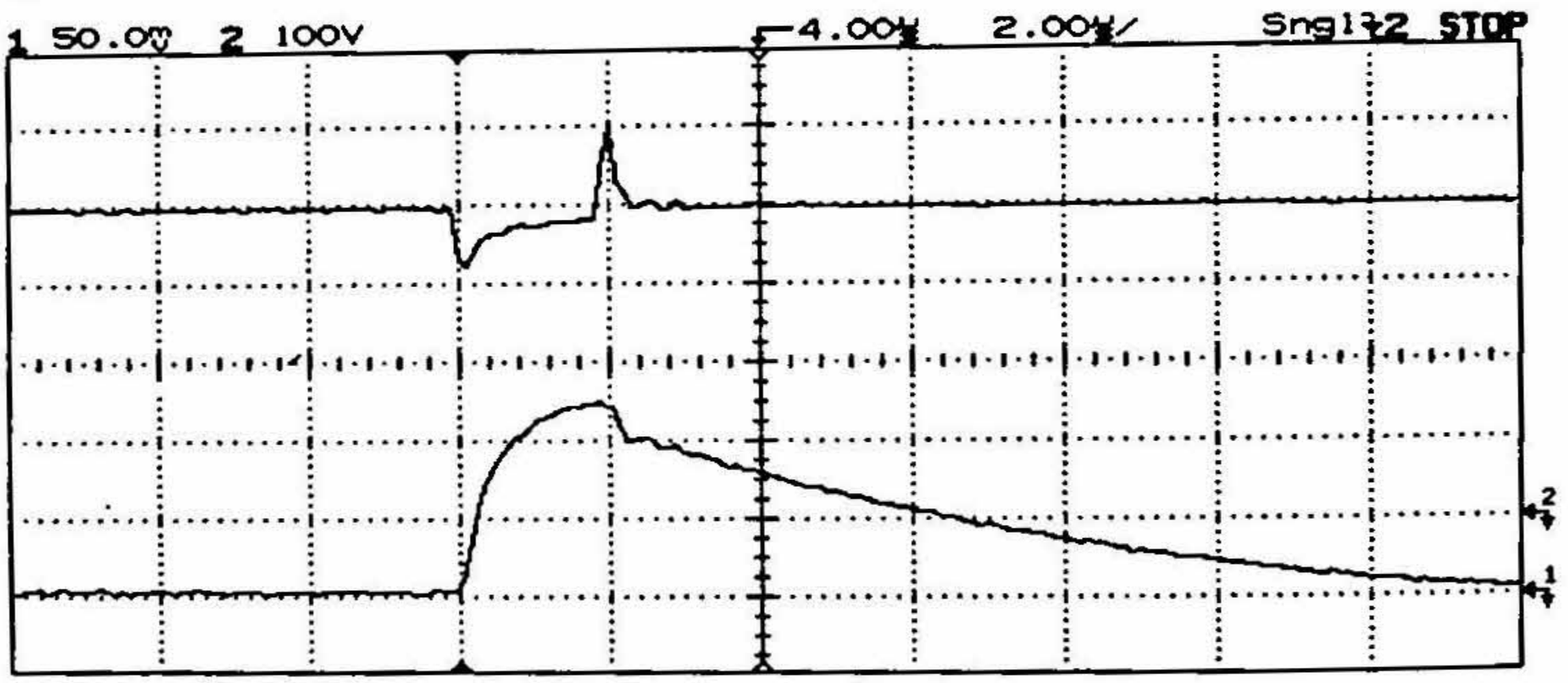

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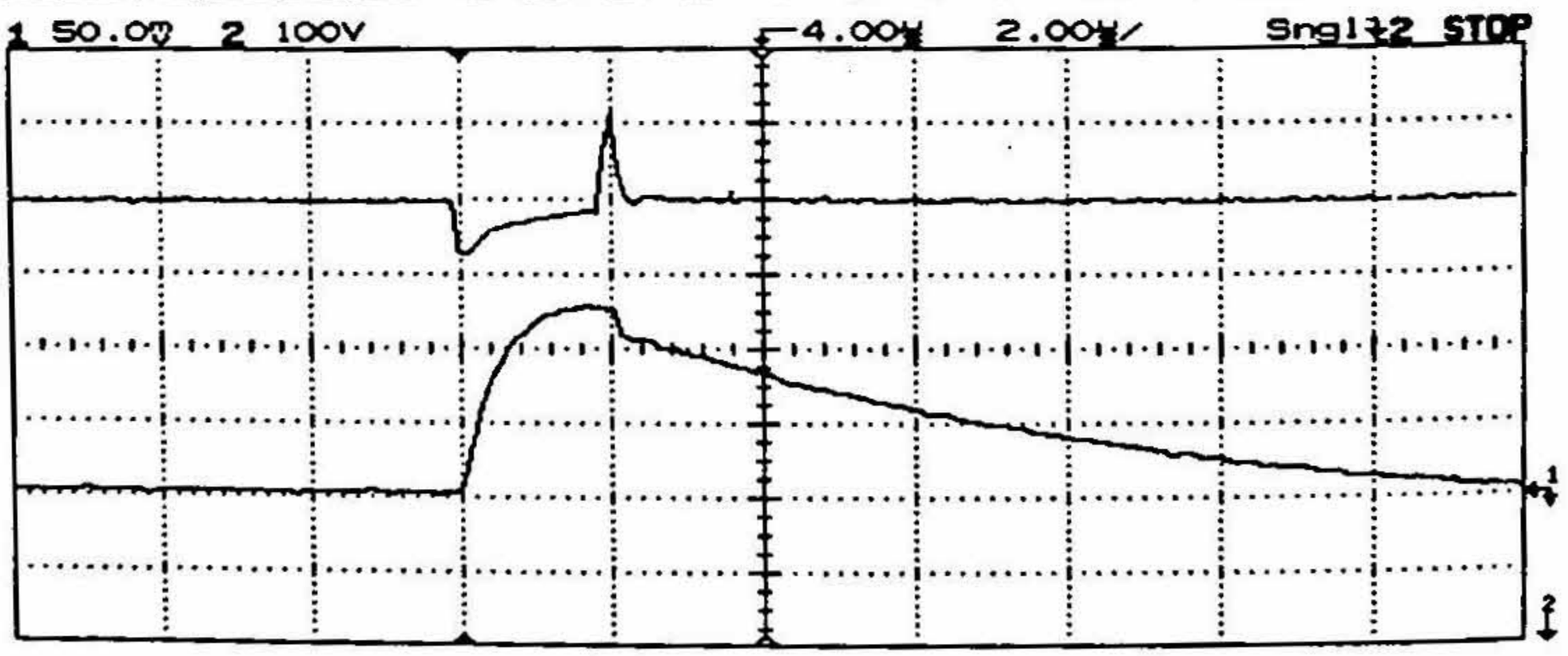
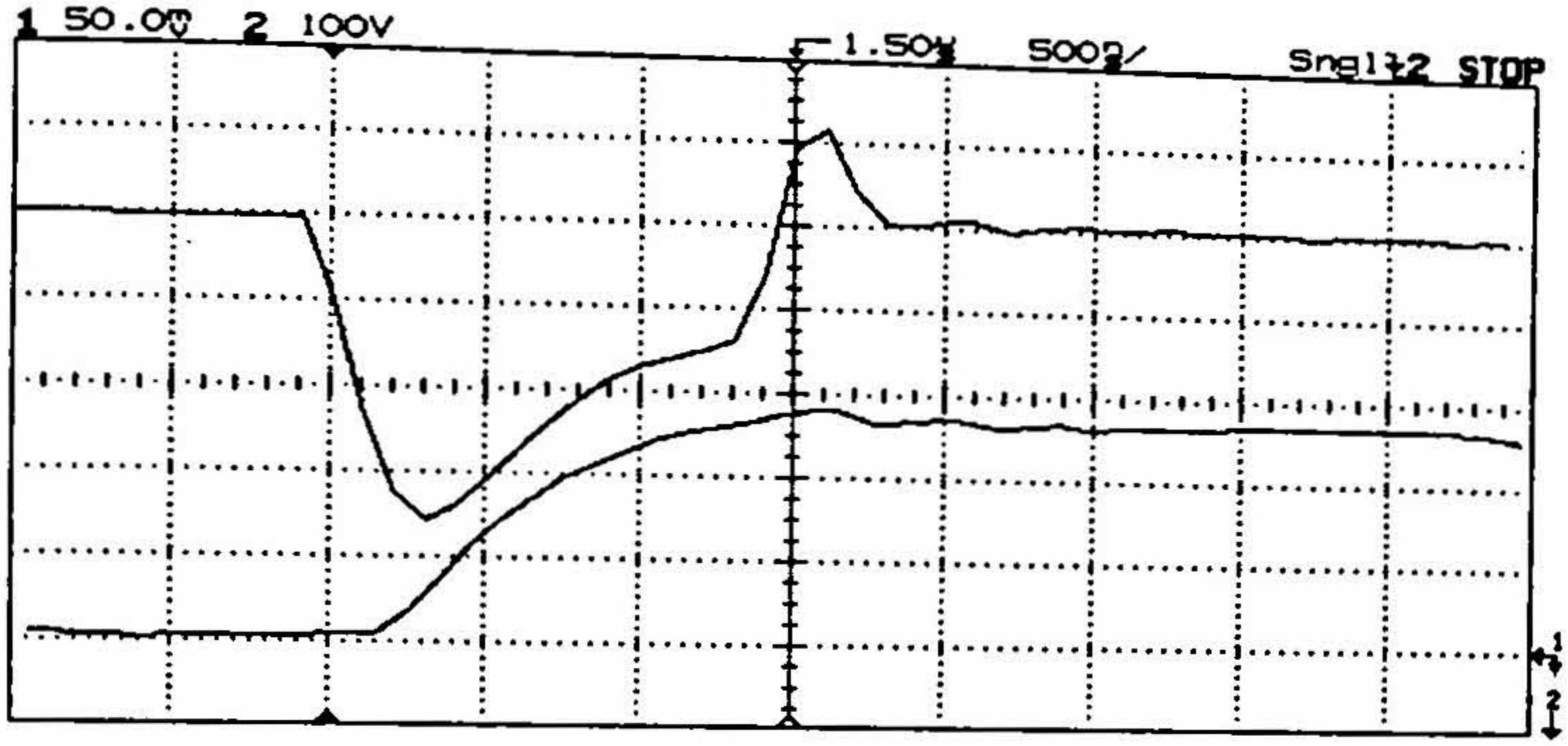


FIG. 7. Testing of drive circuit-II for protection against HSF at different bus voltages with $L = 200$ nH at a) $V_{DC} = 200$ V, b) $V_{DC} = 400$ V and c) $V_{DC} = 600$ V. Channel 1: Fault current (1 division or 50 mV corresponds to 100 A) Channel 2: Device voltage.

The complementary device is first shorted with a short wire and slack just enough to put the current probe on. The test is conducted at different DC bus voltages ranging from 100 V to

a)



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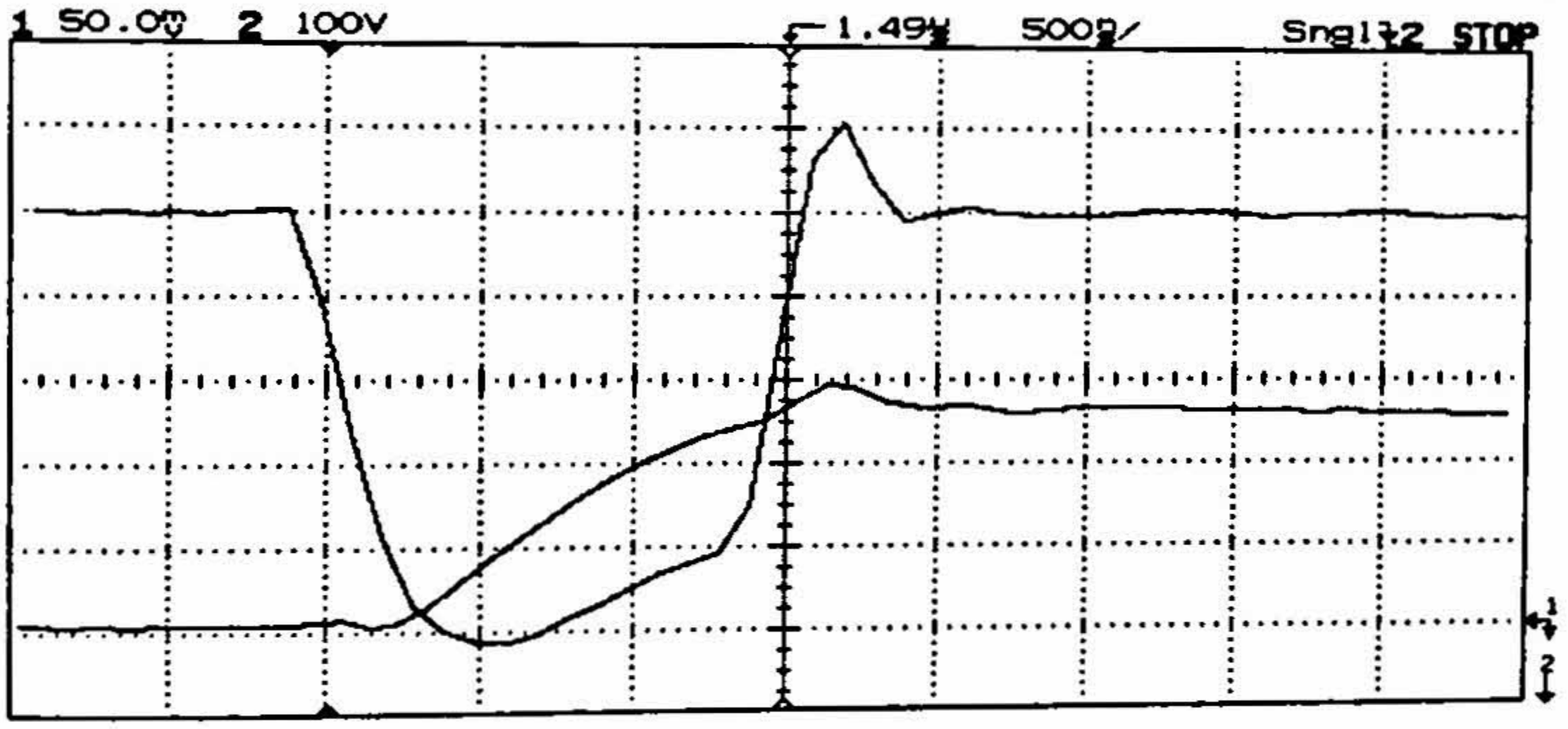

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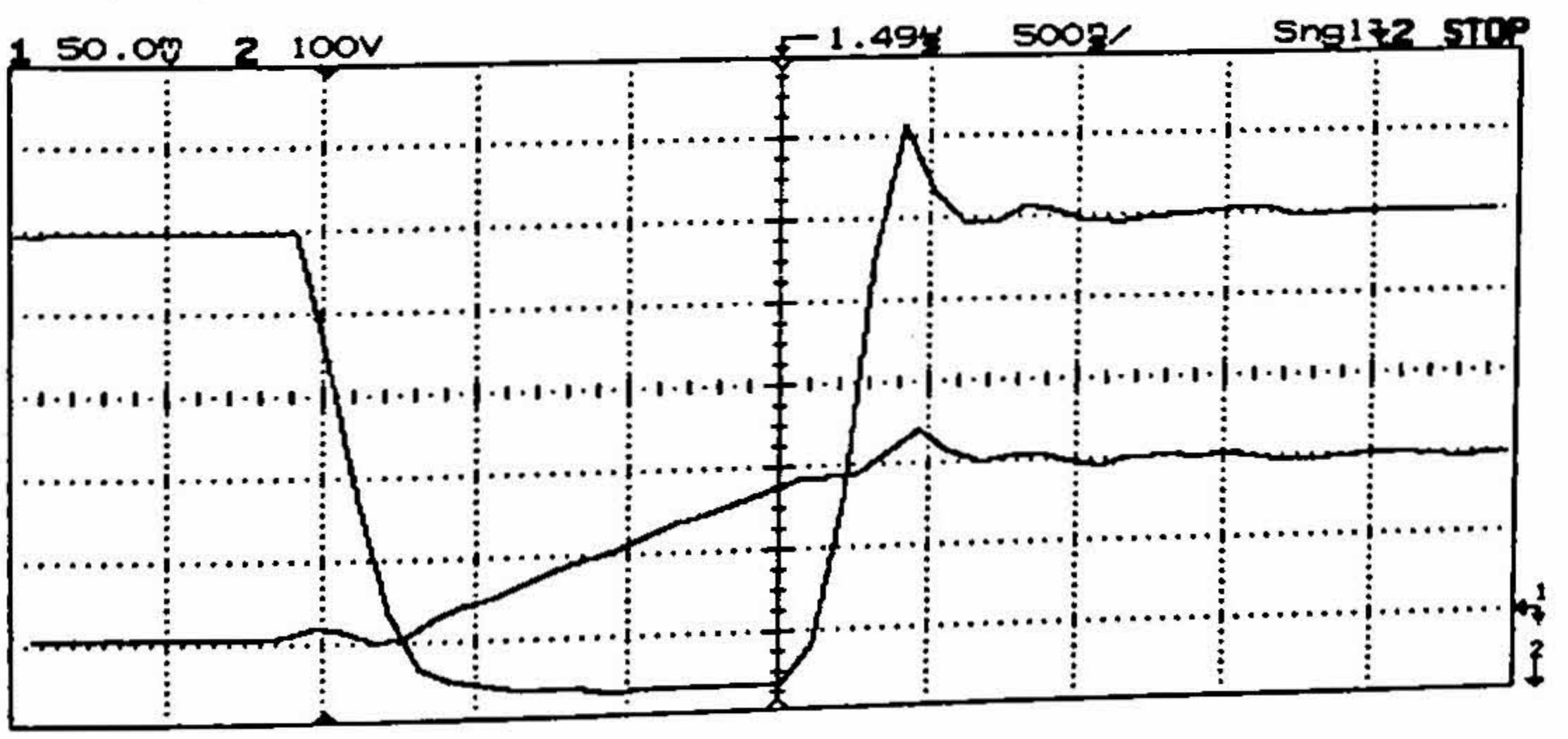
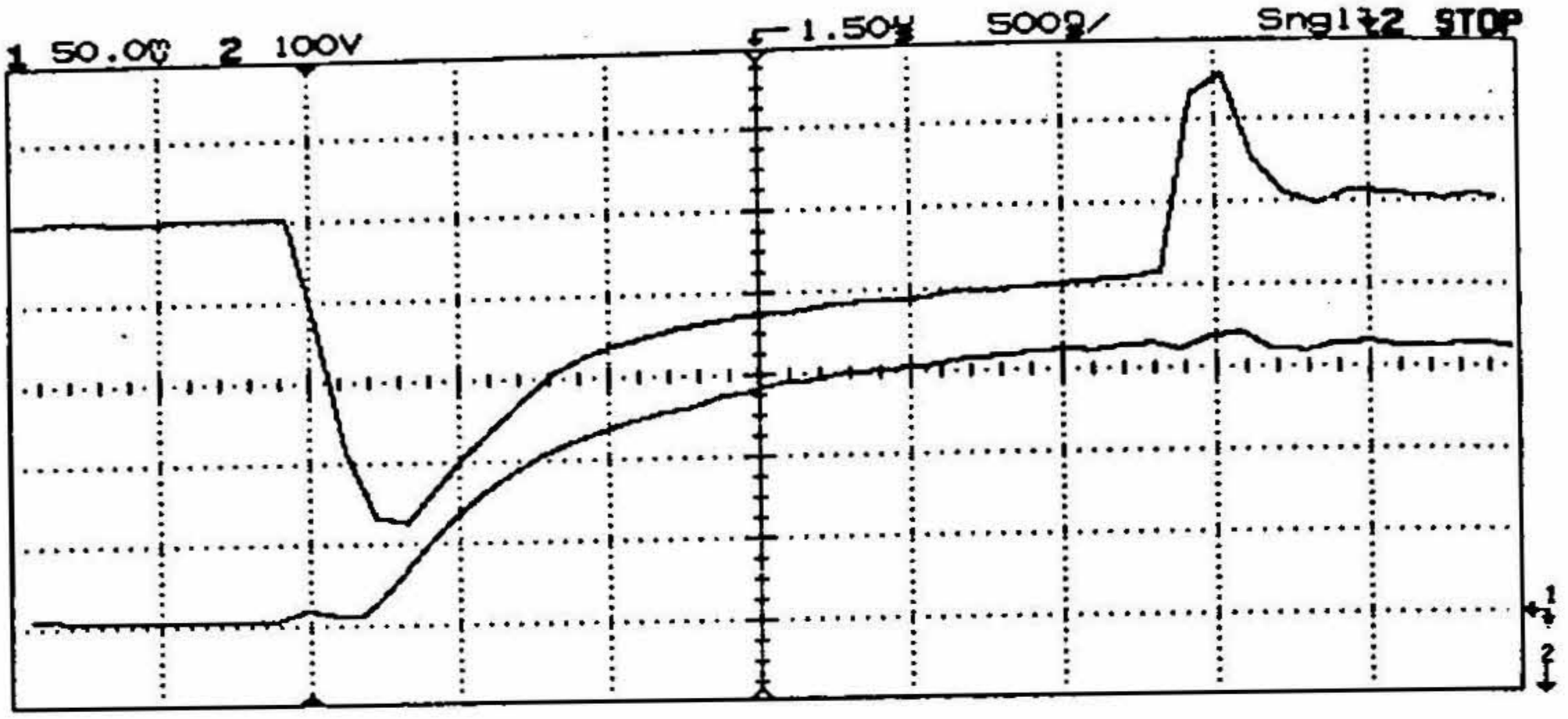


FIG. 8. Testing of drive circuit-I for protection against HSF at different fault inductances at $V_{DC} = 600$ V at a) $L = 750$ nH, b) $L = 1.5$ µH and c) $L = 3.4$ µH. Channel 1: Fault current (1 division or 50 mV corresponds to 100 A) Channel 2: Device voltage.

a)



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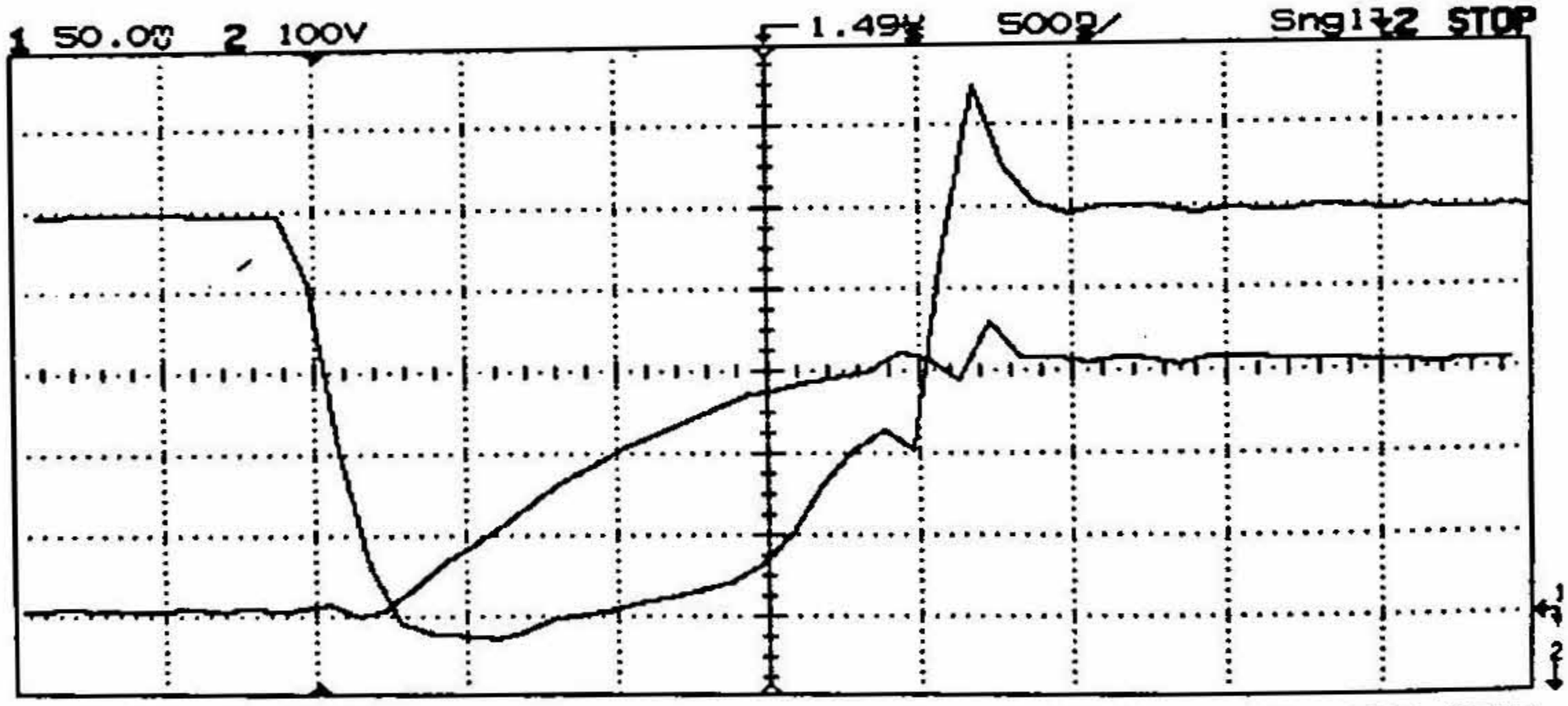

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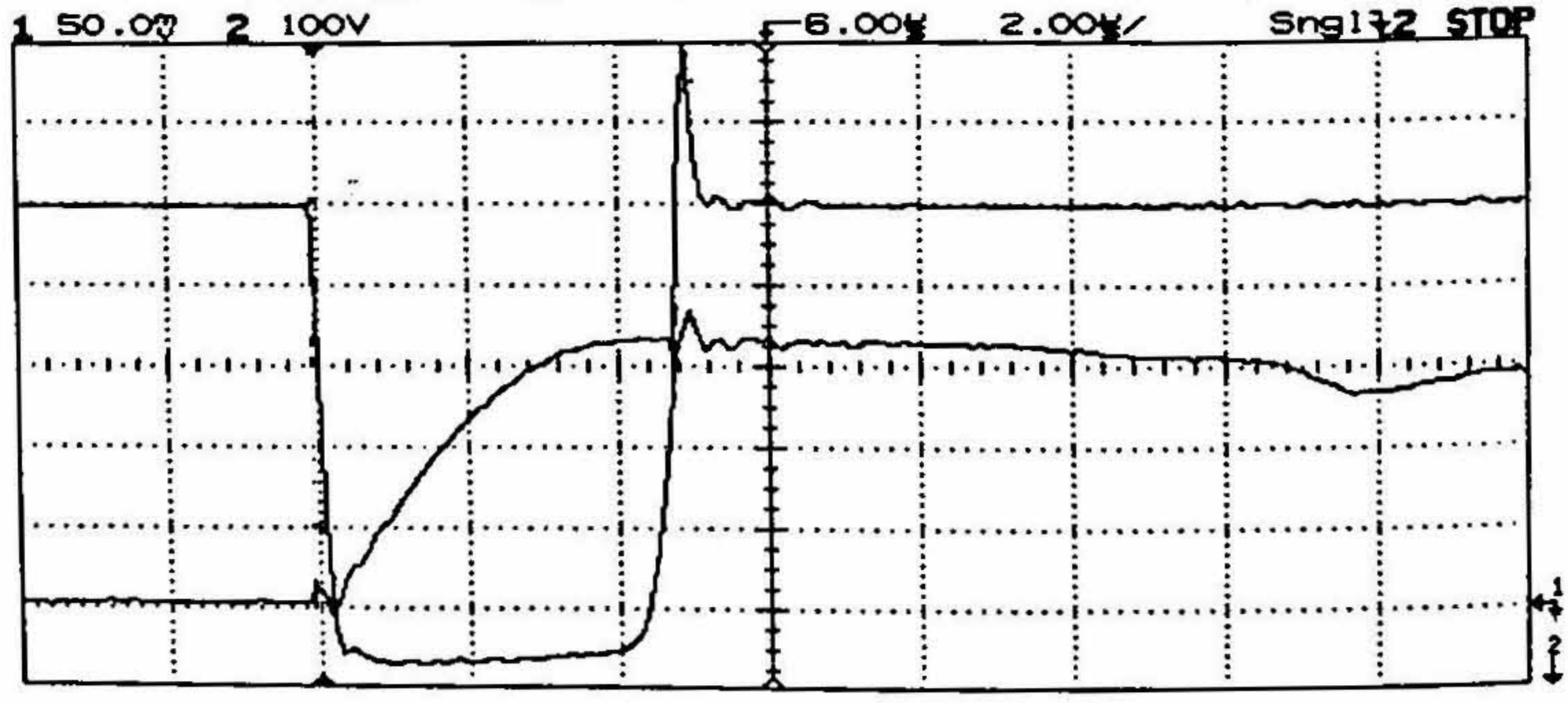


FIG. 9. Testing of drive circuit-II for protection against HSF at different fault inductances at $V_{DC} = 600$ V at a) $L = 750$ nH, b) $L = 1.5$ µH and c) $L = 3.4$ µH. Channel 1: Fault current (1 division or 50 mV corresponds to 100 A) Channel 2: Device voltage.

600 V in steps of 100 V. The oscillograms corresponding to drive circuit-I are presented for DC bus voltages of 200 V, 400 V and 600 V in Figs 6a, b and c, respectively. The same results corresponding to drive circuit-II are shown in Figs 7a, b and c, respectively. Channels 1 and 2 pertain to the fault current and the collector–emitter voltage, respectively. One division corresponds to 100 A in the case of Channel 1, and as mentioned in the figures in the case of Channel 2.

The complementary device is then shorted with increasing lengths of wire and increasingly higher loop areas so as to increase the fault inductance. The short-circuit test is carried out for different values of fault inductance with a DC bus voltage of 600 V. The test results corresponding to drive circuits-I and II are shown in Figs 8 and 9, respectively.

Prior to the fault, the bus voltage is supported by the test device and there is no current through the device. Soon after the application of the gate drive, for a short duration (around 100 ns), there is no significant increase in the current, while the voltage across the device drops. This drop is essentially across the inductive elements in the circuit.[3–5] Subsequently, the current starts rising rapidly, and the voltage also increases in concert with the current. The rate of rise of current is initially high, and decreases gradually with the current saturating at about 250 A (5 times the rated current of the device). The circuit senses a fault as voltage across the device continues to remain high even after the blanking period, and shuts down the drive. During the turn-off of the device, there is an overvoltage spike. Finally, the voltage settles down to V_{dc} and the current gradually decays to zero.

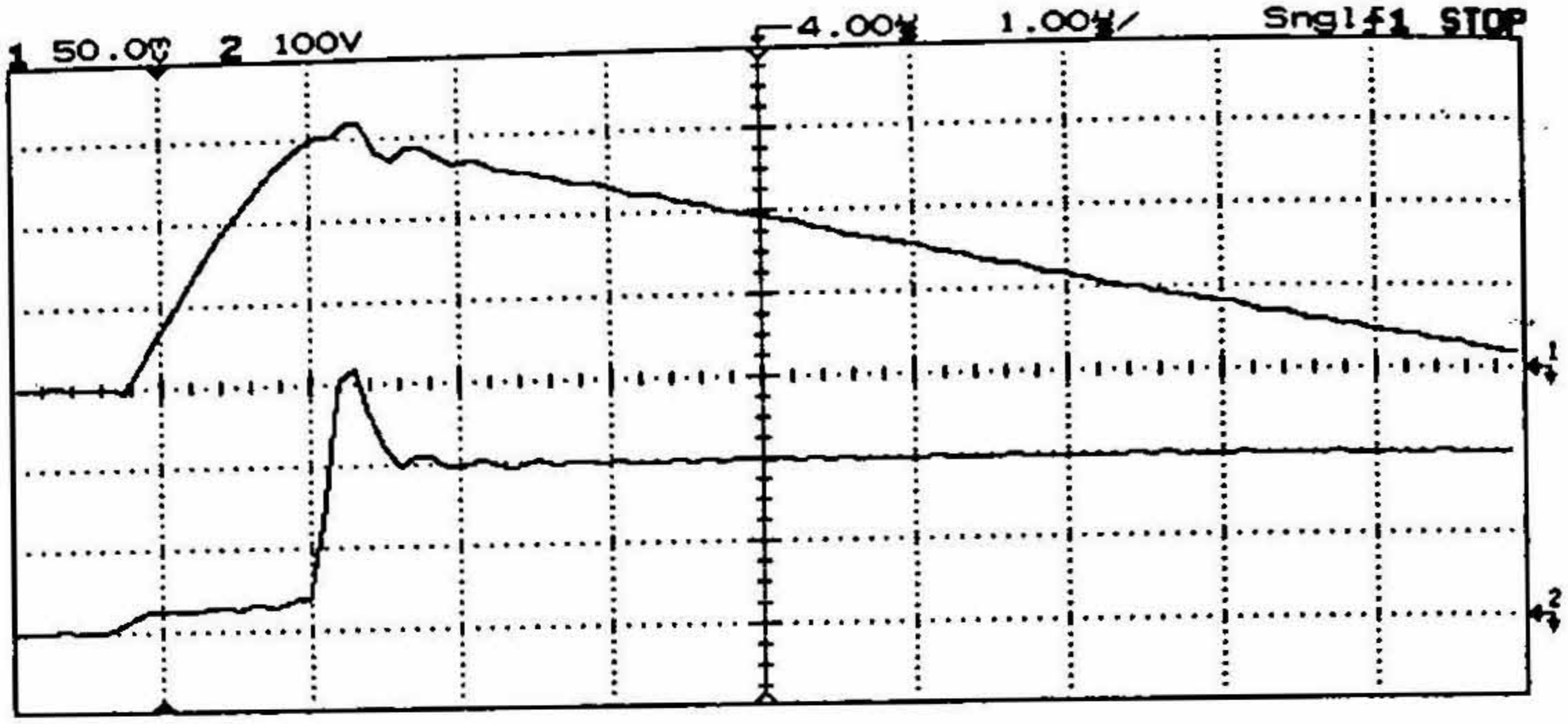
Though most devices have a short-circuit withstand time of 10 µs, it is preferable to shut down the drive within say 2–3 µs to avoid any adverse effect on the life and the long-term reliability of the device.[4] The blanking time remains practically independent of the fault inductance and bus voltage with circuit-I. However, with circuit-II, the blanking time is higher when the loop inductance is larger. MC33153 has an internal current source of 270 µA. Blanking time is equal to the time taken by this current source to charge the 47 pF capacitor connected to pin 8 of the IC to the desaturation voltage of 6.5 V. Though the charging rate is expected to be a constant, it seems to be affected by the conditions in the power circuit and gets reduced when the fault inductance is higher. On the other hand, with gate drive circuit-I, the blanking time mechanism is independent of the transients in the power circuit.

4.2. *FUL*

The testing circuit for protection against FUL is as shown in Fig. 5b. In this test, fault is created by shorting the load while the device is in conduction. The testing is carried out at different bus voltages and with different values of fault inductance as earlier. The experimental oscillograms corresponding to drive circuit-I are presented for 200 V, 400 V and 600 V in Figs 10a, b and c, respectively. Those corresponding to circuit-II are presented in Figs 11a, b and c, respectively. Fault inductance $L = 0.6$ µH in both these cases. The results with $L = 2.4$ µH corresponding to circuits-I and II are shown in Figs 12 and 13, respectively.

Once the load is shorted, the fault current starts increasing. The voltage across the device also increases as shown. When the device voltage crosses the reference, the drive circuit senses a fault and shuts down the gate drive. There is an overvoltage spike during the turn off as before. The device voltage settles down to V_{DC} and the current gradually decays to zero.

a)



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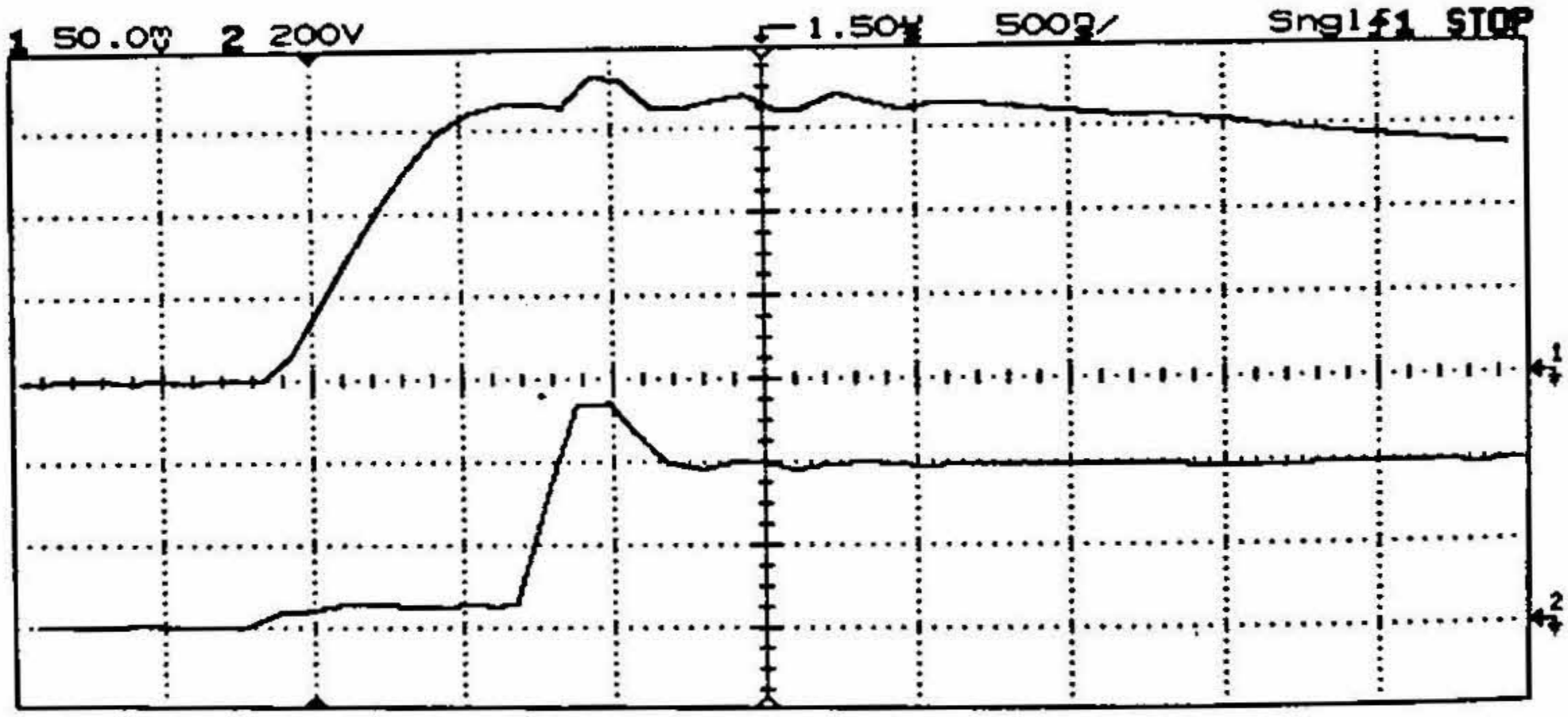


c)

FIG. 10. Testing of drive circuit-I for protection against FUL at different bus voltages with $L = 0.6\ \mu H$ at a) $V_{DC} = 200$ V, b) $V_{DC} = 400$ V and c) $V_{DC} = 600$ V. Channel 1: Fault current (1 division or 50 mV corresponds to 100 A) Channel 2: Device voltage.

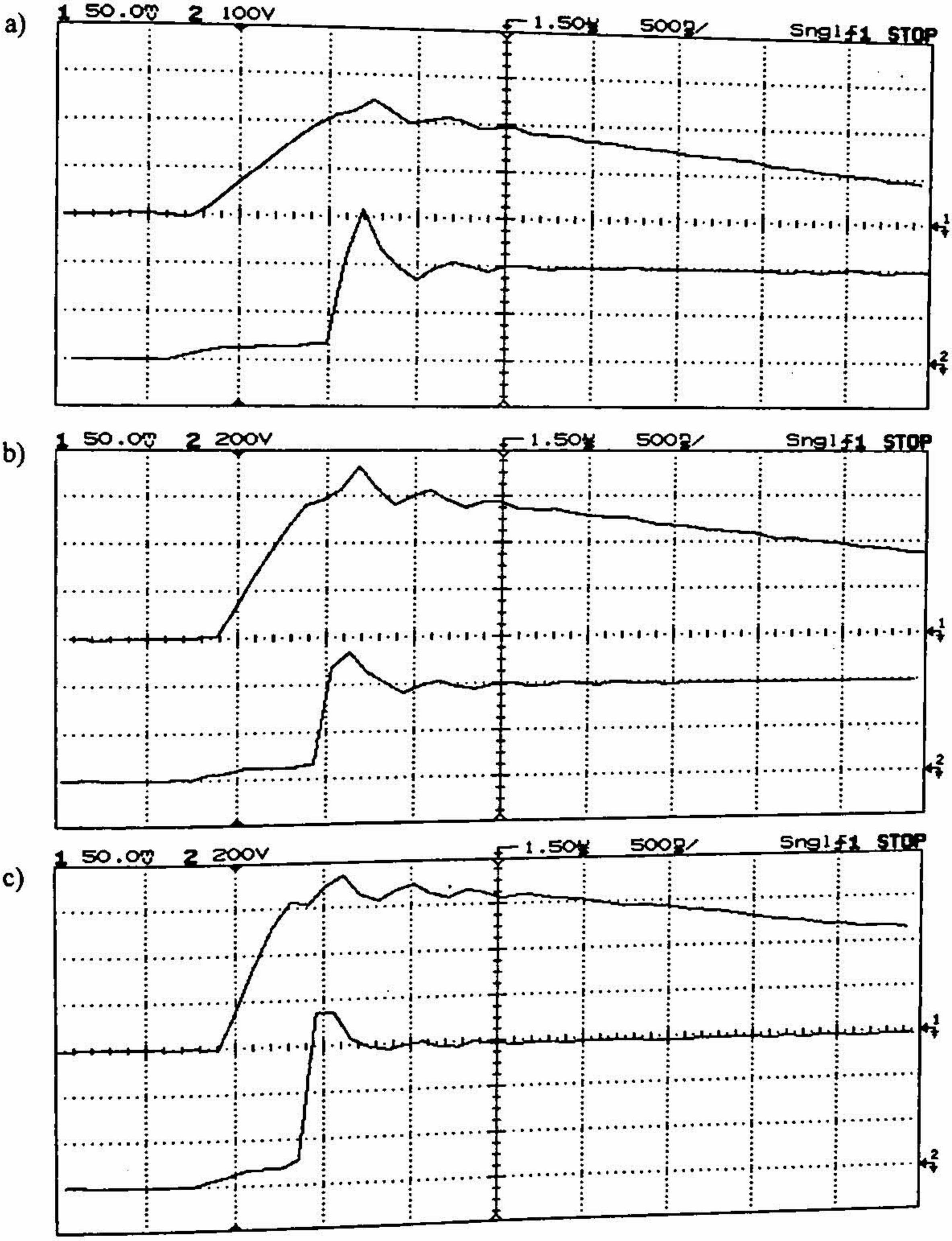


FIG. 11. Testing of drive circuit-II for protection against FUL at different bus voltages with $L = 0.6\ \mu H$ at a) $V_{DC} = 200$ V, b) $V_{DC} = 400$ V and c) $V_{DC} = 600$ V. Channel 1: Fault current (1 division or 50 mV corresponds to 100 A) Channel 2: Device voltage.

From the instant when the device voltage crosses the reference voltage, a short delay can be noticed in the oscillograms before shut down takes place. This is due to the delay in the different stages of the gate drive circuit. The delay is slightly lesser in the case of circuit-II which uses the IC driver. Also, the delay is constant with circuit-II, while it varies from case to case in circuit-I. The saturation in the input stage of the LM339 comparator is responsible for this. In any case, the delay is only of the order of a few 100 ns, which is too small to be of any consequence in the protection of the device.

Thus, both the proposed drive circuits protect the IGBT effectively against HSF as well as FUL. They are effective over a wide range of bus voltages and loop inductances as demonstrated by the test results.

5. Effect of DC bus voltage and loop inductance on short-circuit transients

The lumped equivalent circuit of the test set-up for short-circuit protection of IGBTs is shown in Fig. 14. The equivalent series inductance of the DC bus capacitors is denoted as L_{ESL}. The distributed parasitic inductance of the bus-bar and its connections can be lumped into an equivalent inductance (L_{BUS}). The stray inductance between the collector power terminal and its semiconductor contact inside, and that between the emitter power terminal and its semiconductor contact inside are represented by L_C and L_E, respectively. These two can be summed up as L_{CE}, the value of which is usually specified in the device data sheets.[11] The DC side-loop inductance $L_{DC} = L_{ESL} + L_{BUS} + L_{CE}$. The inductance corresponding to the shorting wire and the switch, if any, is designated as L_{LOAD}. The total inductance of the short-circuit path or the fault inductance $L = L_{ESL} + L_{BUS} + L_{CE} + L_{LOAD}$.

The test results presented in the earlier section bring out the influence of the DC bus voltage and that of the loop inductance of the short-circuit path on the fault current and device voltage under fault.

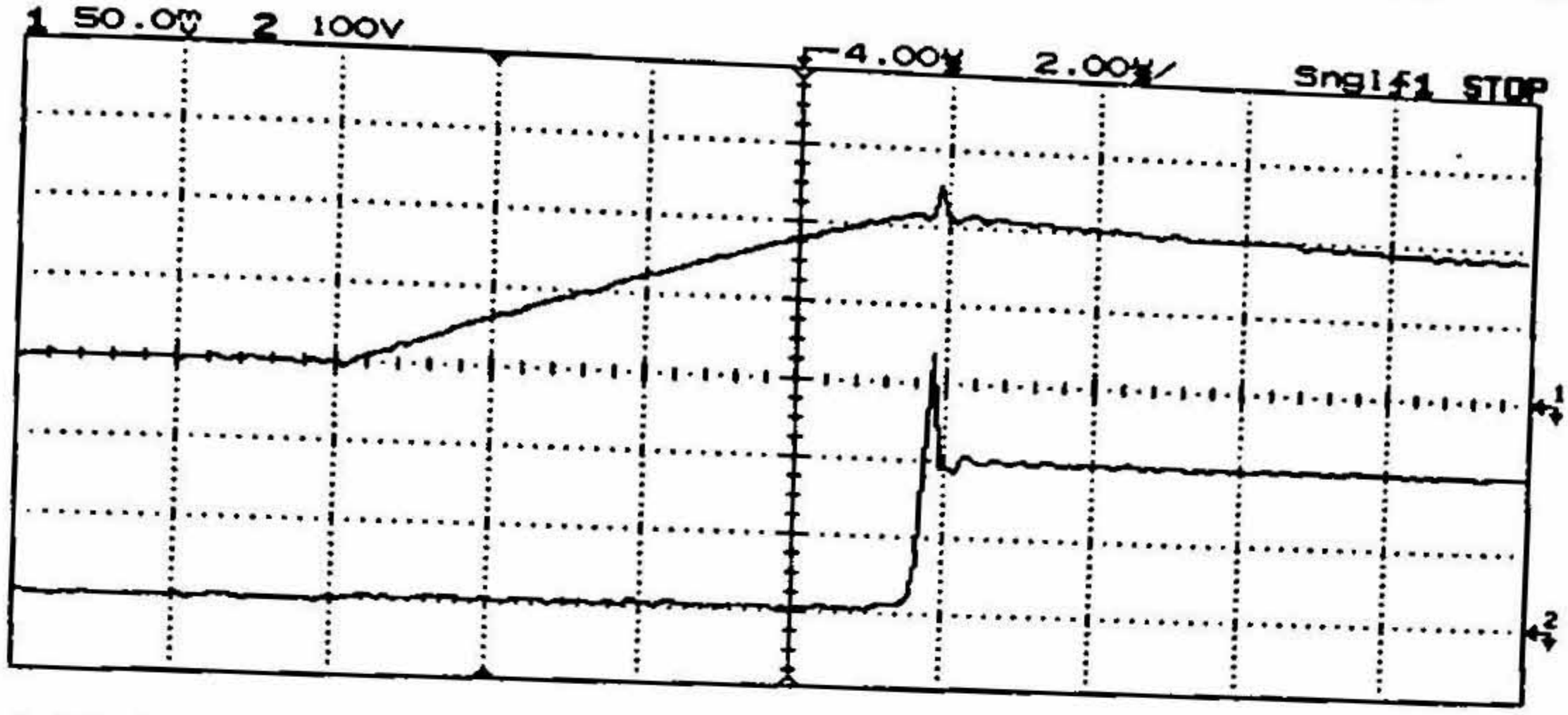
5.1. *Effect of DC bus voltage*

Short-circuit transients corresponding to DC bus voltages of 200 V, 400 V and 600 V are presented in Figs 6, 7, 10 and 11. With increase in the DC bus voltage, the rate of rise of fault current increases. However, the peak value of the fault current is independent of the bus voltage. Also, the initial dip in the device voltage in the case of HSF and the overvoltage spike during shut down remain practically unaffected by the DC bus voltage.

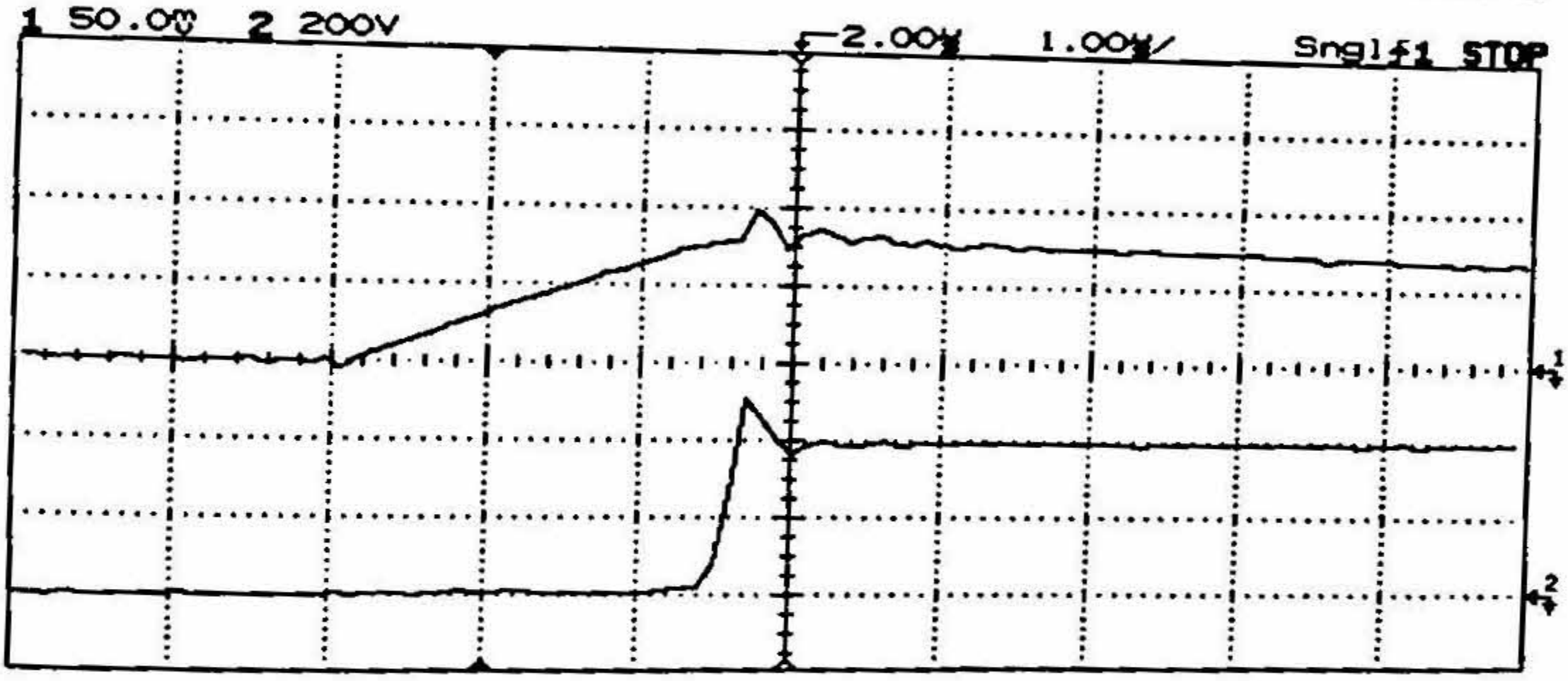
5.2. *Effect of loop inductance (L)*

Given a device, L_{CE} is fixed. Given a set of DC link capacitors and a bus-bar arrangement, L_{ESL} and L_{BUS} are also fixed. Essentially, L is varied by varying L_{LOAD}. Short-circuit transients corresponding to different values of fault inductance (L) are shown in Figs 8, 9, 12 and 13, respectively. With increase in L, the rate of rise of fault current decreases. In the case of HSF, the dip in the device voltage soon after the turn-on increases with increase in L. The overvoltage spike at turn-off remains independent of L_{LOAD} as shown by the oscillograms. However, from the equivalent circuit in Fig. 14, it can be seen that it depends on L_{DC}. More discussion on this is provided in Sections 5.3 and 6.

a)



b)



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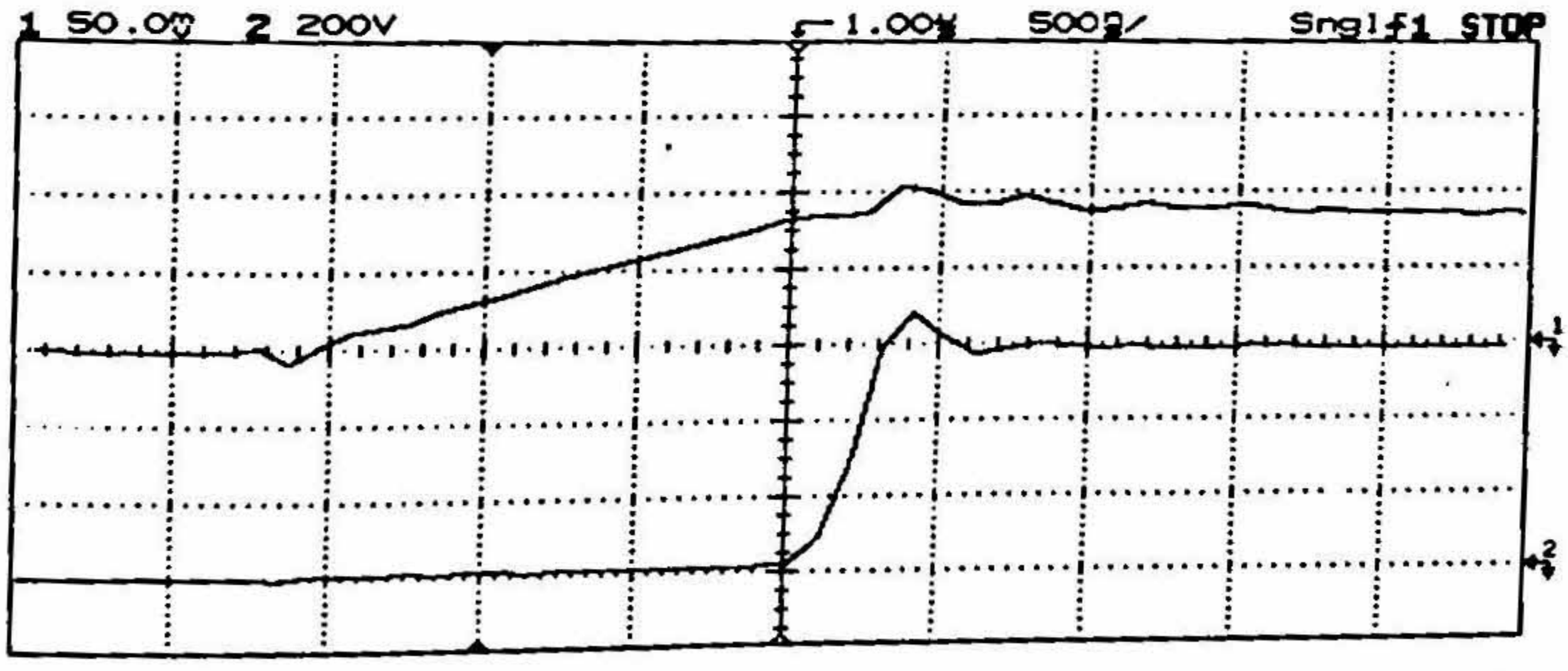
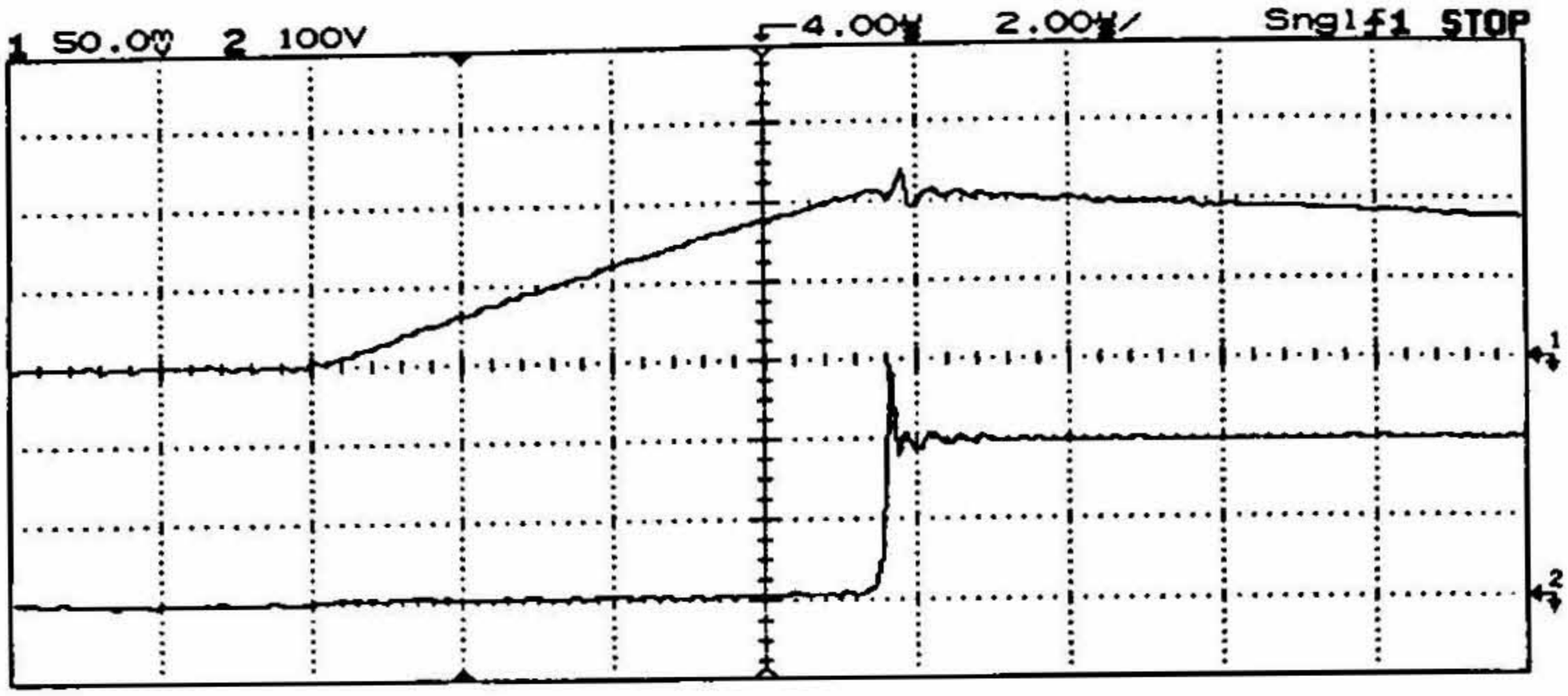


FIG. 12. Testing of drive circuit-I for protection against FUL at different bust voltages with $L = 2.4\ \mu H$ at a) $V_{DC} = 200$ V, b) $V_{DC} = 400$ V and c) $V_{DC} = 600$ V. Channel 1: Fault current (1 division or 50 mV corresponds to 100 A) and Channel 2: Device voltage.

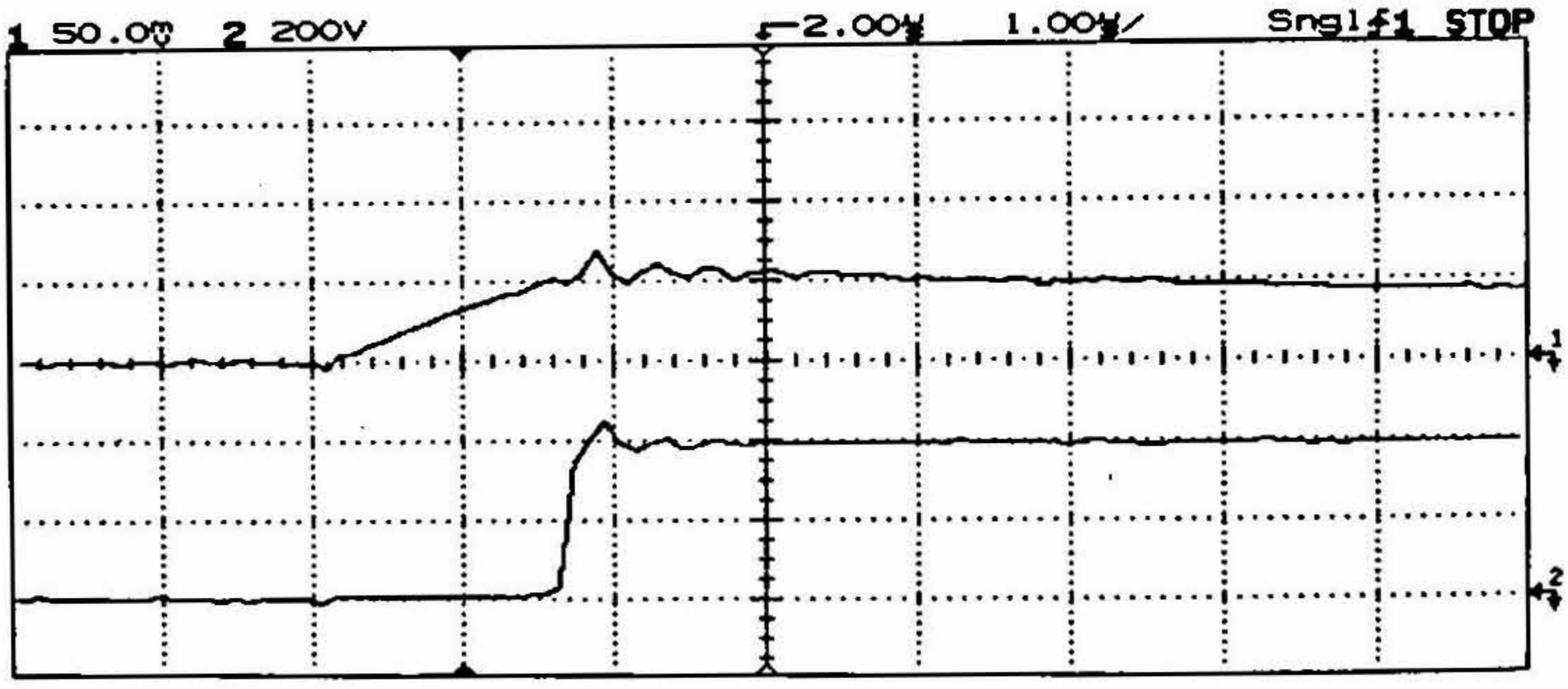
5.3. *Estimation of fault inductance (L)*

The loop inductance of the short circuit path can be estimated from the fault current and the device voltage under fault. This can be done for both types of faults. The fault current can be

a)



b)



c)

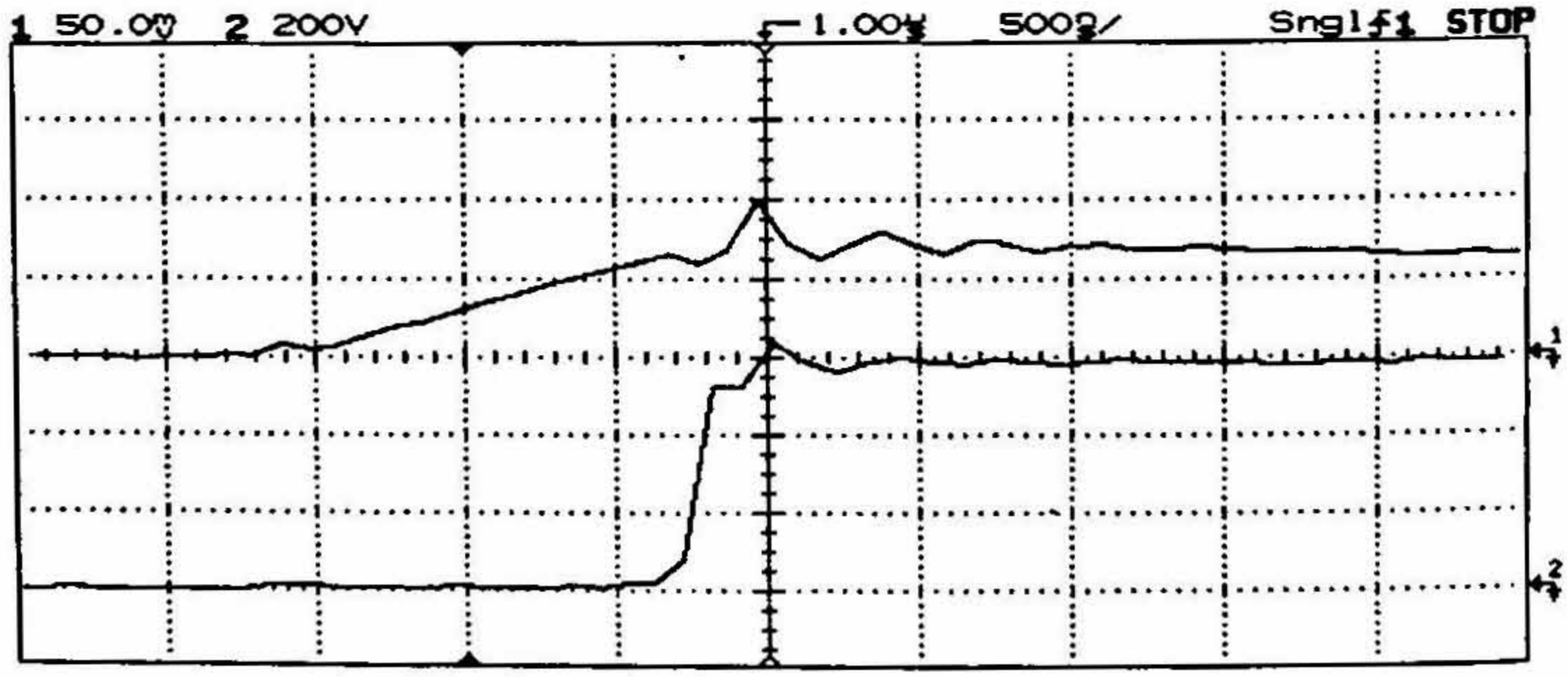


FIG. 13. Testing of drive circuit-II for protection against FUL at different bus voltages with $L = 2.4\ \mu H$ at a) $V_{DC} = 200$ V, b) $V_{DC} = 400$ V and c) $V_{DC} = 600$ V. Channel 1: Fault current (1 division or 50 mV corresponds to 100 A) and Channel 2: Device voltage.

considered to be a constant initially (zero in the case of HSF) and then to be rising exponentially. Let the initial rate of rise of the exponent be $(di/dt)_{IN}$. Let the difference between the DC

bus voltage and the voltage across the device at that instant be ΔV. This is the drop across the sum of inductances – L_{ESL}, L_{BUS} and L_{LOAD}. Both ΔV and $(di/dt)_{IN}$ can be measured from the oscillograms. Now, the value of the fault inductance can be estimated as per eqn (1).

$$L = \Delta V/(di/dt)_{IN} + L_{CE}. \tag{1}$$

L_{CE} is available from the data sheets.[11] The values of L quoted in Figs 6–13 are based on such an estimation.

6. Overvoltage spikes and bus-bar design

Overvoltage spikes occur during switching due to parasitic inductance and high di/dt. These must be decreased by reducing di/dt or the parasitic inductance or both. Reducing di/dt means increasing the gate resistances, which leads to increase in losses. Hence this is not desirable. However, reducing parasitic inductance by using a sandwich bus-bar is a move in the right direction. The sandwich bus-bar must preferably be designed in such a way that the spikes are tolerable even with the worst di/dt expected. The worst di/dt occurs during shut down following fault detection. The overvoltage spike then is a yardstick for the design of the bus-bar. The experimental results in Figs 6–13 show the spikes to be quite low (about 120 V in the case of HSF and about 150 V in the case of FUL) vindicating the design of the bus-bar.

Reducing the fault current before the shut down can also reduce the overvoltage spike. But this requires gate clamping, which makes the drive circuit complex as mentioned earlier. Further, this is not very essential as the experimental results demonstrate. Reduction in the stray inductance by a proper design of the bus-bar is adequate to keep the spikes within tolerable limits.

7. Selection of gate resistances

Selection of gate resistances is very critical in the design of a gate drive circuit. For normal operation, the gate resistances are selected based on the switching losses, stress on the devices, etc. using the characteristics in the device data sheet. During fault and subsequent shut down, the stress on the device is expected to be higher. Hence, one may consider using higher values of gate resistances than those used under normal conditions to decrease the stresses. This section attempts to find an answer to the question whether such an increase is required.

With increase in gate resistances, the switching losses increase. During test it was found that increasing $R_{G(ON)}$ from 22 to 47 Ω resulted in nuisance trips at higher bus voltages and load currents. Thus, such an increase clearly deteriorates the normal performance.

As mentioned in the previous section, the voltage spikes can be adequately handled by proper design of bus-bar. It is neither necessary nor desirable to increase the gate resistances to control the voltage spikes.

Further, if $R_{G(ON)}$ is low, the turn-on time is less and hence the blanking time can also be less. This decreases the dissipation in the device under fault. Depending on the device technology, the value of gate resistances and gate voltage, the fault current can rise to a very high value initially and then reduce subsequently to a lesser value. The initial peak fault current

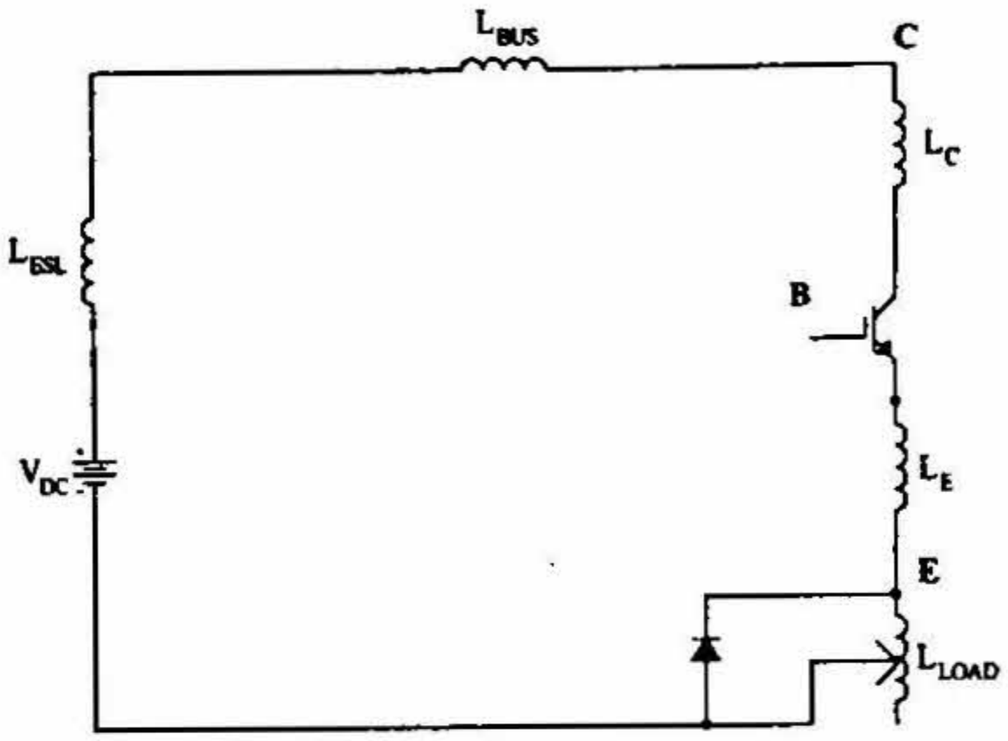


FIG. 14. Lumped equivalent circuit under fault.

($I_{SC(PEAK)}$) can be as high as twice the steady value.[8] It increases with increase in $R_{G(OFF)}$.[3] The steady fault current slightly decreases with increase in $R_{G(ON)}$.[7] However, this is not very significant.

In the present work, the gate resistances have been chosen for a good performance under normal conditions. Higher values are not used to reduce the stress under fault. The experimental results show that increase in gate resistances is not essential for effective fault protection. Also, it may not be advisable to increase them for the reasons stated above.

8. Conclusion

Two IGBT gate drive circuits capable of protecting the devices against short circuit are presented. These are shown to be effective in protecting the devices against both hard-switched fault as well as fault under load under different circuit conditions. The test results bring out the influence of the DC bus voltage and the fault inductance on the short-circuit transients. Both the circuits use collector–emitter voltage for sensing fault. Though the collector–emitter voltage gives only a coarse distinction between the fault and the normal conditions, the test results establish that it is sufficient for protecting the devices effectively. A simple gate drive circuit like the ones proposed and a well-designed low-stray inductance bus-bar form a cost-effective solution to improve the reliability of IGBT-based power converters.

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