Proton Tolerance of Multiple-Threshold Voltage and Multiple-Breakdown Voltage CMOS Device Design Points in a 0.18 μm System-on-a-Chip CMOS Technology

Ying Li, *Student Member, IEEE*, John D. Cressler, *Fellow, IEEE*, Yuan Lu, *Student Member, IEEE*, Jun Pan, *Student Member, IEEE*, Guofu Niu, *Senior Member, IEEE*, Robert A. Reed, *Member, IEEE*, Paul W. Marshall, *Member, IEEE*, Christopher Polar, Michael J. Palmer, and Alvin J. Joseph, *Member, IEEE*

***Abstract*—The paper presents the results of an investigation of the proton tolerance of the multiple-threshold voltage and multiple-breakdown voltage device design points contained in a 0.18 μm system-on-a-chip CMOS technology. The radiation response of the CMOS devices having three different device design configurations are characterized and compared for equivalent gamma doses up to 300 krad(Si), using the threshold voltage, off-state leakage, and effective mobility to assess the *dc* performance. All three CMOS device configurations show a very slight degradation of threshold voltage and effective mobility with increasing dose. We also present for the first time the frequency response and S-parameters of these RF CMOS devices under proton radiation. The S-parameters and cut-off frequency show little degradation up to 300 krad(Si) total dose. These results suggest that the CMOS devices in this 0.18 μm SoC CMOS technology are well-suited for RF circuit applications in an ionizing radiation environment without intentional total-dose hardening.**

***Index Terms*—CMOS, proton radiation, RF technology, system-on-chip.**

I. Introduction

IT is well known that CMOS scaling improves the transistor frequency response, and scaled CMOS technologies are being increasingly used to address low-end (1–2 GHz) RF transceiver IC applications for low-cost wireless communications systems. Clearly, however, RFIC design places much more stringent demands on device performance and hence traditional core CMOS technologies used in digital logic are typically not well-suited to RF CMOS implementations. Because of this, so-called "system-on-a-chip" (SoC) CMOS technologies [1] have recently emerged, and contain multiple CMOS device design points in order to address multiple application arenas, and include, for instance, RF CMOS (thick oxide, high V_{DD}), high-speed digital logic (thin oxide, nominal $V_{\rm th}$), and low-power digital logic (thin oxide, high $V_{\rm th}$), all in the same technology core. As a viable option for space missions, clearly the radiation tolerance of this technology must be carefully scrutinized. The radiation response of the devices in such a CMOS technology, especially from the viewpoint of their *RF* performance under radiation, has not been reported to date. In this paper, we investigate the proton radiation response of the *dc* and *RF* characteristics of the multiple CMOS device design points in a 0.18 μm SoC CMOS technology. The threshold voltage, off-state leakage, and effective mobility are used to assess the *dc* performance of the devices in each of the three different device design points. For the first time, the frequency response and S-parameters of these RF CMOS devices are used to characterize the *RF* performance under proton radiation.

Manuscript received July 16, 2003; revised September 4, 2003. This work was supported by DTRA under the Radiation Tolerant Microelectronics Program, NASA-GSFC under the Electronics Radiation Characterization Program, and the NASA Jet Propulsion Laboratory.

Y. Li, J. Pan, G. Niu and M. J. Palmer are with the Alabama Microelectronics Science and Technology Center, Electrical and Computer Engineering Department, Auburn University, Auburn, AL 36849 USA (e-mail: yingli@eng.auburn.edu).

J. D. Cressler and Y. Lu are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

R. A. Reed is with NASA-GSFC, Code 562, Greenbelt, MD 20771 USA.

P. W. Marshall is a consultant to NASA-GSFC, Code 562, Greenbelt, MD 20771 USA.

C. Polar is with Jackson and Tull Chartered Engineers, Washington, DC 20018 USA.

A. Joseph is with IBM Microelectronics, Essex Junction, VT 05401 USA.

Digital Object Identifier 10.1109/TNS.2003.821800

II. Experiment

The CMOS devices under investigation are contained in a commercially-available 0.18 μm CMOS technology. The basic CMOS fabrication process is as follows: after subcollector and epilayer formation, the deep- and shallow-trench isolation are completed. CMOS wells are then implanted, followed by gate oxidation, poly gate and spacer formation, and LDD implants [2]. This CMOS technology was not radiation-hardened in any way.

Table I shows the parameters of test devices in three different configurations (design points): 0.18 μm 1.8 V nominal $V_{\rm th}$ (for high speed digital logic), 0.18 μm 1.8 V high $V_{\rm th}$ (for low power digital logic), and a thick oxide, 0.30 μm 3.3 V RF CMOS. The gate oxide is 3.5 nm for the 1.8 V nominal/high $V_{\rm th}$ configurations, while for the 3.3 V RF CMOS, the device has 6.8 nm gate oxide thickness. Compared with the 1.8 V nominal $V_{\rm th}$ device, the 1.8 V high $V_{\rm th}$ device has a heavier doping in the channel to reach a higher $V_{\rm th}$ value. The devices for each of these three design points have the identical edge termination configurations. For each device design point, three different sizes of devices were investigated: 1) 10/0.18 ($\mathrm{W/L} = 10\ \mu\mathrm{m}/0.18\ \mu\mathrm{m}$),

TABLE I
PARAMETERS OF TEST DEVICES

Device Design Point	t_{ox} (nm)	V_{DD} (V)	V_{th} (V) (L)
1.8 V nominal V_{th}	3.5	1.8	0.50 (0.18μm)
1.8 V high V_{th}	3.5	1.8	0.65 (0.18μm)
3.3 V configuration	6.8	3.3	0.69 (0.30μm)

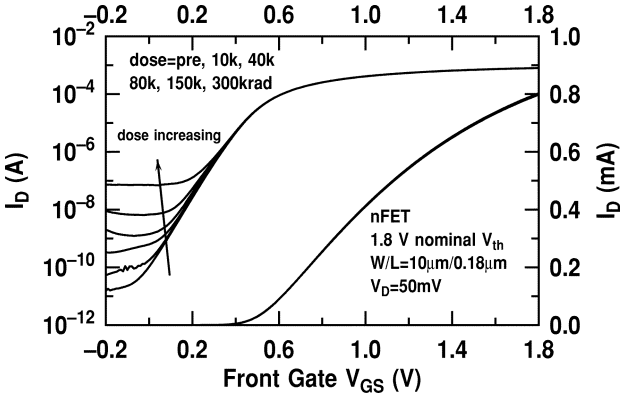

Fig. 1. Front-gate subthreshold characteristics of a 10/0.18 nFET in 1.8 V nominal $V_{\rm th}$ configuration before and after radiation.

10/0.24, and 10/10 nFETs for 1.8 V nominal/high $V_{\rm th}$; 10/0.30, 10/0.40 and 10/10 nFETs for the 3.3 V RF CMOS configuration. The pFETs were found to be radiation hard and for brevity are not discussed here.

Samples for *dc* measurements were mounted in 24 pin DIP packages, wire-bonded, and then exposed to 62.5 MeV protons up to 300 krad(Si) equivalent gamma dose at the Crocker Nuclear Laboratory Cyclotron located at the University of California at Davis. The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup. Ta scattering foils located several meters upstream of the target establish a beam spatial uniformity of 15% over a 2 cm radius circular area. Beam currents from about 5 pA to 50 nA allow testing with proton fluxes from 10^6 to 10^{12} $\rm protons/cm^2/sec$. The dosimetry system has been previously described [3], [4] and is accurate to about 10%. At a proton fluence of 1×10^{12} $\rm p/cm^2$, the measured equivalent gamma dose was approximately 136 krad(Si).

During irradiation, the devices were biased in the "ON-gate" configuration ($V_{GS}=V_{DD}$, $V_D=V_S=V_{sub}=0$) to realize worst-case conditions. The *dc* characteristics of the test devices (a total of three samples were irradiated from 10 krad to 300 krad total dose at the same environment, and each sample has one set of the test devices) were measured pre-radiation and immediately after each radiation dose at room temperature (300 K) using an Agilent 4155 Semiconductor Parameter Analyzer. The samples for the *ac* measurements were mounted on ceramic holders and exposed to proton radiation up to 300 krad(Si) equivalent gamma dose with terminal floating. At present, a terminal floating condition is the only possibility to facilitate post-radiation broadband on-wafer measurements of intrinsic transistor performance, which involve not only the device under test, but also specially designed open and test structures for de-embedding of the pad parasitics. Since

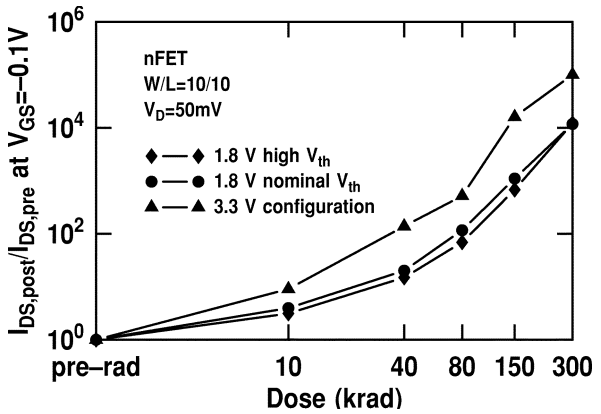

Fig. 2. Normalized off-state leakage for the 10/10 nFETs in the three device configurations as a function of equivalent total dose.

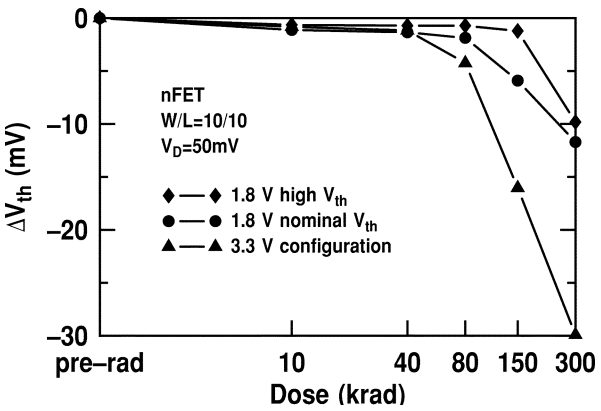

Fig. 3. The threshold voltage shift for the 10/10 nFETs in the three configurations as a function of equivalent total dose.

radiation damage can depend on the device bias conditions during exposure, the ac degradation results obtained here may not represent the worst case.

A total of six samples for *ac* measurements were irradiated, and each sample has one set of the test devices for the *ac* measurements. An Agilent 8510C Vector Network Analyzer (VNA) was used for scattering parameter (S-parameter) measurements before and after irradiation [5]. The high-frequency device measurement system used in this work centers around an HP8510C VNA with an HP 8517B S-parameter test set and HP 83651A synthesized sweeper, both with a 45 MHz to 50 GHz bandwidth. This system can be used to characterize any n-port network having a maximum output power of $+17$ dBm (power relative to 1 mW) over the measurement frequency range [6].

III. RESULTS AND DISCUSSION

A. Dc Performance

Fig. 1 shows the pre- and post-radiation drain current (I_D) versus gate voltage (V_{GS}) characteristics for a 10/0.18 nFET in the 1.8 V nominal $V_{\rm th}$ configuration. The same I_D is plotted on a logarithmic scale on the left y-axis, and on a linear scale on the right y-axis. It is clearly seen that the off-state leakage increases from 10 *pA* before radiation to about 90 *nA* after 300 krad total dose. This off-state leakage is attributed to the device region where the gate overlaps the shallow trench

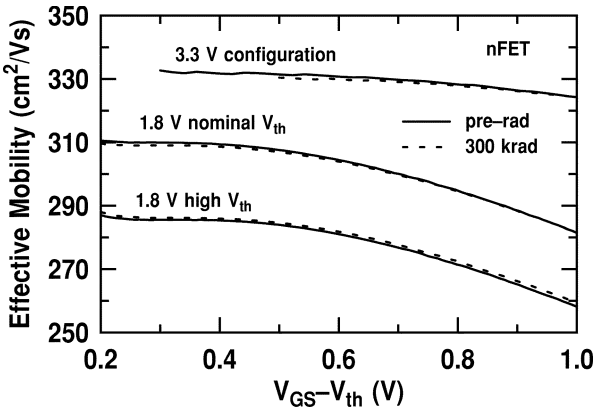

Fig. 4. Effective channel mobility versus gate overdrive for the three configurations at pre-radiation and after 300 krad.

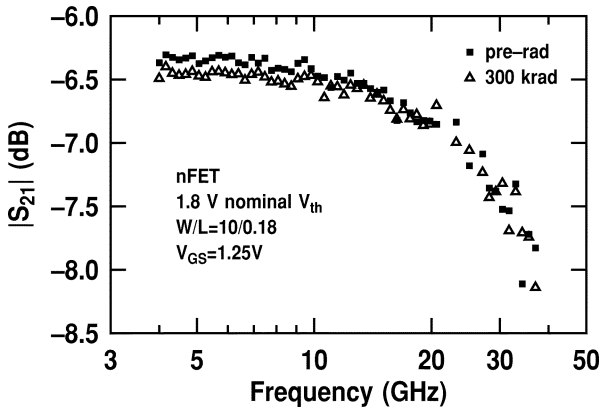

Fig. 6. S_{21} magnitude versus frequency at $V_{GS} = 1.25$ V for the 10/0.18 nFET at pre-radiation and after 300 krad.

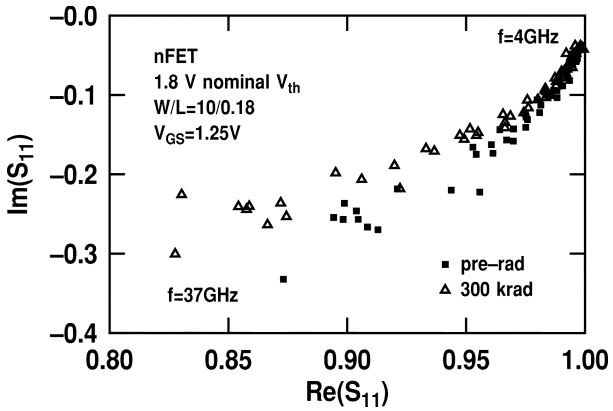

Fig. 5. Comparison of $\mathrm{Re}(S_{11})$ and $\mathrm{Im}(S_{11})$ at pre-irradiation and after 300 krad exposure.

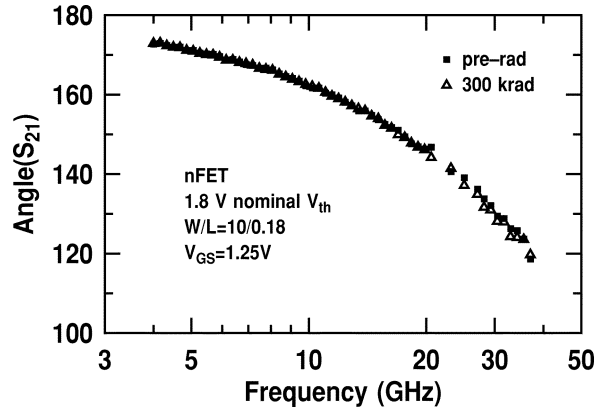

Fig. 7. Angle (S_{21}) versus frequency at $V_{GS} = 1.25$ V for the 10/0.18 nFET at pre-radiation and after 300 krad.

isolation, where a parasitic inversion channel is produced at sufficiently high damage, resistively shunting the source to the drain. Clearly, however, this device technology is robust to total-dose exposure up to at least 150 krad. Observe that there is almost no degradation in the linear $I_D - V_{GS}$ characteristics in this 10/0.18 nFET. Fig. 1 shows that the radiation-induced threshold voltage and transconductance degradation is negligible, as expected, since this device has very thin, high-quality gate oxide (3.5 nm in this case). Similar results can also be seen for the 10/0.18 nFET in 1.8 V high $V_{\rm th}$ configuration with the same gate oxide thickness but the higher pre-radiation threshold voltage.

To more closely examine the radiation-induced off-state leakage of the nFETs in the three different device configurations, we chose devices with identical geometry (10/10) for ease of comparison. As shown in Fig. 2, the normalized off-state leakage of the 10/10 nFET in the 3.3 V RF CMOS configuration increases much more quickly than in both the 1.8 V nominal $V_{\rm th}$ and the 1.8 V high $V_{\rm th}$ configurations, which is attributed to the reduced gate control on the shallow trench isolation edge in the 3.3 V RF CMOS configuration, due to its thicker gate oxide (6.8 nm in this case) [7], though these three design point devices have the identical edge termination configuration. That is, for the same amount of STI damage, the gate cannot as effectively deplete that parasitic leakage channel if the gate oxide thickness is increased.

Fig. 3 compares the radiation-induced threshold voltage shift ($\Delta V_{\rm th} = V_{\rm th,post} - V_{\rm th,pre}$) for the same 10/10 nFETs shown in Fig. 2 for the three different device configurations. Although $\Delta V_{\rm th}$ is small for all three devices, we can still see that the 10/10 nFET in the 3.3 V RF CMOS configuration has a larger threshold voltage shift (about 30 mV at 300 krad) than the other two configurations (about 11 mV at 300 krad), because the radiation damage on the thicker gate oxide (6.8 nm) of the 3.3 V RF CMOS configuration is much stronger than the thin gate oxide (3.5 nm) found in the two 1.8 V configurations. The $\Delta V_{\rm th}$ of 1.8 V nominal $V_{\rm th}$ device is slightly larger than that of 1.8 V high $V_{\rm th}$ device.

The effective channel mobilities ($\mu_{\rm eff}$) for these three device configurations were extracted as a function of gate overdrive using a recently proposed technique which is capable of taking into account the bias dependence of R_{SD} in LDD CMOS technologies [8]. The results are shown in Fig. 4 for both pre-radiation and after 300 krad total dose. The change of $\mu_{\rm eff}$ after irradiation is negligible for all three configurations. With increasing $V_{GS} - V_{\rm th}$ (i.e., vertical field), $\mu_{\rm eff}$ decreases rapidly, as expected. At $V_{GS} - V_{\rm th} = 0.6$ V, $\mu_{\rm eff}$ is 275, 305 and 330 $\mathrm{cm}^2/(\mathrm{Vs})$ for 1.8 V high $V_{\rm th}$, 1.8 V nominal $V_{\rm th}$, and 3.3 V RF CMOS configurations, respectively. The 1.8 V high $V_{\rm th}$ device has the smallest effective mobility due to the heavier doping in the channel required to reach the higher $V_{\rm th}$ value compared with the 1.8 V nominal $V_{\rm th}$, while the 3.3 V RF

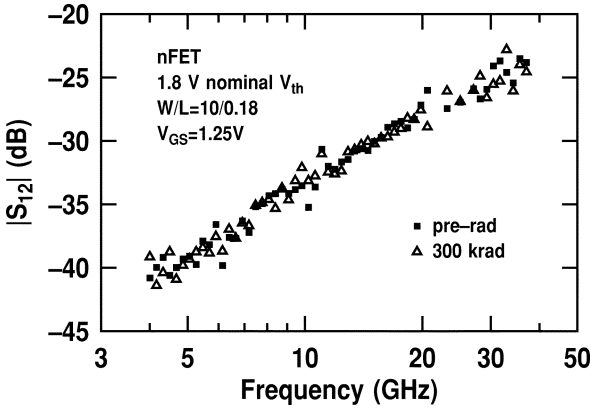

Fig. 8. S_{12} magnitude versus frequency at $V_{GS} = 1.25$ V for the 10/0.18 nFET at pre-radiation and post-radiation.

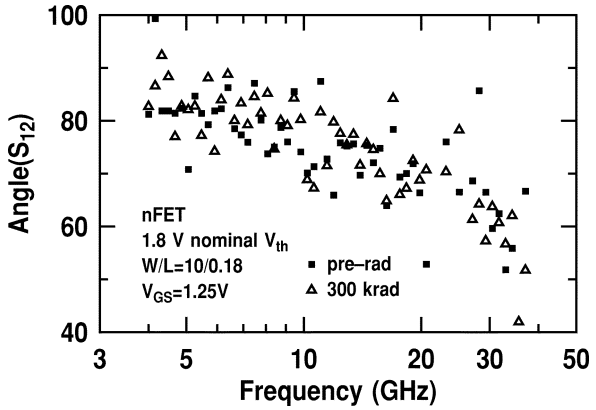

Fig. 9. Angle (S_{12}) versus frequency at $V_{GS} = 1.25$ V for the 10/0.18 nFET at pre-radiation and post-radiation.

CMOS configuration has the largest effective mobility due to the thicker gate oxide.

B. RF Performance

S-parameters are commonly used to characterize the electrical response of high frequency transistors. The important RF figures-of-merit of the transistors can be extracted from the measured S-parameters, after appropriate parasitic deembedding. The typical radiation response of the four S-parameters up to 300 krad in a 10/0.18 nFET of 1.8 V nominal $V_{\rm th}$ configuration is shown in Figs. 5–10. The other device configurations show a similar response. Fig. 5 shows the comparison of $\mathrm{Re}(S_{11})$ and $\mathrm{Im}(S_{11})$ before radiation and after 300 krad. We see that the S_{11} for the nFET always moves clockwise as frequency increases from 4 to 37 GHz because S_{11} is the reflection coefficient corresponding to the input impedance when the output is terminated with the characteristic impedance Z_0. After 300 krad radiation, there is only a slight increase of the S_{11}, which can be considered negligible.

Figs. 6 and 7 show the magnitude of S_{21} and the angle of S_{21} as a function of frequency at pre-irradiation and after 300 krad, respectively. The S_{21} magnitude decreases with increasing frequency, as expected, because of decreasing forward transducer gain. A small decrease of the S_{21} magnitude can be observed in Fig. 6 after 300 krad radiation, however there are no changes in the angle of S_{21} after radiation (Fig. 7).

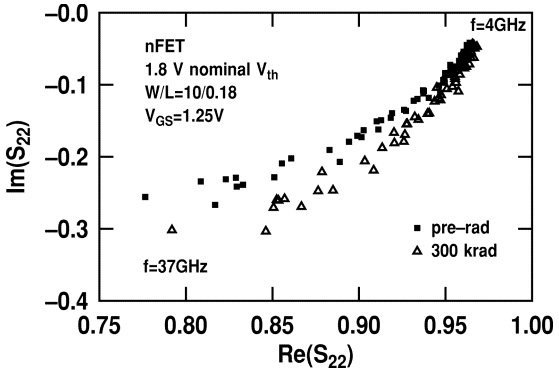

Fig. 10. Comparison of $\mathrm{Re}(S_{22})$ and $\mathrm{Im}(S_{22})$ at pre-radiation and after 300 krad.

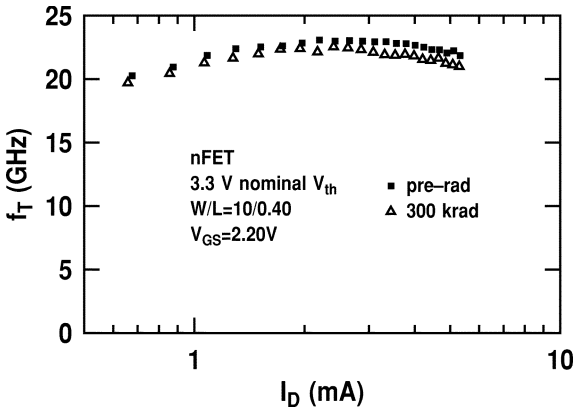

Fig. 11. The cutoff frequency as a function of drain current at pre-radiation and after 300 krad.

S_{12}, the reverse gain, increases with increasing frequency, as shown in Fig. 8, which plots its magnitude versus frequency. No radiation-induced degradation can be observed for both the S_{12} magnitude in Fig. 8 and the angle of S_{12} in Fig. 9.

S_{22} is essentially the output reflection coefficient looking back into the output port for a Z_0 source termination. The radiation response of S_{22} can be seen in Fig. 10. Both $\mathrm{Re}S_{22}$ and $\mathrm{Im}S_{22}$ decrease after radiation, although only slightly.

From an RF CMOS perspective, all of the S-parameters experience negligible degradation after 300 krad total dose exposure, suggesting that the RF CMOS device from this SoC CMOS technology is radiation hard for RF applications in the proton environment. The cutoff frequency f_T can be extracted from the measured S-parameters. For this 10/0.18 nFET presented above, the peak f_T is 55 GHz at pre-radiation and 53 GHz after 300 krad, yielding a negligible change in overall frequency response, as expected. The cutoff frequency f_T of a 10/0.40 nFET in 3.3 V configuration is shown in Fig. 11 before and after irradiation. Only a slight decrease of f_T can be observed for this 3.3 V configuration device after irradiation. The peak f_T is 23.5 GHz at pre-radiation and 23 GHz after 300 krad.

IV. Summary

The proton tolerance of the multiple-threshold voltage and multiple-breakdown voltage system-of-a-chip CMOS devices contained in a 0.18 μm SoC CMOS technology is presented. The radiation response of the CMOS devices having three

different device design configurations were characterized and compared for equivalent gamma doses up to 300 krad(Si), using the threshold voltage, off-state leakage, and effective mobility to assess *dc* performance. All three CMOS device configurations show a very slight degradation of threshold voltage and effective mobility with increasing dose. The transistor frequency response and S-parameters of these RF CMOS devices show little degradation up to 300 krad(Si) total dose. These results suggest that the multiple CMOS devices in this 0.18 μm SoC CMOS technology are well-suited for RF circuit applications in an ionizing radiation environment without intentional total-dose hardening.

ACKNOWLEDGMENT

The devices were fabricated at IBM Microelectronics. The authors would like to thank L. Cohn and K. LaBel for their support of this work.

REFERENCES

[1] P. H. Woerlee, M. J. Knitel, R. Langevelde, D. B. M. Klaassen, L. F. Tiemeijer, A. J. Scholten, and A. Duijnhoven, "RF-CMOS performance trends," *IEEE Trans. Electron Devices*, vol. 48, pp. 1776–1782, Aug. 2001.

[2] A. Joseph, D. Coolbaugh, M. Zierak, R. Wuthrich, R. Geiss, Z. He, X. Liu, B. Orner, J. Johnson, G. Freeman, D. Ahlgren, B. Jagannathan, L. Lanzerotti, V. Ramachandran, J. Malinowski, H. Chen, J. Chu, P. Gray, R. Johnson, J. Dunn, S. Subbanna, K. Schonenberg, D. Harame, R. Groves, K. Watson, D. Jadus, M. Megheli, and A. Rylyakov, "A 0.18 μm BiCMOS technology featuring 120/100 GHz (f_T / $f_{\max}$) HBT ans ASIC-compatible CMOS using copper interconnect," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Minneapolis, MN, Sept. 2001, pp. 143–146.

[3] K. M. Muray, W. J. Stapor, and C. Castenada, "Calibrated charge particle measurement system with precision dosimetric measurement and control," *Nucl. Instrum. Methods*, vol. B56/57, p. 616, 1991.

[4] P. W. Marshall, C. J. Dale, M. A. Carts, and K. A. Label, "Particle-induced bit errors in high performance fiber optic data lines for satellite data management," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1958–1965, Dec. 1994.

[5] S. Zhang, G. Niu, J. D. Cressler, S. D. Clark, and D. C. Ahlgren, "The effects of proton irradiation on the RF performance," *IEEE Trans. Nucl. Sci.*, vol. 46, pp. 1716–1721, Dec. 1999.

[6] W. E. Ansley, "Microwave Characterization and Modeling of Silicon-Germanium Heterojunction Bipolar Transistor," Ph.D. dissertation, Auburn Univ., Auburn, AL, 1998.

[7] J. D. Cressler, R. Krithivasan, G. Zhang, G. Niu, P. W. Marshall, H. S. Kim, R. A. Reed, M. J. Palmer, and A. J. Joseph, "An investigation of the origins of the variable proton tolerance in multiple SiGe HBT BiCMOS technology generations," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3203–3207, Dec. 2002.

[8] G. Niu, J. D. Cressler, S. J. Mathew, and S. Subbanna, "Total resistance slope-based effective channel mobility extraction method for deep submicrometer CMOS technology," *IEEE Trans. Electron Devices*, vol. 46, pp. 1912–1914, Sept. 1999.