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***Abstract*—Wide bandgap semiconductors enable high voltage (10 kV and more) switches. As a consequence, new packaging solutions are required to prepare the ground for such devices. The metallized ceramic substrate is a well-known and established technology for voltages up to 3.3kV, but it exhibits some weaknesses at higher voltages: due to its manufacturing process, the profile of the metallization is sharp and induces a reinforcement of the electric field at the "triple point" area (where the ceramic, the conductor and the encapsulating material meet), which can lead to Partial Discharges (PD), eventually causing a failure of the module. In this paper, we present a new substrate structure, where the triple point is moved away to an area where the electric field is lower. In this structure, the ceramic is machined to form protrusions, and round-edge metallizations are brazed on top. The design of the substrate, based on finite-elements is described, and calculations show that a 1 mm-thick AlN layer should be sufficient to withstand 10 kV. The manufacturing process of this substrate is presented. The test results demonstrate the superiority of this new solution, with a partial discharge inception voltage increased by 38 %.**

I. Introduction

Thanks to their physical properties [1], wide bandgap semiconductors enable power devices with voltage ratings exceeding 10 kV. Among these materials, silicon carbide (SiC) is the most technologically advanced, and some high voltage SiC devices have already been demonstrated (10 kV for unipolar devices, 15 kV for bipolar devices [2]). In this paper, we investigate packaging solutions for a 10 kV-rated SiC transistor. In particular, we focus on the metallized ceramic substrate, which concentrates electrical and thermal stresses.

Two phenomena limit the voltage an isolating layer can sustain. The most obvious is the voltage breakdown, which occurs when the electric field exceeds the capability of the material, resulting in arcing, and immediate failure of the isolation. A less energetic phenomenon is the partial discharge (PD). It does not result in immediate breakdown, but the accumulation of PDs over a long time may result in a gradual degradation of the material. Partial discharges that occur in the isolating materials lead to a decreasing of the lifetime [3]. Studies show that partial discharges mainly happen at the edges of the metallizations [4], [5].

A possible solution to avoid both voltage breakdown and partial discharge is to reduce the electric field experienced by the insulating layer, by making this layer thicker. In the case of the ceramic substrate, this solution is un-practical: the ceramic substrate is used to evacuate the heat dissipated by the semiconductor devices. Making it thicker would result in degraded thermal performances. In [6], we showed that although SiC devices can in theory operate at very high temperature, it strongly affects the performances of unipolar devices. As a consequence, junction temperatures of more than 100 °C are not desirable. Such temperature can be achieved using a very efficient cooling system, which (among other things) requires thin ceramic layers.

Proper material selection is very important: among the various ceramics used in power electronic substrates, large differences can be observed regarding dielectric strength (20 to 40 kV/mm) and thermal conductivity (28 to 175 W/m.K) [7]. Overall, Aluminium Nitride (AlN) is found to be the best material on both counts. This is the material we selected for this study.

Another way to increase the Partial Discharge Inception Voltage (PDIV) is to add coatings of a specific material whose properties (*e.g.* permittivity in [8], resistivity in [9]) allow a relaxation of the electric field, especially at the triple poin (where the ceramic, the conductor and the encapsulating material meet). In the present study, we investigated an alternative approach, in which we alter the geometry of the structure so that the maximum electric field no longer occurs at the triple point.

In the next section, we present data regarding some industrial substrates (with a standard manufacturing process), which are used as a reference. In section III, we use simulation to design and optimize a new substrate structure. In section IV we describe the manufacturing process of this substrate. Test results are given in section V.

II. Industrial Grade Substrates

Partial discharge measurements were performed according to IEC 60270 standard to evaluate the PDIV according to the ceramic thickness. The test vehicles are AMB AlN substrates with a 20 mm copper disc on the top and a 34mm square shape on the bottom side. Two AlN thicknesses are investigated (0.635 mm and 1 mm). The PDIV is found to be 5.02 kV and 5.95 kV for 0.635 and 1 mm-thick AlN ceramic respectively. This is almost 3 times lower than the dielectric strength of the material as quoted by its manufacturer (20 kV/mm).

The cross section of one of the industrial substrates is presented in Fig. 1. It shows the edge of a copper track, which forms an acute angle at the interface with the ceramic (the "triple point"). This is reinforced by the active metal braze layer (Fig. 1, bottom), which forms a thin protrusion.

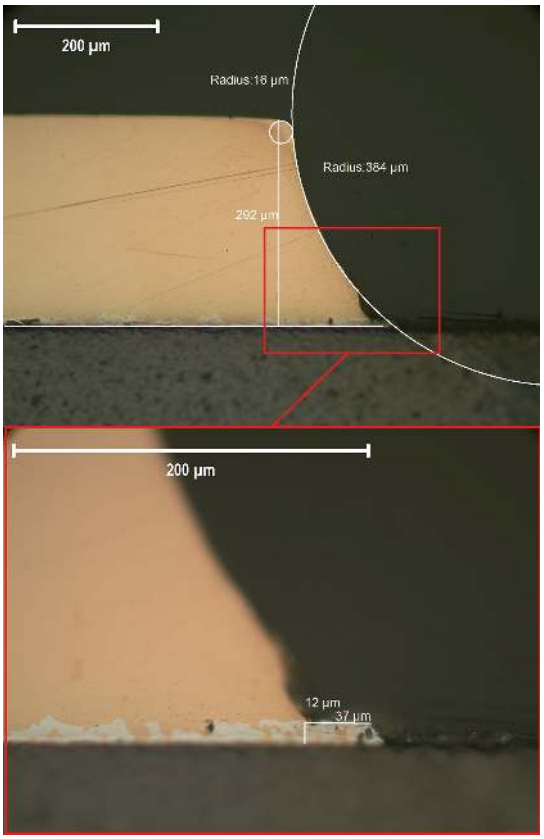


Fig. 1: Cross section of an industrial AMB substrate, showing that the edge of the metallization is sharp, due to the etching process.

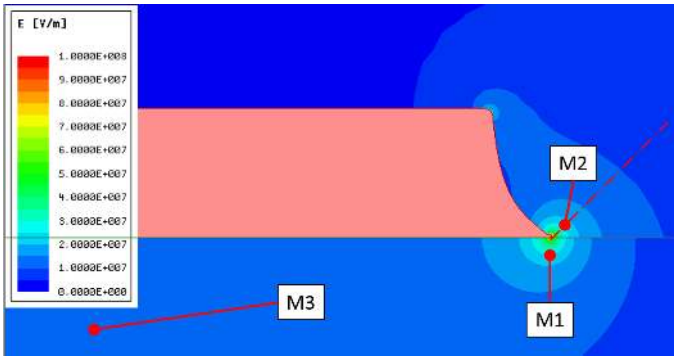


Fig. 2: FEM simulation of an industrial-grade substrate showing the field reinforcement at the edge of the metallization. The mesh was defined so that within 100 μm distance from the triple point, no element is allowed to exceed 1 μm in size, to limit singularity issues.

TABLE I: Simulated electric field intensity (kV/mm) for both ceramic thicknesses, in the PDIV test conditions.

	M1	M2	M3
635 μm @ 5.02 kV	26.90	23.38	7.91
1000 μm @ 5.95 kV	25.03	22.19	5.95

TABLE II: Simulated electric field (kV/mm) intensity for both ceramic thicknesses, with 10 kV applied.

	M1	M2	M3
635 μm @ 10 kV	53.58	46.58	15.75
1000 μm @ 10 kV	42.06	37.29	10.0
2000 μm @ 10 kV	29.12	26.31	5.0

This geometry was then reproduced in the Ansys Maxwell simulation environment (finite elements modeling, FEM). Electrostatic conditions were used, with a relative permittivity of 9 for the AlN and 1.96 for the environment material (corresponding to the Galden HT270 dielectric fluid used during the tests). The backside electrode was kept at 0 V, while the topside was raised at the measured PDIV values. With FEM, the actual electric field values at singular points (such as the triple points) are known to be strongly dependent on the mesh resolution (basically, the finer the mesh, the higher the electric field). To avoid this problem, we assessed the electric field intensity at 2 key locations, slightly away from the triple point (Fig. 2): M1 (located in the ceramic, 15 μm under the triple point), M2 (in the encapsulant, 15 μm from the triple point, following a 45° line). In addition, we placed the point M3 in the middle of the ceramic, where the electric field is uniform.

The simulation results are summarized in table I. The electric field intensity at M1 is consistent with the dielectric strength of the AlN (quoted at 20 kV/mm, but with measured values as high as 40 kV/mm [7]). The field at M3 is equal to the applied voltage divided by the ceramic thickness, which indicates that the electric field is indeed uniform there. Furthermore, the electric field values calculated at M1 and M2 are very close for 0.635 mm and 1 mm thick substrates, while they differ for M3. This indicates that the partial discharges occur probably at the periphery of the metallization.

The next step is to simulate the same structure, this time with 10 kV applied between the electrodes. The results are given in the first two rows of table II. The electric field values at M1 and M2 far exceed the values in table I (53.58 or 42.06 kV/mm for M1, vs $\approx$ 26 in table I). Then, we simulated the same structure, with increasingly thick ceramic layers, in order to evaluate the ceramic thickness which would be required to sustain 10 kV. For these simulations, we assumed that the partial discharge inception voltage is reached for the same electric field values at points M1 as in table I. According to these simulations, a 10 kV-rated substrate would require an AlN layer thicker than 2 mm (last row in table II). From a thermal point-of-view, this means (at least) doubling the thermal resistance compared to a 1 mm-thick ceramic. Furthermore, 2 mm-thick ceramic is out of the manufacturer's standards. As a consequence, it is considerably more expensive.

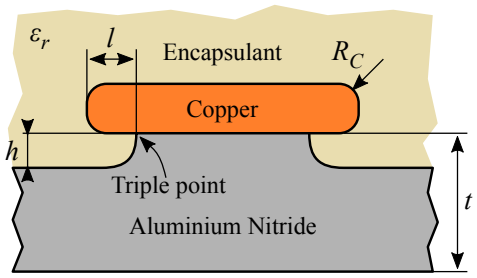


Fig. 3: Schematic view of the protruding structure, with the 5 design parameters under investigation.

III. Design of a new structure

A. Presentation of the structure

The main weakness of the standard structure, described in the previous section, is the reinforcement of the electric field caused by the sharp edge of the metallizations. In the structure presented in Fig. 3, the metallization is brazed on top of a protrusion in the ceramic. With this structure, the triple point is moved away from the edge of the metallization, so it is no longer at the place where the electric field is the strongest. In addition, the metallizations have rounded edges to limit the reinforcement of the electric field. Finally, this (smaller) reinforcement occurs in the encapsulant (silicone gel), which has a higher dielectric strength than the ceramic (50 kV/mm vs. 20 kV/mm).

B. Optimization of the structure

A Design of Experiment (DoE) approach was followed using a simple full factorial plan to identify the effect of each parameter as well as their possible interactions. The corresponding parametric simulations were run, and the resulting maximum electric field intensities in the encapsulant and in the ceramic were recorded (for this structure, because of the rounded geometry, there is no numerical singularity which could cause infinite field reinforcement). In the full version of the DOE (not presented here for the sake of clarity), 5 parameters were assessed (Fig. 3):

- the edge curvature of the metallization (radius R_c);
- the relative permittivity of the encapsulating material (ε_r);
- the thickness of the ceramic (t);
- the height of the protrusion (or rather the depth of the recess surrounding the protrusion, as the ceramic thickness was considered including the protrusion) h;
- the length of the copper extension (l).

In this analysis, h and l were found to have an almost negligible effect. h was set at 150 μm to form a visible protrusion and facilitate manufacturing. l was set at 500 μm because of the manufacturing tolerances. As a consequence, this section will only discuss the effect of R_C, ε_r and t.

The values used for the parameters are listed in Table III. For R_C, the minimum value (6 μm) corresponds to an almost perfect square edge (but allows to avoid numerical singularities), while 250 μm corresponds to the maximum value for a 500 μm-thick metal layer. For ε_r, values were chosen between 1 (vacuum) and 9 (permittivity of AlN). For t, we investigated both thicknesses we had (so we could use exactly the same ceramic material as the tests in section II): 0.635 and 1 mm.

TABLE III: Values used for the optimization of the protruding structure.

	Rc (μm)	*ε_r*	*t (mm)*
Low Value	6	1	0.635
High Value	250	9	1

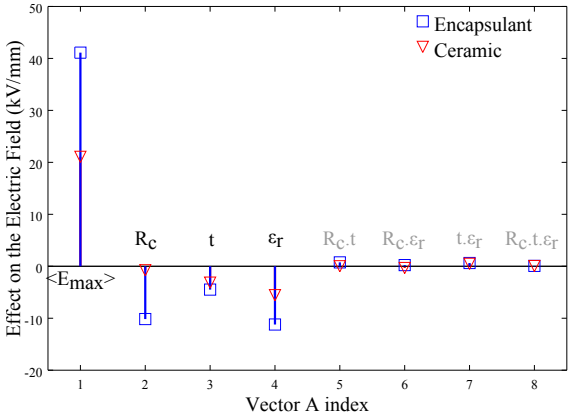


Fig. 4: Effect of each parameter on the maximum electric field (with 10 kV applied). Increasing R_C, t, or ε_r was found to decrease the maximum electric field in both the encapsulant and the ceramic. No significant interaction (bars 5 to 8) was found.

The results of the simulations are presented in Figs. 4 and 5.

The vector A in Fig. 4 is the result of the DoE. The first value A(1) is the maximum value of the electric field in the encapsulant and in the ceramic, averaged over all the simulations. Values A(2) A(3) and A(4) are respectively the sensibility of the electric field to the curvature of the copper electrode, to the ceramic thickness and to the relative permittivity of the encapsulant. All three parameters have negative effects, which means that the maximum electric field

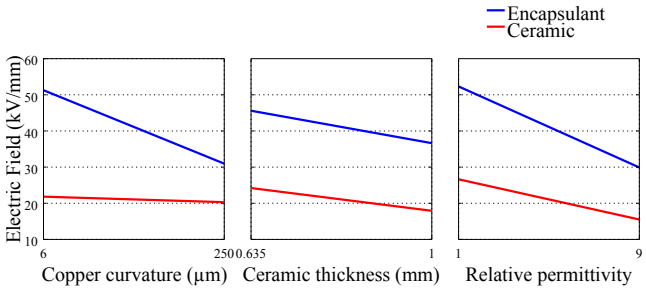
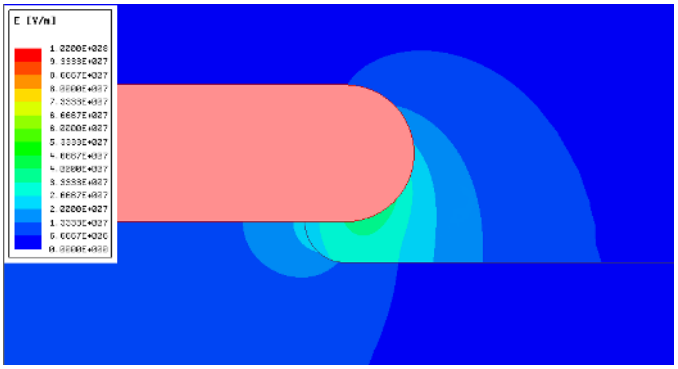
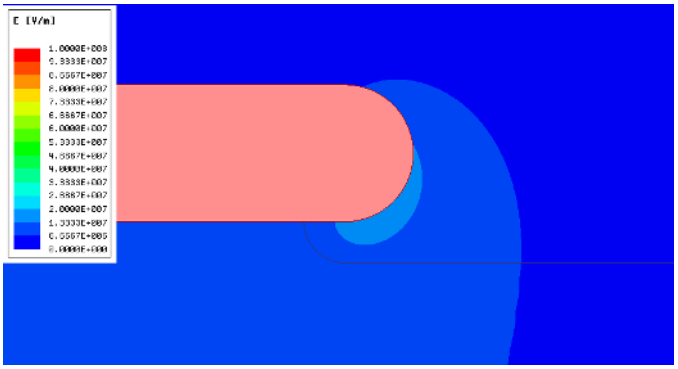


Fig. 5: Individual effect of R_C, t and ε_r on the average maximum electric field in the encapsulant and in the ceramic.



(a)



(b)

Fig. 6: Examples of electric field distribution for two protruding substrate configurations: $R_C = 250$ μm, $t = 1$ mm, and $\varepsilon_r = 1$ (a) and $\varepsilon_r = 9$ (b), for a 10 kV voltage applied.

is found to decrease when any of these parameters increase. The remaining values (A(5) to A(8) are coupled effects, which are found to be negligible. This means that the parameters produce independent effects.

Another way to present the results is given in Fig. 5. It confirms that the curvature of the copper electrode has a strong effect on the maximum electric field in the encapsulant, but not so much in the ceramic. This makes sense, because in the protruding structure, the field reinforcement caused by the copper metallization occurs in the encapsulant. Increasing the ceramic thickness is also beneficial, because the voltage is applied across a thicker structure. Finally, increasing the relative permittivity of the encapsulant reduces the maximum electric field density in both the encapsulant and the ceramic.

Two examples of electric field distributions are given in Fig. 6. It can be seen that compared with the industrial substrate (Fig. 2), the electric field experienced by the ceramic substrate is much lower in the case of the protruding substrate: the maximum electric field is 22.53 kV/mm for Fig. 6a and 11.78 kV/mm for Fig. 6b (as compared with 42.06 kV/mm for the industrial substrate, Fig. 2). For the encapsulant, the maximum electric field is similar for $\varepsilon_r = 1$ (Fig. 6a, 37.49 kV/mm, the max. electric field in the industrial substrate being 37.29 kV/mm, see Tab. II), but much lower for $\varepsilon_r = 9$ (Fig. 6b, 16.95 kV/mm).

As a result, the best substrate was found to have $R_C = 250$ μm and $t = 1$ mm. Changing the the relative permittivity of the encapsulant, would require mixing it with some high permittivity material (such as $BaTiO_3$), but this would require an entiere development altogether, and was considered out of the scope of this paper. For the practical tests, the encapsulant will be used as is ($\varepsilon_r = 2.5$).

IV. Fabrication of the Test Vehicles

Because of their un-conventional structure, the substrates investigated in this paper required a different manufacturing process, which was performed in-house. Here are the main process steps.

A. Preparation of the Parts

To form the protrusion in the ceramic, 1 mm AlN tiles were machined by a specialized company (Sceram, France). The ceramic tiles come from the same mastercard as that used in section II, to guarantee consistent results. The curvature of the 150 μm-tall protrusion is naturally formed by the grinding tool. No noticeable cracks was observed on the surface of the tile. Some small dents were visible on the rim of the protrusion, but were not considered critical. The surface roughness of the machined area was measured (Bruker Dektak 150) at $R_a = 0.6$ μm, which is acceptable for our procedure. Note that mechanical machining was chosen for our prototypes because it was simpler. In the case of industrial production, the protrusion would be made either by patterning the ceramic prior to sintering (net shaping) or by chemical etching (AlN can be etched by strong alkalies). In the case of chemical etching, it could be performed after the metallizations are bonded, so they can be used as masks ("self aligning process").

For the metallization, 20 mm, 500 μm-thick copper disks with rounded edges were machined by another specialized company (Micro-tollerie Dallard, France). Preforms of the active metal braze alloy (TKC-651 Tanaka, Japan, a AgCuSnTi alloy with a melting point of 770 °C) were cut using a 16 mm punch.

B. Assembly of the Substrates

To align the copper disk, brazing preform and AlN tile, an alignment device (Fig. 7) was designed. Because of the high temperature experienced during the brazing process (800 °C), a machinable vitroceramic (Macor, Corning Inc.) was used to form the main parts of the device (graphite is probably also suitable). A small hole was machined in the bottom part to receive a thermocouple for process control.

A metal weight is used to ensure a good contact between the parts to join. Tungsten was chosen because of its density (19.3 g.cm^{-3}), to form a small (10 mm heigh by 19.5 mm diameter), yet heavy (60 g) cylindrical weight. Small size is required because of the limited height available in the furnace (Jipelec jetfirst 100 rapid thermal annealing furnace). A picture of the assembly placed in the furnace is shown in Fig. 8.

The bonding process is performed in vacuum (the chamber is evacuated and filled with N_2 three time, to lower the residual

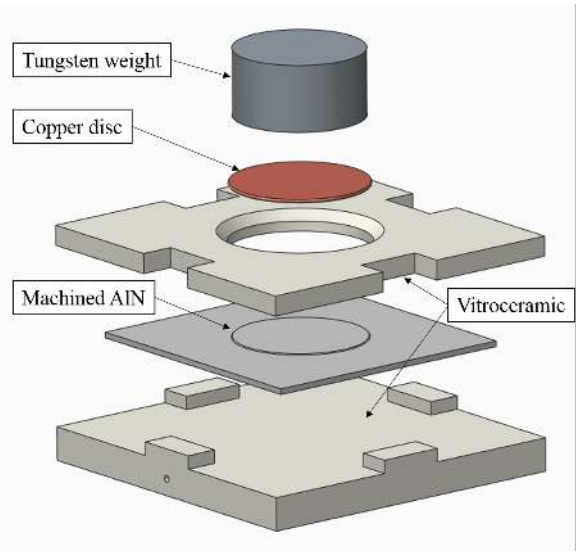


Fig. 7: Exploded CAD view of the alignment device designed to align the copper disk and the AlN tile (brazing preform not shown).

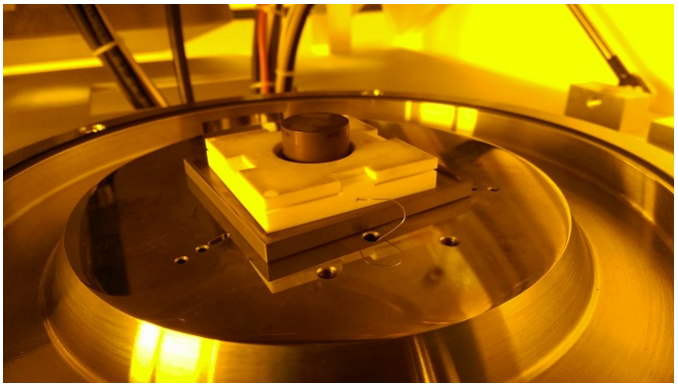


Fig. 8: The ceramic tile, the brazing alloy foil and the copper plate are placed in the alignment jig. A 60g tungsten weight is placed on the top of the assembly. Photograph taken in the furnace, prior to the brazing process.

oxygen concentration, and then evacuated once more). The process temperature profile (Fig. 9) was defined as follows: A slow ramp (up to the 1500 s mark) is used to bring all the parts to a uniform temperature (700 °C), slightly below the melting point of the solder alloy. This temperature is maintained for 250 s, to further improve temperature uniformity. Then, the temperature is rapidly raised to 800 °C, and maintained for 300 s, to perform the brazing step. A controlled cooling-down is enforced down to let the brazing alloy to solidify, followed by natural cooling.

A photograph of the substrate after assembly is visible in Fig. 10.

C. Connection/Encapsulation of the Test Vehicles

After assembly, the substrates were prepared for the dielectric tests. First, a metallization was applied on the backside

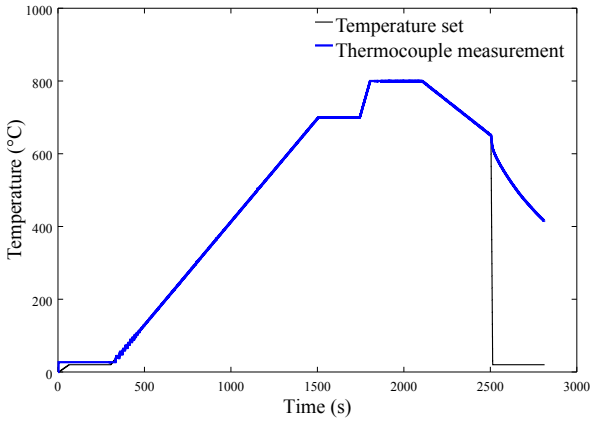


Fig. 9: Temperature profile during the brazing process, as a function of time. Black: set temperature, blue: measured (they only differ during cooling-down, which is un-controlled).

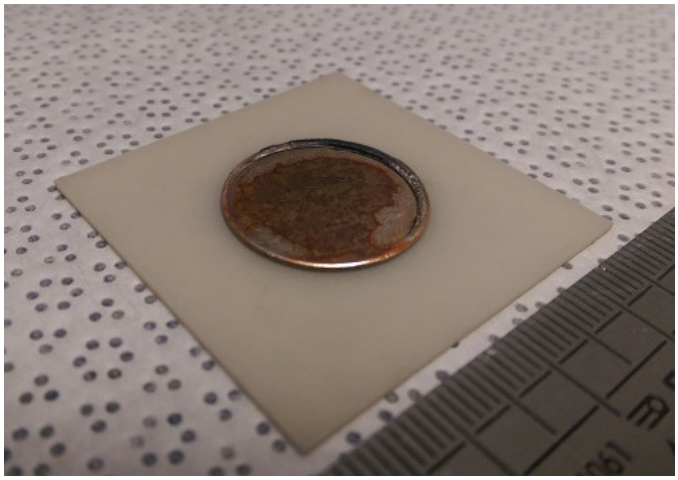


Fig. 10: Substrate after the brazing process.

of the ceramic to form a second electrode (the first being the brazed copper disk). The edges of the ceramic were masked with some polyimide tape, and a Ti/Ag coating (20 nm/500 nm) was applied by evaporation (Alliance Concept EVA 300).

Then, metal terminals (4 mm screws) were bonded on the electrodes using a conductive epoxy glue (Epo-Tek E4110) for easy connection to the test system. Finally, the substrates were encapsulated in a Silicone elastomer (Wacker Elastosil RT 745). This material was chosen because of its high dielectric strength (50 kV/mm), because it is easy to handle (not sticky in cured form) and because it is rigid enough not to need mechanical support (it is an elastomer, not a gel). For the encapsulation, the substrates were placed in molds formed by PTFE plates assembled with polyimide tape. The two parts of the silicone elastomer were mixed, degassed under vacuum for 15 minutes, and then poured in the molds. After a second degassing step (15 min), the molds were placed for curing at 100 °C for 40 min.

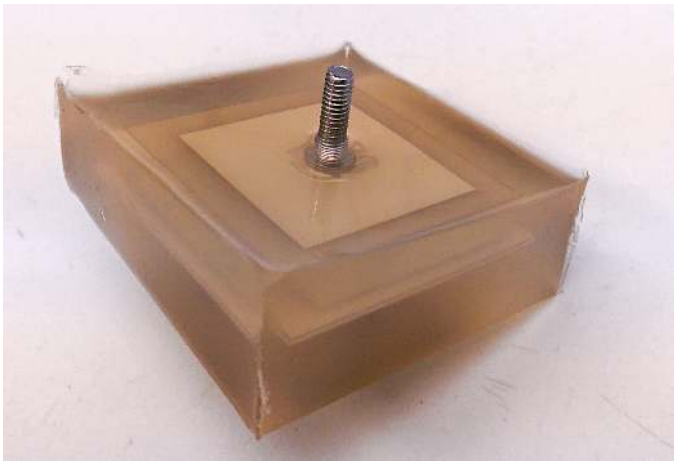


Fig. 11: Photograph of a test vehicle with the substrate (showing the square backside Ti/Ag metallization), equipped with bonded terminals, and encapsulated in silicone elastomer. Approximate size of the silicone block: 50x50x20 mm^3.

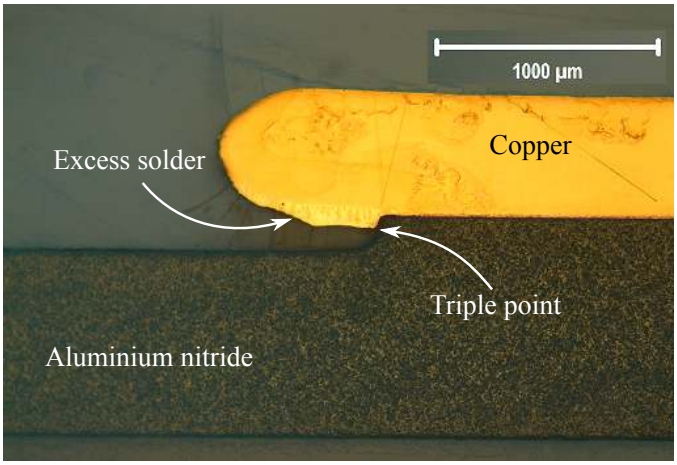


Fig. 12: Cross section of the protruding substrate. The quality of the metal-ceramic interface is satisfying, with no visible void. An excess of brazing alloy is visible at the bottom of the copper electrode, but the solder alloy did not flow over the ceramic, producing a clear triple point (albeit a bit lower than expected.

A photograph of the test vehicles (after removal of the PTFE molds), ready for dielectric testing is presented in Fig. 11. In total 8 test vehicles were prepared (4 with silicone encapsulant, 4 without).

The cross section of one substrate is shown in Fig 12. The brazing process is found to produce a good bondline (no voiding was observed). Some of the solder alloy flowed out of the interface, and was found to follow the copper electrode. In some cases, such as in Fig. 10, solder residues can even be observed on top of the electrode. This is not a major issue, as the solder does not flow over the ceramic (this would have much more impact on the distribution of the electric field).

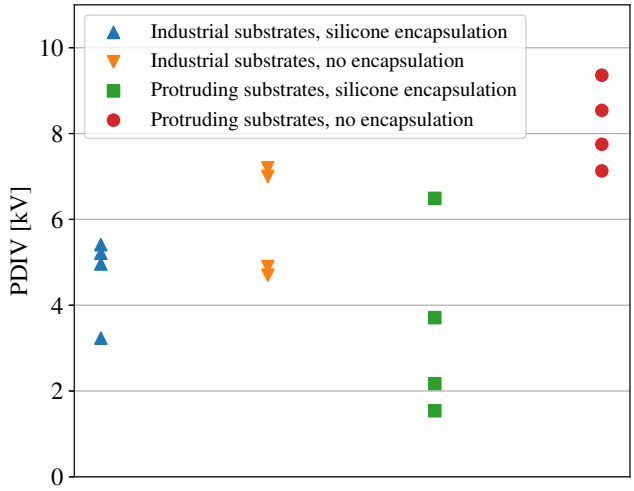


Fig. 13: Partial Discharge Inception Voltage (PDIV) measurements (10 pC) for 4 substrates configurations: industrial substrates with and without silicone encapsulant and protruding substrates, with and without silicone encapsulant. Non encapsulated substrates were immersed in a bath of dielectric fluid for testing.

V. Partial Discharge Measurements

Partial Discharge measurment were performed at the LAPLACE laboratory (Paul Sabatier University, Toulouse) using an ICMsystem (Power Diagnostix Systems GmbH) measurement device. The un-encapsulated test vehicles were clamped between two metallic spheres where the potentials are applied. The clamping device was then immersed in a bath of dielectric fluid (Galden HT270 or Novec 649) to avoid any surface discharge along the test vehicle. For the encapsulated samples, the connection was made using crocodile clamps on the terminals. In both cases, the test vehicles were then carefully placed in a metallic enclosure to avoid most of the electromagnetic perturbations.

The voltage (AC 50 Hz) was slowly raised (manual control) until 10 pC PDs occurred. A 30 s pause at this first PDIV allowed for some relaxation of the charges in the test vehicle. The voltage was then decreased back to 0 V. After this first cycle, the actual PDIV value at 10 pC was measured by increasing the voltage until continuous 10 pC discharges were observed.

The results of the measurements are presented in Fig. 13. 4 configurations were evaluated, each with 4 test vehicles: two configurations with industrial substrates (those presented in section II), with RT 745 silicone encapsulation, and without any encapsulant (in this case, the test vehicles were immersed in some Galden HT270 dielectric fluid to prevent arcing or partial discharges in air); two configuration with the protruding substrates, also with and without encapsulant (for practical reasons, the dielectric fluid used was Novec 649). In all 4 configurations, the top electrode had a round shape (20 mm in diameter) and the AlN thickness was 1 mm (under the

electrode, in the case of the protruding substrate).

The following conclusions can be drawn from the data in Fig. 13:

- The silicone encapsulant tends to degrade the PDIV value (average value 5.95 kV for non encapsulated industrial substrates vs. 4.70 kV for encapsulated ones; 8.20 kV for non encapsulated protruding substrates, 3.48 kV for encapsulated ones). This indicates a poor quality of the encapsulant or of the encapsulant/substrate interface (for example, trapped air bubbles or delamination of the interface). This might be due to insufficient degassing, or to contamination at the surface of the ceramic.
- The protruding structure appears to be more sensitive to the quality of the encapsulation than the industrial substrates (PDIV reduced by 58 % when encapsulating the protruding structure and only by 21 % when encapsulating industrial substrates). This could be expected because with the protruding structure, all the electric field reinforcement occurs in the encapsulant.
- Because of this higher sensitivity to the quality of the encapsulant, and because our encapsulation was not so good, the experimental data is very dispersed for the encapsulated protruding substrates (PDIV ranging from 1.54 to 6.49 kV).
- Non-encapsulated protruding substrates perform much better than any other configuration. This proves the potential of the structure, with PDIV near the objective (10 kV), using a 1 mm AlN substrate.
- The absolute experimental scattering for non-encapsulated, protruding substrates (2.23 kV) is comparable to that of the industrial substrates. This means that the "in-house" brazing process did not introduce major defects (such as large voids at the interface).

Breakdown tests (where the voltage is increased up to the failure of the test vehicle) were performed for the encapsulated test vehicles (protruding and industrial substrates). No significant difference was found: 21.9$\pm$1.7 kV for the protruding substrate, 24.2$\pm$0.9 kV for the standard substrate. This means that the poor quality of the encapsulant and the thinner ceramic layer (0.85 mm vs.1 mm) outside of the protrusion had little effect on the breakdown voltage of the substrate.

VI. Conclusion

The structure of metallized ceramic substrates available in the industry for power electronic applications is not very well suited to high voltage (10 kV) because of the sharp edges of the copper metallizations. In this paper, we introduced a new structure, with a protrusion in the ceramic. A metallization (with rounded edges) is brazed on this protrusion. With this structure, the "triple point" is located in an area where the electric field is lower, and the maximum electric field occurs in the encapsulant (which has a higher dielectric strength than the ceramic).

The design and manufacturing of this new structure has been detailed. The results of the testing show that although the silicone encapsulation was not satisfying, the proposed structure shows very promising results, with a PDIV clearly better than industrial substrates produced on the same ceramic material (average PDIV 8.2 kV for the protruding substrate, 5.95 kV for the industrial substrate). Further improvement can be expected with proper encapsulation, especially if the relative permittivity of the encapsulant can be increased to approach that of the AlN ceramic ($\varepsilon_r = 9$).

The protruding structure allows for the use of thin ceramic layers (1 mm for 10 kV-rated modules), resulting in lower thermal resistance and therefore better cooling of the semiconductor devices.

VII. Acknowledgement

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