Pseudo-Three-Stage Miller Op-Amp With Enhanced Small-Signal and Large-Signal Performance

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***Abstract*— A simple technique to implement highly power efficient class AB–AB Miller op-amps is presented in this paper. It uses a composite input stage with resistive local common mode feedback that provides class AB operation to the input stage and essentially enhances the op-amp's effective transconductance gain, the dc open-loop gain, the gain-bandwidth product, and slew rate with just moderate increase in power dissipation. The experimental results of op-amps in strong inversion and subthreshold fabricated in a 130-nm standard CMOS technology validate the proposed approach. The op-amp has 9 V·pF/μs·μW large-signal figure of merit (FOM) and 17 MHz · pF/μW small-signal FOM with 1.2-V supply voltage. In subthreshold, the op-amp has 10 V · pF/μs · μW large-signal FOM and 92 MHz · pF/μW small-signal FOM with 0.5-V supply voltage.**

***Index Terms*— Analog integrated circuits, class AB–AB Miller op-amps, Miller compensation, resistive local common mode feedback.**

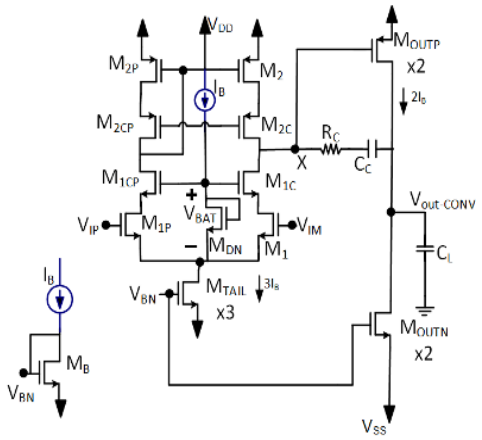

Fig. 1. Conventional high gain class-A two-stage Miller op-amp with telescopic input stage.

I. Introduction

THE increasing demand for battery-operated portable electronics equipment requires power-efficient analog circuits. The operational amplifier (op-amp) is the essential building block of analog signal processing units [1], [2]. Due to the reduction of the supply voltage in deep sub-micrometer mixed-signal design, the op-amp may suffer from slew rate limitation, insufficient bandwidth, lower gain, reduced dynamic range, inadequate noise performance, and linearity problems [3]. Hence, the energy-efficient high-speed op-amp design is a challenging task for the analog designer in today's energy-constrained electronic world. Along with the low power and high speed, the op-amp must have a large-signal swing, high linearity, and high load driving capability. To achieve close to rail-to-rail output swing in low-voltage applications, a two-stage Miller op-amp is a wise choice. In this paper, a simple design approach of a Miller op-amp is presented to enhance gain-bandwidth product (GBW) by a large factor (63 times in the circuit presented here) and the dc open-loop gain by about one order of magnitude with just moderate increase (∼factor 2) in static power dissipation with respect to the conventional op-amp of Fig. 1. The approach also provides class AB operation to the input stage, improving the slew rate (SR). The efficiency of the op-amp is validated by measurements of a test chip and compared to other op-amps reported in the literature in terms of three figures of merit (FOMs): 1) the large-signal $\text{FOM}_{\text{LS}} = (\text{SR}.C_L)/P_Q$, where P_Q is the total static power dissipation and C_L is the load capacitance; 2) the small-signal $\text{FOM}_{\text{SS}} = (\text{GBW}.C_L)/P_Q$; and 3) a global FOM $\text{FOM}_G = (\text{FOM}_{LS}\text{FOM}_{SS})^{1/2}$. In order to account for silicon area and total quiescent current ($I_{\text{Total}Q}$), four additional FOM are also reported here: $\text{AFOMs} = (\text{SR}.C_L)/(P_Q.\text{Area})$, $\text{AFOM}_L = (\text{GBW}.C_L)/(P_Q.\text{Area})$, $\text{IFOMs} = (\text{GBW}.C_L)/(I_{\text{Total}Q})$ [4], and $\text{IFOM}_L = (\text{SR}.C_L)/(I_{\text{Total}Q})$ [4].

This paper is organized as follows. Section II summarizes the limitations of a conventional two-stage class-A Miller op-amp. Section III describes the proposed op-amp designed

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in 130-nm CMOS technology operating in strong inversion with ±600-mV dual supplies and a bias current $I_B = 14\ \mu$A; and in subthreshold with ±250-mV supply voltages and a bias current $I_B = 70$ nA. Section IV presents simulation results. Section V provides the experimental results of test chip prototypes of the proposed and conventional op-amps both in strong inversion and subthreshold. Conclusions are drawn in Section VI.

II. Two-Stage Class-A Miller Op-Amp

A two-stage Miller op-amp with a telescopic input stage is shown in Fig. 1. This circuit can provide high open-loop dc gain, $A_{\text{OLDC}} \sim (g_m r_0)^3/4$, where g_m and r_0 are transconductance gain and output resistance of a unit size transistor, respectively. For simplicity, the parameters g_m and r_0 are considered equal here for all unit size transistors. It also provides a moderate gain bandwidth product (GBW).The GBW of the class A op-amp of Fig. 1 can be obtained from its dc open-loop gain and the dominant pole at node X is given by the following equation:

$$f_{\text{PDOM}} = 1/(2\pi R_X C_X). \tag{1}$$

Here, $R_X = g_m r_0^2/2$ is the impedance at node X and C_X is the Miller capacitance given by the following equation:

$$C_X = (1 + A_{II})C_C. \tag{2}$$

Here, $A_{II} = g_m r_0/2$ is the gain of the output stage. As the dc open-loop gain of the op-amp is $A_{\text{OLDC}} = (g_m r_0)^3/4$, the gain-bandwidth product is $\text{GBW}_{\text{cnv}} = g_m/2\pi C_C$. The high-frequency pole f_{Pout} at the output node of the op-amp is given by the following equation:

$$f_{\text{POut}} = g_{m\text{OUTP}}/(2\pi C_L) \tag{3}$$

Here, $g_{m\text{OUTP}}$ is the transconductance gain of the pMOS output transistor M_{OUTP} and C_L is the load capacitance. To achieve a high phase margin PM $> 50°$ when the zero introduced by C_C is shifted to infinity (by selecting $R_C = 1/g_{m\text{OUTP}}$), it is common to select $C_C = C_L$ with transistors at the output stage scaled-up by a factor of 2. In this case, the GBW has a value $\text{GBW}_{\text{cnv}} = g_m/2\pi C_L$ and the high-frequency pole has a value $f_{\text{Pout}} = 2\ \text{GBW}_{\text{cnv}}$.

Both GBW and f_{POut} can be increased by a factor N by selecting $C_C = C_L/N$ and scaling-up the output transistors by a factor $2N$. Unfortunately, this increases the bias current and the quiescent power dissipation of the op-amp of Fig. 1 by a factor $F = 0.4\ (\text{N} + 1.5)$ and maintains the open-loop gain constant.

A drawback of this circuit is the asymmetrical slew rate. Though it can have a large positive slew rate (SR^+), its negative slew rate (SR^-) is constrained by the bias current of the output stage $I_{\text{OUTQ}} = 2I_B$. Hence, to improve SR^-, it is required to increase I_{OUTQ} which increases the static power dissipation. Slew rate (SR) can be enhanced without increasing static power dissipation by utilization of a class AB (push–pull) output stage. The SR of the input stage (given by $\text{SR}_{\text{inp}} = I_{\text{inp}}/C_C$, where $I_{\text{inp}} = 2I_B$ is the maximum current generated at node X by the input stage) can also limit the SR

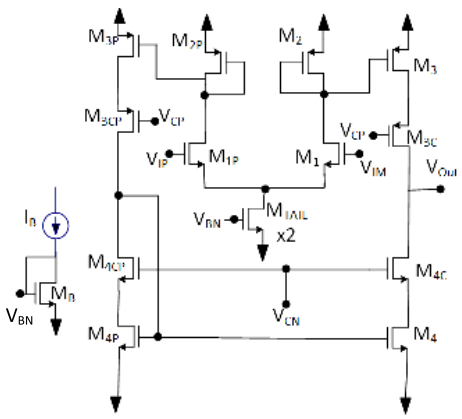


Fig. 2. Cascoded current mirror OTA [5].

of the op-amp since the input stage has to provide current to the compensation capacitor C_C at node X. For this reason, it is convenient that the op-amp has also a class AB input stage that can generate $I_{\text{inp}} > 2I_B$.

Though class AB operation can improve the current efficiency of the op-amp and decrease the linear part of the settling time, the exponential part of the settling time, determined by GBW, and phase margin (PM) can still lead to long total settling times in class AB op-amps. Hence to implement a high-speed op-amp both SR and GBW need to be improved simultaneously [5].

Power constraints in modern VLSI design demand an approach that can simultaneously increase GBW, SR, and open-loop gain. In Section III, an op-amp is proposed which can achieve large dc open-loop gain, enhanced GBW, and higher SR with just moderate increase in quiescent power. This op-amp can also work in subthreshold with little modification as shown in Section III-I. The small-signal and large-signal analysis for both op-amps are similar.

III. Proposed Circuit

A. Operating Principle of the Proposed Op-Amp

The proposed Class AB-AB Miller op-amp is shown in Fig. 3. It is a pseudo-three-stage op-amp derived from the conventional class-A op-amp of Fig. 1 by replacing the input stage with a modified version of the cascoded current mirror OTA [6] shown in Fig. 2 and a free class AB [7] output stage. The diode-connected transistors M_2, $M_{2\text{P}}$ of the current mirror OTA are replaced by a resistive local common mode feedback (RLCMFB) load [8]. The second stage (M_3–M_4) is a high gain fully cascoded amplifier (shown in blue). The combination of first and second stages is denoted as "composite input stage" (M_1–M_4). It is framed by a blue dotted line in Fig. 3. The resistors R_{CM} are selected so that the first stage (M_1–M_2 shown in red and R_{CM}) of the composite input stage provides moderate gain and generates high-frequency poles ω_{PX} at nodes X and X' that have a negligible effect on the phase margin of the op-amp.

The output (third) stage (M_{OUTP} and M_{OUTN}) is a push–pull amplifier with the free class-AB operation. The RLCMFB with two matched resistors (R_{CM}) in conjunction with the scaling of

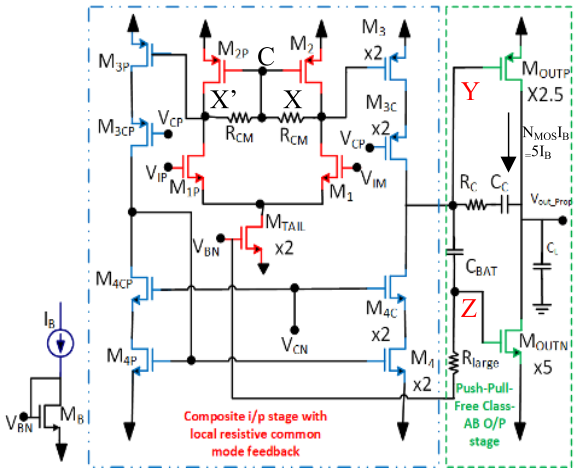


Fig. 3. Proposed class AB-AB op-amp with $N_{MOS} = 5$.

M_3, M_4 by a factor 2 provides: 1) approximately one order of magnitude enhanced effective transconductance g_{meff}, open-loop gain, and higher GBW and 2) class AB operation at the op-amp's internal node Y. The output node of the composite input stage (node Y) has high output resistance R_Y, and thus yields high gain. The output stage provides moderate gain, close to rail-to-rail output swing and class AB operation with comparably high positive and negative peak output currents. The class AB operation of both input and output stages of the op-amp prevents SR limitation of node Y by the bias current of the first stage. It results in high SR, and hence high FOM_{LS}. The class AB output stage has the added advantage that it reduces the output impedance at high frequencies. This shifts the high-frequency output pole to higher frequencies, which improves the phase margin of the op-amp. The enhanced transconductance of the composite input stage g_{meff} leads to essential improvement in GBW and in the dc open-loop gain. This results in much higher FOM_{SS} and high phase margin, with just moderate additional power consumption as discussed in the following analysis.

B. Analysis of Class AB Operation of Input Stage

In this section, it is shown that besides high gain, the input stage of the proposed op-amp has class AB operation and can deliver currents to C_C at node Y, which are larger than the static currents ($2I_B$) of transistors M_3 and M_4. Under quiescent conditions, no current flows through the RLCMFB resistors R_{CM}. Hence, M_2–M_3 and M_{2P-3P} behave as conventional current mirrors at dc. The branch with M_3 in the second stage of the composite input stage is scaled up by a factor of 2 and has a quiescent current $2I_B$. In the presence of a differential input voltage V_{id}, a signal current $i = g_m V_{id}/2$ flows through the R_{CM} resistors and generates complementary voltage variations ΔV_X, $\Delta V_X{}'$ across each R_{CM}. The effective resistance at nodes X and X' is

$$R_X = (R_{CM}||r_{o1}||r_{o2}). \tag{4}$$

R_{CM} should be smaller than the output resistance of transistors $M_{1,2}$, i.e., $R_{CM} << r_{o1,2}$ so that $R_X \approx R_{CM}$. Complementary voltage variations with value $\Delta V_X = iR_X$ appear at nodes X, X' with maximum swing $\Delta V_{Xmax} = I_B R_X$. The maximum source–gate voltage of transistors M_3 and M_{3P} is

$$V_{SG3max} = V_{SG3Q} + \Delta V_{Xmax} = |Vth| + VSDsat + I_B R_X. \tag{5}$$

Transistor M_3 in the second stage can provide a maximum current I_{3max} at node Y which is given by the following equation:

$$\begin{aligned} I_{3max} &= \beta_3 (V_{SG\,max3} - |V_{th}|)^2 \\ &= \beta 3 (V_{SD\ sat3} + |V_{th}| + I_B R_X - |V_{th})|^2 \\ \beta_3 &= \frac{1}{2}\mu_P C_{OX} \left(\frac{W}{L}\right)_3. \end{aligned} \tag{6}$$

Defining $M = (I_B R_X)/V_{SDsat3}$, I_{3max} can be expressed by the following equation:

$$I_{3max} = \beta_3 (M+1)^2 V_{SD\ sat3}^2 = I_{B3Q}(M+1)^2. \tag{7}$$

Hence, depending on the value of R_X and I_B, resistors R_{CM} can help to increase the positive and negative peak currents I_{peakY} delivered to the compensation capacitor C_C at node Y. Design values of $R_{CM} \approx R_X = 16$ kΩ, $|V_{DSsat3}| = 160$ mV, $I_B = 14$ μA, and $I_{B3Q} = 2I_B = 28$ μA were selected here. These selections result in $M+1 \approx 2.4$, which leads to a current $I_{3max} = 6I_{B3Q} = 12I_B = 168\mu$ A at node Y. Increasing R_X results in higher M values (and higher gain), but this decreases the high-frequency poles at nodes X, X', and can lead to a reduction of the phase margin of the op-amp, as discussed in Section III-E.

C. Class AB Operation of Output Stage

To improve the SR, it is also necessary to increase the negative peak current of the output stage. This is done based on the free class AB technique [7]–[9] by means of a large resistance R_{Large} and as mall capacitor C_{BAT} that provides dynamic class AB operation at the output node of the op-amp. Under quiescent conditions, R_{Large} provides equal bias voltage V_{BN} to M_{TAIL} and M_{OUTN}, and consequently currents $2I_B$ and $N_{MOS}I_B$ flow through M_{TAIL} and the two output transistors M_{OUTN} and M_{OUTP}, respectively. M_{OUTN} is scaled by a factor $N_{nMOS} = 2N = 5$ in the proposed design. This leads to a quiescent current $I_{outQ} = 5I_B$ in the output branch transistors. Under dynamic conditions, when the op-amp is slewing in the negative direction, the voltage at node Y faces a positive change. Due to the presence of the large valued resistor, the capacitor cannot charge or discharge rapidly. Hence, it acts as a floating battery and transfers the voltage variations from node Y to node Z. Hence, a large dynamic negative current (higher than the quiescent output current $N_{MOS}I_B$), can be obtained at the op-amp's output node, improving current efficiency CE = I_{omax}/I_{TotalQ} where I_{omax} is the maximum output current and I_{TotalQ} is the total op-amp's quiescent current.

D. Open-Loop-Gain Analysis of the Proposed Op-Amp

The simplified small-signal model of the proposed op-amp is shown in Fig. 4, leading to three poles: two at the internal

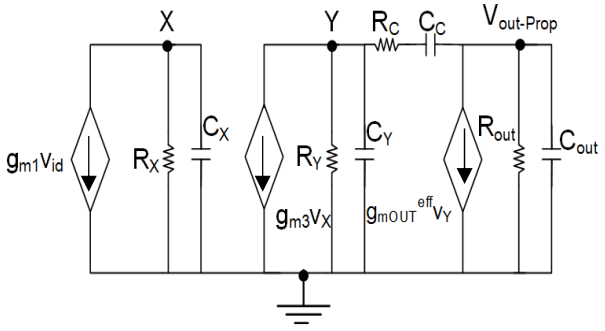


Fig. 4. Small-signal model of the proposed class AB-AB op-amp.

nodes X and Y, and one at the output node. The feedforward path formed by R_C and C_C creates a zero. The corresponding open-loop transfer function $A_{\rm OL}(s)$ of the proposed op-amp is expressed by the following equation:

$$A_{\rm OL}(s) = \frac{A_I A_{II} A_{III}(1 + s/\omega_z)}{(1 + s/\omega_{\rm PDOM})(1 + s/\omega_{\rm POut})(1 + s/\omega_{\rm PX})} \quad (8)$$

where A_I, A_{II}, and A_{III} are the dc gains of the first, second, and third stage, respectively. Gain A_I is $A_I = (V_X - -V_{X'})/V_{id} = g_{m1}R_X$. Cascoded transistors M_{3C} and M_{4C} are used to increase the gain of the second stage $A_{II} = g_{m3}R_Y$. R_Y is expressed by the following equation assuming that all r_o's are equal and $g_{m3} = g_{m4} = g_{m3C} = g_{m4C}$:

$$R_Y = (g_{m\,3C}\, r_{o\,3C}\, r_{o3})||(g_{m\,4C}\, r_{o\,4C}\, r_{o\,4}) \approx g_{m\,3} r_{o3}^2/2. \quad (9)$$

The resultant dc open-loop gain from the composite input stage is

$$A_{\rm input} = A_I A_{II} = g_{m1} R_X (g_{m\,3} r_{o3})^2/2. \quad (10)$$

The output stage consists of a push–pull amplifier that provides moderate gain and close to rail-to-rail output swing. The dc gain of the output stage is $A_{III} = (g_{m\rm OUTP})(r_{\rm OUTP}||\ r_{\rm OUTN})$. Hence, the total dc open-loop gain is given by $\rm A_{OLDC}$

$$\begin{aligned} A_{\rm OLDC} &= A_I A_{II} A_{III} \\ &= (g_{m1} R_X)\frac{(g_{m3} r_{o3})^2}{2} g_{\rm mOUTP}(r_{\rm OUTP}||r_{\rm OUTN}) \\ A_{\rm OLDC} &\approx g_m R_{\rm CM} (g_m r_o)^3/4. \end{aligned} \quad (11)$$

E. Pole-Zero Analysis of the Proposed Op-Amp

Equation (8) shows that the op-amp has three poles and one zero. The selection of $R_{\rm CM}$ plays an important role in this design, as it poses a tradeoff between the boosting of the gain $A_I = g_{m1}R_X$ in the input stage, the value of the high-frequency poles (ω_{PX}) at node X (X'), and the peak current $I_{3\rm max}$ at node Y, as discussed in Section III-B. The pole of the circuit at node X, X' is given by the following equation:

$$\omega_{PX} = 1/R_X C_X \approx 1/R_{C\,M} C_X. \quad (12)$$

Node C at the input stage operates with constant voltage (ac ground). Due to this, the effects of $C_{\rm GS2,2P}$ are nullified at node X. Thus, the parasitic capacitance at node X is given by the following equation:

$$C_X = C_{\rm GS3} + C_{\rm db2} + C_{\rm db1} + C_{\rm GD1} + C_{\rm GD2}. \quad (13)$$

Since C_X is very small and $R_X \ll r_o$, ω_{PX} is a high-frequency pole(much higher than GBW), as shown later in Section III-G. In this case, its effect can be neglected, and $A_{\rm OL}(s)$ of the op-amp can be approximated by a conventional two-pole one-zero system and given by the following equation:

$$A_{\rm OL}(s) \approx \frac{A_I A_{II} A_{III}(1 + s/\omega_z)}{(1 + s/\omega_{\rm PDOM})(1 + s/\omega_{\rm POut})}. \quad (14)$$

The dominant pole at node Y is given approximately by the following equation:

$$\omega_{\rm PDOM} \approx \frac{1}{R_Y A_{III}\, C_c}. \quad (15)$$

The GBW (in hertz) of the op-amp in Fig. 3 is given in the following equation:

$$\begin{aligned} \rm GBW &= A_{\rm OLDC}\omega_{\rm PDOM} = A_I A_{II} A_{III}\omega_{\rm PDOM} \\ &\approx (A_I(g_{m3}R_Y)A_{III})/(R_Y C_C A_{III}) \\ &\approx A_I g_{m3}/C_C = g_{m\rm eff}/(2\pi C_C). \end{aligned} \quad (16)$$

Equation (16) implies that the effective transconductance of the composite input stage and of the op-amp of Fig. 3 is given by $g_{m\rm eff} = A_I g_{m3}$. Hence, A_I, in conjunction with the factor 2 scaling of M_3, increases the effective transconductance, the GBW, and the dc open-loop gain of the op-amp approximately by a factor $2A_I$ at the expense of a moderate increase in power dissipation and the introduction of the high-frequency poles ω_{PX}. In the proposed design, the value of $R_{\rm CM}$ and the scaling by a factor 2 of M_3 in the second stage provides a gain boosting in the composite input stage by a factor close to 10.

The nondominant pole in (14) corresponds to the output terminal and is given by the following equation:

$$\omega_{\rm POut} = \left(g_{m\rm OUT}^{\rm eff}/C_L\right). \quad (17)$$

Here, $g_{m\rm OUT}^{\rm eff} = g_{m\rm OUTP} + g_{m\rm OUTN}$ is the output conductance of the op-amp at high frequencies. The zero is given by the following equation:

$$\omega_z = \frac{1}{\left(C_C R_C^{\rm eff}\right)} \quad (18)$$

where $R_C^{\rm eff} = (R_C - 1/g_{m\rm OUT^{eff}})$.

Now, to achieve high GBW and high phase margin with low silicon area, C_C is selected to have a moderate-low value $C_C = C_L/10$ and R_C is selected so that the output pole $\omega_{P\rm Out}$ matches the zero ω_z. In this case, $\omega_{P\rm out}$ and $\omega_{\rm z}$ can be lower than GBW, but the op-amp can still have high phase margin. This is discussed in detail in Section III-F with a design example.

The proposed approach enhances the open-loop gain and the effective $g_{m\rm eff}$ of the op-amp by providing an additional gain in the first stage with a negligible impact on the PM. This is possible in current technology (like in 0.13-μm CMOS technology and finer technologies) since the value of C_X is

very small. Thus, $\omega_{PX} \gg$ GBW. Hence, the enhancement of $g_{m\text{eff}}$ improves GBW and the dc open-loop gain. On the contrary, using RLCMFB to enhance gain in previous technologies (like in 0.5-μm technology) [8], the value of C_X was not so small and the poles at node X and X'could be lower or close to GBW. So, in order to achieve a high PM phase, lead compensation was required. This uses a left half s plane zero generated by a resistor R_s connected in series with C_L to compensate for the phase shift of ω_{PX} which can limit the op-amp's maximum dynamic output current. Thus, this proposed op-amp in 130-nm technology does not require phase lead compensation if the RLCMFB provides only moderate gain enhancement in the input stage.

F. Stability Analysis

As mentioned above [see (18)], in general for stability with PM $> 50°$, the Miller op-amp is designed with $R_C = 1/g_{m\text{OUT}}^{\text{eff}}$ to shift the right half-s plane zero to infinity and the high-frequency output pole $\omega_{P\text{Out}}$ must be higher than GBW by at least a factor of 2. As indicated in Section II, a common practice to achieve this is to scale the output transistors by a factor 2 and to select $C_C = C_L$. In this case, the high-frequency output pole limits the maximum value of GBW to a value $f_{P\text{Out}}/2 = g_m/(2\pi C_L) = g_m/(2\pi C_C)$. As discussed in Section II, GBW can be increased by a factor N by selecting $C_C = C_L/N$ and scaling the output transistors by a factor of $2N$. This increases quiescent power dissipation by a factor of $0.4(N + 1.5)$ and maintains the same dc open-loop gain.

The approach followed here allows to achieve higher GBW values with lower power dissipation as shown below. It consists of matching the value of the zero ω_z to the output pole ω_{POut}. From (17) and (18), the condition for pole-zero matching $\omega_{\text{POut}} = \omega_z$ leads to $R_C = (1 + C_L/C_C)/g_{m\text{OUT}}^{\text{eff}}$.

Consider, for example, the design of the proposed circuit of Fig. 3 with scaling factors $N_{\text{pMOS}} = 2.5$ and $N_{\text{nMOS}} = 5(I_{\text{OUTQ}} = 5I_B)$ in the output stage transistors M_{OUTP} and M_{OUTN}, respectively, with $C_C = C_L/10$, $R_{\text{CM}} = 16$ kΩ, and a factor 2 scaling of transistor M_3. The free class AB output stage can provide a $g_{m\text{OUT}}^{\text{eff}}$ value given by the following equation:

$$g_{m\text{OUT}}^{\text{eff}} = (g_{m\text{OUTP}} + g_{m\text{OUTN}}). \tag{19}$$

As $g_{m,n} = (2I_B\mu_{n,p}C_{\text{ox}}(W/L)_{n,p})^{1/2}$, $g_{\text{mOUT}}^{\text{eff}} = ((N_{\text{nMOS}}N_{\text{pMOS}} + N_{\text{nMOS}})^{1/2})g_{m1} = 8.5$ gm1. The scaling of the output transistors shifts both the high-frequency output pole (and the matching zero) by almost an order of magnitude. Hence, this approach, in conjunction with the enhancement of $g_{m\text{OUT}}^{\text{eff}}$ and the reduction of C_C leads to an essentially higher GBW value than the conventional op-amp and places the output pole and zero at higher values, such that high PM is possible. Note that the enhancement of GBW is also possible due to the enhancement of $g_{m\text{eff}}$ introduced by the RLCMFB and by the factor of 2 scaled-up transistors M_3 and $M_{3\text{P}}$ in the composite input stage. In the proposed approach, a value GBW $= A_I g_{m3}/C_C$ is obtained from (16) where $A_I \approx 3.5$ is the gain introduced by the RLCMFB in the first stage. Thus, $g_{m\text{eff}}$ is enhanced by a factor of $2A_I \approx 7$.

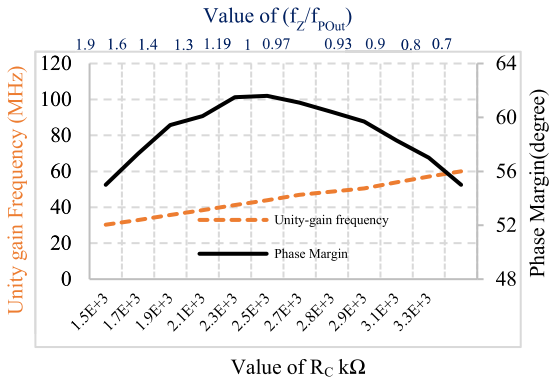


Fig. 5. Variation of phase margin, unity-gain frequency, and pole-zero mismatch with R_C.

Scaling down C_C by a factor 10 provides additional GBW enhancement by the same factor. Hence GBW of the proposed circuit is given by $\text{GBW}_{\text{prop}} = 2A_I(g_m/2\pi C_c) = 20A_I(g_m/2\pi C_L) = 70\ \text{GBW}_{\text{cnv}}$. This is a factor 70 times higher than the GBW of the conventional approach. This is achieved by: 1) enhancing $g_{m\text{eff}}$ in three steps in the input stage; 2) scaling down C_C; and 3) matching the high-frequency pole to the high-frequency zero. Downscaling of capacitor C_C also saves silicon area and simultaneously relaxes the SR requirements at the internal node Y of the composite input stage. Enhancing $g_{m\text{eff}}$ also enhances the dc open-loop gain by a factor $2A_I$.

Fig. 5 shows the variation of the PM and pole-zero mismatch factor f_z/f_{Pout} as a function of R_C obtained from simulations with $C_L = 50$ pF. According to (18), the changes in R_C lead to changes in ω_z. It is desirable to have a high PM. From Fig. 5, it can be observed that the approach proposed here is robust against R_C manufacturing variations since PM $> 60°$ for 2 kΩ $< R_C <$ 2.8 kΩ, which corresponds to a pole-zero mismatch range $0.93 < f_Z/f_{\text{Pout}} < 1.4$. PM also remains higher than 55° in the range from 1.5 kΩ $< R_C <$ 3.3 kΩ and $0.8 < f_Z/f_{\text{Pout}} < 1.9$. It is noticeable that the phase margin is within 55° for a large pole and zero mismatch factor between 0.7 and 1.9. Note that the accurate pole-zero matching is not required to achieve a high PM. However, pole-zero pairs (doublets) can affect the settling time(t_{Setl}) of class A and class AB op-amps [10]. According to [11], the exponential part of the transient response of the op-amp to a step input of amplitude V is given by the following equation:

$$V_{\text{Out}}(t) = V\left[1 - \exp(-\text{GBW} * t) + \frac{\omega_z - \omega_p}{\text{GBW}}\exp(-\omega_z t)\right]. \tag{20}$$

Here, ω_z and ω_p are pole and zero doublet frequencies. The third term can lead to long settling times if there is large relative pole-zero mismatch (ω_z-ω_p)/ GBW and/or low pole-zero doublet frequencies relative to GBW: ω_z, $\omega_p \ll$ GBW. In the design proposed here, ω_z and ω_{pOut} are approximately a factor 4–5 lower than GBW. Simulations shown in Section IV-A with relatively large pole-zero mismatch values ($\omega_z/\omega_{\text{pOut}}$ in the range from 0.8 to 1.7) caused by variations in R_C and C_L show that even in these large ranges the pole-zero mismatches do not lead to long settling times in the proposed design. Fig. 6

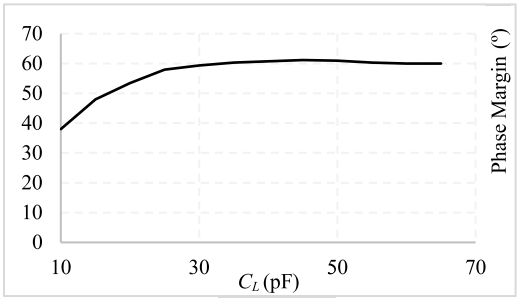


Fig. 6. Phase margin as a function of C_L.

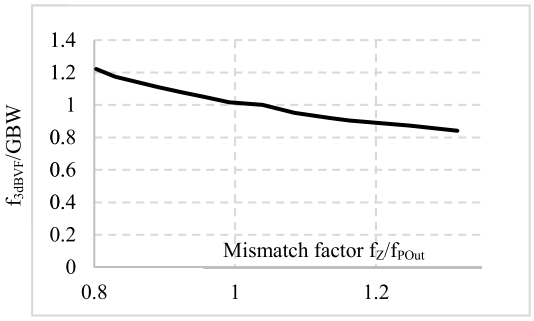


Fig. 7. f_{3dBVF}/GBW as a function of f_Z/f_{POut}.

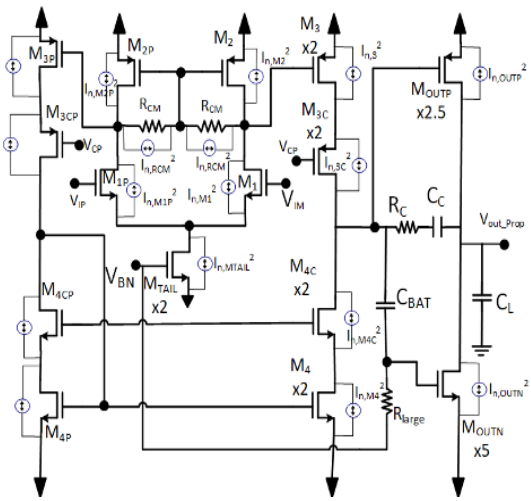


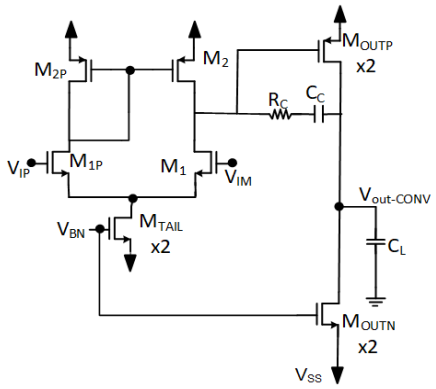
Fig. 8. Noise model of the proposed op-amp.

shows the phase margin of the op-amp as a function of C_L. It can drive a load $C_L = 20$ pF with PM = 54°.

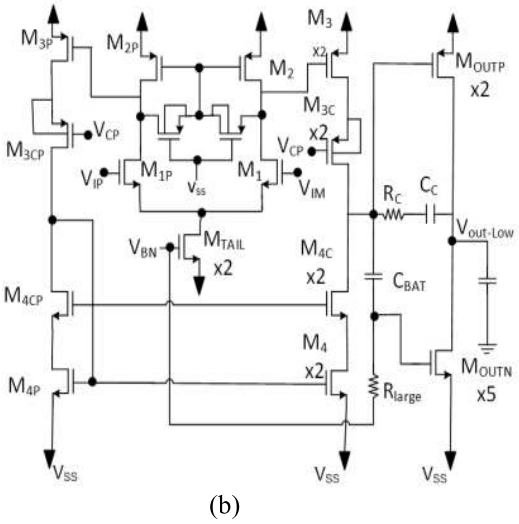
The transfer function of the proposed op-amp in voltage follower (VF) configuration is given by the following equation:

$$G_{\mathrm{CL}}(s) = \frac{A_{\mathrm{OLDC}}\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{\mathrm{PDOM}}}\right)\left(1+\frac{s}{\omega_{\mathrm{POut}}}\right)+A_{\mathrm{OLDC}}\left(1+\frac{s}{\omega_z}\right)}. \quad (21)$$

For $f_Z/f_{\mathrm{POut}} = 1$ (pole matches the zero), (21) reduces to a one pole transfer function. In that case, the BW of the VF is $f_{3\mathrm{dBVF}} =$ GBW. Fig. 7 shows $f_{3\mathrm{dBVF}}/$ GBW as a function of mismatch f_Z/f_{Pout}. It can be noticed that for the range of $0.8 < f_Z/f_{\mathrm{Pout}} < 1.32$, $f_{3\mathrm{dBVF/GBW}}$ lies in the range of



** (a)



(b)

Fig. 9. (a) Subthreshold implementations of Conv-A op-amp. (b) Subthreshold implementations of the Proposed-AB-AB Op-amp. **No telescopic Conventional op-amp is considered here. Due to the low supply voltage constrain (±0.25 V).

$0.8 < f_{3\mathrm{dBVF/GBW}} < 1.22$. Therefore, $f_{3\mathrm{dBVF}}$ is not highly sensitive to pole-zero mismatch.

G. Design Considerations

Table I shows the design parameters of the proposed design (column 2) and of the conventional op-amp of Fig. 1 for two cases: 1) with $C_C = C_L$ and R_C selected in such a way that f_z is shifted to infinity (column 3) and 2) with $C_C = C_L/10$ and R_C selected to achieve pole-zero cancellation (column 4). In the proposed design the nominal value of the zero f_Z is 16 MHz obtained from (18) and the first high-frequency pole f_{POut} is close to 14 MHz from (17). Hence, the effect of the 1st nondominant pole is approximately nullified by the left-hand plane zero. The dominant pole obtained from (15) has a value $f_{\mathrm{PDOM}} = 4.8$ kHz. The dc open-loop gain is $A_{\mathrm{OLDC}} =$ 82.3 dB from (11), and GBW = 63 MHz from (16). From (12), the second-high-frequency pole is at $f_{pX} = 200$ MHz. Hence in this design, $f_{3\mathrm{dB}}$ in VF configuration is 57 MHz for the values of f_Z and f_{POut}. Notice that the conventional op-amp has a value GBW = 12 MHz with pole-zero cancellation and $C_c = C_L/10$, while it has a value GBW = 1.1 MHz with

TABLE I

VALUES OF DESIGN PARAMETERS OF THE PROPOSED AND CONV OP-AMP IN STRONG INVERSION

Parameter	C_C=C_L/10 (proposed)	C_C=C_L Conv	C_C=C_L/10 Conv
I_B(μA)	14	14	14
R_{large}(kΩ)	500	NA	NA
R_{CM}(kΩ)	16	NA	NA
C_C (pf)	4.6	50	4.6
C_L (pF)	50	50	50
R_C (kΩ)	2.3	1	12
C_{bat} (pF)	2	NA	NA
NMOS(unit transistor's W/L)(μm)	5/0.18	5/0.18	5/0.18
PMOS(unit transistor's W/L)(μm)	20/0.18	20/0.18	20/0.18
g_{m1},g_{m3},g_{mOUTP},g_{mOUTN}(μA/V)	311,492,1770, 2700	351,NA, 931,1082	351,NA, 931,1082
g_{ds1}, g_{ds2}, g_{ds3}, g_{dsOUTP}, g_{dsOUTN} (μA/V)	11.81,9.62, 21.33,50.54, 73.47	17,12,NA,26,33	17,12,NA,26, 33
A_{OLDC},GBW, f_{PDOM}, f_{pX}, f_{pOut}, f_z, t_{Setl^+}, t_{Setl^-} ,PM	82.3dB, 63MHz, 4.8kHz,200MHz, 14MHz,16MHz, 45ns,50ns, 60^0	70.5dB, 1.1MHz,311Hz, NA, 3MHz, infinity, 1.2μs, 2μs, 70^0	70.5dB, 12MHz, 3.3kHz,NA, 3MHz, 2.9MHz, 285ns, 890ns 98^0

$C_c = C_L$ and f_z shifted to infinity. In both cases, the GBWs are lower since the proposed g_{meff} boosting technique is not used. The 0.1% positive and negative settling times ($t^+_{\rm Setl}$ and $t^-_{\rm Setl}$) of the proposed op-amp for the design parameters given in Table I are 45 and 50 ns, respectively, whereas for the Conv-A op-amp with $C_C = C_L/10$, $t^+_{\rm Setl}$ and $t^-_{\rm Setl}$ are 285 and 890 ns, respectively. For $C_C = C_L$, $t^+_{\rm Setl}$ and $t^-_{\rm Setl}$ are 1.2 and 2 μs, respectively.

H. Noise Analysis

The most significant sources of the internal noise in the op-amp are the thermal noise of the MOSFETs and resistors and the flicker noise of the MOSFETs. A simple expression of the noise current spectral density of a MOSFET is [12]

$$I_n^2(f) = 4\gamma k_B T g_m + \frac{K_f g_m^2}{{\rm WLC_{ox}} f} = 4\gamma k_B T g_m + \frac{2\mu K_f I_D}{L^2 f} \quad (22)$$

with T the absolute temperature, k_B the Boltzmann's constant, μ the carrier mobility, K_f the flicker noise coefficient, and γ a factor that varies from 1/2 to 2/3 from weak to strong inversion. The first term in (22) corresponds to thermal noise and the second term to flicker noise. The thermal noise of the resistor $R_{\rm CM}$ can also be modeled by a current source with a power spectral density of $I^2_{\rm nRCM}(f) = 4\ k_B T/R_{\rm CM}$. Fig. 8 shows the noise sources. Assuming that they are uncorrelated and that all transistors have the same γ factor, the input-referred mean-square thermal noise of the amplifier in a bandwidth Δf is

$$\overline{v^2_{\rm nt,in}} = \frac{4\gamma k_B T \Delta f}{g_{m1}} \times \left[1 + \frac{g_{m1P}}{g_{m1}} + \frac{g_{m2}}{g_{m1}} + \frac{g_{m2P}}{g_{m1}} + \frac{2}{\gamma g_{m1} R_{\rm CM}} + 1/(g_{m3}R_{\rm CM})^2 \left(\frac{g_{m3}}{g_{m1}} + \frac{g_{m4}}{g_{m1}}\right) + 1/(g_{m3P}R_{\rm CM})^2 \left(\frac{g_{m3P}}{g_{m1}} + \frac{g_{m4P}}{g_{m1}}\right)\right]. \quad (23)$$

The noise contribution of the output stage is not considered as it is divided by the high-gain of the input-stage when referred to the input. Noting that $g_{m3} = g_{m4} = 2g_{m2}$ and $g_{m3P} = g_{m4P} = g_{m2P} = g_{m2}$ and $g_{m1} = g_{m1P}$, from (23)

$$\overline{v^2_{\rm nt,in}} = \frac{8\gamma k_B T \Delta f}{g_{m1}} \left[1 + \frac{g_{m2}}{g_{m1}} + \frac{1}{\gamma g_{m1} R_{\rm CM}} + \frac{1}{g_{m1} g_{m3} R^2_{\rm CM}} + \frac{1}{g_{m1} g_{m3P} R^2_{\rm CM}}\right]. \quad (24)$$

Note that for moderately large $g_{m3}R_{\rm CM}$ and $g_{m3P}R_{\rm CM}$ noise is dominated by the first stage.

Regarding flicker noise, assuming as before uncorrelated noise sources and the same K_f for all the transistors of the same type (nMOS or pMOS), the input-referred spectral noise density of the amplifier is

$$V^2_{\rm nf,in}(f) = \frac{K_{\rm fn}}{C_{\rm ox} f W_1 L_1} \times \left\{ 2\left[1 + \frac{K_{\rm fp}}{K_{\rm fn}} \frac{\mu_p}{\mu_n} \left(\frac{L_1}{L_2}\right)^2\right] + \frac{1}{(g_{m3}R_{\rm CM})^2} \left[\left(\frac{L_1}{L_4}\right)^2 + \frac{K_{\rm fp}}{K_{\rm fn}} \frac{\mu_p}{\mu_n} \left(\frac{L_1}{L_3}\right)^2\right] + \frac{1}{(g_{m3P}R_{\rm CM})^2} \left[\left(\frac{L_1}{L_{4P}}\right)^2 + \frac{K_{\rm fp}}{K_{\rm fn}} \frac{\mu_p}{\mu_n} \left(\frac{L_1}{L_{3P}}\right)^2\right] \right\}. \quad (25)$$

As the same L was used for all the transistors ($L = 180$ nm in 130 nm technology), the flicker noise becomes

$$V^2_{\rm nf,in}(f) = \frac{K_{\rm fn}}{C_{\rm ox} f W_1 L} \left(1 + \frac{K_{\rm fp}}{K_{\rm fn}} \frac{\mu_p}{\mu_n}\right) \times \left(2 + \frac{1}{(g_{m3}R_{\rm CM})^2} + \frac{1}{(g_{m3P}R_{\rm CM})^2}\right). \quad (26)$$

Note that for the moderately large $g_{m3}R_{\rm CM}$ and $g_{m3P}R_{\rm CM}$, the expression corresponds to the well-known flicker noise of a simple differential pair, as the first stage dominates noise contribution. Note also that, in these conditions, noise is dominated by the input pair M_1 and M_{1P}, as $K_{\rm fn} > K_{\rm fp}$ and $\mu_n > \mu_p$.

I. Subthreshold Op-Amp

The proposed op-amp can work in the subthreshold region with little modification. In the subthreshold region, quiescent power dissipation is lower as transistors can be biased with very low bias current (nAs) and with a supply voltage below 1 V. In biomedical applications and wireless sensor networks,

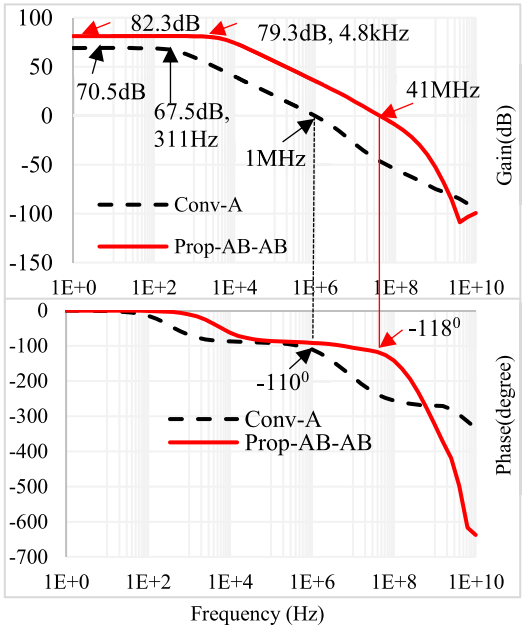


Fig. 10. Open-loop response of Conv-A and Proposed-AB-AB op-amp.

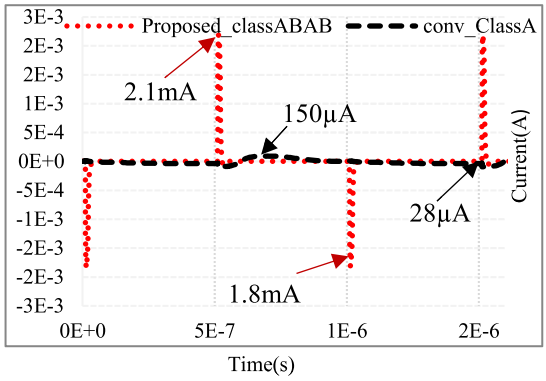


Fig. 11. Transient output currents of Conv-A and Proposed-AB-AB op-amp.

subthreshold op-amps are a good choice where high-speed is not a primary concern nevertheless a very low quiescent power dissipation is the foremost requirement.

Fig. 9(a) shows a conventional Miller op-amp (without telescopic input stage) working in the subthreshold region. Fig. 9(b) shows a modified version of the proposed op-amp for operation in subthreshold. To avoid body effect and reduce the supply requirements in subthreshold, the substrates of the two pMOS cascode transistors (M_{3CP} and M_{3C}) are connected to their source. In order to save the Silicon area, resistors used for local common mode feedback shown in Fig. 3 are replaced by MOS transistors operating in triode region with their gate connected to V_{SS}. These transistors are designed to implement 1.5 MΩ resistors in order to provide again A_I close to as in the strong-inversion case. In Section IV, simulation results of the op-amps in strong-inversion and in subthreshold regions are discussed.

IV. Simulation Results

The Proposed-AB–AB and conventional op-amps were designed in 130-nm CMOS technology with nMOS and pMOS

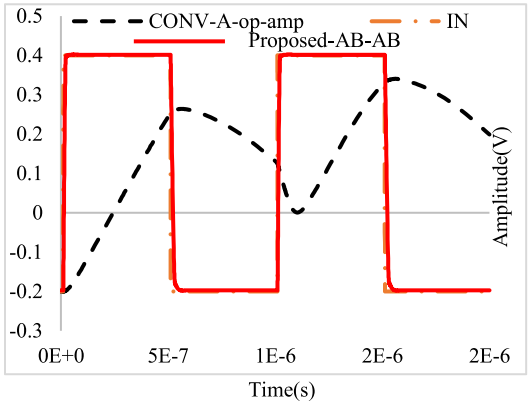


Fig. 12. Transient response of Proposed-AB-AB and Conv-A op-amp.

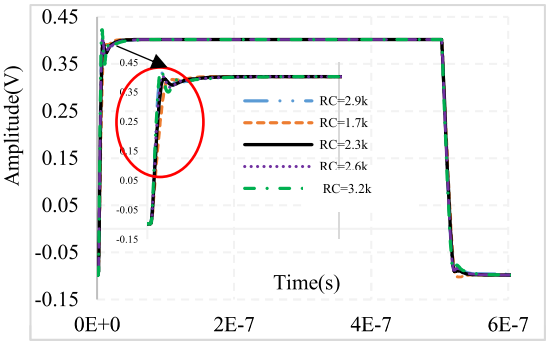


Fig. 13. Transient response of proposed op-amp for varying R_C in strong inversion.

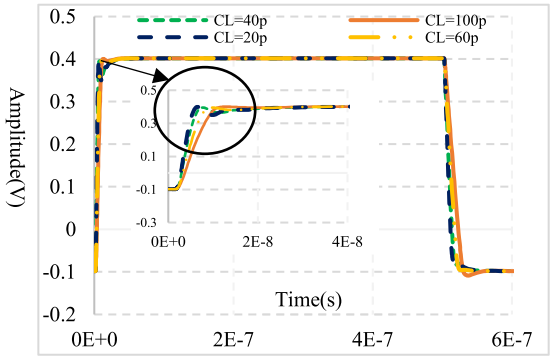


Fig. 14. Transient response for different C_L strong inversion.

unit transistor sizes $(W/L)_N = 5\ \mu$m/0.18 μm and $(W/L)_P = 20\ \mu$m/0.18 μm, respectively. They were simulated both with the same bias current and load capacitance $C_L = 50$ pF.

A. Simulation Results in Strong Inversion

The circuits of Figs. 1 and 3 were simulated with ±0.6-V dual supplies and bias current $I_B = 14\mu$A. Fig. 10 shows its open-loop frequency response. It can be seen that the circuit of Fig. 1 (Conv-A) with telescopic input stage has a dc open-loop gain $A_{OLDC} = 70$ dB, a unity gain frequency $f_U = 1$ MHz, a 3-dB frequency $f_{3dB} = 311$ Hz, and GBW $= A_{OLDC} f_{3dB} = 1.1$ MHz.

TABLE II
CORNER ANALYSIS OF OP-AMP OPERATING IN STRONG INVERSION AT DIFFERENT TEMPERATURES

	At T=27^{0}C						At T=100^{0}C						At T=0^{0}C					
Corner	tt	ff	fs	sf	ss	**SD**	tt	ff	fs	sf	ss	**SD**	tt	ff	fs	sf	ss	**SD**
I_{TotalQ}(μA)	158	163	156	161	156	**3.1**	154	159	150	156	149	**4**	162	166	158	164	157	**3.8**
THD (dB)	-58	-59	-54	-55	-45	**5.5**	-59	-62	-62	-60	-55	**2.88**	-48	-60	b54	-42	-40	**8.3**
GBW(MHz)	63	68	61	63	60	**3**	43	46	41	42	39	**2.5**	77	82	73	77	82	**3.8**
PM	61	60	60^0	60^0	58	**1**	59	58	58	59	58	**1.3**	60	59	58	61	58	**1.3**
Gain	81	83	83	82	84	**1**	80	75	80	78	82	**2.6**	83	82	83	83	84	**0.7**
SR^+	48	45	44	49	40	**3.7**	44	47	40	46	38	**3.8**	40	49	43	48	47	**3.7**
SR^-	33	37	40	35	34	**2.77**	26	25	29	25	25	**1.7**	39	47	46	40	44	**3.5**

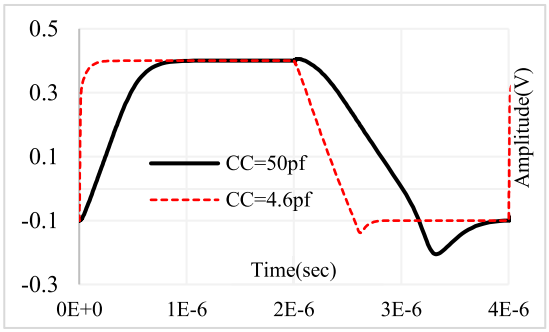


Fig. 15. Transient response shows settling time of Conv-A op-amp for $C_C = 50$ pF and $C_C = 4.6$ pF for 250-kHz pulse in strong inversion.

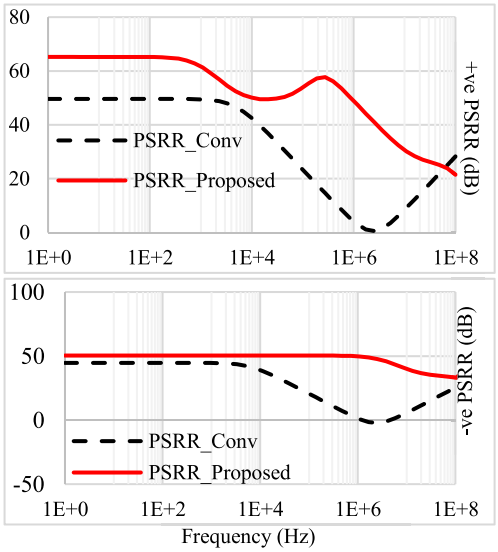


Fig. 16. Positive PSRR and negative PSRR in strong inversion.

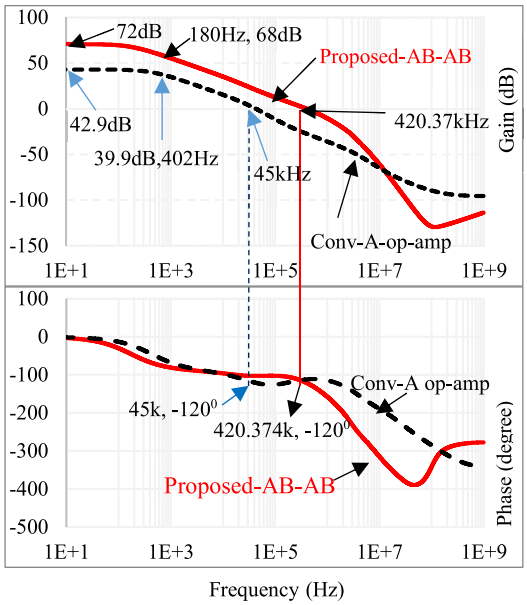


Fig. 17. Open-loop frequency response of op-amps in subthreshold.

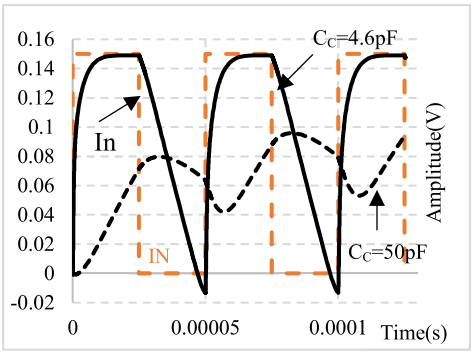


Fig. 18. Transient response of Conv-A op-amp for value of $C_C = 4.6$ pF and $C_C = 50$ pF.

The Proposed class AB-AB op-amp (Proposed-AB-AB) has $f_U = 41$ MHz, $A_{OLDC} = 82.3$ dB, $f_{3dB} = 4.8$ kHz, and GBW = 63 MHz. Hence, the proposed op-amp can provide 13 dB higher open-loop gain, 63 times higher GBW, and 41 times higher f_U at the expense of only 2.2 times increase in quiescent power dissipation compared to the conventional op-amp. Figs.11 and 12 show the transient responses of the Proposed-AB-AB and the Conv-A op-amp in voltage follower configuration with a 600 mVpp 1-MHz input square wave. From Figs. 11 and 12, it can be asserted that the Conv-A op-amp has much lower SR than the Proposed-AB-AB op-amp in both directions. The Conv-A op-amp delivers much lower positive and negative output peak currents (150 and 28 μA) than the Proposed-AB-AB op-amp (2.1 and 1.8 mA) to the load capacitor C_L. Although conventional class A Miller op-amps with nMOS input stage can theoretically deliver large positive output currents (and negative output currents limited by the bias current of the output stage), the output current of the Conv-A op-amp in this example is limited in both directions by the SR of the internal node X.

TABLE III

CORNER ANALYSIS OF THE PROPOSED OP-AMP OPERATING IN SUBTHRESHOLD AT DIFFERENT TEMPERATURES

	At T=27^{0}C						At T=100^{0}C						At T=0^{0}C					
Corner	tt	ff	fs	sf	ss	**SD**	tt	ff	fs	sf	ss	**SD**	tt	ff	fs	sf	ss	**SD**
I_{TotalQ}(µA)	0.77	0.77	0.77	0.81	0.76	**0.02**	1.4	1.2	1.4	1.2	1.2	**0.16**	0.9	0.9	0.8	0.9	0.8	**0.05**
THD(dB)	-50	-49	-40	-45	-54	**5.5**	-50	-40	-55	-45	-56	**7**	-51	-53	-56	-40	-42	**7**
GBW(kHz)	716	700	720	700	723	**16**	632	600	614	630	600	**16**	532	495	492	486	490	**18**
PM	62º	73º	57º	69º	59º	**6**	77º	93º	63º	88º	63^0	**13**	65º	73º	68º	73º	66º	**4**
Gain	71	66.4	72	67.2	72.4	**2.8**	46	32	53.6	36	57	**10**	80	69	62	63	61	**7**
SR^+	0.10	0.08	0.11	0.10	0.11	**.01**	0.07	0.07	0.08	0.06	0.09	**.01**	0.10	0.09	0.09	0.09	0.04	**.02**
SR^-	0.13	0.12	0.08	0.18	0.73	**.04**	0.10	0.06	0.12	0.07	0.15	**.04**	0.05	0.18	0.03	0.15	0.02	**.07**

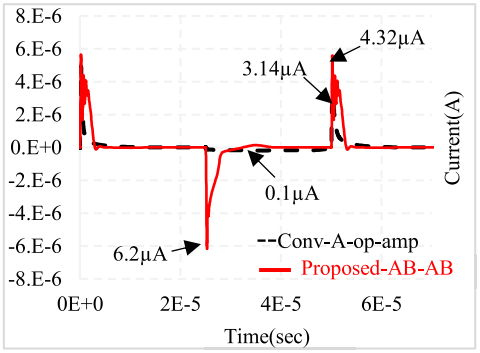


Fig. 19. Transient output current for op-amp in subthreshold.

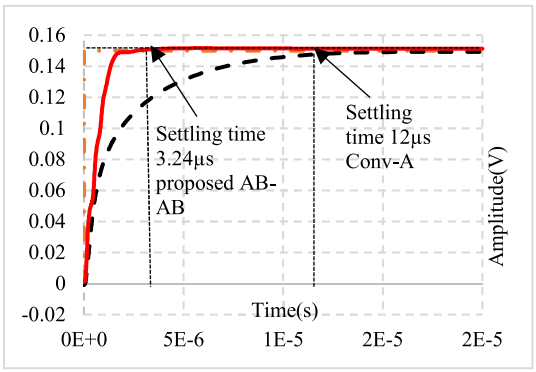


Fig. 20. Settling time of op-amps in subthreshold.

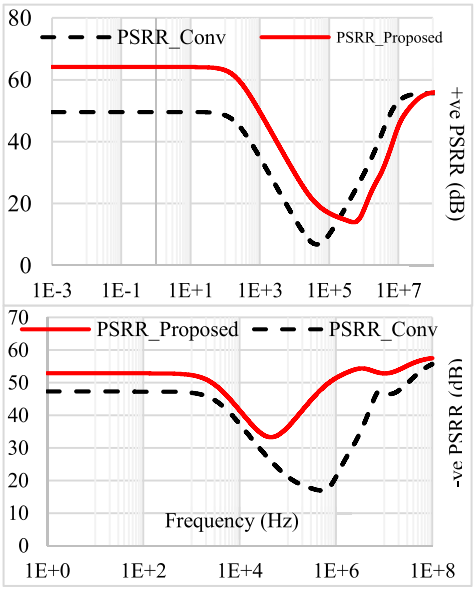


Fig. 21. Positive and negative PSRR of the Proposed-AB-AB Op-amp.

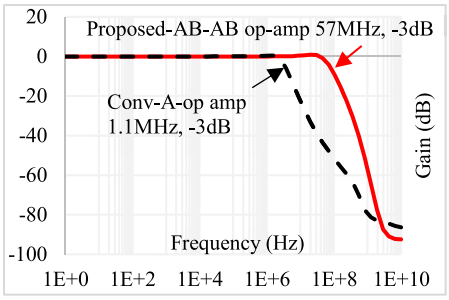


Fig. 22. Experimental frequency response of op-amps (strong inversion) in voltage follower configuration.

The class-A input stage of the Conv-A op-amp can deliver maximum positive and negative currents with value $2I_B$ to the compensation capacitor C_C at node X. The inclusion of a class-AB output stage does not lead to an improvement in the settling time as it is determined by the slew rate of the class-A input stage at node X. In addition, the much lower GBW value of the Conv-A op-amp also results in long exponential settling times in both directions. From Figs. 11 and 12, it can be observed that the inclusion of class-AB input and output stages enhances the dynamic output current in the Proposed-AB-AB op-amp. The Proposed-AB-AB op-amp has positive and negative output current enhancement factors 14 and 63, compared to the conventional op-amp. These results satisfy the theory of the proposed op-amp described in the previous section. To observe the effect of pole-zero doublet mismatches in the settling time Fig. 13 shows a transient response for R_C in the range from 1.7 to 3.2 kΩ. The 0.1% t_{Setl} of the op-amp is measured considering the time required for the response to reach and stay within a range of ±0.1% of the final value [13]. For a 1-MHZ 500 mV peak-to-peak amplitude step input the 0.1% positive settling time t^+_{Setl} varies from 28 to 66 ns and the negative settling time t^-_{Setl} varies from 35 to 70 ns for f_z/f_p mismatch factor within the range 1.67–0.8. Fig. 14 shows the transient response of the proposed op-amp for different C_L values that lead to a pole-zero mismatch factor within the range of 0.4–2.4. In this case, the 0.1% t^+_{Setl} varies from 52 to 35 ns and 0.1% t^-_{Setl} varies from 68 to 60 ns for load capacitances within the range 20 pF $< C_L <$ 100 pF. An ideal single pole op-amp has a 0.1% settling time

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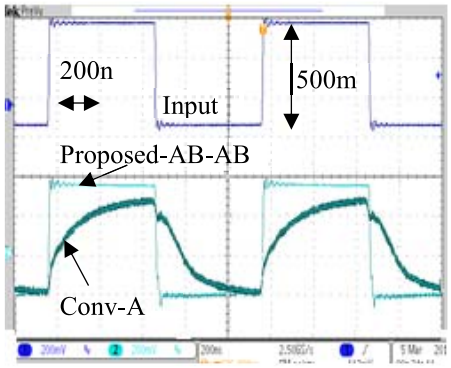

Fig. 23. Experimental transient response of the proposed op-amp at strong-inversion for 1-MHz 500-mV input amplitude pulse.

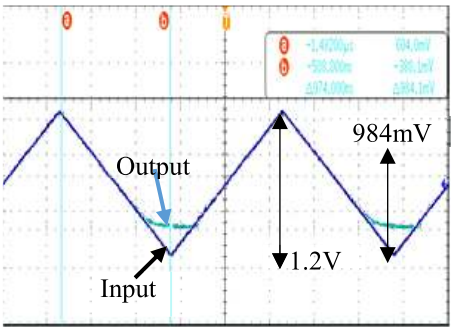

Fig. 24. Experimental input range for the Proposed-AB-AB op-amp for ±600 mV 1-MHz triangular pulse at strong inversion.

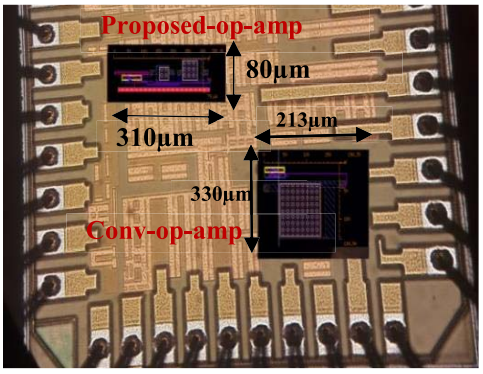

Fig. 25. Micrograph of the Proposed-AB-AB and Conv-A op-amp in strong inversion.

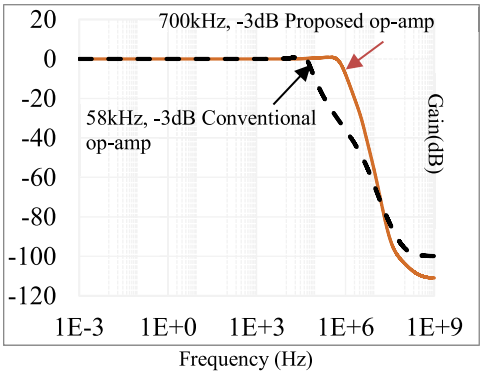

Fig. 26. Experimental frequency response of the Proposed-AB-AB and Conv-A op-amp at subthreshold.

$t_{setl} = 6.9/(2\pi$ GBW) which for GBW = 63 MHz results in $t_{setl} = 17.3$ ns. The 0.1% settling times of the proposed op-amp are factors 2–4 larger than for an ideal single pole op-amp but essentially lower than for the conventional op-amp. Fig. 15 shows the settling time of the Conv-A op-amp for $C_C = 4.6$ pF ($t^+_{Setl} = 285$ ns, $t^-_{Setl} = 890$ ns) and $C_C = 50$ pF ($t^+_{Setl} = 1.2$ μs and $t^-_{Setl} = 2$ μs).

Fig. 16 shows the positive and negative PSRR of the Proposed-AB-AB and Conv-A op-amp. The Proposed-AB-AB op-amp provides 67- and 50-dB positive and negative PSRR. The positive PSRR is 17 dB higher than the conventional op-amp and remains high over a wider range of frequencies. This is attributed to the higher dc gain and BW. To show the robustness of the proposed op-amp against process and temperature variations, corner analysis at three different temperatures for important performance parameters of the circuit are given in Table II. It can be asserted that proposed op-amp is robust against variation of process and temperature and can provide wide GBW. Standard deviation (SD) is shown in the table for each parameter for variation of the process for considered temperatures.

B. Simulation Results in Subthreshold Region

The proposed and conventional op-amps were also simulated in subthreshold with ±0.25-V supply voltage and bias current $I_B = 70$ nA. Fig. 17 shows the frequency response of the conventional and proposed op-amps. The Proposed-AB-AB op-amp has 72-dB open-loop dc gain and unity gain frequency $f_U = 420.37$ kHz with 60° phase margin. The Conv-A op-amp has 42.9-dB open-loop dc gain, unity gain frequency $f_U = 45$ kHz and 60° phase margin. Fig. 18 shows that the Conv-A op-amp suffers from a poor settling time for the larger compensation capacitor. The Conv-A op-amp in subthreshold was fabricated with $C_C = 4.6$ pF. Fig. 19 shows the transient output current of the proposed and conventional op-amps in subthreshold. The Proposed-AB-AB op-amp can provide maximum positive and negative output currents of 4.32 and 6.24 μA, respectively. Hence, the negative current limitation is significantly improved in the Proposed-AB-AB op-amp. The positive setting times of the Proposed-AB-AB and Conv-A op-amps are 3.2, and 12 μs, respectively, according to Fig. 20. The negative settling times of the Proposed-AB-AB and Conv-A-op-amps are 13 and 197 μs, respectively. Positive and negative PSRRs are 64 and 53 dB, respectively, whereas conventional op-amp has 50- and 47-dB positive and negative PSRRs. Fig. 21 shows the PSRR responses of the op-amps. Corner analysis of the proposed op-amp at different temperatures operating in the subthreshold region is given in Table III. It can be observed that the proposed op-amp is stable against the variation of process and temperature. The SD of each parameter for variation of the process has been given in Table III for the considered temperatures (0 °C, 27 °C, 100 °C).

V. Experimental Results

Test chip prototypes of the proposed op-amps with $C_C = 4.6$ pF and conventional op-amps with $C_C = 50$ pF for strong inversion were fabricated in 130-nm CMOS process

TABLE IV
SUMMARY OF THE MEASUREMENT RESULTS AND PERFORMANCE COMPARISON

Parameter(units)	**Conv-A**		**This work**		**[14]**	**[15]**	**[9]**	**[16]**	**[17]**	**[18]**	**[4]**	**[19]**
Inversion level	SI	SBT	SI	SBT	SI	SI	SI	SBT	SI	SI	SBT	SBT
CMOS process (nm)	130	130	130	130	180	500	180	180	NA	180	350	130
Supply voltage (V)	±0.6	±0.25	± 0.6	±0.25	1.8	±1	±1.65	0.7	±1.65	±0.9	1	0.25
Capacitive load (pF)	50	50	50	50	200	70	20	20	30	25	200	15
SR+ (V/µs)	1.5	.07	37	.08	74.1	9.8	88.2	1.8	24	31	.007	.0006
SR- (V/µs)	0.3	.002	34	.12	NA	7.6	42	3.8	22	28	.003	.0008
DC gain (dB)	70	43	83	72	72	81.7	82	57.5	68	90.8	120	60
PM (º)	70	60	62	60	50	60	NA	60	73	58.4	54	52.5
GBW (MHz)	1.1	.058	63	0.72	86.5	4.75	NA	3	21.8	12.5	.02	.0018
CMRR @DC (dB)	164	160	158	190	NA	78	NA	19	75	68	70	NA
PSRR+ @DC (dB)	49	49	67	64	NA	72	95	52.1	78	64	98	NA
PSRR-@DC (dB)	45	47	50	53	NA	74	83	66.4	75	66	NA	NA
Eq.input-noise (nV/√Hz)	68@.1 M	220 @10k	25@ 1M	160 @.1M	0.8 @.1M	35@ 1M	NA	100 @1M	NA	27	4850 @1kHz	3300
I_{TotalQ}(µA)	70	0.3	158	.78	6611	60	82	36.3	418	43	.195	.072
Power (µW)	84	0.15	190	.39	11900	120	270	25.4	1380	80	.195	.018
Area (mm^2)	.07	.01	.02	.02	.07	.02	.02	.02	.03	.02	.004	.08
FoM_{LS}(V.pF/ µs.µW)	0.2	0.7	9	10	1.25	4.4	3.2	2.2	0.47	8.7	3.07	0.5
FoM_{SS} (MHz.pF/ µW)	0.7	19	17	92	1.45	2.7	NA	2.36	0.47	3.9	20.5	1.5
FOM_G	0.37	3.6	12	30	1.3	3.4	NA	2.3	0.47	5.86	8	0.9
$AFOM_L$	2.5	67	447	512	18	222	155	71	16	438	769	6
$AFOM_S$	0.9	1933	828	4651	21	138	NA	118	16	195	5128	19
$IFOM_L$	.2	0.3	11	5	2	9	10	1	2	16	3	0.1
$IFOM_S$	0.8	10	20	46	3	5	NA	2	2	7	20	0.4

*SI Strong-Inversion *SBT Sub-threshold

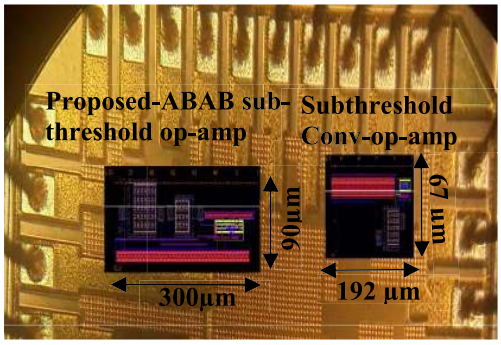

Fig. 27. Micrograph of the Proposed-AB-AB and Conv-A op-amp in subthreshold.

technology. For subthreshold operation, the proposed and Conv-A op-amps were fabricated with $C_C = 4.6$ pF in 130-nm CMOS process also. The chips were tested with ±0.6-Vsupply voltage, quiescent current $I_{\text{Total}Q} = 158$ μA in strong inversion, ±0.25-V supply voltage and total quiescent current 0.78 μA in the subthreshold region. In both cases, the load capacitance C_L is 50 pF.

A. Operation in Strong Inversion

The measured frequency response of the Conv-A and Proposed-AB-AB op-amps as voltage followers are shown in Fig. 22. The Proposed-AB-AB op-amp has a bandwidth of 57 MHz, whereas the Conv-A op-amp of Fig. 1 has a bandwidth of 1.1 MHz. Note that the bandwidth of the op-amp is improved by a factor of 52 compared to the conventional one. Transient responses of the op-amps are shown in Fig. 23 to

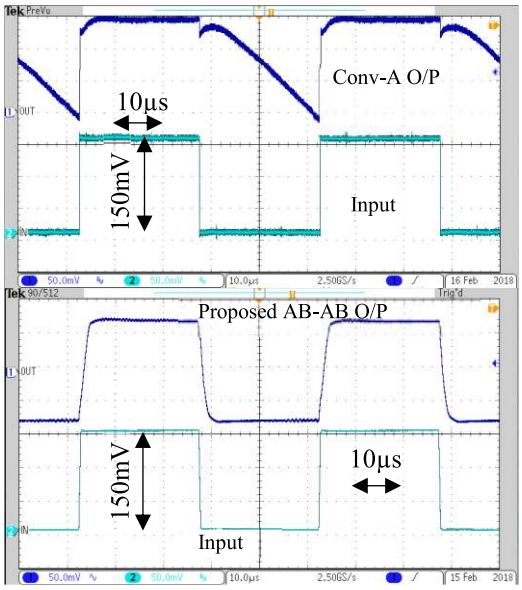

Fig. 28. Experimental transient response of the Proposed-AB-AB and Conv-A op-amp for 20-kHz pulse of 150-mV amplitude at subthreshold.

a 1-MHz, 500-mV pulse input waveform. The positive SRs of the Proposed-AB-AB and Conv-A op-amp are 37 and 1.5 V/μs, respectively. The negative SRs are 34 and 0.3 V/μs for the Proposed-AB-AB and Conv-A op-amps. Thus, the SR of the proposed op-amp is 113 times higher than for the Conv-A op-amp obtained from the experimental results. The SR of the op-amp is given by $\text{SR} = I_{\text{OutMax}}/(C_L + C_C)$. From this expression of SR experimental maximum positive and negative current can be calculated.

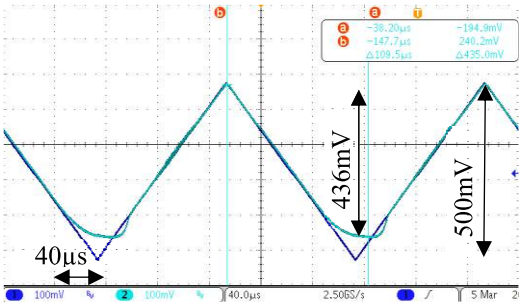

Fig. 29. Experimental input range for the Proposed-AB-AB op-amp at subthreshold for ±250 mV, 5-kHz triangular pulse.

Experimental maximum positive output currents for the Conv-A and Proposed-AB-AB op-amp are 150 μA and 2 mA. The maximum negative currents for Conv-A and Proposed-AB-AB op-amps are 30 μA and 1.8 mA. Hence, current efficiency CE of the Proposed-AB-AB op-amp is 11, whereas for Conv-A it is only 0.4. The input/output common mode ranges of the proposed op-amp are shown in Fig. 24 for a ±600-mV, 1-MHz triangular input waveform. They have values of +600 and −384 mV for the proposed op-amp. Fig. 25 shows the chip micrograph of the proposed and conventional op-amps. Designed layouts are superimposed due to the opaque passivation layer. The silicon area consumed by the conventional op-amp is 0.07 mm^2, whereas the area of the proposed op-amp is only 0.02 mm$^{2.}$ Hence, in the proposed approach, higher large- and small-signal FOM can be obtained, while the silicon area can be essentially reduced because of smaller C_C.

B. Operation in Subthreshold Region

Fig. 26 shows the experimental frequency response of the Proposed-AB-AB and Conv-A op-amp in voltage follower configuration. The bandwidths of the Proposed-AB-AB and Conv- A op-amp are 700 and 58 kHz, respectively. Fig. 27 shows the micrograph of the fabricated chip with the op-amps designed for subthreshold operation. The area occupied by the Proposed-AB-AB op-amp is 0.02 mm^2 which is two times more than the Conv-A op-amp designed in subthreshold. Though the proposed and conventional class-A op-amps are using similar compensation capacitor, the former occupied a larger area because the Proposed AB-AB op-amp has an extra capacitor C_{BAT}. The transient responses of conventional and proposed op-amps are given in Fig. 28 for a 20-kHz square waveform with 150-mV amplitude. The positive and negative SRs of the Proposed-AB-AB op-amp are 0.08 and 0.12 V/μs, whereas for Conv-A, they are 0.07 and 0.002 V/μs, respectively.

Hence, the negative SR of the Conv-A op-amp is very poor. The maximum positive and negative output currents for the Proposed-AB-AB op-amp are 4.2 and 6.24 μA, while the Conv-A op-amp has maximum positive and negative current of 3.6 and 0.1 μA. The CE in subthreshold for the Proposed AB-AB op-amp is 6 and for Conv-A, it is 0.3. Hence, the proposed op-amp can achieve improved negative SR. Finally, the proposed op-amp can provide 12 times higher GBW, 62 times higher negative output current at the expense of increasing the quiescent power dissipation by a factor 2.6. The input/output common mode ranges for the Proposed-AB-AB op-amp are between 242 and –194.9 mV for ±250-mV 5-kHz triangular pulse, as shown in Fig. 29.

A comprehensive comparison of the proposed op-amp's performance with other state-of-the-art class-AB amplifiers is given in Table IV. From the table, it can be asserted that except the Si area related FOMs (strongly technology dependent), the Proposed-AB-AB op-amp has the highest small-signal, large-signal, and global FOM in strong inversion and subthreshold region. However, in strong inversion [18], it has 1.4 times higher IFOM$_L$; all other FOMs of it are lower.

VI. Conclusion

A power-efficient Miller op-amp architecture was reported and experimentally verified. Two versions of the op-amp were presented here: working in strong inversion as well as in subthreshold with little modification. These two versions were fabricated in 130-nm CMOS technology.

Experimental results verified that the proposed op-amp working with 1.2-V supply voltage has essentially improved large- and small-signal FOM$_{\text{LS}}$ = 9 and FOM$_{\text{SS}}$ = 17. The proposed op-amp operating in subthreshold also has the largest FOMs: FOM$_{\text{LS}}$ and FOM$_{\text{SS}}$ of 10 and 92, respectively. According to the literature presented in this paper, consequently, the highest value of the global FOM can be achieved which determines the ultimate speed of the proposed op-amp.

As in the subthreshold region, the op-amp can also operate with a very low supply voltage (±0.25 V); it can be used in applications where power constraints exist, such as in biomedical instruments and wireless sensor networks. Finally, it can be asserted that experimental results validated the proposed circuit's principle.

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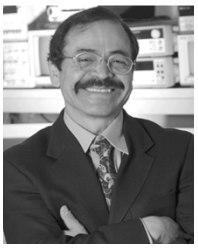

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