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Pulse delay control for capacitor voltage balancing in a three-level boost neutral point clamped inverter

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Abstract: The cross regulation effect in multi-output DC/DC converters offers a reliable support for the grid integration of multilevel inverters by balancing the capacitor voltages. The capacitor voltage balancing by single input dual output boost converter is often realised by conventional three-level switching scheme. The three-level operation benefits lower inductor ripple current, but it limits the maximum possible compensation voltages. In this study, the entire operating modes of the boost converter is presented and all the possible cases which contribute to the voltage balancing are employed for balancing the capacitor voltages in a three-level neutral point clamped inverter. A proportional-integral controller based duty ratio control and pulse delay control are used for DC link voltage regulation and capacitor voltage balancing. Since the classical state-space averaging technique is not suitable for SIDO converters, inductor current ripple averaging technique is utilised for controller design. The circuit simulation is performed in Matlab/Simulink. The digital controller is realised using the Virtex-5FPGA in Labview/CompactRIO module. Both simulation and experimental results are presented to validate the controller performance.

1 Introduction

The increased grid integration of renewable energy resources, especially from offshore platforms, demands power transmission at high voltage to limit the current and thereby, associated losses. The power conditioning systems such as inverters and DC/DC converters are often required to provide electricity to the load centres. In response to the growing demand for medium and high power applications, multilevel converters are chosen to be the inevitable appliance for power conversion. Neutral point clamped (NPC) inverter is one of the main attractive topology among multilevel inverters for renewable energy conversion and for drive industry so far. However, capacitor voltage imbalance with respect to the neutral point is one of the key areas under discussion [1]. Several voltage balancing techniques for conventional NPC inverter are discussed in literature. Every method is generally based on either adjusting the modulation strategy, or adding passive or active elements. Jie Shen *et al.* have presented the self-balancing property of a three-level NPC converter in [2]. Since the neutral-point (NP) voltage drifts for small variations in the system parameters, self-balancing technique will not always suffice. NP voltage control methods based on carrier pulse width modulation (CPWM) and space vector modulation (SVM) strategies are discussed in [3–10]. In addition, several hybrid modulation strategies are also developed for voltage balancing [11–13]. In contrast, these modified PWM methods increase the complexity and digital resource consumption. Several NP voltage balancing circuits for NPC inverter are presented in literature [14–16].

A single input dual output (SIDO) boost converter, which is often called as three-level boost (TLB) converter, can halve the power device voltage stress compared with the conventional two-level boost converter, which is more suitable in low voltage input-high voltage output applications. Additionally it has several advantages in high voltage applications such as reduced switching losses and lower reverse recovery losses of the diode compared with the conventional boost converters [17, 18]. The SIDO boost circuit for power factor correction is discussed in [17–19]. The maximum power point tracking by direct duty ratio control of this converter using a power hysteresis is presented in [20]. A TLB converter circuit is proposed for NP voltage balancing in [17, 18, 20–22]. Independent duty ratio control of the switches are considered for voltage balancing of dc-link capacitors in [20, 21]. Xia, *et al.* have proposed switch signal phase delay control (SSPDC) method for balancing the NP voltage with simulation results, where the signal phase delay lies between d and $(1-d)$ for a duty ratio d [22]. A similar method is experimentally proved for resistive loads at 50% duty ratio in [23]. PDC technique is based on the dynamic variation of pulse delay to compensate the capacitor voltages, which results different cases, including either two, three or four modes of operation of the SIDO boost converter. In this article, the authors extend the operation of the converter to eight different cases to compensate the neutral voltage imbalance where the delay varies from zero to the switching period, T.

This paper discusses the control and implementation of the SIDO boost converter for DC voltage boosting and PDC based NP voltage balancing. It operates as front-end of a three-level NPC inverter. The capacitor voltage deviation at steady state and proportional-integral (PI) controller parameter calculation methods are derived for each cases. The simulation and experimental results are provided to validate the DC link and NP voltage control techniques.

2 SIDO boost converter

The schematic circuit of three-level boost NPC (TLBNPC) inverter considered for analysis is shown in Fig. 1*a*. The input is a DC voltage source in series with an inductor L. The NP of the inverter is connected to the midpoint of the switches S_1 and S_2. R_s, C_s and D_s are the snubber circuit elements for transient voltage protection. C_1 and C_2 are the DC link capacitors. The NPC inverter is connected to a RL load. The boost converter allows four different modes of operation. It gives different behaviours depending on the switching sequence and the time of operation of each mode. To analyse the modes of operation, the NPC inverter can be replaced by variable resistive loads. It is assumed that the inductance L is large enough to maintain the current in continuous conduction mode and the capacitors are large enough to keep the output voltage constant. The four modes of operation of boost converter in steady state with relevant voltage and current equations in ideal condition can be summarised as follows.

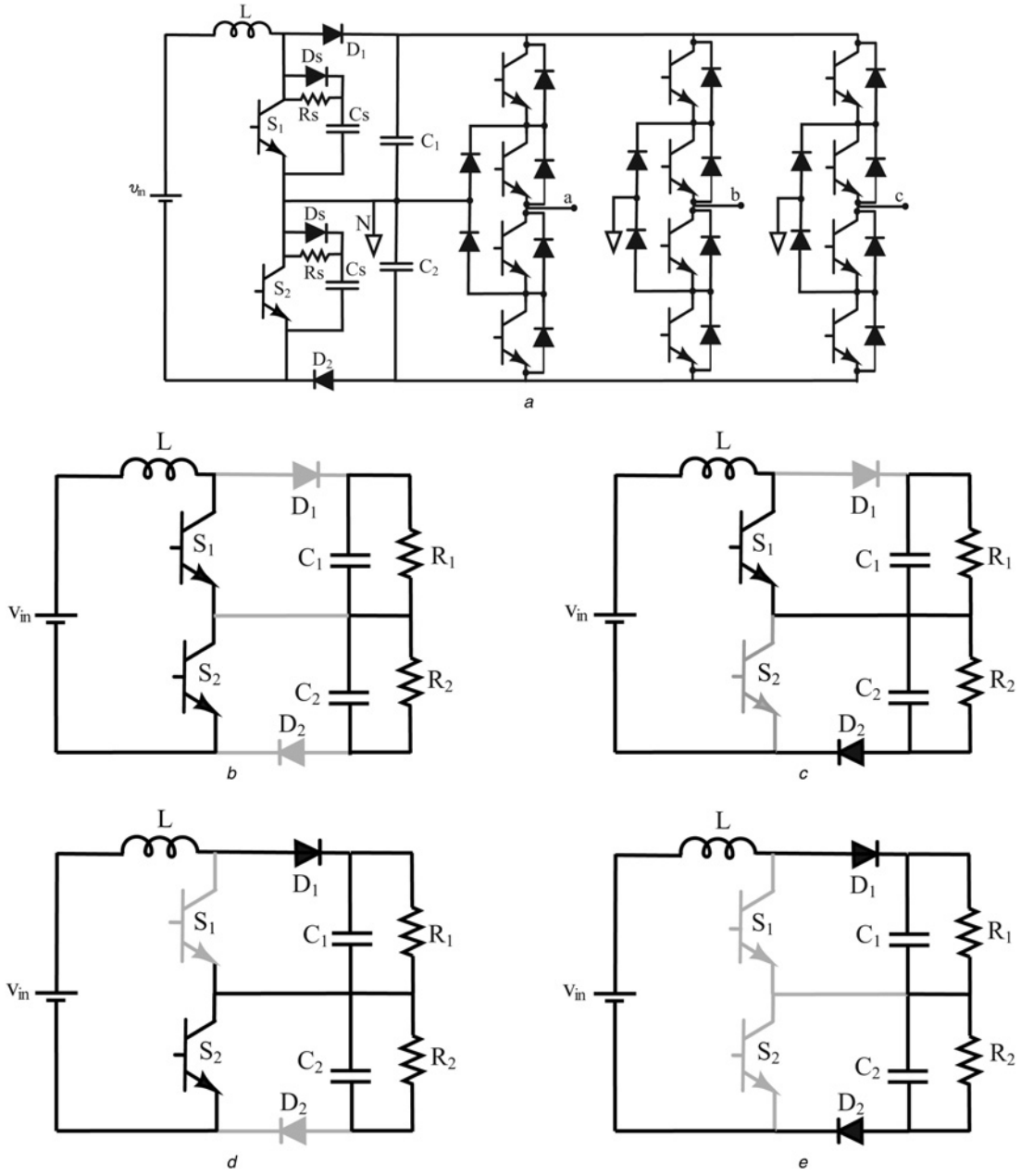

Fig. 1 *Schematic circuit of TLBNPC inverter considered for analysis*

a Circuit schematic of TLBNPC inverter, Principle of operation of SIDO boost converter
b Mode 1
c Mode 2
d Mode 3
e Mode 4

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In mode 1, both S_1 and S_2 are ON. Therefore, the inductor current increases and the load current is supplied by C_1 and C_2 as shown in Fig. 1*b*. The relevant voltage and current equations during this interval is given in (1)

$$\begin{aligned} pi_{\mathrm{L}} &= \frac{v_{\mathrm{in}}}{L} \\ pv_{\mathrm{C1}} &= -\frac{v_{\mathrm{C1}}}{R_1 C_1} \\ pv_{\mathrm{C2}} &= -\frac{v_{\mathrm{C2}}}{R_2 C_2} \end{aligned} \tag{1}$$

where p is the differential operator d/dt. v_{in} is the input voltage, v_{C1}, v_{C2} represent the corresponding voltages across C_1 and C_2, i_{L} is the inductor current and R_1, R_2 are the load resistors.

In mode 2, S_1 is ON and S_2 is OFF. Therefore, the capacitor C_2 charges and the capacitor C_1 discharges to the load as shown in Fig. 1*c*. The state equations in this mode are presented in (2)

$$\begin{aligned} pi_{\mathrm{L}} &= \frac{v_{\mathrm{in}} - v_{\mathrm{C2}}}{L} \\ pv_{\mathrm{C1}} &= -\frac{v_{\mathrm{C1}}}{R_1 C_1} \\ pv_{\mathrm{C2}} &= \frac{i_{\mathrm{L}} R_2 - v_{\mathrm{C2}}}{R_2 C_2} \end{aligned} \tag{2}$$

In mode 3, S_1 is OFF and the switch S_2 is ON. The input current flows only through the first output (C_1 and R_1) and current through R_2 is supplied by the capacitor C_2 as shown in Fig. 1*d*. Equation (3) shows the voltage and current equations during this interval

$$\begin{aligned} pi_{\mathrm{L}} &= \frac{v_{\mathrm{in}} - v_{\mathrm{C1}}}{L} \\ pv_{\mathrm{C1}} &= \frac{i_{\mathrm{L}} R_1 - v_{\mathrm{C1}}}{R_1 C_1} \\ pv_{\mathrm{C2}} &= -\frac{v_{\mathrm{C2}}}{R_2 C_2} \end{aligned} \tag{3}$$

In mode 4, both S_1 and S_2 are OFF as shown in Fig. 1*e* The input current flows through both outputs and delivers energy to both. The state equations can be expressed as in (4)

$$\begin{aligned} pi_{\mathrm{L}} &= \frac{v_{\mathrm{in}} - v_{\mathrm{C1}} - v_{\mathrm{C2}}}{L} \\ pv_{\mathrm{C1}} &= \frac{i_{\mathrm{L}} R_1 - v_{\mathrm{C1}}}{R_1 C_1} \\ pv_{\mathrm{C2}} &= \frac{i_{\mathrm{L}} R_2 - v_{\mathrm{C2}}}{R_2 C_2} \end{aligned} \tag{4}$$

3 SIDO boost converter control

The NPC inverter input voltage control and capacitor voltage balancing are considered as the control objectives of the SIDO boost converter. The controls are realised using two PI controllers. The DC link voltage control and balancing can be achieved by minimum number of sensors. The control block diagram is given in Fig. 2.

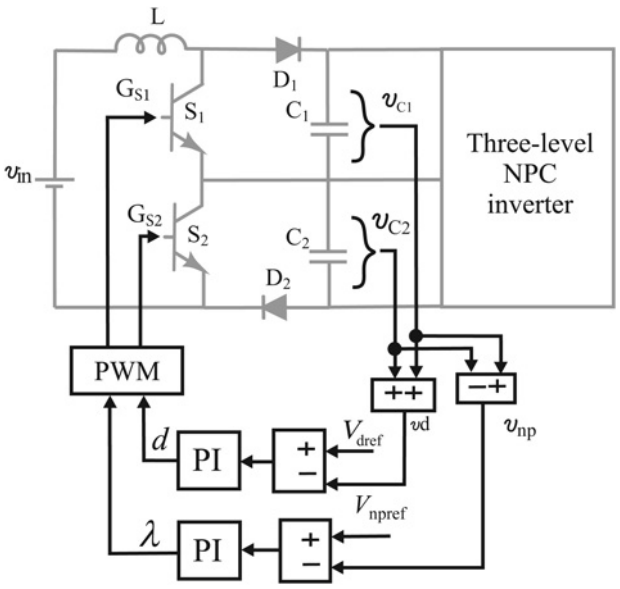

Fig. 2 *Block diagram representation of SIDO boost converter control*

3.1 DC voltage control

Similar to the conventional boost converters, the steady state output voltage of the SIDO converter can be calculated approximately using the input voltage V_{in} and the duty ratio d as in (5).

$$V_{\mathrm{d}} \simeq \frac{V_{\mathrm{in}}}{1-d} \tag{5}$$

The DC link voltage control utilises the boost capability of the SIDO converter to calculate the duty ratio of the switches to obtain the desired voltage across the DC link capacitors. It provides a high voltage at the input of the NPC converter; thereby total harmonic distortion of the inverter output voltage improves. The DC link control is achieved by a PI controller as shown in Fig. 2. The output of the PI controller is proportional to the duty ratio of the switches to achieve the desired DC link voltage. The voltage error e_{vd} can be defined as $V_{\mathrm{dref}} - v_{\mathrm{d}}$; where V_{dref} is the desired DC link voltage and v_{d} is the actual voltage across C_1 and C_2.

3.2 Pulse delay control (PDC)

The capacitor voltages are regulated by PDC using a PI controller as shown in Fig. 2. In this method, both switches operate at the same duty ratio and constant switching frequency. To compensate the voltage in neutral point a delay is introduced to move the control signal G_{S1} either forward or backward in relation with G_{S2}, where G_{S1} and G_{S2} are the control signals of S_1 and S_2, respectively. In the PDC control, two capacitor voltages are sensed and the voltage difference is compared with the set point. The output of the PI controller is proportional to the delay between the two control signals to achieve NP voltage to zero. To balance voltages of both capacitors the reference value of NP voltage, V_{npref} is set to be zero. Therefore, the error in NP voltage, e_{np} can be defined as

$$e_{\mathrm{np}} = -v_{\mathrm{np}} = v_{\mathrm{C2}} - v_{\mathrm{C1}} \tag{6}$$

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Table 1 Operational cases

Case	Mode sequence
I	Mode1 ⇒ Mode4
II	Mode1 ⇒ Mode3 ⇒ Mode4 ⇒ Mode2
III	Mode1 ⇒ Mode2 ⇒ Mode4 ⇒ Mode3
IV	Mode2 ⇒ Mode3
V	Mode1 ⇒ Mode2 ⇒ Mode3
VI	Mode1 ⇒ Mode3 ⇒ Mode1 ⇒ Mode2
VII	Mode1 ⇒ Mode3 ⇒ Mode2
VIII	Mode2 ⇒ Mode4 ⇒ Mode3
IX	Mode2 ⇒ Mode4 ⇒ Mode3 ⇒ Mode4
X	Mode2 ⇒ Mode3 ⇒ Mode4

The pulse delay ratio is defined as

$$\lambda = \frac{\text{Delay between } G_{S1} \text{ and } G_{S2}}{T} \tag{7}$$

Depending on the value of duty ratio d and pulse delay ratio λ, the SIDO converter operates in ten different cases which are shown in Table 1.

In contrast with [22], according to PDC method, mode 1 is also possible when $d < 0.5$. The duration of mode 1 (d_1) can have two values d_{11} and d_{12} in case VI. Similarly, for the mode 4 in case IX, each duration is represented by d_{41} and d_{42}. The duration of mode 2 (d_2) and mode 3 (d_3) are the same in all cases. The expressions to calculate the duration of each mode for all the cases are given in (8)

$$\begin{aligned} d_{11} &= \begin{cases} (d-\lambda) & d \geq \lambda \\ 0 & d < \lambda \end{cases} \\ d_{12} &= \begin{cases} (d-1+\lambda) & d \geq 1-\lambda \\ 0 & d < 1-\lambda \end{cases} \\ d_2 &= \min\{d, (1-d), \lambda, (1-\lambda)\} \\ d_3 &= \min\{d, (1-d), \lambda, (1-\lambda)\} \end{aligned}$$

$$\begin{aligned} d_{41} &= \begin{cases} (\lambda - d) & d \leq \lambda \\ 0 & d > \lambda \end{cases} \\ d_{42} &= \begin{cases} (1-d-\lambda) & 1 \geq (d+\lambda) \\ 0 & 1 < (d+\lambda) \end{cases} \end{aligned} \tag{8}$$

Equation (5) can be rewritten as

$$V_d \simeq \frac{V_{in}}{d_2 + d_4} \tag{9}$$

where $d_4 = d_{41} + d_{42}$.

The cases of SIDO converter with the variation in d and λ are given in Fig. 3.

4 Controller design

The parameter identification for total DC link voltage regulation is similar to the conventional boost converter using classical state space averaging technique. The transfer function of $v_d(s)/d(s)$ for case II can be simplified into $G_1(s)$

$$G_1(s) = \frac{-I_L}{C(s + (2/RC))} \tag{10}$$

where $C = C_1 = C_2$ and $R = R_1 = R_2$.

In contrast, the conventional state space averaging technique may not be useful for designing the voltage imbalance regulator as the ripple in the inductor cannot be ignored [24]. Inductor current ripple based averaging method is used for deriving the system transfer function $v_{np}(s)/\lambda(s)$ and also for the controller design. For example, the voltage imbalance regulator design for case II is given below.

In Fig. 4*a*, the switching pulses, inductor current and voltage across the inductor for case 2 operation is given. The inductor current ripple levels are denoted by m, n, p

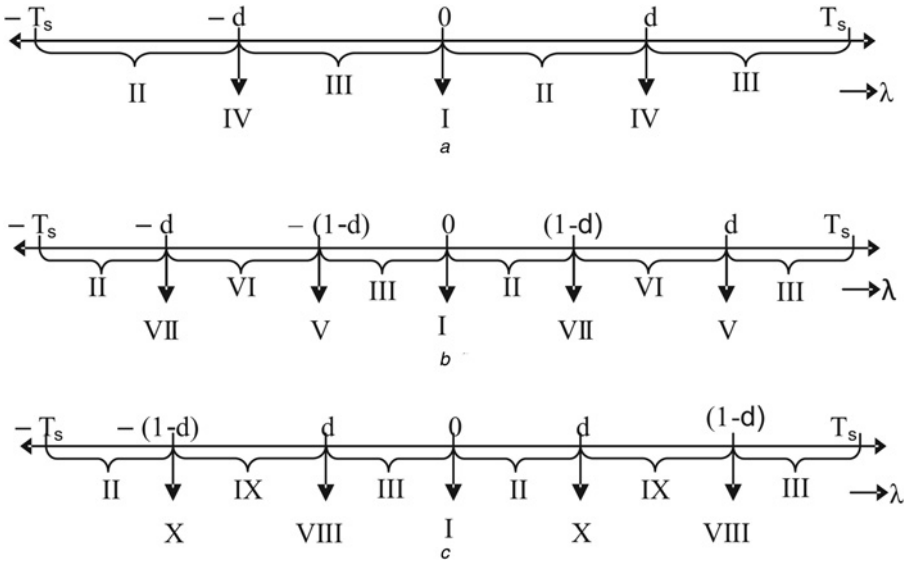

Fig. 3 *Operational cases*

a When $d = 0.5$
b When $d > 0.5$
c When $d < 0.5$

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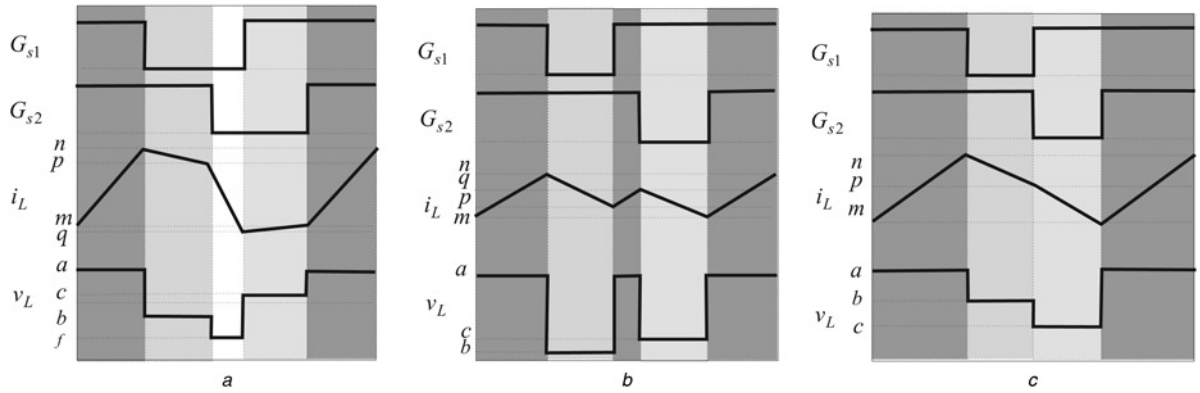

Fig. 4 *Gate signals G_{S1} and G_{S2}, inductor current and inductor voltage of SIDO converter in*

a Case II
b Case VI
c Case VII

and q

$$i_L = \frac{(m+n)}{2}d_1 + \frac{(n+p)}{2}d_3 + \frac{(p+q)}{2}d_4 + \frac{(q+m)}{2}d_2 \tag{11}$$

$$\begin{aligned} n &= m + ad_1 \\ p &= n + bd_3 = m + (ad_1 + bd_3) \\ q &= p + cd_4 = n + (bd_3 + cd_4) = m + (ad_1 + bd_3 + cd_4) \end{aligned} \tag{12}$$

In (12), $a = v_{\text{in}}T/L$, $b = (v_{\text{in}} - v_{\text{C1}})T/L$ and $c = (v_{\text{in}} - v_{\text{d}})T/L$. Substituting (12) in (11), the average inductor current in each mode can be estimated as follows

$$\left(\frac{n+p}{2}\right) = i_{\text{L}} + \frac{T}{2L}[v_{\text{in}}(d_1 - d_4) + v_{\text{C1}}(d_4 - d_1(d_3 + d_4)) + v_{\text{C2}}d_4(d_4 + d_2)] \tag{13}$$

$$\left(\frac{p+q}{2}\right) = i_{\text{L}} + \frac{T}{2L}\left[v_{\text{in}}(d_1 + d_3) - v_{\text{C1}}(d_3 + d_1(d_3 + d_4)) - v_{\text{C2}}d_4(d_1 + d_3)\right] \tag{14}$$

$$\left(\frac{q+m}{2}\right) = i_{\text{L}} + \frac{T}{2L}\left[-v_{\text{C1}}\, d_1(d_3 + d_4) - v_{\text{C2}}\, d_4(d_1 + d_3)\right] \tag{15}$$

In general, the system representation in state space form is $\dot{x} = \boldsymbol{A}x + \boldsymbol{B}u$. The state variable matrix $\boldsymbol{x}$ is chosen as $\begin{bmatrix} i_{\text{L}} & v_{\text{C1}} & v_{\text{C2}} \end{bmatrix}^{\text{T}}$; u is the input variable v_{in}. From the above stated inductor current ripple based averaging technique, the state matrix $\boldsymbol{A}$ and input matrix $\boldsymbol{B}$ can be calculated as follows

$$\begin{aligned} \boldsymbol{A} &= \boldsymbol{a}_1 d_1 + \boldsymbol{a}_2 d_2 + \boldsymbol{a}_3 d_3 + \boldsymbol{a}_4 d_4 \\ \boldsymbol{B} &= \boldsymbol{b}_1 d_1 + \boldsymbol{b}_2 d_2 + \boldsymbol{b}_3 d_3 + \boldsymbol{b}_4 d_4 \end{aligned} \tag{16}$$

The average inductor current, I_L in each mode is replaced by the corresponding expressions given in (13), (14) and (15).

The state matrix in each mode can be expressed as (see (17) at the bottom of next page).

$$\boldsymbol{b}_1 = \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \end{pmatrix} \quad \boldsymbol{b}_2 = \begin{pmatrix} \frac{1}{L} \\ \frac{(d_1 - d_4)T}{2LC_1} \\ 0 \end{pmatrix} \quad \boldsymbol{b}_3 = \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \end{pmatrix} \tag{18}$$

$$\boldsymbol{b}_4 = \begin{pmatrix} \frac{1}{L} \\ \frac{(d_1 + d_3)T}{2LC_1} \\ \frac{(d_1 + d_3)T}{2LC_2} \end{pmatrix}$$

From (8) and Fig. 3, the duration of each mode in case 2 can be calculated as $d_1 = d - \lambda$, $d_2 = d_3 = \lambda$ and $d_4 = 1 - d - \lambda$. (see (19) at the bottom of next page).

$$\boldsymbol{B} = \begin{pmatrix} \frac{1}{L} \\ \frac{(d-\lambda)(1-d)T}{2LC_1} \\ \frac{d(1-d-\lambda)T}{2LC_2} \end{pmatrix} \tag{20}$$

The NP voltage deviation can be derived by subtracting the elements in second row by the third row in (19) and (20). The expressions for neutral point voltage from DC and AC analysis can be derived by perturbation method by adding the disturbance terms to the state variables as $d = D + \tilde{d}$, $\lambda = \Lambda + \tilde{\lambda}$, $v_{\text{np}} = V_{\text{np}} + \tilde{v}_{\text{np}}$, $i_L = I_L + \tilde{i}_L$ and $v_{\text{in}} = V_{\text{in}} + \tilde{v}_{\text{in}}$

$$\frac{d}{\text{d}t}v_{\text{np}} = \frac{\lambda(1-d-\lambda)T}{2LC}v_{\text{d}} + \frac{\lambda(2d-1)T}{2LC}v_{\text{in}} - \frac{v_{\text{np}}}{RC} \tag{21}$$

In steady state

$$\begin{aligned} V_{\text{np}} &= \frac{\Lambda RT}{2L}\left[(1 - D - \Lambda)V_{\text{d}} + (2D-1)V_{\text{in}}\right] \\ &= \frac{\Lambda RT}{2L}\left[\frac{(1 - D - \Lambda)}{(1-D)} + (2D-1)\right]V_{\text{in}} \end{aligned} \tag{22}$$

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$$V_{\rm np} = \frac{k_{\rm dc} RT}{2L} V_{\rm in} \tag{23}$$

$$\frac{\tilde{v}_{\rm np}(s)}{\tilde{\lambda}(s)} = \frac{T}{2LC} \frac{\left[(1-d-2\Lambda)v_{\rm d} + (2d-1)v_{\rm in}\right]}{\left(s + (1/RC)\right)} \tag{24}$$

$$G_2(s) = \frac{\tilde{v}_{\rm np}(s)}{\tilde{\lambda}(s)} = \frac{T}{2LC} \frac{k_{\rm ac}}{\left(s + (1/RC)\right)}$$
$$k_T = \frac{k_{\rm ac} T}{2LC} \tag{25}$$

Closed loop transfer function, $G_{c2}(s)$ can be written as

$$G_{c2}(s) = \frac{k_T k_p s + k_T k_i}{s^2 + \left(\tau + k_T k_p\right) + k_T k_i}$$
$$\tau = \frac{1}{RC} \tag{26}$$

The PI controller parameters can be calculated as

$$k_p = \frac{(2\xi w_n - \tau)}{k_T} \quad \text{and} \quad k_i = \frac{w_n^2}{k_T} \tag{27}$$

where ξ is the damping ratio and $w_{\rm n}$ is the natural frequency of the converter.

The expressions for $k_{\rm dc}$ and $k_{\rm ac}$ in each case are summarised in Tables 2 and 3. The inductor ripple current is similar in case II and case III, case V and case VII, case VI and case IX and case VIII and case X. From the controller design, the parameters values are obtained as positive gains for cases II, III, V and VII. For cases VI, VIII, IX and X, the controller gains are negative. The normalised value of compensation voltages ($V_{\rm np,norm} = V_{\rm np}/V_{\rm d}$) in steady state by SSPDC and PDC methods are presented in Fig. 5. The Fig. 5*a* shows the compensation voltages by SSPDC when Λ varies from d to $(1-d)$. Fig. 5*b* shows the compensation voltages by PDC when Λ varies from zero to one. The maximum and minimum value of $V_{\rm np,norm}$ by SSPDC method is 0.2102 (at $d = 0.7$ and $\Lambda = 0.015$) and -0.1875 (at $d = 0.3$ and $\Lambda = 0.365$). In PDC method, $V_{\rm np,norm}$ varies from -0.3945 (at $d = 0.5$ and $\Lambda = 0.25$) to 0.3945 (at $d = 0.5$ and $\Lambda = 0.75$).

Table 2 Expressions of k_{dc} in each case

case II	$\Lambda(((1-D-\Lambda)/(1-D)) + (2D-1))$
case III	$-(1-\Lambda)(((\Lambda-D)/(1-D)) + (2D-1))$
case V	$-(1-D)(D+\Lambda-1)$
case VI	$(1-D)(1-2\Lambda)$
case VII	$((1-D)^2(2D-1))/(1-D)$
case VIII	$((-D^2(\Lambda-D))/(1-D))$
case IX	$((D^2(1-2\Lambda))/(1-D))$
case X	$((D^2(1-\Lambda-D))/(1-D))$

Table 3 Expressions of $k_{\rm ac}$ in each case

case II	$(1-D-2\Lambda)v_{\rm d} + (2D-1)v_{\rm in}$
case III	$(2D-1)v_{\rm in} - (1-2\Lambda+D)v_{\rm d}$
case V	$(1-D)v_{\rm in}$
case VI	$-2(1-D)v_{\rm in}$
case VII	$(1-D)(v_{\rm d} - 2v_{\rm in})$
case VIII	$D(-v_{\rm d} + v_{\rm in})$
case IX	$2D(-v_{\rm d} + v_{\rm in})$
case X	$D(-v_{\rm d} + v_{\rm in})$

$$\boldsymbol{a}_1 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & \dfrac{-1}{R_1C_1} & 0 \\ 0 & 0 & \dfrac{-1}{R_2C_2} \end{pmatrix} \quad \boldsymbol{a}_2 = \begin{pmatrix} 0 & 0 & -\dfrac{1}{L} \\ 0 & \dfrac{-1}{R_1C_1} & 0 \\ \dfrac{1}{C_2} & \dfrac{-d_1(d_3+d_4)T}{2LC_2} & \dfrac{-d_4(d_1+d_3)T}{2LC_2} - \dfrac{1}{R_2C_2} \end{pmatrix}$$

$$\boldsymbol{a}_3 = \begin{pmatrix} 0 & -\dfrac{1}{L} & 0 \\ \dfrac{1}{C_1} & \dfrac{(d_4 - d_1(d_3+d_4))T}{2LC_1} - \dfrac{1}{R_1C_1} & \dfrac{d_4(d_4+d_2)T}{2LC_1} \\ 0 & 0 & -\dfrac{1}{R_2C_2} \end{pmatrix} \tag{17}$$

$$\boldsymbol{a}_4 = \begin{pmatrix} 0 & -\dfrac{1}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C_1} & \dfrac{-(d_3 + d_1(d_3+d_4))T}{2LC_1} - \dfrac{1}{R_1C_1} & \dfrac{-d_4(d_1+d_3)T}{2LC_1} \\ \dfrac{1}{C_2} & \dfrac{-(d_3 + d_1(d_3+d_4))T}{2LC_2} & \dfrac{-d_4(d_1+d_3)T}{2LC_2} - \dfrac{1}{R_2C_2} \end{pmatrix}$$

$$\boldsymbol{A} = \begin{pmatrix} 0 & \dfrac{d-1}{L} & \dfrac{d-1}{L} \\ \dfrac{1-d}{C_1} & \dfrac{-(d-\lambda)(1-d)^2T}{2LC_1} - \dfrac{1}{R_1C_1} & \dfrac{(1-d-\lambda)(d^2-d+\lambda)T}{2LC_1} \\ \dfrac{1-d}{C_1} & \dfrac{-[(d-\lambda)(1-d)^2 + \lambda(1-d-\lambda)]T}{2LC_2} & \dfrac{-d(1-d)(1-d-\lambda)T}{2LC_2} - \dfrac{1}{R_2C_2} \end{pmatrix} \tag{19}$$

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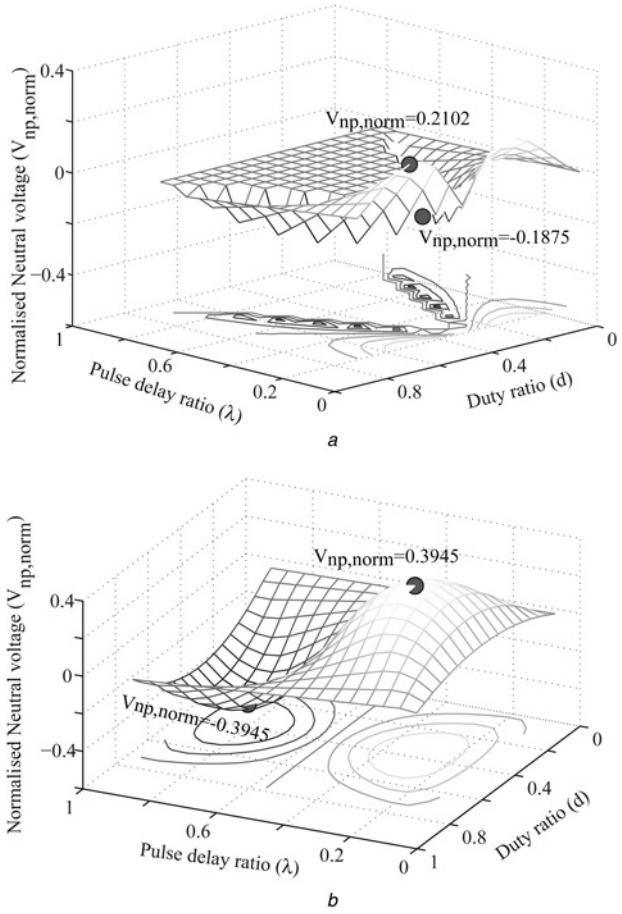

Fig. 5 *Normalised imbalance compensation voltage in*
a SSPDC method
b PDC method

5 NPC inverter modulation

The main modulation techniques for NPC inverter can be classified as CPWM and SVM. The different CPWM techniques for NPC converters are presented in [25]. The three main techniques are phase disposition PWM (PDPWM), alternative phase opposition disposition (APOD) and phase opposition disposition (POD) PWM. The switching state relation of NP voltage imbalance can be clearly explained with SVM. At the same time, it increases the computational complexity. CPWM method is simpler for implementation. PDPWM method considered in this paper needs two carrier signals to specify the boundaries between the voltage levels. This modulation strategy retains lower harmonic energy in the line-line inverter output voltage compared with other CPWM methods such as APOD or POD [26]. The peak value of NPC inverter output phase voltage can be calculated as

$$V_{\mathrm{ac}} = \frac{m_i V_{\mathrm{d}}}{2} = m_i \frac{V_{\mathrm{in}}}{2(1-d)} \tag{28}$$

where m_i is the modulation index.

6 Simulation results

The functionality of the proposed control algorithm is examined via simulations performed in Matlab/Simulink. The circuit and controller parameters used for simulation

Table 4 System parameters

boost inductance (L)	131.5 μH
DC link capacitance (C_1, C_2)	17 mF
Snubber capacitance (C_s)	3.3 μF
Snubber resistance (R_s)	2.5 Ω
load resistance	10 Ω
load inductance	2.5 mH

Table 5 Controller parameters

k_{p1}	1.417
k_{i1}	19
k_{p2}	0.52
k_{i2}	31.25
SIDO converter switching period (T)	200 μs
NPC inverter switching period (T_{sw})	540 μs
dead time (T_0)	22.5 μs

are given in Tables 4 and 5, respectively. These values are chosen to match with the system used for subsequent experiments. The PI controller response for DC voltage control is given in Fig. 6*a*. The capacitor voltages before and after balancing are presented in Fig. 6*b*. The transient period of PDC results a small oscillation in the voltage controller output. The NPC inverter is operated with a RL load at a constant modulation index of 0.8. The inverter voltage and current waveforms before and after NP voltage balancing are given in Figs. 6*c* and *d*. The NP voltage imbalance increases the $\mathrm{d}V/\mathrm{d}t$ and inverter peak current. Moreover, it introduces asymmetry in the output voltage and current waveforms. However, the PDC and DC voltage control provides balanced capacitor voltages and improves the inverter waveforms.

7 Control implementation

The control algorithm is implemented in Labview/FPGA. The complete algorithm is executed in independent synchronised parallel loops. If the error between the controller reference and actual value is less than the tolerance level, the error is assumed to be zero which avoids the oscillations around the set point as given in (29). The control loop updates the duty ratio and the phase value in every 0.04 ms.

$$e_{vd} = \begin{cases} 0 & |e_{vd}| < 0.5 \\ e_{vd} & \text{othercases} \end{cases} \tag{29}$$

$$e_{\mathrm{np}} = \begin{cases} 0 & |e_{\mathrm{np}}| < 0.125 \\ e_{\mathrm{np}} & \text{other cases} \end{cases}$$

The pulse G_{S1} for S_1 is generated from the duty ratio value obtained from the DC voltage controller. The pulse G_{S1} delays G_{S2} with a phase value corresponding to the error in voltage difference. The delay controller receives a new value only when the voltage error is within the tolerance band. It avoids the transients when the duty ratio and phase change occur simultaneously. The control signal G_{S2} is generated in two sequential steps, the first is responsible for the pulse delay and the second is for the pulse generation. The delay loop waiting length (D_{LWL}) is modified with the value from the PI controller in each iteration of the loop. If the delay time is used directly as the loop waiting length, the delay between G_{S1} and G_{S2} grows in every switching

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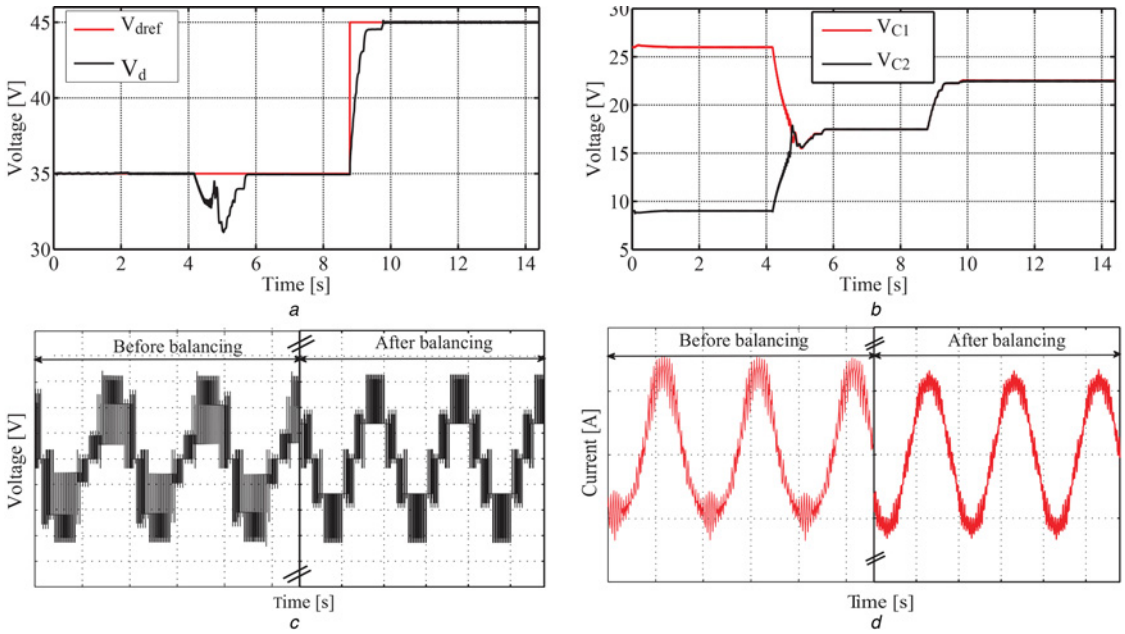

Fig. 6 *Step responses of DC voltage and PDC*

a PI controller response for DC voltage control
b Lower and upper capacitor voltages before and after voltage balancing. NPC inverter output waveforms before Land after capacitor voltage balancing
c Voltage (time axis = 10 ms/div, voltage axis = 10 V/div)
d Current (time axis = 10 ms/div, current axis = 0.5 A/div)

cycle for a positive phase value. This results in deviation of NP voltage from equilibrium. To prevent this delay increment, the loop waiting length is modified as in (30).

$$D_{\mathrm{LWL}} = \begin{cases} \Delta\lambda_k T & \text{for } \lambda_{k+1} \geq \lambda_k \\ (1+\Delta\lambda_k)T & \text{for } \lambda_{k+1} \leq \lambda_k \end{cases} \tag{30}$$

where $\Delta\lambda_k = \lambda_{k+1} - \lambda_k$, is the difference in pulse delay ratio in kth and $(k+1)$th switching period. To keep the frequency constant, the waiting time for the S_2 control signal loop must be equal to the switching period. However, an additional delay of 0.4 µs taken by the internal logic blocks is also considered to synchronise the control signals of S_1 and S_2. The NPC inverter control signals are generated using PDPWM at a frequency of 1.85 kHz in two parallel loops. The reference signals generation and PWM operation are synchronised symmetrically, that is, one sampling point of the reference signal is considered in each carrier interval. The reference signal generation loop takes an internal logic delay of 75 ns. To avoid the DC link shoot through, the control signals are generated with a dead time of 22.5 µs.

8 Experimental results

A laboratory prototype for TLBNPC inverter, shown in Fig. 7, is built and tested to verify the feasibility of the control algorithm. The inductor for the boost converter is designed experimentally in order to keep the process in continuous mode with the smallest possible value. To avoid the inrush current, the hardware circuit is started while the SIDO converter operates in mode 4. During that, there is no NPC input voltage boosting. If the voltage boost control and PDC start simultaneously, there is no risk of unequal voltages at the capacitor even when the boost gain varies. The step response of the PI controller for NPC input voltage control is shown in Fig. 8*a*. The capacitor voltages before and after balancing are presented in Fig. 8*b*.

If the PDC begins after the boost control and especially the NP voltage is higher than the achievable compensation voltage for that particular duty ratio, high voltage oscillation occurs at the NP voltage and that reflects on the duty ratio as well. This situation is noteable to some extent in Figs. 8*c* and *d* where the NP voltage is at the marginal compensation voltage. To re-compensate this situation, the input voltage needs to be increased or the desired voltage at NPC input should be decreased, otherwise a large current will be drawn from the source to balance the voltages. To ensure shoot through protection for SIDO boost circuit, the duty ratio is limited to 99% of the switching period. If the NP voltage is less than the possible compensation voltage at specific duty ratio, the PDC brings the capacitor voltages to equilibrium without any oscillation. Therefore, once the voltages are balanced by PDC, any increase in the desired NPC input voltage or TLB input voltage does not introduce any high voltage oscillation or deviation. The NPC inverter line to line voltage and current before and after balancing are presented in Figs. 10*a* and *b*.

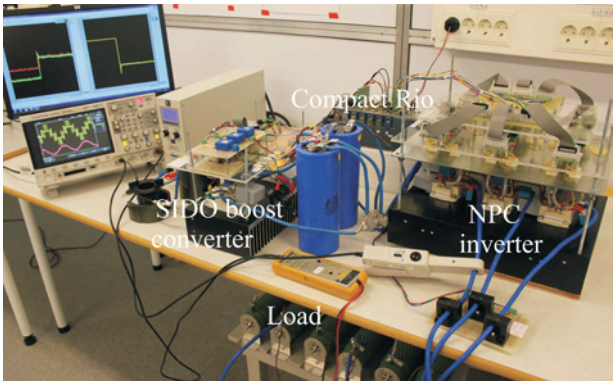

Fig. 7 *Laboratory experimental set up of TLBNPC inverter*

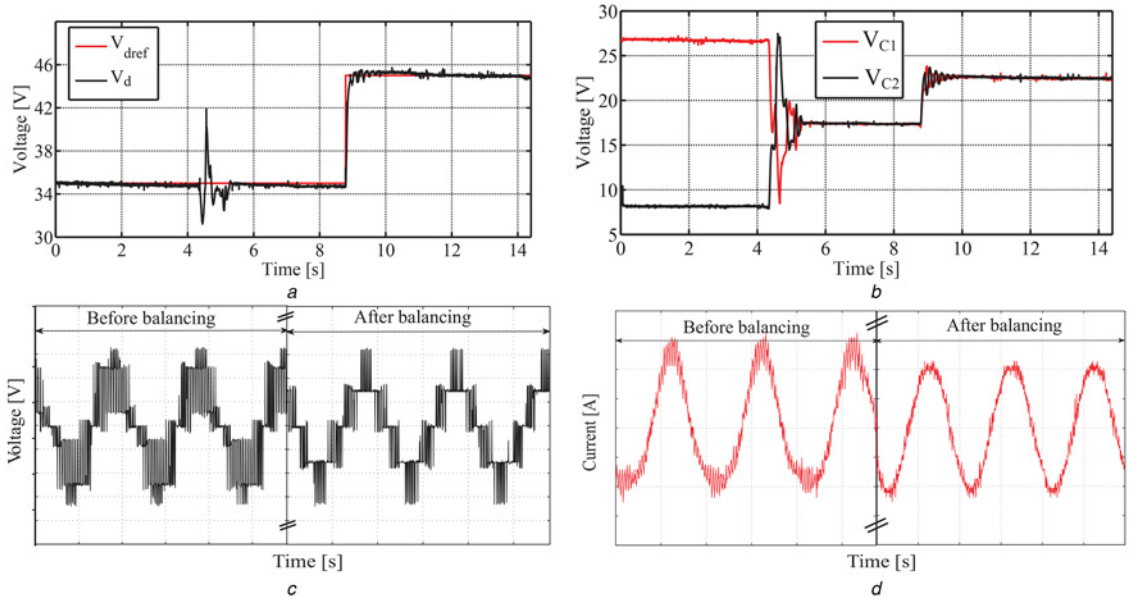

Fig. 8 *Step responses of DC voltage and PDC*

a PI controller response for DC voltage control
b Lower and upper capacitor voltages before and after voltage balancing. NPC inverter output waveforms before and after capacitor voltage balancing
c Voltage (time axis = 10 ms/div, voltage axis = 10 V/div)
d Current (time axis = 10 ms/div, current axis = 0.5 A/div)

Similar to the simulation results, the experimental waveforms are not symmetrical and have high harmonic content before balancing. The waveforms are perfectly symmetrical once the PDC is activated.

9 Conclusion

In this paper, the SIDO boost converter is investigated in all possible switching cases for balancing the NP voltage. The presented boost converter topology is able to achieve high voltage gain conversion compared with Ćuk DC/DC converters [14]. The DC voltage control and the capacitor voltage balancing are achieved by PI controller based duty ratio and pulse delay regulation. The PI controller parameters are designed by inductor current ripple averaging method. The main advantage of three-level operation of SIDO converter is the lower inductor ripple amplitude compared with conventional boost converter. But, the imbalance compensation voltage in each mode depends on the inductor stored energy in the preceding mode. Therefore, the full range variation of delay gives higher compensation voltage than in the three-level operation. Compared with the conventional three-level switching used in SSPDC, 18.43% higher compensation voltage can be achieved by PDC method. In duty ratio control of NP voltage compensation, the total DC link voltage deviates from the reference value if the duty ratio is adjusted for one of the switch. Therefore the controller has to calculate the effective duty ratio and its deviation in addition to the regulation of total DC link voltage as in [20] In PDC method, both switches are operated at same duty ratio which keeps the total DC link voltage same even if the pulse delay varies. Therefore the controller objectives can be reduced. Even though the duty ratio and pulse delay are inter-dependent to produce the compensation voltage, the good agreement between simulation and experimental results show a stable operation of the converter. The capacitor voltages remain in balance if the required compensation voltage is less than 39% of the total DC link voltage, but this value is only 16% for a three-level buck boost converter [27]. Subsequently, the inverter output waveform distortions are decreased after compensating the capacitor voltage balancing.

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