Pulse-density-modulated power control of a 4 kW, 450 kHz voltage-source inverter for induction melting applications

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***Abstract*—This paper presents a 4 kW, 450 kHz voltage-source inverter with a series resonant circuit for induction melting applications, which is characterized by the power control based on pulse density modulation (PDM). The pulse-density-modulated inverter makes an induction melting system simple and compact, thus leading to higher efficiency. A modulation strategy is proposed to realize the induction melting system capable of operation at the frequency and power level of interest. Some interesting experimental results are shown to verify the validity of the concept.**

I. Introduction

With remarkable progress in switching speed and capacity of MOSFET's and SIT's, voltage- or current-source inverters have been researched and developed for induction heating applications such as melting and surface quenching [1]~[4]. They are capable of operation at the output frequency of over 100 kHz at present. A high-frequency voltage-source inverter, however, has no ability to control the output power by itself, so that the output power of such an inverter has to be controlled by adjusting the dc input voltage. A thyristor bridge rectifier having a dc capacitor and reactor has been conventionally used as a variable dc-voltage power supply. This causes some problems in size and cost.

In order to overcome the problems of the thyristor bridge rectifier, the following power control schemes have been proposed with the focus on the use of a diode bridge rectifier as a dc power supply:

- frequency control [5], [6];
- pulse-width-modulation [7];
- phase-shift control [8];
- duty control [9].

These power control schemes, however, may result in an increase of switching losses and electromagnetic noises because it is impossible for switching devices to be always turned on and off at zero current.

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TABLE I
Ratings and Characteristics of MOSFET(2SK1521)

Drain to Source Voltage	450V
Drain Current	50A
On-State Resistance	0.08Ω
Input Capacitance	8700pF
Output Capacitance	2400pF
Turn-on Delay Time	85ns
Rise Time	250ns
Turn-off Delay Time	600ns
Fall Time	250ns

This paper describes an induction melting system of 4 kW, 450 kHz, which is intended to be incorporated in a dental casting machine. The induction melting system consists of a single-phase diode rectifier, a single-phase voltage-source inverter using four MOSFET's, and a series resonant circuit with a matching transformer. The output power control based on PDM enables us to use the diode rectifier as a dc power supply. The proposed PDM inverter has the following features:

- No variation occurs to the operating frequency of the inverter.
- It achieves ZCS(zero-current-switching) operation in a wide range of output power, thus resulting in a great reduction of switching losses and electromagnetic noises.

Moreover, the diode bridge rectifier having no electrolytic capacitor on the dc side plays an important role in shaping the line current of the rectifier into sinusoid and unity power factor. Experimental waveforms, along with the analysis leading to the design, are included to verify the validity of the theory developed in this paper.

II. System Configuration

Fig. 1 shows a system configuration of the induction melting system developed for a dental casting machine. The power circuit of the high-frequency inverter consists of a single-phase voltage-source inverter using four MOSFET's (2SK1521, Hitachi). The MOSFET's are rated at 450 V and 50 A (see Table I). The lossless snubbing circuit consisting of only a small capacitor of 2000 pF is connected between the drain and source of each MOSFET. The output of the inverter is connected to a series resonant circuit with a matching transformer of turn-ratio of 8:1. Several grams of alloy of Cr-Co-Mo in a crucible are required to finish melting within

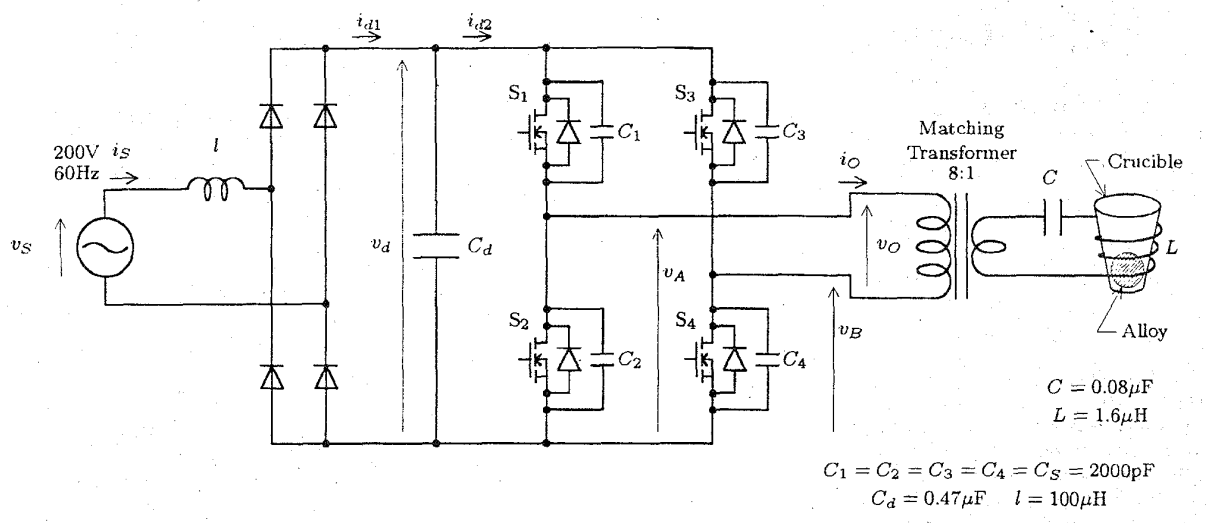


Fig. 1. System configuration.

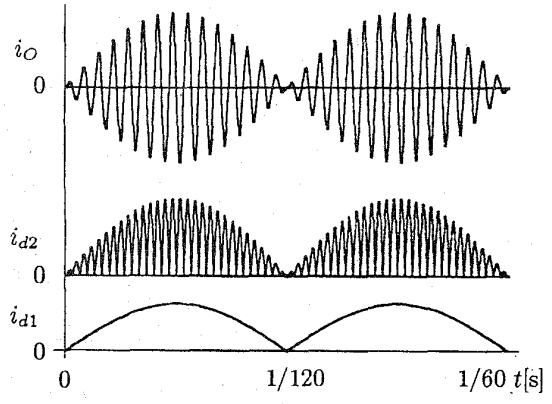


Fig. 2. Current waveforms of i_O, i_{d2}, and i_{d1} under assumption that operating frequency is 1.8 kHz and line frequency is 60 Hz.

about 30 seconds in order to prevent it from oxidation in the dental casting machine.

The dc power supply for the inverter is a single-phase diode bridge rectifier in which neither dc smoothing capacitor nor reactor is connected except for a high frequency capacitor of 0.47 μF. Then the dc voltage across the high frequency capacitor is fluctuating at 120 Hz, that is, twice as high as the line frequency of 60 Hz. This makes a great contribution to shaping the line current of the rectifier into sinusoid and unity power factor.

Fig. 2 shows current waveforms of i_O, i_{d1}, and i_{d2} under the assumption that operating frequency is 1.8 kHz and line frequency is 60 Hz, making the waveforms clear. The envelopes of i_O and i_{d2} fluctuate at twice the line frequency because of no smoothing capacitor. Because the high frequency capacitor absorbs the high frequency current ripples included in i_{d2}, i_{d1} becomes a wave shape which is in proportion to the dc link voltage.

The inverter plus the series resonant circuit looks like a pure resistor, when it is seen from the dc terminals of the rectifier.

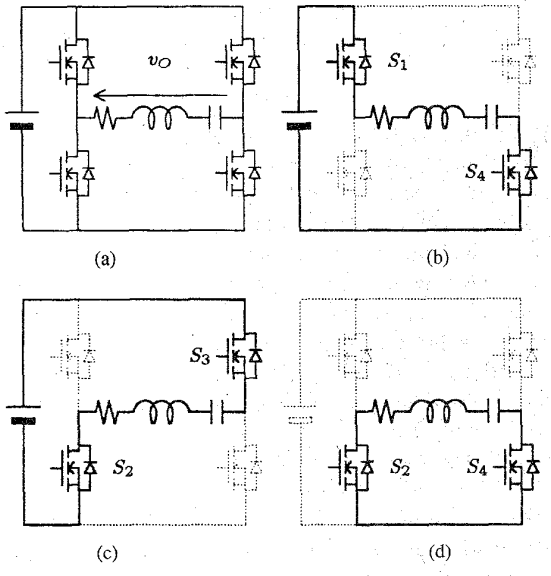


Fig. 3. Switching modes in PDM. (a) Simplified circuit. (b) Mode I. (c) Mode II. (d) Mode III.

Thus, the line current of the rectifier becomes a sinusoidal wave shape with unity power factor as long as the line voltage is sinusoidal. Note that the fluctuation of the output power at twice the line frequency have no effect on induction melting.

III. Pulse Density Modulation

A. Principle of PDM

The proposed PDM inverter repeats alternate run and stop to adjust the average output power, even when both the operating frequency and the dc link voltage are kept constant.

Fig. 3 shows three switching modes in the PDM. Conventional frequency controlled inverters have only two switching modes such as modes I and II, while the pulse-density-

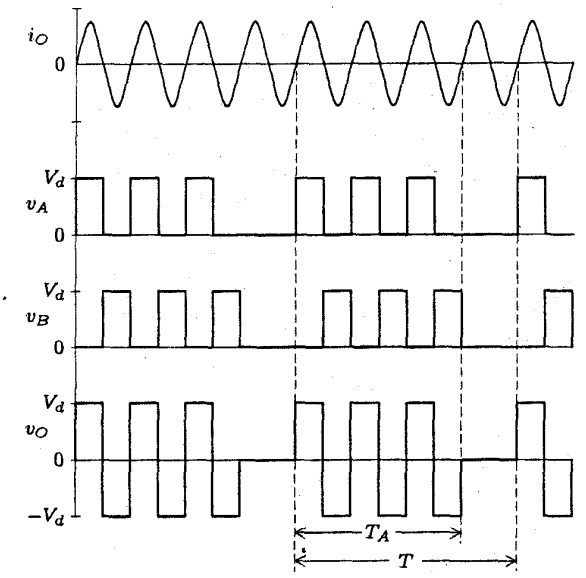


Fig. 4. Switching pattern in PDM.

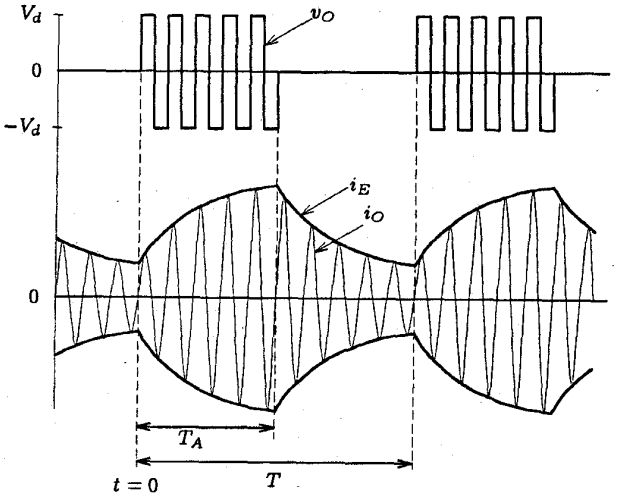


Fig. 5. Voltage and current waveforms in PDM.

modulated inverter additionally has mode III, in which the output voltage of the inverter is zero. In mode III, the resonant current continues flowing through a low side MOSFET in one leg and a low side diode in the other leg, as discussed in the following analysis. Mode III has commonly been used in pulse-width-modulated and phase-shifted inverters.

Fig. 4 shows a switching pattern of the PDM. The inverter acts as a square wave voltage source with the amplitude of V_d for three resonant cycles, while it acts as a zero voltage source for one cycle. If attention is paid to four resonant cycles, the output voltage of the inverter is a periodic waveform, where the average output voltage is $3/4$, compared with the full power operation. Thus, the output power of the inverter can be controlled by adjusting the pulse density of the square wave voltage. Compared with the frequency control in [5] and [6], the PDM can greatly reduce the switching losses because all the MOSFET's are always turned on and off at zero current.

In addition, no dc component should be included in the switching pattern to avoid flux saturation in the matching transformer, because the resonant capacitor is connected to its secondary side. Each pulse consists of the combination of mode I and II in the switching pattern used in the following experiments. A small amount of dc voltage produced by physical asymmetry in the circuit does not cause any flux saturation, because nonnegligible resistances in the MOSFET's and the transformer would keep it from saturating.

Analysis of output power

Let's consider the transient response of the resonant current when the square wave voltage with the angular frequency of ω and with the amplitude of V_d is applied to the series resonant circuit. Since attention is focused on the fundamental component of the square wave voltage, the following equation is obtained

$$L\frac{di_O}{dt} + \frac{1}{C}\int i_O dt + ri_O = \frac{4V_d}{\pi}\sin\omega t. \tag{1}$$

The PDM inverter is operated at the resonant frequency ω_r, as $\omega = \omega_r = 1/\sqrt{LC}$. Assuming $2\omega_r L/r = 2Q \gg 1$, the resonant current i_O is given by

$$i_O = \frac{4V_d}{\pi r}(1 - e^{-\frac{r}{2L}t})\sin\omega_r t. \tag{2}$$

The envelope of the resonant current exhibits the first-order response, although the series resonant circuit is the second-order system. The time constant of the envelope is given by

$$\tau = \frac{2L}{r} = \frac{2Q}{\omega_r}. \tag{3}$$

Q is the quality factor of the series resonant circuit.

Fig. 5 shows specially described waveforms of output voltage and current under the assumption of a finite quality factor of the series resonant circuit. Here, a period of time of the PDM pattern, T is long enough to make the amplitude of the resonant current fluctuate.

The envelope of the resonant current, i_E is given by

$$\begin{cases} i_E(t) = I_{\max}\left(1 - e^{-\frac{t}{\tau}}\right) + I_{E0}e^{-\frac{t}{\tau}} & (0 \le t \le T_A) \\ i_E(t) = i_E(T_A)e^{-\frac{t-T_A}{\tau}} & (T_A \le t \le T) \end{cases} \tag{4}$$

$$I_{E0} = I_{\max}\frac{1 - e^{-\frac{T_A}{\tau}}}{1 - e^{-\frac{T}{\tau}}}. \tag{5}$$

$I_{\max}$ maximum current in case of pulse density of $T_A/T = 1$;

I_{E0} initial value of i_E.

If Q is infinite, the amplitude of the resonant current is in proportion to the pulse density

$$\lim_{\tau\to\infty} i_E = I_{\max}\frac{T_A}{T}. \tag{6}$$

The average output power is obtained as follows:

$$\begin{aligned} P &= \frac{1}{T}\int_0^T v_O i_O dt \\ &= \frac{1}{T}\int_0^{T_A} \frac{4}{\pi} V_d \sin\omega_r t \cdot i_E(t)\sin(\omega_r t-\phi)dt. \end{aligned} \tag{7}$$

If $\tau \gg 1/\omega_r$, (7) is changed into the following equations.

$$\begin{aligned} P &= \frac{2}{\pi}V_d\cos\phi\frac{1}{T}\int_0^{T_A} i_E(t)dt \\ &= P_{\max}\left\{\frac{T_A}{T}+\frac{\tau}{T}\left(\frac{1-e^{-T_A/\tau}}{1-e^{-T/\tau}}\right)\left(e^{\frac{-T_A}{\tau}}-e^{\frac{-T}{\tau}}\right)\right\} \end{aligned} \tag{8}$$

where $P_{\max} = (2/\pi)V_d I_{\max}\cos\phi$, which is equal to the output power in case of $T_A/T = 1$.

If the periodic time of the PDM, T is much smaller than the time constant τ, the amplitude of the resonant current is in proportion to the pulse density, and no fluctuation occurs in the amplitude of the resonant current. Thus, the output power is in proportion to the square of the pulse density as given by

$$\lim_{\tau\to\infty} P = P_{\max}\left(\frac{T_A}{T}\right)^2. \tag{9}$$

If $T \gg \tau$, the output power is in proportion to the pulse density because the resonant current becomes a discontinuous waveform

$$\lim_{\tau\to 0} P = P_{\max}\frac{T_A}{T}. \tag{10}$$

IV. Design of Lossless Snubbing Circuits

The lossless snubbing circuit achieves zero-voltage-switching (ZVS) while the PDM realizes zero-current-switching (ZCS) in a wide range of output power. Exactly speaking, the inverter developed in this paper performs both ZVS and quasi-ZCS because the MOSFET's are always turned on at zero voltage and they are always turned off at almost zero current. The combination of PDM and lossless snubbing makes a great contribution to effective reduction of dv/dt and spike voltage across the MOSFET's.

A. Lossless Snubbing Circuit

Fig. 6 shows the operating principle of a lossless snubbing circuit consisting of only one capacitor without any additional diode or resistor, which is connected in parallel with each MOSFET. Let's consider the commutation from Fig. 6(b) to (d).

First, it is assumed that the resonant current is flowing through S_1 and S_4 as shown in Fig. 6(b). The voltages across the snubbing capacitors C_1 and C_4 are zero, and those across C_2 and C_3 are the same as the dc link voltage. S_1 and S_4 can be turned off with zero-voltage-switching the instant that the gate pulses are removed from S_1 and S_4. During the commutation

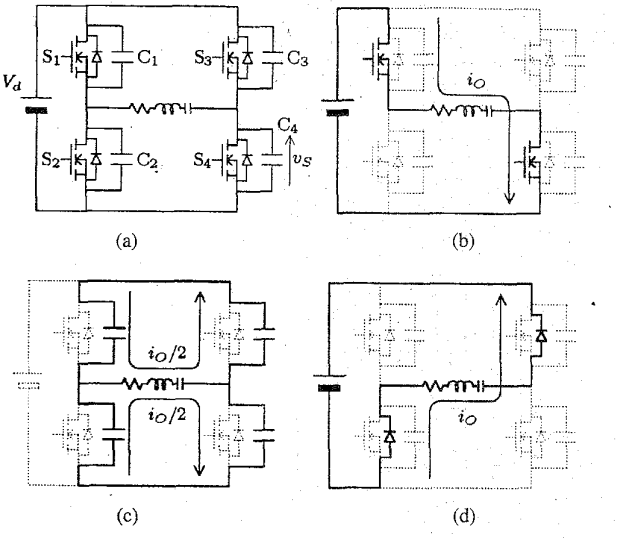


Fig. 6. Principle of lossless snubbing circuit.

shown in Fig. 6(c), the capacitors C_1 and C_4 are being charged, while C_2 and C_3 are being discharged. Since all the snubbing capacitors have the same capacity, half of the resonant current flows through the upper snubbing capacitors and the other flows through the lower ones. When the voltages across C_2 and C_3 reach zero, the free wheeling diodes D_2 and D_3 start to conduct as shown in Fig. 6(d). S_2 and S_3 are provided with the gate pulse before D_2 and D_3 turn off. S_2 and S_3 can be turned on with zero voltage as soon as the direction of the resonant current starts to change.

If the inverter were operated with a leading power factor, the lossless snubbing circuits would not work well, because the MOSFET's would short out the snubbing capacitors. It should be noted that the inverter equipped with the snubbing circuit in each leg, has to be operated with a lagging power factor.

B. Discussion on Blanking Time

Fig. 7 shows detailed waveforms of voltage and current of the inverter with the lossless snubbing circuit. Here, let the peak value of the resonant current be I as follows:

$$i_O = -I\sin\omega_r t. \tag{11}$$

When a MOSFET is turned off at the time of $-T_{\text{off}}$, the voltage across the snubbing capacitor, v_C starts to rise up as given by

$$\begin{aligned} v_C(t) &= \frac{1}{C_S}\int_{-T_{\text{off}}}^{t}\frac{i_O}{2}dt \\ &= \frac{I}{2\omega_r C_S}(\cos\omega_r t - \cos\omega_r T_{\text{off}}). \end{aligned} \tag{12}$$

C_S is the capacitance of snubbing capacitor

The time of $-T_d$, at which v_C reaches the dc link voltage of V_d, is obtained by substituting into (12) that $v_C(-T_d) = V_d$

$$T_d = \frac{1}{\omega_r}\cos^{-1}\left(\cos\omega_r T_{\text{off}} + 2\omega_r C_S\frac{V_d}{I}\right). \tag{13}$$

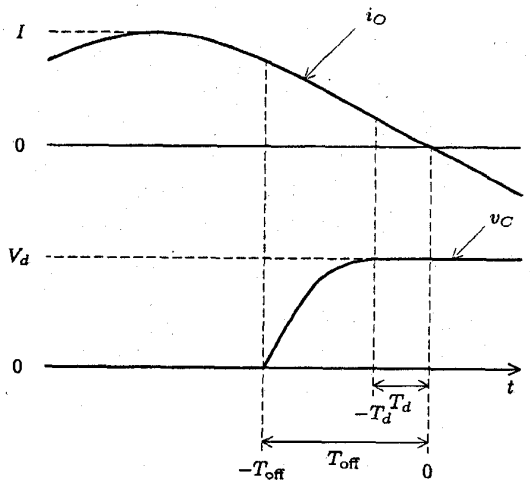


Fig. 7. Waveforms of lossless snubbing circuit.

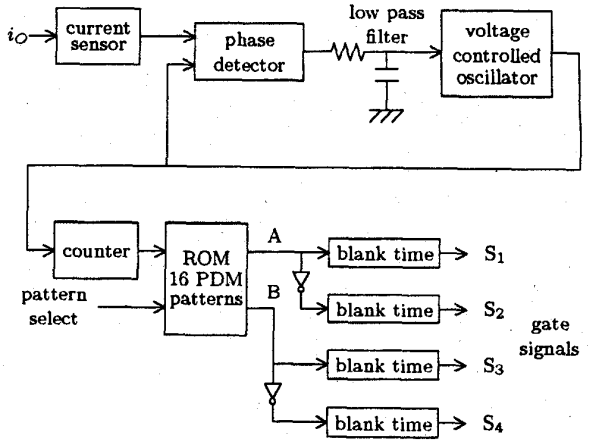


Fig. 8. Control circuit.

The condition that v_C reaches V_d at $t = 0$ gives the minimum value of T_{off} as follows:

$$T_{\min} = \frac{1}{\omega_r} \cos^{-1}\left(1 - 2\omega_r C_S \frac{V_d}{I}\right). \tag{14}$$

Although (14) shows an ideal condition which gives the minimum value of dv/dt, T_{off} should be set up to $T_{\min}$ for minimum pulse density because the amplitude of the resonant current is varied by pulse density. The amplitude of the resonant current of 15 A, which is equal to 3/4 of the rated current of 25 A, and the dc link voltage of V_d = 200 V are assumed in the design of the experimental system. The capacitance of the snubbing capacitor is designed to be 2000 pF, which is as large as the output capacitance of the MOSFET's used here. Since $T_{\min}(= 180$ ns) is obtained from (14), T_{off} is set up as $T_{\text{off}} = 200$ ns for the experimental system. The blanking time or lock-out time is also set as 150 ns because $T_d = 85$ ns is given by (13).

V. Control Circuit

Fig. 8 shows a control circuit of the pulse-density-modulated inverter. The control circuit forms a type of phase-locked loop, which outputs the gate pulses in phase with the resonant current. The amplitude of the resonant current is too small to detect the phase at the time of zero-crossing of the source voltage with the line frequency of 60 Hz because no smoothing capacitor is connected to the dc link. Thus, the cut-off frequency of the low pass filter is set to 1.5 ms to eliminate the frequency change of the voltage-controlled oscillator at the zero-crossing. The output of the voltage-controlled oscillator is a pulse train, the frequency of which is twice as high as the operating frequency of the inverter. The pulse train is applied to the five-bit step-up counter and then a desired PDM pattern is selected out of 16 patterns which are stored in a ROM.

Fig. 9 shows the 16 PDM patterns used in the experimental system as a parameter of pulse density of T_A/T from 1/16 to 16/16. The period of time of each PDM pattern stored in the ROM is equal to sixteen times as long as the resonant

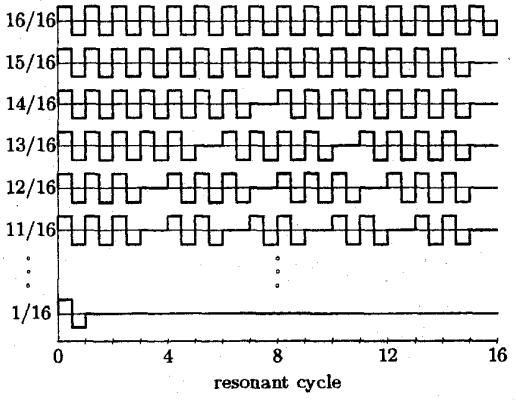


Fig. 9. PDM patterns stored in ROM.

period. The PDM patterns are determined so as to reduce the amplitude fluctuation of the resonant current which is caused by the PDM. As a result, an actual period of time depends on the PDM pattern which is chosen by a pattern select signal. The PDM pattern signals A and B are applied to four blanking time circuits to produce four gate drive signals.

VI. Experimental Results

Figs. 10, 11, and 12 show experimental waveforms obtained by a prototype system. Since the quality factor of the series resonant circuit developed for a dental casting machine is about 30, the time constant of the envelope of the resonant current is given by

$$\tau = 2Q/\omega_r = 2 \times 30/2\pi \times 450 \times 10^3 = 21\ \mu\text{s}.$$

First, an electrolytic capacitor of 3000 μF is connected with the dc link to verify the operating principle of the pulse density modulation in the following experiments.

Fig. 10 shows an output voltage and current in the case of the full power operation of about 3.6 kW. Since the snubbing capacitor of 2000 pF suppresses dv/dt, that is, the derivative of the drain to source voltage with respect to time, the rise-time is about 150 ns. No voltage spike occurs in the output voltage.

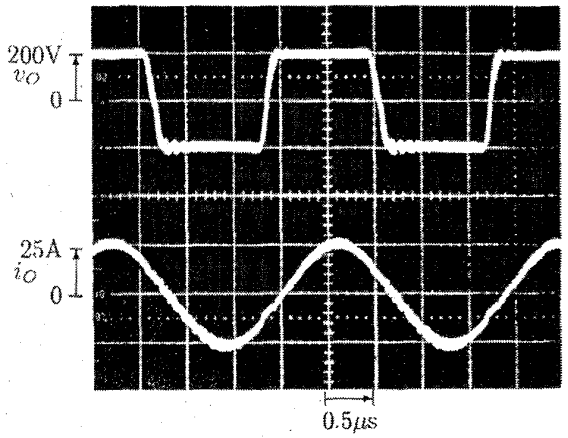


Fig. 10. Output voltage and current waveforms of inverter in case of $T_A/T = 16/16$.

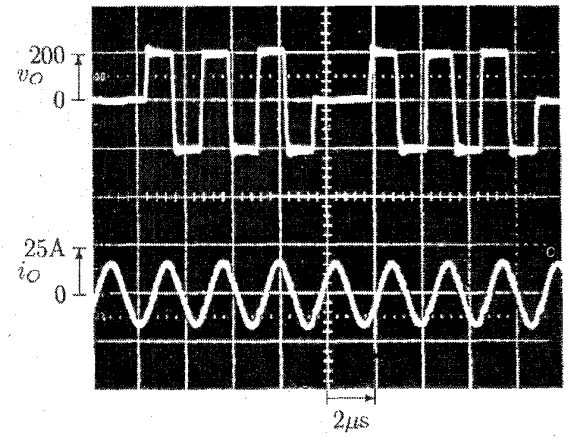


Fig. 11. Output voltage and current waveforms of inverter in case of $T_A/T = 12/16$.

Figs. 11 and 12 show those in the case of the PDM operation. Since the pulse density is equal to 12/16 in Fig. 11, the amplitude of i_O becomes smaller than that in Fig. 10. Almost no decay appears in the amplitude of i_O because τ is longer than the PDM period of $T = 9$ μs. In Fig. 12, the amplitude of i_O is much smaller so that the output power of the inverter is 80 W, which is only 2%, compared with that in Fig. 10. The actual period of time of the PDM in Fig. 12 is longer than that in Fig. 11, thus causing the fluctuation of i_O.

Fig. 13 indicates a relationship between the pulse density and the dc input power of the inverter. Note that it is difficult to calculate the ac output power of the inverter from the pulse-density-modulated waveforms. The theoretical curves are obtained by substituting the dc input power in the full power operation for the maximum power $P_{\max}$ into (8) and (9). The curve obtained from (8) agrees well with the experimental results in the overall range. The curve given by (9) has a small difference in the range of pulse density from 2/16 to 12/16. This means that (9) is applicable in a range of output power from 70% to 100%.

Finally, the electrolytic capacitor of 3000 μF is removed from the diode rectifier, so that no capacitor is connected

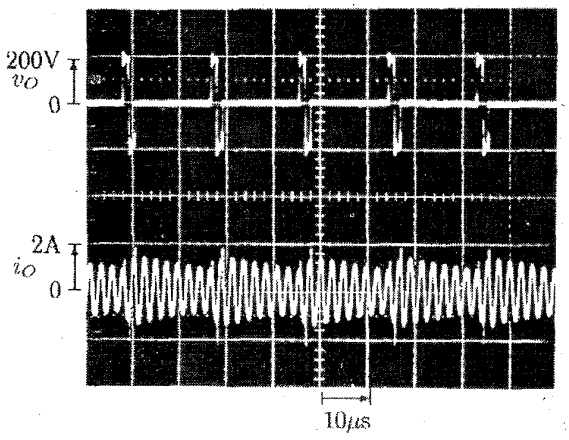


Fig. 12. Output voltage and current waveforms of inverter in case of $T_A/T = 2/16$.

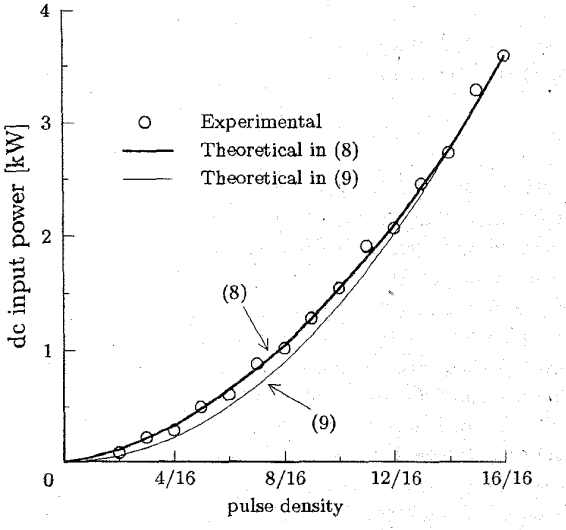


Fig. 13. Relationship between pulse density and dc input power.

to the diode rectifier except for a high frequency capacitor of 0.47 μF in the following experiments. Fig. 14 shows the waveforms of the line voltage and current of the diode rectifier in the case of the full power operation. Fig. 15 shows those with the 12/16 pulse density. The line current is an almost sinusoidal waveform with unity power factor, the amplitude of which depends on the pulse density. A small amount of current distortion included in the line current is due to the line voltage distortion. If the line voltage, v_S had a purely sinusoidal wave shape, no harmonic current would be contained in the line current. The pulse-density-modulated inverter produces an amount of current ripple but the ripple frequency is so high that the high frequency capacitor of 0.47 μF can easily absorb it.

VII. Characteristic Comparison

Table II shows characteristic comparison among three control schemes of a high frequency inverter, each of which is capable of adjusting the output power by itself. Table II gives

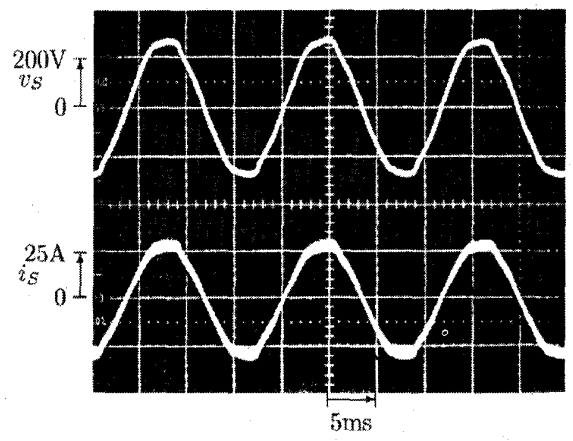


Fig. 14. Input voltage and current waveforms of diode rectifier in case of $T_A/T = 16/16$ (no electrolytic capacitor).

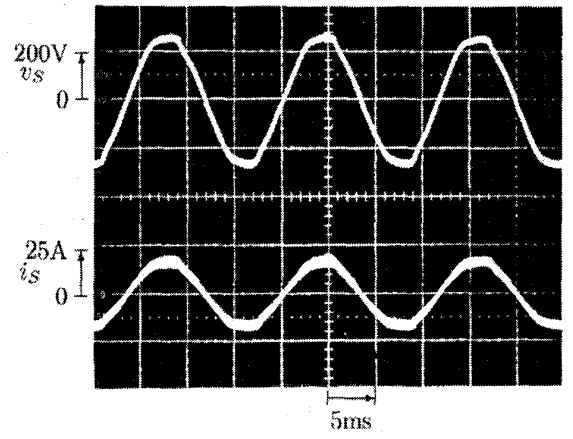


Fig. 15. Input voltage and current waveforms of diode rectifier in case of $T_A/T = 12/16$ (no electrolytic capacitor).

an example of calculation results obtained from the theoretical analysis (see Appendix A and B). The following assumptions are made in the calculation.

- The load of the inverter is an LCR resonant circuit with quality factor of 10.
- There is neither snubbing capacitor nor output capacitance of the MOSFET's.
- The inverter is operated at half the full power.

The PS inverter is operated at the phase-shift angle of 65.5°, which is twice the phase angle of $\phi = 32.7°$ in Table II, and the PDM inverter at the pulse density of 11/16. The operating frequency varies with the output power; it increases by 5% in the FC inverter, and by 3% in the PS inverter at half the full power. The operating frequency is equal to the actual switching frequency. On the other hand, the operating frequency is equal to the resonant frequency in the PDM inverter, but the actual switching frequency goes down to 68% of the resonant frequency because no switching occurs during mode III.

The most important item in Table II is that the drain current being turned off, I_{off}, is always zero in the PDM inverter

TABLE II
CHARACTERISTICS COMPARISON AMONG THREE CONTROL SCHEMES UNDER CONDITION OF 50% OF FULL POWER AND $Q = 10$

	FC	PS	PDM
operating frequency	$1.05f_r$	$1.03f_r$	f_r
actual switching frequency	$1.05f_r$	$1.03f_r$	$0.68f_r$
phase angle: ϕ[deg]	45	32.7	0
drain current being turned off: I_{off}/I_0	50%	64%(lead) 0%(lag)	0%
ripple frequency of i_{d2}	$2.1f_r$	$2.06f_r$	$0.31f_r$

FC: frequency controlled inverter
PS: phase-shifted inverter
PDM: pulse-density-modulated inverter
f_r: resonant frequency

under all the operating conditions while it is not zero in the other inverters except under the operating condition of the full power. This means that the PDM inverter gets zero-current switching (ZCS) in all the operating conditions. The drain current being turned off, I_{off} also affects both dv/dt and spike voltage across the MOSFET's. Even if the zero-voltage-switching topology was employed, high dv/dt would produce switching losses because the rise and fall time of the switching devices is not zero in fact.

Although the drain current being turned off is always zero in one pair of lagging legs of the PS inverter, it reaches 64% of the peak current in the other pair of leading legs. This means that the PS inverter needs a larger snubbing capacitor to avoid high dv/dt. However, the larger snubbing capacitor limits the maximum output power because it requires to finish charging or discharging the snubbing capacitor before the resonant current reaches zero. On the contrary, a small snubbing capacitor can effectively suppress dv/dt in the PDM inverter because the drain current being turned-off is equal to zero. The PDM inverter would make a great contribution to reducing switching losses and electromagnetic noises, and to achieving high reliability.

The ripple frequency of i_{d2} in the FC and PS inverters is twice the operating frequency, while that in the PDM inverter is about 1/3 of the operating frequency. Thus, the PDM inverter makes the voltage ripples in the dc link larger than the FC and PS inverters do. However, this may not be any problem in high frequency inverters, the operating frequency of which is over 100 kHz, because the ripple frequency is high enough to be absorbed by a high-frequency capacitor in the dc link.

VIII. CONCLUSION

The purpose of the described study was to develop a pulse-density-modulated inverter of 4 kW, 450 kHz for induction melting applications. The PDM inverter is capable of adjusting the output power by itself, performing both ZVS and ZCS in all the operating conditions. Thus, a single-phase diode bridge rectifier without electrolytic capacitor in the dc link is applicable at the front-end of the inverter, so that the line current of the rectifier has a sinusoidal waveform with unity power factor. This results not only in improving efficiency but also in reducing the size of the induction melting system incorporated

in a dental casting machine. The quantitative comparison shown in Table II concludes that the pulse-density-modulated inverter would be more suitable for various induction heating applications.

APPENDIX

A. Analysis of Frequency Variation

The frequency variation is discussed in the FC and PS inverters. At first, assume that a series resonant circuit consisting of L, C, and r is connected to the high frequency inverter. The quality factor of the resonant circuit is given by

$$Q = \frac{\omega_r L}{r} = \frac{1}{\omega_r C r} \tag{15}$$

where the resonant angular frequency $\omega_r = 1/\sqrt{LC}$. Assuming that the inverter runs at an angular frequency ω, the phase angle between the output voltage and current of the inverter, ϕ is represented by using Q, as

$$\tan\phi = \frac{\omega L - \frac{1}{\omega C}}{r} = Q\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right). \tag{16}$$

From (16), the frequency variation is given by

$$\frac{\omega}{\omega_r} = \frac{\tan\phi + \sqrt{\tan^2\phi + 4Q^2}}{2Q}. \tag{17}$$

B. Analysis of Drain Current Being Turned Off

The impedance of the resonant circuit is also represented by using Q and ϕ as

$$|Z| = \left|r + j\omega L + \frac{1}{j\omega C}\right| = r|1 + j\tan\phi| = \frac{r}{\cos\phi}. \tag{18}$$

The FC inverter outputs a square-shape voltage, the fundamental component of which is a constant amplitude V_0. The output power of the FC inverter is given by

$$P = rI^2 = r\frac{{V_0}^2}{|Z|^2} = \frac{{V_0}^2}{r}\cos^2\phi. \tag{19}$$

The drain current being turned off, I_{off} depends on the phase angle ϕ as follows:

$$I_{\text{off}} = I\sin\phi = I_0\cos\phi\sin\phi = \frac{I_0}{2}\sin 2\phi. \tag{20}$$

I_0 is the peak value of the drain current under the full power operation.

On the other hand, the PS inverter can control not only the operating frequency but also the fundamental component of the output voltage to adjust the output power of the inverter. It should be assumed that one pair of lagging legs is always turned on or off at zero current to make the maximum output power equal to that in the FC inverter. Then the phase-shift angle, which is the difference in switching angle between the leading and lagging legs, is equal to twice the phase angle ϕ, and the fundamental component of the output voltage is given by

$$V = V_0\cos\phi. \tag{21}$$

The output power of the PS inverter is given by

$$P = rI^2 = r\frac{V^2}{|Z|^2} = \frac{{V_0}^2}{r}\cos^4\phi. \tag{22}$$

The drain current being turned off is always zero in one pair of lagging legs while it is not zero in the other pair of leading legs except under the condition of the full power, that is,

$$I_{\text{off}} = I\sin 2\phi = I_0\cos\phi\sin 2\phi. \tag{23}$$

REFERENCES

[1] W. E. Frank and C. F. Der, "Solid state RF generators for induction heating applications," in *IEEE/IAS Annu. Meet.*, 1982, pp. 939–944.

[2] S. Bottari, L. Malesani, and P. Tenti, "High frequency 200 kHz inverter for induction heating applications," in *IEEE/PESC Rec.*, 1985, pp. 308–316.

[3] H. Akagi, T. Sawae, and A. Nabae, "130 kHz 7.5 kW current-source inverters using static induction transistors for induction heating applications," *IEEE Trans. Power Electron.*, vol. 3, no. 3, pp. 303–309, 1988.

[4] T. Yokoo, H. Itho, and A. Sano, "High frequency inverter for induction heating equipment by using static induction transistors," in *PCIM Proc.*, 1988, pp. 101–108.

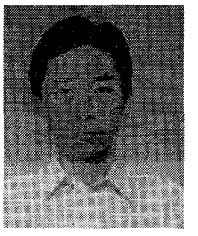
[5] P. P. Roy, S. R. Doradla, and S. Deb, "Analysis of the series resonant converter using a frequency domain model," in *IEEE/PESC Rec.*, 1991, pp. 482–489.

[6] A. Dmowski, R. Bugyi, and P. Szewczyk, "A novel series-resonant DC/DC converter with full control of output voltage at no-load condition. Computer simulation based design aspects," in *IEEE/IAS Annu. Meet.*, 1992, pp. 924–928.

[7] M. Nakaoka, Y. J. Kim, H. Ogiwara, and H. Uemura, "Modern digitally-controlled constant high-frequency PWM resonant DC-DC converter using lumped parasitic reactive circuit components of high-voltage transformer & feeding cable and its new practical application," in *IEEE/IAS Annu. Meet.*, 1991, pp. 1088–1097.

[8] L. Grajales, J. A. Sabaté, K. R. Wang, W. A. Tabisz, and F. C. Lee, "Design of a 10 kW, 500 kHz phase-shift controlled series-resonant inverter for induction heating," in *IEEE/IAS Annu. Meet.*, 1993, pp. 843–849.

[9] W. H. Kwon and G. H. Cho, "Modified quantum and phase control of series resonant converter," in *IEEE/PESC Rec.*, 1991, pp. 498–503.



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