Pulse Width Modulation with Resonant dc Link Converters

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***Abstract*— A technique for realizing pulse width modulation (PWM) capability in resonant dc link converters is presented in this paper. This technique eliminates the subharmonics present in the conventional discrete pulse modulated converters without requiring any additional switching devices. Detailed design-oriented analysis enumerating the tradeoffs involved are presented. Control techniques for simultaneously accomplishing link and output control are considered. Simulation results verifying the principle of operation are presented and backed up by experiments.**

I. Introduction

THE ADVENT OF higher switching frequencies is an inevitable trend in the area of power converters. This stems from the smaller filters, higher power density, low acoustic noise, and improved transient response resulting from the increase in switching frequency. The availability of high-performance devices such as IGBT's in recent years has raised the expectation of correspondingly higher performance from pulse width modulated (PWM) inverters used in multikilowatt (2–500 kW) adjustable-speed drive and UPS applications. The performance of IGBT inverters is severely limited by two factors: the switching loss in the devices and the high dv/dt on the output of the inverter. The limitation due to the first is well known and limits the switching frequency to 4–8 kHz, unless excessive derating of device current ratings is incurred. At a frequency of 20 kHz, which is normally considered to be a desirable lower limit, the switching loss in an IGBT could be as high as four times the conduction loss in the device [1]. The second factor, i.e., the dv/dt on the output, is receiving greater attention in the literature. The dv/dt for IGBT's could be as high as 10 000 V/μ s and could be the source of conducted and radiated EMI. There have also been documented cases of motor insulation breakdown in the presence of such steep wavefronts. The International Electrotechnical Commission (IEC) has a working group investigating the possibility of limiting the dv/dt to less than 500 V/μ s [2].

It is not surprising that in the face of problems related to "hard switching," i.e., high switching loss and high dv/dt, soft switching inverters have attracted great interest in industry. Soft switching inverters, in particular, zero voltage switching topologies, offer virtually zero switching loss and moderate dv/dt stresses. One of the most successful and popular soft switching topologies is the resonant dc link inverter, this is a circuit that has been shown to be viable in both its voltage and current source versions [3]–[7]. Frequencies in the order of 65 kHz at a power level of 40 kVA have been demonstrated, with potential for applications in the 200-kVA range [8].

The biggest problem facing the family of resonant link inverters stems from the need for discrete pulse modulation (DPM). Low switching loss is typically realized by turning devices on and off when the bus voltage is zero which is an event that occurs almost periodically at a rate given by the bus oscillation frequency. The constraint of switching at bus zero crossings create energy at frequencies substantially below the link frequency. In the case of PWM inverters, the harmonics occur only at side bands around multiples of the switching frequency and are, thus, well constrained. The possibility of realizing true PWM capability in resonant link inverters is thus a desirable objective, as it could preserve the advantages of zero losses, high-switching frequency, and elimination of subharmonic energy content. Malesani and Divan [9] presented a synchronous PWM resonant dc link inverter raising the possibility of true PWM operation. However, as the resonant bus interval could be modulated above a minimum value, control in a three-phase inverter was seen to be rather limited. Another approach that combined a conventional resonant dc link inverter stage with a single-phase soft-switched PWM input stage was presented in [10]. This paper presents an extension of that technique to three-phase systems utilizing essentially the same topology as the conventional poly-phase resonant dc link inverter but allowing true PWM over a fairly wide operating range. The paper investigates operating characteristics, design tradeoffs, and design methodology for this type of converter and does a detailed comparison with resonant link and conventional PWM inverters. Operation of the proposed inverter is also confirmed experimentally.

II. Operating Principle

Fig. 1 shows the circuit diagram of a conventional actively clamped resonant dc link inverter. The dc link oscillates and sets up switching conditions for the turnon and turnoff of the main inverter devices when the bus voltage is zero. Device turnon presents no problem as the device is gated with its antiparallel diode conducting, i.e., when the bus is clamped to 0 V. Following device turnoff, the current in the device is diverted into the bus resonant capacitor, which causes an

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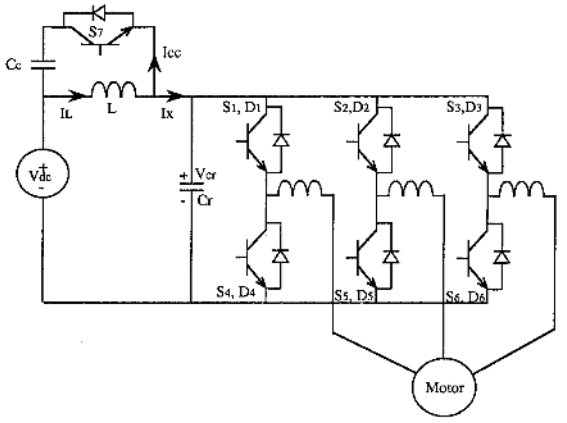

Fig. 1. Circuit schematic of a three-phase actively clamped resonant dc link inverter.

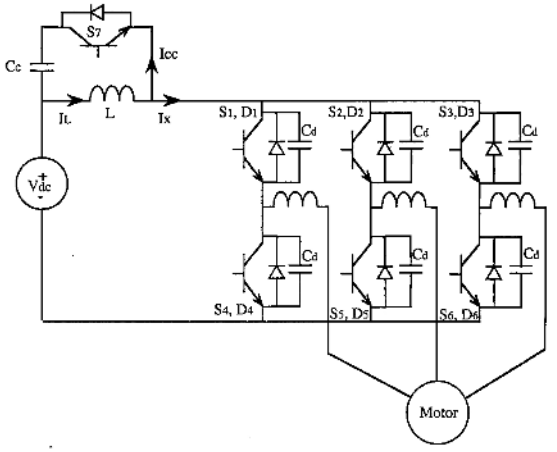

Fig. 2. Circuit schematic of a three-phase actively clamped dc link converter with capacitors across all devices.

initiation of the next resonant cycle. It should be noted that the bus resonant capacitor C_r is typically connected in a distributed fashion across the bus. In some cases, in particular with GTO inverters, some of the capacitance may also be connected across individual devices to provide local snubbing [11]. All these connections are essentially identical in terms of resonant link performance.

Fig. 2 shows an equivalent connection for the actively clamped resonant dc link inverter in which the bulk of the bus equivalent capacitor is connected across individual devices. During a resonant cycle, the equivalent capacitance across the bus is $3.C_d$, where C_d is the capacitance across each individual device. This inverter can be operated in the same manner as the circuit in Fig. 1. However, it can be seen that whenever an active device, say S_1, is conducting, turnoff can be initiated even during the resonant cycle. The current transfers from the device S_1 to the effective snubber capacitor across it and causes the voltage across it to build up until the diode D_4 in antiparallel with the device S_4 is turned on. It should be noted that this turnoff is a soft switching event, which is a result of the capacitance across the device. As may be expected, device turnon requires that the voltage across the device be reset to zero. This is seen to occur due to the action of the resonant link clamp that causes a completion of the bus resonant cycle in the manner associated with resonant link operation. It is clear that there are constraints that need to be satisfied to ensure that the resonant cycle can be completed, and these will be addressed in the next section.

Given the ability to turnoff devices, even within a bus resonant cycle, it is important to see how this feature may be exploited to obtain true PWM capability in the inverter. During the bus shorting interval, the load current direction in each phase is determined, and all the main inverter devices that would be conducting are turned on. This initiates the next bus resonant cycle and gives phase output voltages that are specified by the polarity of the phase output current. More importantly, all active devices are now seen to be conducting. Per the discussion above, any of all of these devices can be turned off at any time during the resonant cycle under zero voltage switching. This shows the possibility of impressing pulses of arbitrary width on the phase outputs from close to zero width to a maximum of somewhat less than the resonant pulse width. As the active devices conduct at the beginning of a resonant cycle, it can be shown that turnoff of an active device within the resonant pulse duration always results in instantaneous energy flow into the clamp capacitor over and above that for the resonant dc link inverter. Consequently, it is possible (within permitted limits) to accomplish charge balance on the clamp capacitor through clamp device control, simultaneously ensuring that the link oscillation is maintained. Fig. 3 depicts the strategy needed for PWM control with reference to one of the phases in a the polyphase inverter. For positive values of load current I_A, the device S_1 is turned on when the bus voltage reaches zero. This device can then be turned off within the resonant cycle whenever desired. For negative values of I_A, the device S_4 would be turned on initially and would be turned off as desired by the control strategy. The three phases can similarly be controlled reasonably independent of each other, as shown in Fig. 4. Some interaction exists between the phases themselves as well as with operation of the resonant link and has to be compensated for by the use of an appropriate feedback loop.

III. Simplified Analysis

Although operation and control of the resonant link circuit seems quite complex, it is possible to perform a simplified dc analysis that gives some insight into the obtainable control range as well as into the limitations of the scheme. The validity of this analysis is based on the assumption that the link frequency is much greater than the output frequency of the inverter. Fig. 5(a) shows one pole of the inverter, without the active clamp, operating with a positive load current I_A. Fig. 5(b) shows the link and output voltage waveforms for various values of conduction time T_{on} for switch S_1. At time $t = 0$, a resonant cycle is started between L and the capacitor C_r, which is across S_2 (assuming S_1 is conducting). If S_1 is turned on part way through the cycle at instants t_1, t_2, etc., then trajectories denoted by V_{r1}, V_{r2} etc. is followed by V_r.

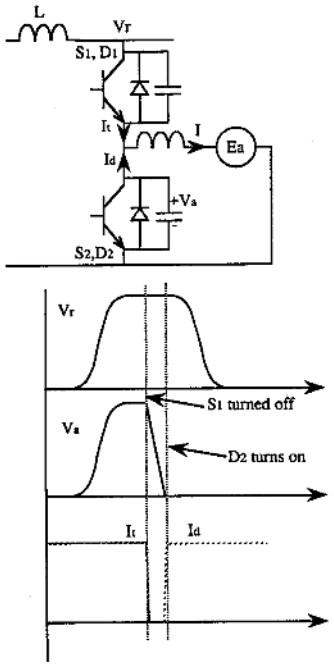

Fig. 3. Schematic of one phase leg of the inverter and typical waveforms under PWM control.

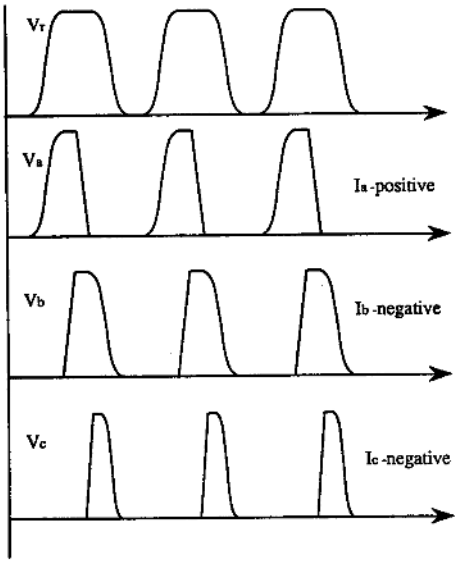

Fig. 4. Waveforms of the three-phase output voltages under PWM operation.

On the output of the inverter, V_A equals V_r until device S_1 is turned off, at which time, it starts decreasing toward zero at a rate dependent on the circuit parameters and the load current I_A. The output voltages for these cases are depicted at V_{a1}, V_{a2}, etc. in Fig. 5(b).

Consequently, three modes of operation can be identified: with S_1 conducting (Mode 1), with both S_1 and D_2 off (Mode 2), and with D_2 conducting (Mode 3). The next resonant

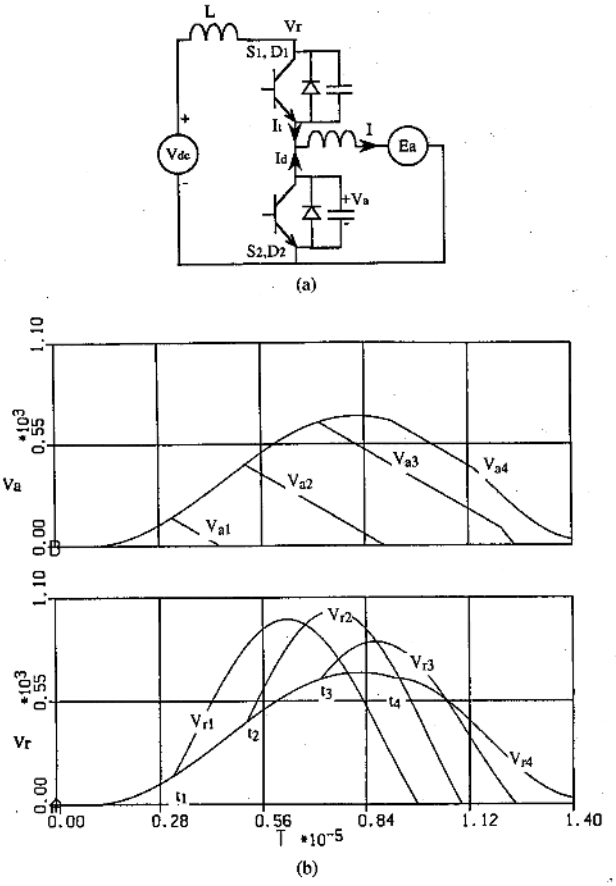

Fig. 5. (a) Simplified version of the resonant dc link converter for dc analysis; (b) link voltage V_r and unfiltered output voltage V_a under different switching instants. Notice that the peak voltage is 1000 V with a supply voltage of just 350 V.

cycle can then be initiated once again when $I_L = I_A$. The equations governing circuit behavior can then be shown to be the following:

Mode 1:

$$\dot{I}_L = \frac{V_{dc} - V_r}{L}; \dot{V}_r = \frac{I_L - I_a}{C_r}; V_A = V_r. \tag{1}$$

Mode 2:

$$\dot{I}_L = \frac{V_{dc} - V_r}{L}; \dot{V}_r = \frac{I_L - \frac{I_A}{2}}{\frac{C_r}{2}}; \dot{V}_A = \frac{-I_A}{2C_r}. \tag{2}$$

Mode 3:

$$\dot{I}_L = \frac{V_{dc} - V_r}{L}; \dot{V}_r = \frac{I_L}{C_r}; V_A = 0. \tag{3}$$

Two interesting behavioral aspects of this circuit need to be noted. First, unlike in the case of the conventional resonant link, turning off the active device always gives additional energy into the tank and causes the higher voltage stress seen in Fig. 5. This also tends to supply the energy needed to

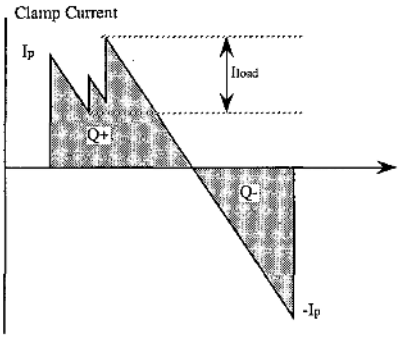

Fig. 6. Simplified current waveforms through the clamp circuit.

compensate for tank circuit losses. Consequently, this circuit can operate without the extra initial energy storage necessary for the normal resonant link. The second observation is that there is a maximum value of T_{on} for which the resonant cycle can be maintained. For instance, in Fig. 5(b), if $T_{\text{on}} = t_4 > t_3$, then the resonant bus will not return to 0 V, and bus oscillation will be lost resulting in resonant link failure. This tends to be a very severe limitation. One way of circumventing this problem is through precharging the inductor with additional current over I_A before the initiation of the resonant cycle.

The dc analysis can be extended to the actively clamped case using the circuit schematic shown in Fig. 3. Fig. 6 shows the relevant waveforms for conditions similar to those in Fig. 5. The resonant cycle is initiated at $t = 0$ when $I_L = I_A$ (assuming a lossless tank). With S_1 conducting, once again, V_r equals V_A until S_1 is turned off. As V_r reaches the clamp voltage (KV_{dc}), the clamp switch conducts the current I_c is seen to flow. When S_1 turns off, the current I_A is now shared between the two capacitors C_r. As the inductor current I_C included I_A, this now results in a step of $I_A/2$ in the clamp current. When the diode D_2 begins to conduct, another step of $I_A/2$ occurs as I_A is diverted completely to D_2.

The initial clamp current $-I_p$ correspond to the energy stored in the LC tank at $t = 0$ and equals

$$I_p = \frac{\sqrt{V_{dc}^2 - V_c^2}}{Z_0}; Z_0 = \sqrt{\frac{L}{2C_r}}. \tag{4}$$

This is also the magnitude of the minimum value for I_p' required if the bus oscillation is to be maintained.

Irrespective of the direction of the current I_A, it can be seen that turnoff of the active device always entails transfer of additional charge into the clamp capacitor for duty ratio ($d = T_{\text{on}}/T_g$) of less than approximately 0.5 ($Q- > Q+$).

For higher duty factors, $Q+ > Q-$, and net charge is removed from the clamp capacitor. The circuit has to be designed such that it can operate indefinitely in both regimes. The case of $Q- > Q+$ is easily handled by increasing I_p' above the minimum required values so that charge balance is obtained. For $Q- < Q+$, the bus shorting interval needs to be increased, caused transfer of more charge into the clamp capacitor. Both techniques result in an effective decrease in the switching frequency, and an increase in the device switching losses incurred. These constraints apply in the steady state and are in addition to the absolute maximum limits on T_{on} described earlier.

IV. Loss Characterization

The loss analysis of modulated resonant link systems is fairly complex and rather difficult to quantify. The use of simulation, although accurate in terms of results, gives no indication of trends and tradeoffs that exist in the design process. Divan *et al.* [12] presented a simplified design methodology that was seen to include most of the major loss mechanisms in the resonant dc link converter topology. The accuracy of the simplified model was extensively verified through simulation and experimental results. The method has also formed the basis for the analysis of other resonant link converters, with similar success [8], [13]. The approach identifies the major loss mechanisms in the converter, including the main device conduction and switching losses (P_{cm}, P_{sm}), the clamp device conduction and switching loss (P_{cc}, P_{sc}) and the loss in the resonant elements, mainly in the inductor equivalent series resistance P_L. The current and voltage waveforms in individual devices are considered along with the impact of the modulation strategy to arrive at the projected loss figures. The loss calculations are also dependent on the device conduction drops V_D, the current fall time t_f, and the effective switching frequency F_S. F_S is calculated based on the link oscillation requirement and charge balance in the clamp capacitor. The impact of modulation strategy is also considered as discussed in [8]. The value for F_S is obtained to be

$$F_S = \frac{1}{2\sqrt{LC_r}\left[\sqrt{2}\cos^{-1}(1-K) + \dfrac{K\sqrt{2-K}}{K-1}\right]} \cdot \frac{\pi V_{dc}(1-K)}{7I_A LK}. \tag{5}$$

The individual loss components are calculated based on the current waveforms through them, as shown in Fig. 6. The conduction loss for the PWM-RDCL main devices is *Pcm* and includes the load current component (considered with unity power factor) as well as a circulating resonant current component. This is unlike the conventional RDCL inverter, where the main devices only carry the load current:

$$P_{cm} = \frac{4}{\pi} V_D \left[I_0 + \frac{V_{dc}}{Z_o}\sqrt{K(2-K)}\right]. \tag{6}$$

The main device switching loss P_{sm} is incurred every resonant bus cycle when the device is turn off. It should be noted that the effective device snubber capacitor is at most $2.C_r$ lower than for the RDCL inverter. Further, the switching frequency for the RDCL devices is typically a third of the link frequency. Both these factors contribute to higher switching loss in the PWM-RDCL inverter at a given frequency. The problem is further exacerbated by the fact that current reversal in the clamp device due to main device turnoff (see Fig. 5) invariably results in a lower switching frequency for given LC components. This implies that for a given frequency, the

capacitance would typically be smaller for the PWM-RDCL inverter as opposed to the conventional RDCL inverter, giving even higher switching loss. An approximate value for P_{sm} can be shown to be

$$P_{sm} = \frac{1}{2}\left[I_0^2 \frac{t_f^2}{C_r} F_s\right]. \tag{7}$$

Similarly, the clamp device conduction loss and clamp device switching loss can be calculated to be

$$P_{cc} = V_D \left[\frac{\sqrt{2LC_rK(2-K)}}{2(K-1)}\right] \left[\frac{V_{dc}(1-K)\pi}{3I_oL}\right] \cdot \left[\frac{V_{dc}\sqrt{K(2-K)}}{Z_o} + \frac{3I_o}{\pi}\right] \tag{8}$$

$$P_{sc} = \frac{V_{dc}^2}{Z_o}\left[\frac{K(1-K)t_f^2F_s}{48C_r}\right]. \tag{9}$$

The loss in the inductor ESR can be calculated by noting that the effective load dc current and the resonant current both flow through it. The loss P_L is then found to be

$$P_L = \frac{V_{dc}^2}{2QZ_o} + \frac{I_o^2Z_o}{2Q}. \tag{10}$$

An optimization of the system losses can then be attempted. The average link switching frequency is maintained constant by varying the inductance L and choosing C_r such that the constraint equation for F_s is satisfied. These values of L and C_r are then used to compute the various loss components in the inverter. Fig. 7 shows the loss curves obtained for a typical three phase PWM-RDCL inverter using IGBT's. Device and circuit parameters are assumed as shown below:

$$V_D = 3.0\text{V}, t_f = 1\mu s,$$
$$Q = 100, V_{dc} = 350\text{V}$$
$$I_o = 100\text{A}, K = 1.5, F_s = 40\text{kHz}$$

where Q is the quality factor of the inductor, V_{dc} is the dc supply voltage, K is the clamping ratio, and I_o is the peak load current. This corresponds to a single-phase inverter rated at 15 kVA. The loss curves exhibit somewhat similar characteristics as for the conventional resonant dc link inverter. For a comparably rated RDCL inverter with similar system parameters, the loss curves at 40 kHz are shown in Fig. 8. Both total loss curves exhibit a minimum in terms of optimum design values for the inductor and capacitor required. Plots for individual loss components are also shown and verify the projections made above.

The optimization exercise is further extended by repeating the process for various values of the link switching frequency F_s. The minimum loss points corresponding to each frequency are then plotted for the RDCL inverter and for the PWM-RDCL inverter, as is shown in Fig. 9. The losses for a conventional hard-switching PWM inverter are also included for comparison. These curves are based on device conduction and switching losses. It can be seen that although both

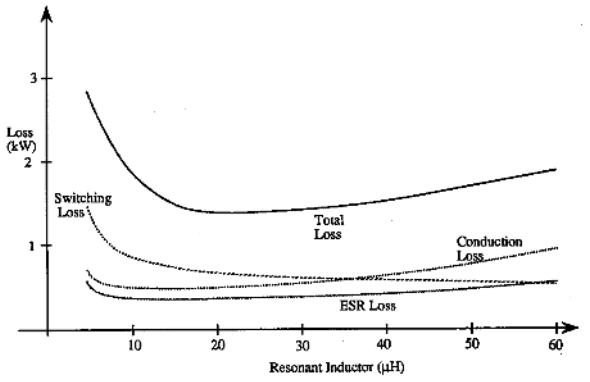

Fig. 7. Variation of loss components with choice of resonant inductor in the PWM RDCL inverter at constant frequency.

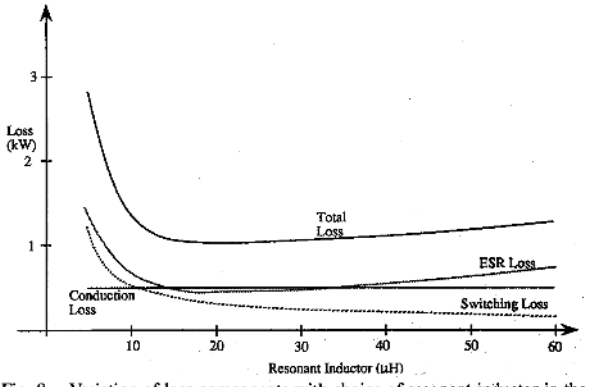

Fig. 8. Variation of loss components with choice of resonant inductor in the PWM RDCL inverter at constant frequency.

the resonant link topologies are far superior to the hard-switching inverter, the conventional RDCL inverter always has significantly lower losses than the proposed PWM-RDCL inverter. In fact, the loss for the PWM-RDCL at 10 kHz is already higher than the loss in the RDCL inverter at 120 kHz. Further, the sensitivity of losses to the link frequency is much lower for the RDCL inverter than for the PWM-RDCL circuit. Consequently, it seems that the PWM-RDCL inverter would be hard pressed to improve on system losses when compared with the conventional RDCL inverter. A more exact analysis that includes the effect of device storage time, tail time, and type of modulation strategy is possible and can be performed as shown in [8]. It is expected that the comparative performance analysis will be affected only marginally.

V. Spectral Performance and Control

Loss calculations indicate that both the RDCL and the PWM-RDCL inverter can switch at high frequencies with reasonable switching loss, although the former has, by far, the lower loss. The existence of true PWM capability for the PWM-RDCL inverter indicates that a lower switching frequency may still yield superior harmonic performance when compared with a DPM system. The use of spectral information, although important, is not very helpful in either of these two

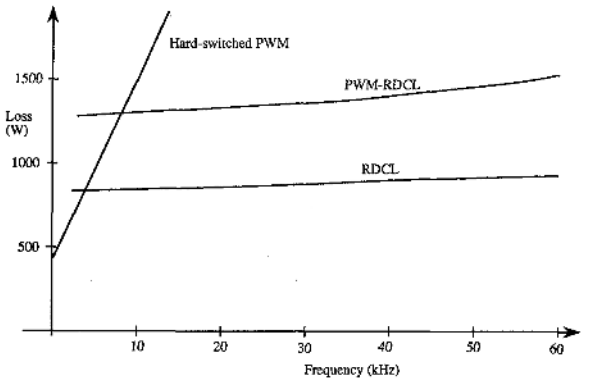

Fig. 9. Variation of minimum losses with frequency in the RDCL and PWM-RDCL converter.

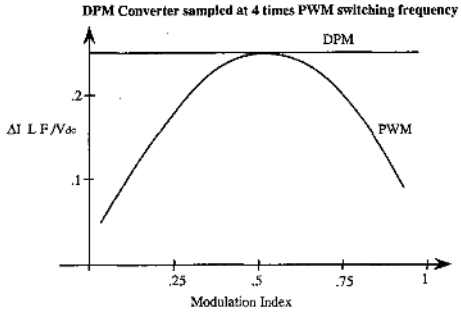

Fig. 10. Variation of output current ripple with modulation index in a PWM and a DPM converter.

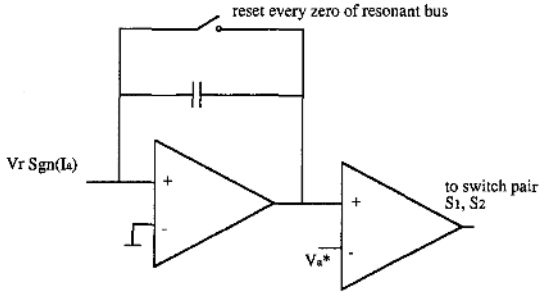

Fig. 11. Block schematic of voltage regulator for PWM-RDCL converter for phase A.

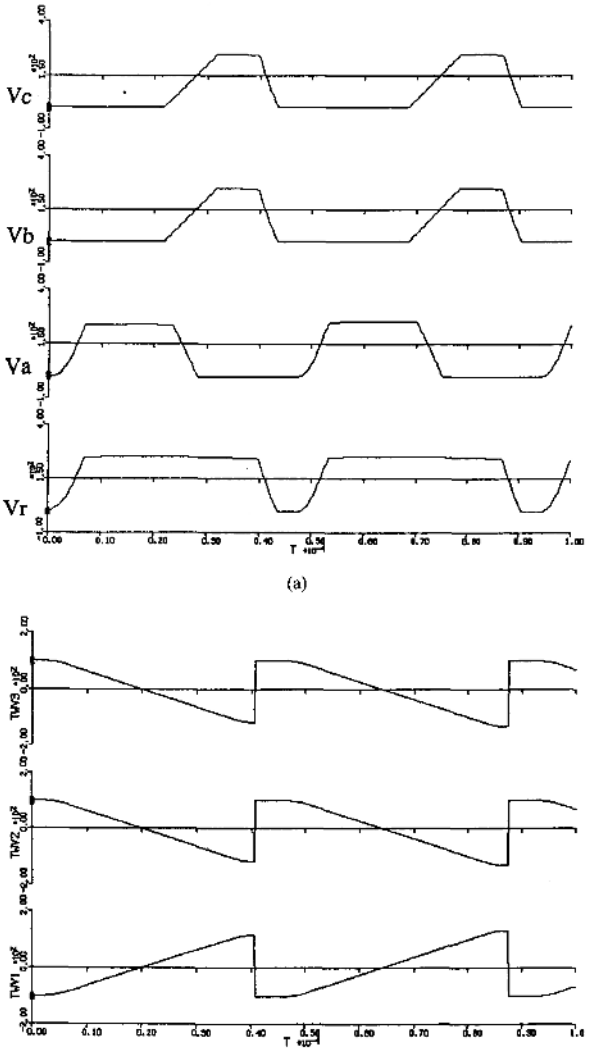

Fig. 12. Simulation results from the voltage-controlled PWM-RDCL converter: (a) Three-phase voltages; (b) carrier waveforms generated by appropriate integration of the link voltage.

cases. In the case of the RDCL inverter under DPM control, the output waveform is seen to be nonstationary and cannot be characterized by a line spectrum. For the PWM-RDCL inverter, on the other hand, the switching waveforms have soft edges that are significantly influenced by the load and make it difficult to compute waveform spectra. Further, the ability to perform PWM control is rather limited, and the inverter would typically need to be operated in a hybrid manner with distinct PWM and DPM control regimes.

Consequently, a better representation of harmonic performance is seen to be the current ripple in the output, which is indicative of both harmonics and torque ripple. Fig. 10 depicts the variation of the peak-to-peak current ripple in a single-phase PWM and DPM inverter [15]. The PWM case shows the actual ripple magnitude, whereas the DPM case indicates an upper bound on the ripple value. The DPM sampling frequency is taken to be four times the PWM switching frequency. From Fig. 10, it can be seen that increasing the frequency by a factor of four results in DPM and PWM systems that have comparable worst-case errors. Where the PWM system has an undeniable advantage is at lower output voltages, where the ripple can tend toward zero. Although PWM-RDCL inverter would have no problem working in that region, it has been seen earlier that modulation indices greater than 0.5 are not possible under steady-state conditions due to clamp charge balance considerations. The favorable operating regime for the PWM-RDCL inverter thus encompasses the range from 0 V

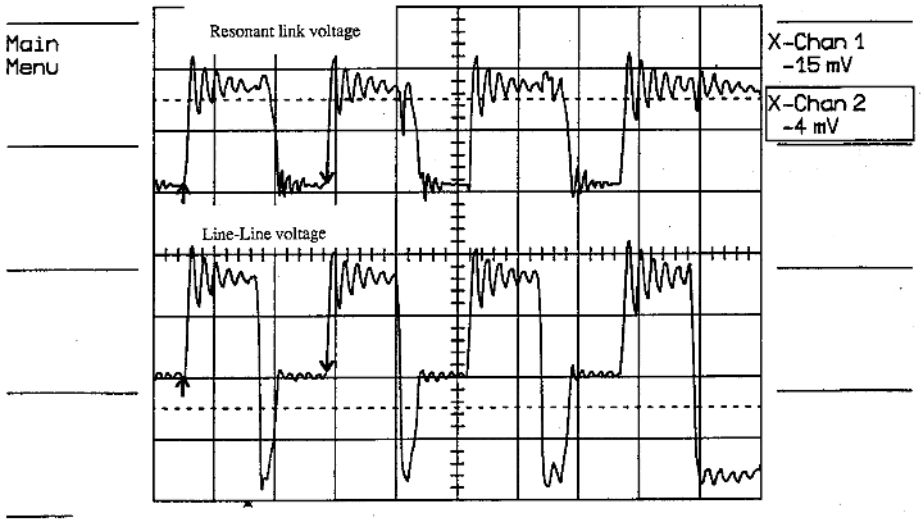

Fig. 13. Traces of resonant link voltage and modulated output voltage from an experimental PWM-RDCL converter: voltage 100 V/div, time 20 μs/div.

to an average duty cycle of less than 0.5, above which a DPM strategy would need to be adopted.

The PWM-RDCL inverter can be controlled in a manner akin to the sinusoidal PWM method. A block diagram of the proposed controller is shown in Fig. 11. The carrier for modulating the link voltage is derived by integrating the resonant link voltage. The integrator is reset at every zero crossing of the bus voltage. The slope of the carrier could be positive or negative, determined by the polarity of the phase current at the zero crossing of the bus. This allows the carrier wave to be inverted based on which device is initially conducting. The turnoff instant for the conducting device is then determined by the intersection of the carrier and control signal. Subcycle turnoff of the device is only permitted within limiting bounds, beyond which the entire resonant pulse appears on the phase output. The error can obviously be carried over from one cycle to the next to further improve performance. Fig. 12 shows simulation waveforms for the PWM-RDCL inverter operating under voltage control. Current control of the PWM-RDCL inverter is also possible but will not be discussed here in the interest of brevity.

VI. Experimental Verification

An existing 15-kVA resonant dc link inverter using BJT's with a switching frequency of 25 kHz was modified to operate under a PWM strategy. Fig. 13 shows the resonant link voltage and the output line-to-line voltage on an expanded scale to illustrate the operation of modulation within the cycle as opposed to DPM.

VII. Conclusions

This paper has presented a means form introducing true PWM capability into the family of zero voltage switching resonant dc link inverters. This approach allows the possibility of reducing subharmonic levels typically found in discrete pulse modulated inverters. A detailed discussion of the tradeoffs showed that the subcycle switching capability was obtained at the expense of significantly higher losses and device stresses. Further, the regime over which true PWM capability could be applied was seen to be rather restricted, being limited by energy constraints required to maintain link oscillations and by the need to conserve charge in the clamp capacitor.

In terms of control, the PWM-RDCL inverter opens up the possibility of realizing extremely low current ripple, even at zero speed and with low torque on the output. This overcomes the most significant of the drawbacks of the conventional discrete pulse-modulated RDCL inverter and opens up a range of even more demanding applications, such as high-power traction. In cases where the midrange torque ripple performance of conventional PWM inverters is deem acceptable, the RDCL inverter still offers an attractive alternative because of the significantly lower losses. The concept of the proposed PWM-RDCL inverter has also been verified experimentally.

Acknowledgment

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