Pulsewidth Modulations for the Comprehensive Capacitor Voltage Balance of n-Level Three-Leg Diode-Clamped Converters

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***Abstract*—In the previous literature, the introduction of the virtual-space-vector (VV) concept for the three-level, three-leg neutral-point-clamped converter has led to the definition of pulsewidth modulation (PWM) strategies, guaranteeing a dc-link capacitor voltage balance in every switching cycle under any type of load, with the only requirement being that the addition of the three phase currents equals zero. This paper presents the definition of the VVs for the general case of an n-level converter, suggests guidelines for designing VV PWM strategies, and provides the expressions of the leg duty-ratio waveforms corresponding to this family of PWMs for an easy implementation. Modulations defined upon these vectors enable the use of diode-clamped topologies with passive front-ends. The performance of these converters operated with the proposed PWMs is compared to the performance of alternative designs through analysis, simulation, and experiments.**

***Index Terms*—Capacitor voltage balance, diode-clamped, multilevel, pulsewidth modulation (PWM), virtual vector.**

I. Introduction

MULTILEVEL converters [1]–[4] have opened the door for advances in electric energy conversion technology. These converters present the advantages of a lower device voltage rating, lower harmonic distortion, and higher efficiency compared with conventional two-level converters.

These converters are typically considered for high-power applications [5]–[8], because they allow operating at higher dc-link voltage levels with the currently available semiconductor technology. But they can also be interesting for medium- or even low-power/voltage applications, since they allow operating with lower voltage-rated devices, with potentially better performance/economical features [9], [10].

There are three basic multilevel converter topologies: diode-clamped, flying capacitor, and cascaded H-bridge with separate dc sources. Among these topologies, diode-clamped converters are especially interesting because of their simplicity; the multiple voltage levels are generated passively through a set of series-connected capacitors (see Fig. 1). The simplest family member, the three-level converter, has been widely studied [11]–[15]. Conventional pulsewidth modulations (PWMs), based on the selection of the nearest three space vectors (NTV), cause an unbalance of the dc-link capacitor voltages, increasing the device voltage stress and generating a low-frequency output-voltage distortion [12]. In higher level diode-clamped converters, conventional modulation solutions also produce unbalances of capacitor voltages, and even lead to the collapse of some of these voltages under a wide range of operating conditions [16]–[20].

To overcome these limitations of diode-clamped topologies, some authors propose the addition of circuitry specifically designed to guarantee the balance [5], [21]–[23]. Other authors introduce a fourth leg [24], [25]. Finally, some authors use a back-to-back connection of multilevel converters to extend the operating range through which the balance can be guaranteed [26]–[28]. A majority of authors, though, have discarded the use of diode-clamped converters with more than three levels in favor of other topologies: flying capacitor, cascaded H-bridge with separate dc sources, and hybrid converter topologies.

The virtual-space-vector (VV) PWM presented in [15], a modulation for the three-level converter based on the definition of a set of VVs, is capable of maintaining the capacitor voltage balance in every switching cycle for any load (linear or nonlinear, balanced or unbalanced) and modulation index, provided that the addition of the output phase currents equals zero and these phase currents are approximately constant over each switching cycle. References [29] and [30] successfully extend this concept to the four-level converter, presenting a VV PWM guaranteeing the dc-link capacitor voltage balance.

The introduction of appropriate VVs for the three-level and four-level converters has proven beneficial, enabling the use of these converters without the need to add circuitry to maintain the balance of the dc-link capacitor voltages. This encourages exploring whether the VV concept can be extended to higher level multilevel converters. This paper concludes that it is possible, presents the definition of such vectors for the general case of an n-level converter, and presents the leg output-terminal duty-ratio expressions to easily implement the most interesting family of VV PWMs for an n-level three-leg diode-clamped converter. The performance of these converters operated with the proposed PWMs is compared with the performance of alternative designs through analysis, simulation, and experiments, from the point of view of component count, PWM algorithm computation time, dc-link capacitor voltage balance, harmonic

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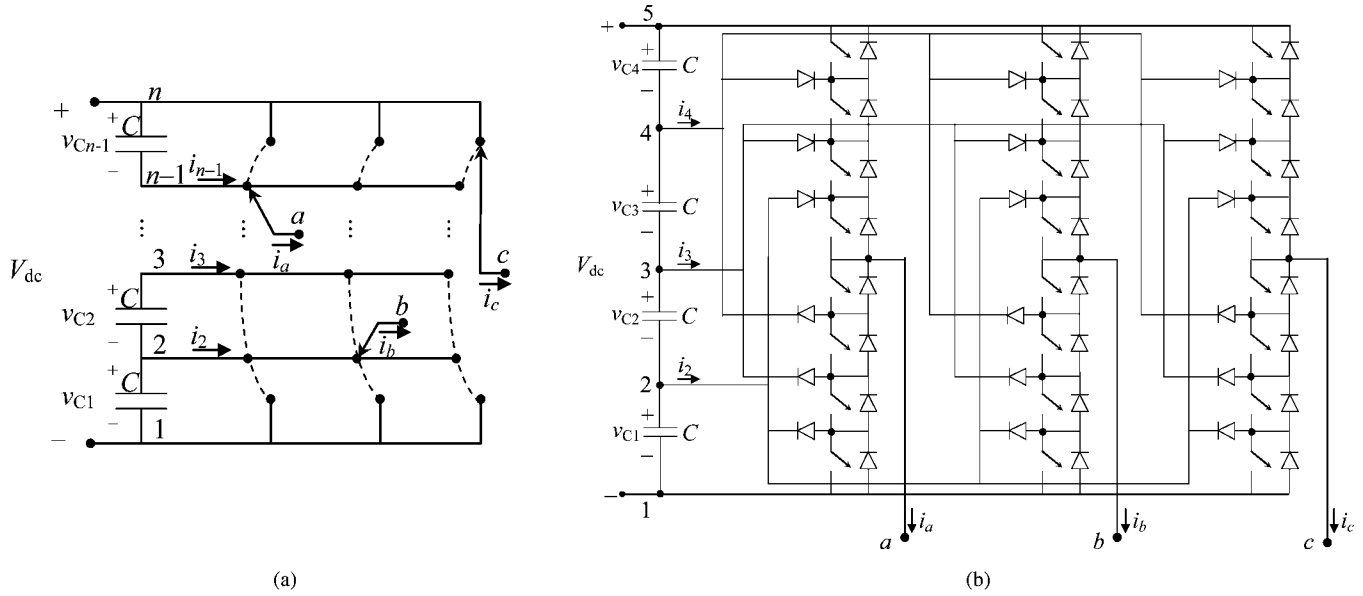

Fig. 1. Multilevel three-leg diode-clamped converters. (a) Functional diagram of an n-level converter. (b) Five-level converter topology.

distortion, and device switching losses. Experimental results are presented for a five-level three-leg diode-clamped converter.

II. n-Level VV PWM

In this section, a generalization of the PWM strategy proposed in [15] and [30] for the three- and four-level converters, respectively, is presented.

A. VV Definition

In an n-level three-leg converter, n^3 switching states are available, designated as *xyz*, where x, y, and z correspond to the dc-link points to which the leg output terminals a, b, and c are connected, respectively. These switching states define $3n^2-3n+1$ vectors in the converter space vector diagram (VD) (see Fig. 2).

To maintain the balance of the $n-1$ capacitor voltages in every switching cycle, we must ensure that all the average intermediate currents $i_2, i_3, \ldots, i_{n-1}$ in every switching cycle equal to zero. In Fig. 2, currents $i_2, i_3, \ldots, i_{n-1}$ corresponding to each switching state are specified in brackets ($[i_2, i_3, \ldots, i_{n-1}]$). Assuming that the addition of the three phase currents is equal to zero ($i_a+i_b+i_c=0$) and the phase currents are approximately constant over each switching cycle, we can define a set of VVs as a linear combination of certain switching states (all the coefficients of the linear combination being equal and their sum equal to 1) such that their associated average i_2, average $i_3, \ldots,$ and average i_{n-1} are equal to zero.

In terms of the switching states involved, a virtual vector $\mathbf{V}$ can be expressed as

$$\mathbf{V}=\frac{1}{\mathrm{nss}_{\mathbf{V}}}\cdot\sum_{i=1}^{\mathrm{nss}_{\mathbf{V}}}(x_i y_i z_i) \tag{1}$$

where $\mathrm{nss}_{\mathbf{V}}$ is the number of switching states *xyz* that defines $\mathbf{V}$. The definition of some of these vectors is

$$\begin{aligned}
\mathbf{V}_z &= \frac{1}{n-2}[(222)+(333)\\
&\quad +\cdots+((n-1)(n-1)(n-1))]\\
\mathbf{V}_{\alpha 1} &= (n11)\\
\mathbf{V}_{\delta 1} &= (nn1)\\
\mathbf{V}_{\alpha(n-1)} &= \frac{1}{n-1}[(211)+(322)+\cdots+(n(n-1)(n-1))]\\
\mathbf{V}_{\delta(n-1)} &= \frac{1}{n-1}[(221)+(332)+\cdots+(nn(n-1))]\\
\mathbf{V}_{\lambda(n-3),0} &= \frac{1}{n}[(321)+(432)+\cdots+(n(n-1)(n-2))\\
&\quad +(211)+(nn(n-1))].
\end{aligned} \tag{2}$$

In general, the remaining VVs present redundancy, i.e., they can be obtained from more than one combination of switching states. The redundancy increases as the number of levels increases. Every available switching state, except for 111 and *nnn*, appears in at least the definition of one of these VVs. The complete definition of these VVs for the three- and four-level converters can be found in [15] and [30].

Fig. 3 shows the tip of these n^2-2n+3 vectors in the first sextant of the VV diagram (VVD). The expression of these vectors in α, β coordinates is

$$\begin{aligned}
\mathbf{V}_z &= (0,0)_{\alpha,\beta}\\
\mathbf{V}_{\alpha i} &= \left(\frac{2}{i\sqrt{3}},0\right)_{\alpha,\beta}, \qquad 1\le i\le n-1\\
\mathbf{V}_{\delta i} &= \left(\frac{1}{i\sqrt{3}},\frac{1}{i}\right)_{\alpha,\beta}, \qquad 1\le i\le n-1
\end{aligned}$$

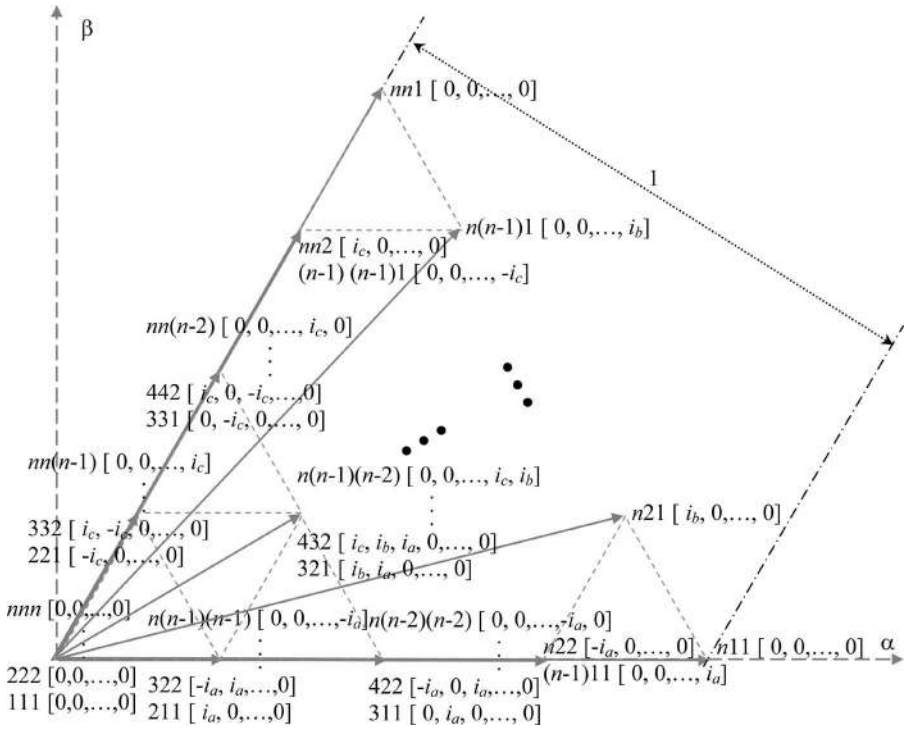

Fig. 2. First sextant of the normalized n-level, three-leg converter VD.

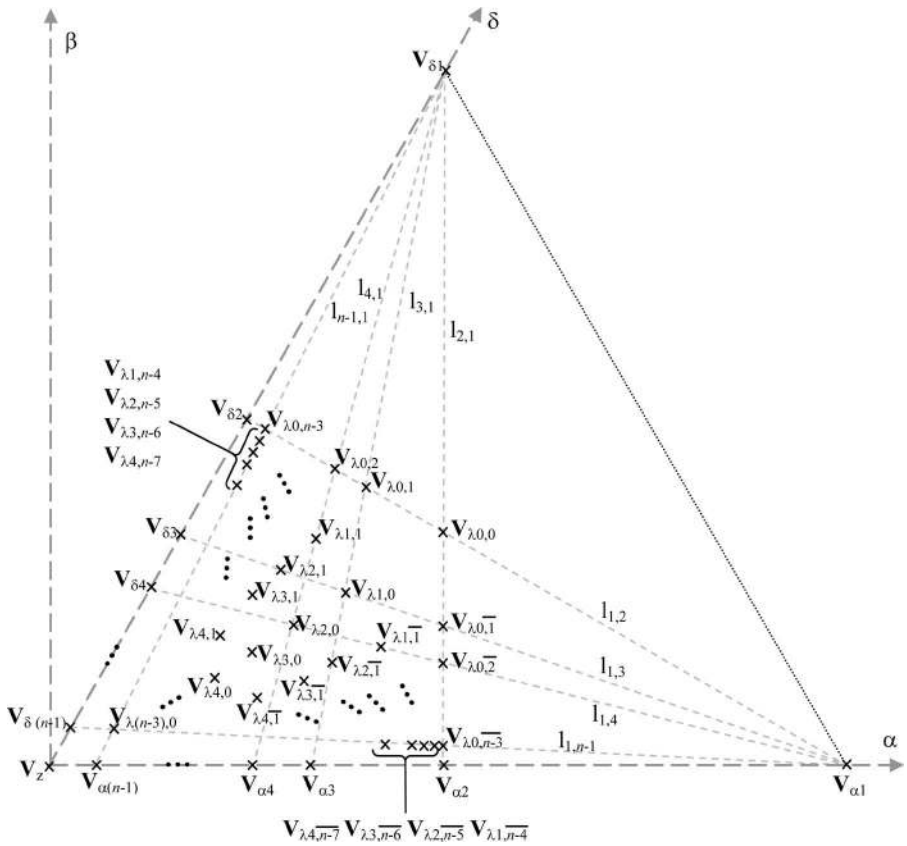

Fig. 3. First sextant of the normalized n-level, three-leg converter VVD.

$$\mathbf{V}_{\boldsymbol{\lambda} i,j} = \left(\frac{3+j}{(3+i+2j)\cdot\sqrt{3}}, \frac{1+j}{3+i+2j} \right)_{\alpha,\beta} \quad 0 \le i \le n-3, \quad 0 \le j \le n-3-i$$

$$\mathbf{V}_{\boldsymbol{\lambda} i,\bar{j}} = \left(\frac{3+2j}{(3+i+2j)\cdot\sqrt{3}}, \frac{1}{3+i+2j} \right)_{\alpha,\beta} \quad 0 \le i \le n-4, \quad 1 \le j \le n-3-i. \tag{3}$$

The location of the vector $\mathbf{V}_{\boldsymbol{\lambda}}$ is defined by the intersections of lines $l_{1,j}$ with $l_{2,k}$ and lines $l_{j,1}$ with $l_{k,2}$, $\forall\, j,\, k$, where $l_{j,k}$ is the straight line joining the tip of the vectors $\mathbf{V}_{\alpha,j}$ and $\mathbf{V}_{\delta,k}$.

B. VV Selection and Switching-State Duty-Ratio Computation

The desired three-phase output voltage is represented by a reference vector ($\mathbf{V}_{\mathrm{ref}} = m\, e^{i\theta}$), $m \in [0,1]$ for a linear modulation, which is obtained as a linear combination of VVs in each switching cycle

$$\mathbf{V}_{\mathrm{ref}} = d_{\mathbf{V}z}\cdot\mathbf{V}_z + \sum_{i=1}^{n-1} d_{\mathbf{V}\alpha i}\cdot\mathbf{V}_{\alpha i} + \sum_{i=1}^{n-1} d_{\mathbf{V}\delta i}\cdot\mathbf{V}_{\delta i} + \sum_{i=0}^{n-3}\sum_{j=0}^{n-3-i} d_{\mathbf{V}\boldsymbol{\lambda} i,j}\cdot\mathbf{V}_{\boldsymbol{\lambda} i,j} + \sum_{i=0}^{n-4}\sum_{j=1}^{n-3-i} d_{\mathbf{V}\boldsymbol{\lambda} i,\bar{j}}\cdot\mathbf{V}_{\boldsymbol{\lambda} i,\bar{j}}$$

$$0 \le d_{\mathbf{V}} \le 1 \qquad \forall\mathbf{V} \qquad \sum_{\mathbf{V}} d_{\mathbf{V}} = 1 \tag{4}$$

where $d_{\mathbf{V}}$ is the duty ratio of vector $\mathbf{V}$. Since VVs are employed, the modulation strategy will preserve the capacitor voltage balance.

As VVs are defined as a linear combination of switching states, $\mathbf{V}_{\mathrm{ref}}$ is ultimately synthesized in each switching cycle by a sequence of switching states. The duty ratio of the switching state *xyz* can be computed as

$$d_{xyz} = \sum_{\mathbf{V}} \frac{1}{\mathrm{nss}_{\mathbf{V}}}\cdot d_{\mathbf{V}} \tag{5}$$

where $\mathbf{V}$ is a virtual vector defined using *xyz*. A few simple examples of switching state duty-ratio computation are

$$d_{222} = d_{333} = \cdots = d_{(n-1)(n-1)(n-1)} = \left[\frac{1}{n-2}\right]\cdot d_{\mathbf{V}z}$$

$$d_{n11} = d_{\mathbf{V}\alpha 1}$$

$$d_{nn1} = d_{\mathbf{V}\delta 1}. \tag{6}$$

Not all VVs need to be employed to approximate $\mathbf{V}_{\mathrm{ref}}$ in each switching cycle, i.e., some of the VV duty ratios in (4) can be set to zero. A set of guidelines follow to perform the selection of VVs to approximate $\mathbf{V}_{\mathrm{ref}}$ in each switching cycle.

1) Select the minimum number of VVs to approximate $\mathbf{V}_{\mathrm{ref}}$ to reduce the number of switching transitions per switching cycle.
2) Choose VVs as close as possible to $\mathbf{V}_{\mathrm{ref}}$ to minimize the output voltage harmonic distortion.

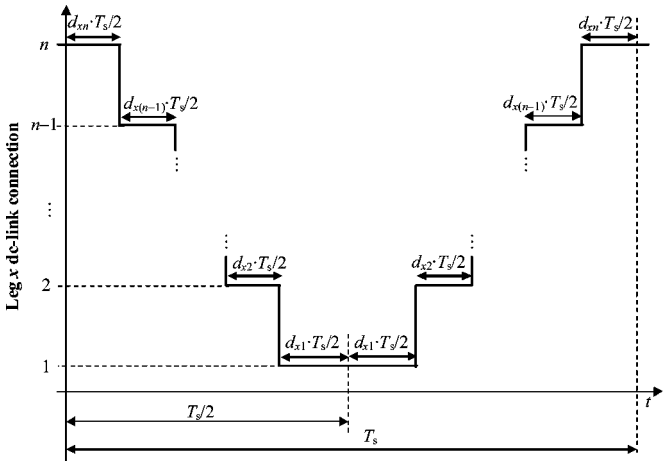

Fig. 4. Selected sequence of connection of leg output terminal x (a, b, or c) to each of the dc-link points (1, 2, . . . , and n).

3) Choose VVs whose associated switching states can be arranged to follow the sequence defined in Section II-C. This allows a simple modulation implementation by using prederived leg duty-ratio expressions in terms of the desired modulation index (m) and output line angle (θ) similar to those presented in [15], [29], and [30] for the three- and four-level converters, and avoid performing any VVD-related computation online.
4) Choose VVs so that the final leg duty-ratio expressions are simple.

C. Switching-States Sequence

Once the switching-state duty ratios have been determined, the sequence over time within a switching cycle of the application of the different switching states has to be decided. The chosen switching-states' order is such that each leg output terminal is connected to the dc-link points following the symmetrical sequence shown in Fig. 4. This can be achieved by simply ordering the switching states three-digit number in a descending–ascending order if appropriate VVs have been selected in the preceding section.

As a consequence, the implementation of a VV PWM only requires the computation of duty ratios $d_{a1}, d_{b1}, d_{c1}, d_{a2}, d_{b2}, d_{c2}, \ldots, d_{an}, d_{bn}, d_{cn}$ (where d_{xy} is the duty ratio of the leg output-terminal-x connection to the dc-link point y), as the addition of the appropriate switching-state duty ratios calculated in Section II-B. For example, in the first sextant, to obtain d_{a2}

$$d_{a2} = d_{222} + d_{221} + d_{211}. \tag{7}$$

D. Leg Duty-Ratio Expressions and Modulation Implementation

The expressions of the leg duty ratios corresponding to the family of VV PWMs for an n-level three-leg diode-clamped converter are shown in (8). These simple equations have been obtained after an extensive analysis of the VV PWM strategies for the three- [15], four- [30] and five-level converters, and

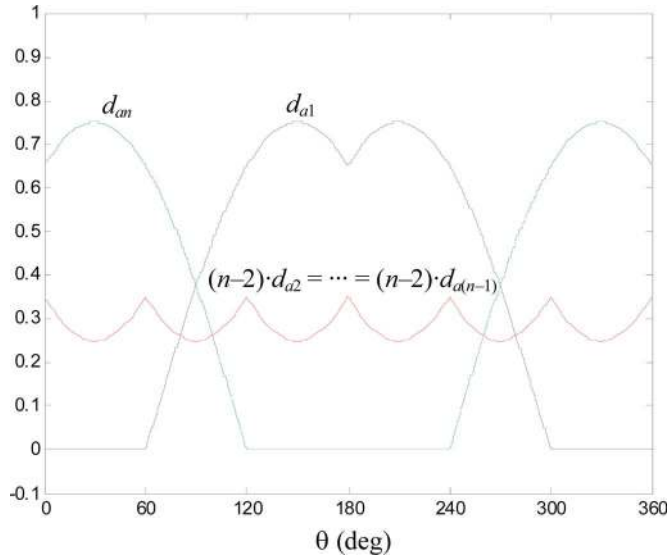

Fig. 5. Leg a duty-ratio pattern for an n-level three-leg converter ($m = 0.75$).

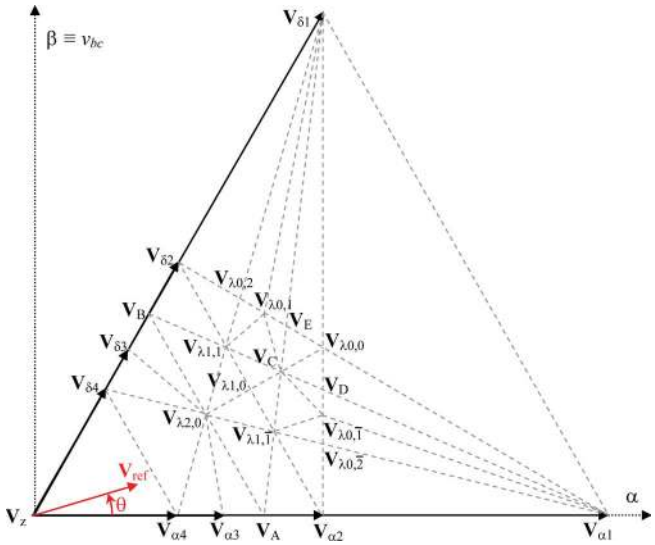

Fig. 6. VVD for the five-level three-leg converter.

through an inductive reasoning process. Although the problem seems complex and rough, the equations obtained are simple and require low computational effort, as shown in (8), at the bottom of the page.

Actually, the average current through the inner dc-link points is zero in every switching cycle if the addition of phase currents equals zero, and these currents are approximately constant over the switching cycle, since

$$i_k = d_{ak}\cdot i_a + d_{bk}\cdot i_b + d_{ck}\cdot i_c = d_k\cdot(i_a + i_b + i_c) = 0 \qquad k = 2,3,\ldots,n-1. \quad (9)$$

An interesting particular VV PWM can be defined with the addition of expressions (10). Fig. 5 depicts the leg a duty ratios for $m = 0.75$ and a line cycle of this particular VV PWM. Legs b and c duty ratios are the same but phase-shifted $\pm 120°$, respectively. This particular VV PWM has two major advantages. First, since all inner dc-link point leg duty ratios are greater than zero, we have margin in every switching cycle to regulate all capacitor dc-link voltages using the control scheme presented in [31]. Additionally, the margin to regulate is balanced, since all inner dc-link point leg duty ratios have the same value. Second, another important advantage is the simplicity of the leg duty-ratio expressions

$$d_{ai} = d_{bi} = d_{ci} = \frac{1-d_{a1}-d_{an}}{n-2} = \frac{1-d_{b1}-d_{bn}}{n-2} = \frac{1-d_{c1}-d_{cn}}{n-2}, \qquad i = 2,3,\ldots,n-1. \quad (10)$$

The PWM defined by (8) and (10) corresponds to a particular VV selection. For example, Fig. 6 presents the VVD for a five-level converter. $\mathbf{V}_{\rm ref}$ is approximated in every switching cycle by the three VVs defining the vertices of the triangle where it is located. The auxiliary virtual vectors $\mathrm{V_A}, \mathrm{V_B}, \mathrm{V_C}, \mathrm{V_D}$, and $V_{\rm E}$ are defined as a combination of certain VVs, as

$$\mathbf{V}_{\rm A} = \frac{2}{5}\cdot\mathbf{V}_{\alpha 2} + \frac{3}{5}\cdot\mathbf{V}_{\alpha 3} = \frac{1}{5}[(533)+(311)+(544)+(422)+(211)] = \left(\frac{4}{5\sqrt{3}},0\right)_{\alpha,\beta}$$

$$\begin{aligned}
0 \le \theta < 2\pi/3: &\quad d_{an} = m\cos(\theta-\pi/6), \quad d_{bn} = m\cos(\theta-\pi/2), \quad d_{cn} = 0\\
2\pi/3 \le \theta < 4\pi/3: &\quad d_{an} = 0, \quad d_{bn} = m\cos(\theta-5\pi/6), \quad d_{cn} = m\cos(\theta-7\pi/6)\\
4\pi/3 \le \theta < 2\pi: &\quad d_{an} = m\cos(\theta+\pi/6), \quad d_{bn} = 0, \quad d_{cn} = m\cos(\theta+\pi/2)\\
-\pi/3 \le \theta < \pi/3: &\quad d_{a1} = 0, \quad d_{b1} = m\cos(\theta+\pi/6), \quad d_{c1} = m\cos(\theta-\pi/6)\\
\pi/3 \le \theta < \pi: &\quad d_{a1} = m\cos(\theta-5\pi/6), \quad d_{b1} = 0, \quad d_{c1} = m\cos(\theta-\pi/2)\\
\pi \le \theta < 5\pi/3: &\quad d_{a1} = m\cos(\theta-7\pi/6), \quad d_{b1} = m\cos(\theta+\pi/2), \quad d_{c1} = 0.\\
&d_{ai} = d_{bi} = d_{ci}, \quad i = 2,3,\ldots,n-1\\
&\sum_{j=1}^{n} d_{aj} = 1, \quad \sum_{j=1}^{n} d_{bj} = 1, \quad \sum_{j=1}^{n} d_{cj} = 1.
\end{aligned} \quad (8)$$

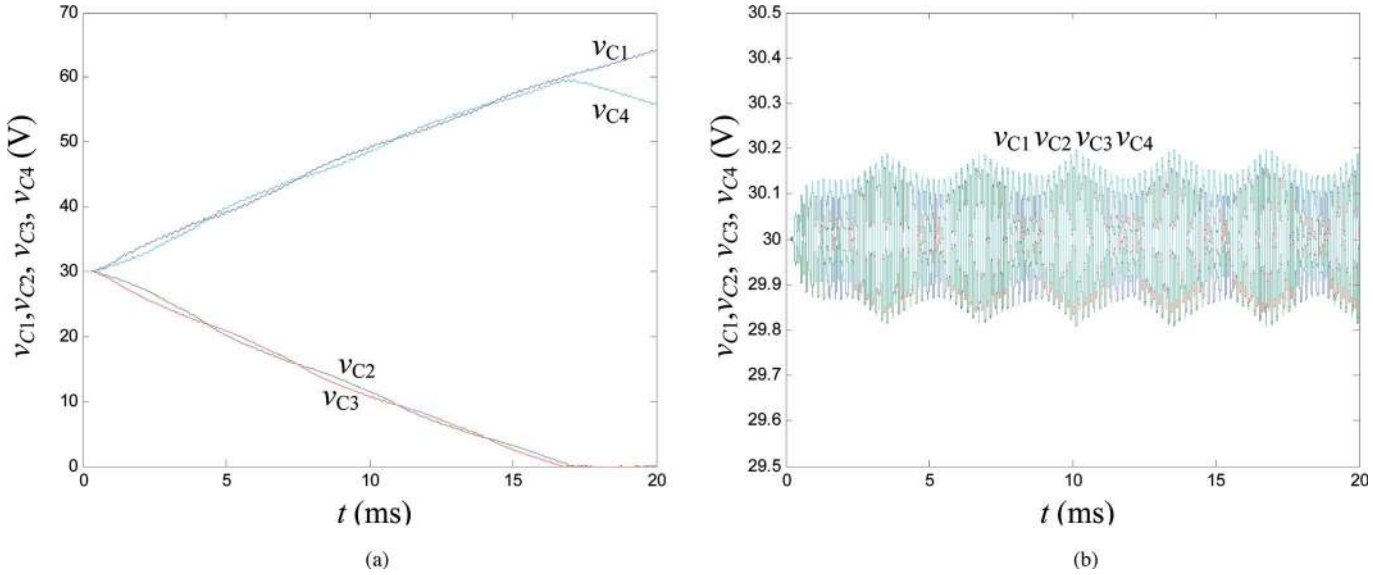

Fig. 7. Simulation results for v_{C1}, v_{C2}, v_{C3}, and v_{C4} (five-level converter) under the following conditions: $V_{dc} = 120$ V, $m = 0.75$, $C = 155$ μF, switching frequency $f_s = 5$ kHz, and a linear and balanced load with per-phase impedance $Z_L = 33.5\ \Omega\ \angle 8.5^\circ$ (series R–L load). (a) Reference NTV PWM. (b) Proposed VV PWM.

$$\begin{aligned}
\mathbf{V}_B &= \frac{2}{5}\cdot\mathbf{V}_{\delta 2} + \frac{3}{5}\cdot\mathbf{V}_{\delta 3} = \frac{1}{5}[(553)+(331)+(554)\\
&\quad +(442)+(221)] = \left(\frac{2}{5\sqrt{3}}, \frac{2}{5}\right)_{\alpha,\beta}\\
\mathbf{V}_C &= \frac{3}{7}\cdot\mathbf{V}_{\lambda 0,0} + \frac{4}{7}\cdot\mathbf{V}_{\lambda 1,0} = \frac{1}{7}[(553)+(531)+(311)\\
&\quad +(554)+(542)+(421)+(211)] = \left(\frac{6}{7\sqrt{3}}, \frac{2}{7}\right)_{\alpha,\beta}\\
\mathbf{V}_D &= \frac{3}{8}\cdot\mathbf{V}_{\lambda 0,0} + \frac{5}{8}\cdot\mathbf{V}_{\lambda 0,\bar{1}} = \frac{1}{8}[(553)+(531)+(311)\\
&\quad +(554)+(542)+(521)+(411)+(211)] = \left(\frac{1}{\sqrt{3}}, \frac{2}{8}\right)_{\alpha,\beta}\\
\mathbf{V}_E &= \frac{3}{8}\cdot\mathbf{V}_{\lambda 0,0} + \frac{5}{8}\cdot\mathbf{V}_{\lambda 0,1} = \frac{1}{8}[(553)+(531)+(311)+(554)\\
&\quad +(552)+(541)+(421)+(211)] = \left(\frac{7}{8\sqrt{3}}, \frac{3}{8}\right)_{\alpha,\beta}.
\end{aligned} \tag{11}$$

The expressions in (8) and (10) allow the direct calculation of $d_{a1}, d_{b1}, d_{c1}, \ldots, d_{an}, d_{bn}$, and d_{cn} as a function of the reference vector coordinates, without the need for identifying the triangle in which it is located and then performing calculations (4)–(7). This significantly simplifies the computations. That is, to implement a VV PWM for an n-level three-leg converter, the controller just needs to be programmed with the expressions in (8) and (10) and the sequence in Fig. 4. There is no need to perform any VVD computation online. The VVD analysis in Sections II-A and II-B is only presented to illustrate the problem and the process followed to obtain the final PWM strategy completely defined and implemented by (8) and (10), and Fig. 4.

The particular PWM defined by (8) and (10) presents $3n-5$ pairs of switching transitions (one switch turns off and another turns on) per half switching cycle in all regions of the VVD. Other VV PWM solutions verifying (8) may present lower number of switching transitions and lower ac-side harmonic distortion (see examples in [29] for a four-level converter), but they are not considered here for the sake of simplicity.

III. Simulation Results

In this section, the performance of a three-leg diode-clamped converter connected to a single dc bus through terminals 1 and n (Fig. 1) and operated with the proposed VV PWM ((8) and (10)) is analyzed through simulation in MATLAB–Simulink and compared to other alternative design solutions. It is assumed that the dc bus is already available and that other systems might be connected to it. The dc bus can be generated, for instance, from the mains or other ac sources employing a simple diode rectifier. In inverting applications feeding the dc bus from a low-frequency ac source and already requiring a transformer (e.g., for galvanic isolation), this transformer can be designed to have $n-1$ secondaries connected to rectifiers to generate the different voltage levels and this, together with a proper NTV PWM strategy for the multilevel converter, is possibly the optimal design solution. However, these particular applications are not considered here for the sake of generality, and therefore, the introduction of such low-frequency transformers is discarded because they are typically bulky, expensive, and lossy components.

Fig. 7 shows the results of the dc-link capacitor voltage balance in a five-level converter. A particular NTV PWM is used as a reference for comparison. In this reference NTV PWM, the duty ratio assigned to each space vector (a vector is defined here as a combination of line-to-line voltages or an arrow in Fig. 2) is equally shared in every switching cycle by all associated switching states. That is, the reference vector is synthesized

in every switching cycle using the nearest three vectors in the space VD. Then, each voltage vector is generated by equally using all associated switching states. For instance, if in a given switching cycle we need to produce a particular vector for a time equal to t^*, and two switching states are possible (e.g., $n22$ and $(n-1)11$), we will use $n22$ during $t^*/2$ and $(n-1)11$ during $t^*/2$). The only exception is for the zero vector where switching states *nnn* and 111 are not used. This particular NTV PWM strategy presents, at low modulation indexes, a higher number of switching transitions than other typical NTV PWM schemes presented in the literature, but it presents a lower output ac-side voltage total harmonic distortion (THD), as demonstrated in [32]. At high modulation indexes the number of switching transitions is reduced and it is comparable to typical particular NTV PWM strategies, while keeping an optimum output ac-side voltage THD. Over all the modulation index range, it presents a good capacitor voltage balance behavior compared to other particular open-loop NTV PWM strategies. In Fig. 7, both this reference NTV PWM and the proposed VV PWM are tested at an operating point outside the limits for a balanced and stable operation specified in [16]–[20]. While the use of the conventional NTV PWM leads to the collapse of some capacitor voltages, the proposed VV PWM maintains a balanced dc-link capacitor voltage operation. Additionally, the peak-to-peak value of the capacitor voltage ripple is inversely proportional to the switching (or carrier) frequency. Hence, for a given capacitor voltage ripple specification, the required capacitance can be reduced by increasing the switching frequency.

Let us compare the proposed n-level diode-clamped converter connected to a single dc bus and operated with a VV PWM (design A) to two alternative converter designs based on the same topology. The first alternative design (design B) consists of an n-level diode-clamped converter with regulated dc voltage sources replacing the dc-link capacitors and operated with the reference NTV PWM described earlier. The second alternative design (design C) corresponds to a two-level converter operated with a conventional space vector modulation using the two possible switching states available for the zero vector in every switching cycle.

A. Component Count

From the point of view of component count, design C presents the minimum number of components, as it uses a simple two-level converter. Design A presents fewer components than design B, since it does not require the addition of regulated dc voltage sources replacing the dc-link capacitors. These sources can be implemented with $n-1$ output-voltage-regulated dc power supplies drawing the energy from the dc bus or through the introduction of specific PWM balancing circuits [5], [21]–[23].

B. Modulation Algorithm Computation Time

From the point of view of the computation time required by the modulation algorithm, designs A and C are clearly superior to design B. For instance, the computation of 10 000 line cycles with $f_s/f_o = 100$ (where f_o is the output fundamental frequency), $m = 0.75$, on a personal computer with an Intel Pentium D processor at 3 GHz, 1 GB of RAM, and using MATLAB 7.2, takes 1.45 s for design C. The computation time for design A (see [30, algorithm in the Appendix]) is slightly higher (1.53 s for $n = 3$, 1.61 s for $n = 4$, and 1.66 s for $n = 5$), and the computation time for design B (employing the algorithm presented in [33]) is significantly higher (7.44 s for $n = 3$, 10.95 s for $n = 4$, and 12.65 s for $n = 5$).

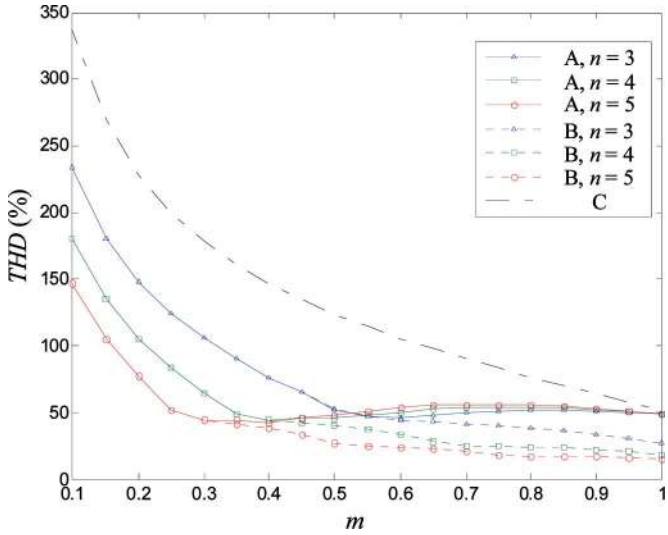

Fig. 8. THD as a function of the modulation index m. Conditions: $f_s/f_o = 100$ and harmonics considered up to $40f_s$.

C. Total Harmonic Distortion

Fig. 8 shows the THD in the line-to-line output voltage of all three designs as a function of the modulation index. Design B is clearly superior to designs A and C, particularly as the number of levels n increases. Design A is clearly superior to design C. The THD of designs A and B is the same for low modulation index values. In fact, the particular NTV PWM strategy selected for design B is equivalent to the proposed VV PWM for modulation indexes $m < 1/(n-1)$. As the modulation index increases, design A presents a progressively higher THD than design B and reaches the level of design C for $m = 1$.

D. Semiconductor Device Losses

A discussion follows regarding the comparison of semiconductor device losses in the main converter of all three designs. The comparison is made for the same dc-link voltage $V_{\rm dc}$, the same output power, sinusoidal and balanced three-phase currents, negligible ac-side current ripple, unity displacement factor, and the same carrier frequency f_s.

Assuming a similar value of the conduction voltage drop per rated voltage for all semiconductor devices, conduction losses should be similar in all three designs. The main differences in device losses will be due to the different switching pattern. For each converter leg, switching transitions occur in pairs: one switch turns off and the other switch turns on. To simplify the analysis, it is assumed that diodes are ideal (lossless) and the losses are concentrated either in the controlled device turning

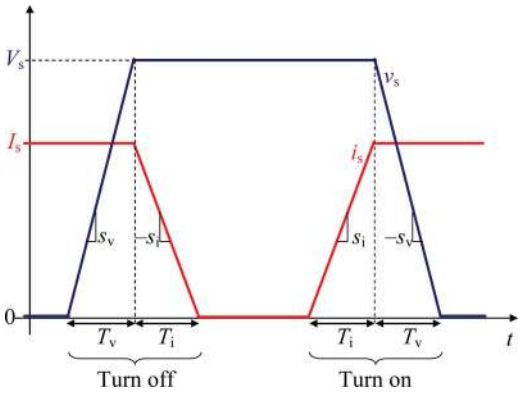

Fig. 9. Voltage and current waveforms during switching transitions in the controlled devices concentrating the switching losses.

on or the device turning off, according to the pattern described in Fig. 9, where $v_s(t)$ and $i_s(t)$ are the voltage across the switch and the current through the switch, respectively. The absolute values of the voltage and current slopes during transitions are assumed to be constant and equal to $\pm s_v$ and $\pm s_i$, regardless of the value of V_s and I_s. With these assumptions, the energy lost in a switching transition of an n-level converter leg is

$$E_s = \frac{V_{\rm dc}^2 \cdot I_s}{2\,(n-1)^2\, s_v} + \frac{V_{\rm dc} \cdot I_s^2}{2\,(n-1)\, s_i}. \qquad (12)$$

Let us additionally assume that $s_v/s_i = V_{\rm dc}/I_{\rm pk}$, where $I_{\rm pk}$ is the peak value of the phase current, i.e., the voltage and current transition times (T_v and T_i) are equal for $V_s = V_{\rm dc}$ and $I_s = I_{\rm pk}$. Fig. 10 shows the ratio of the switching losses in designs A ($P_{s,\rm A}$) and B ($P_{s,\rm B}$) with regard to the switching losses in design C ($P_{s,\rm C}$), for $n = 3, 4$, and 5. It can be observed that both designs A and B produce lower switching losses than design C. Design B is clearly the optimum, particularly for high modulation indexes and the number of levels. This means that design B produces lower switching losses in the multilevel converter than design A. However, from the point of view of the whole design losses, for a fair comparison, the losses in the regulated dc voltage sources replacing the dc-link capacitors must be considered in design B, which will probably lead to a higher total loss than in design A, since these regulated dc voltage sources process most of the energy flowing in between the dc-link and the ac side.

Fig. 11 shows the ratio $P_{s,\rm A}/P_{s,\rm C}$ as a function of the converter number of levels. This ratio depends on the total amount of switched voltage in design A (equal to $V_{\rm dc}\cdot(3n-5)/(n-1)$ for $n \geq 3$) and the ratio s_v/s_i. As n increases, $P_{s,\rm A}/P_{s,\rm C}$ tends to settle at a given value because the addition of all switching losses in design A occurring within T_v tends to zero, while the addition of all switching losses occurring within T_i remains constant. This asymptotical value depends on the ratio s_v/s_i. As the ratio s_v/s_i decreases, the proportion of the switching losses occurring during the current transitions decreases, and the asymptotical value of the ratio $P_{s,\rm A}/P_{s,\rm C}$ also decreases.

Multilevel diode-clamped topologies present a problem of loss distribution unbalance among different devices [35]. Al-

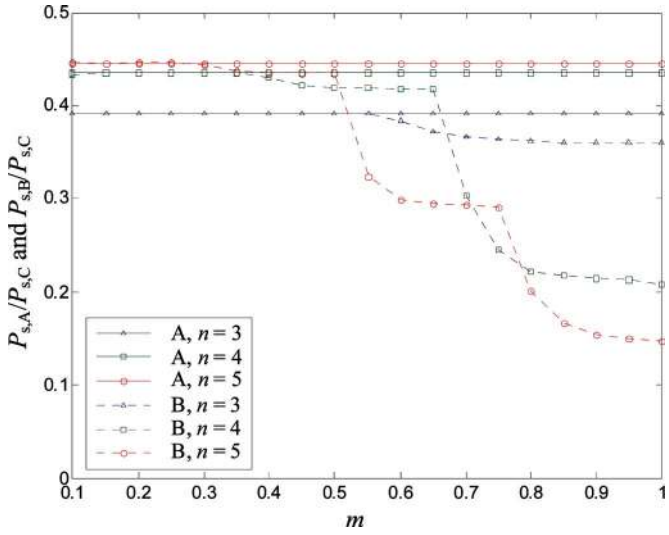

Fig. 10. Ratio of the switching losses in designs A ($P_{s,\rm A}$) and B ($P_{s,\rm B}$) with regard to the switching losses in design C ($P_{s,\rm C}$), for $n = 3$, 4, and 5.

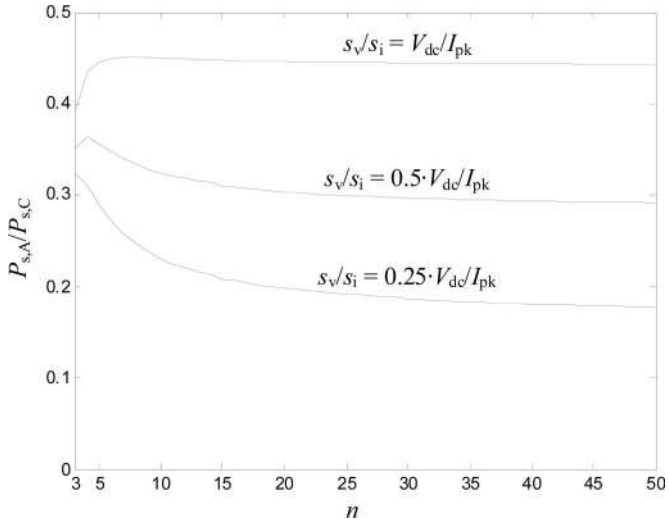

Fig. 11. Ratio $P_{s,\rm A}/P_{s,\rm C}$ as a function of the number of levels n.

though the use of the VV PWM does not solve this problem, it may help redistribute the losses at certain operating points [36]. The combination of the proposed VV PWM with the active diode-clamped topology [35] could be explored to improve the loss distribution performance.

IV. Experimental Results

Experimental tests have been conducted to verify the performance observed in the simulation results of Fig. 7 for a five-level three-leg converter. A prototype built with 150-V MOSFETs has been used for this purpose. The converter is operated in inverter mode and open loop, with a dc power supply connected between dc-link points 1 and 5, and a three-phase series R–L load connected to the ac side. The computation of 12 independent leg duty ratios [see (8) and (10)] is performed by the embedded PowerPC of dSpace DS1103. This information is sent to

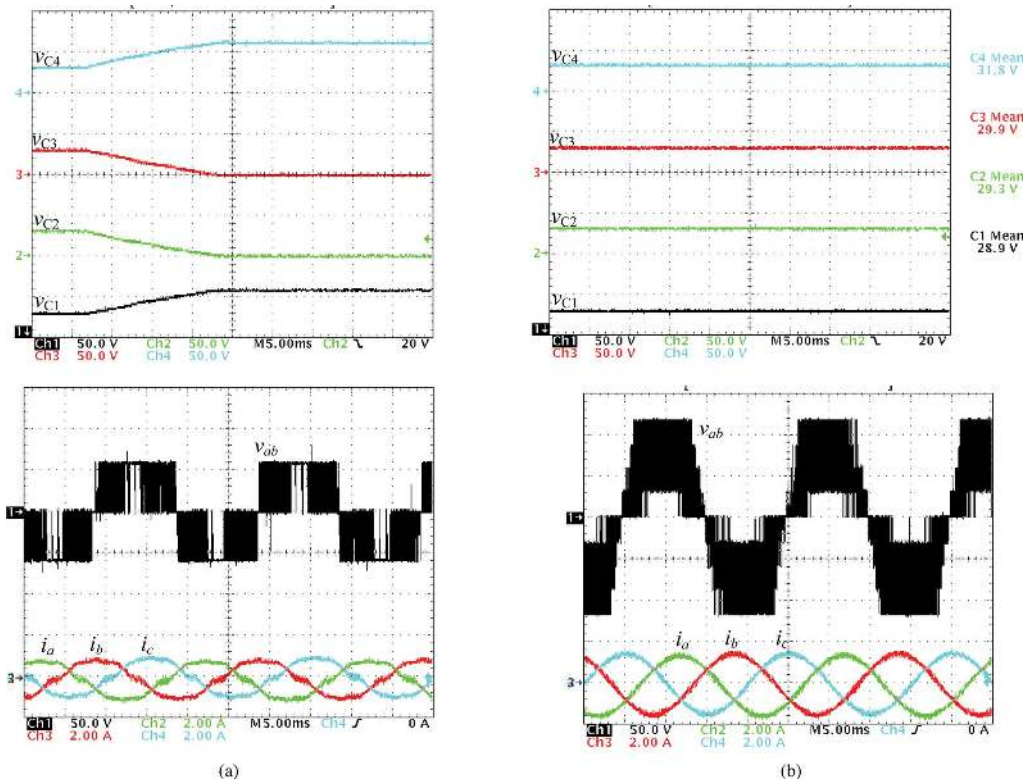

Fig. 12. Experimental results for $v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_{ab}, i_a, i_b$, and i_c under the following conditions: $V_{dc} = 120$ V, $m = 0.75$, $C = 155$ μF, $f_s = 5$ kHz, a linear and balanced load with per-phase impedance $Z_L = 33.5\ \Omega\ \angle 8.5^\circ$ (series R–L load), and a prototype using 150 V MOSFETs. (a) Reference NTV PWM. (b) Proposed VV PWM.

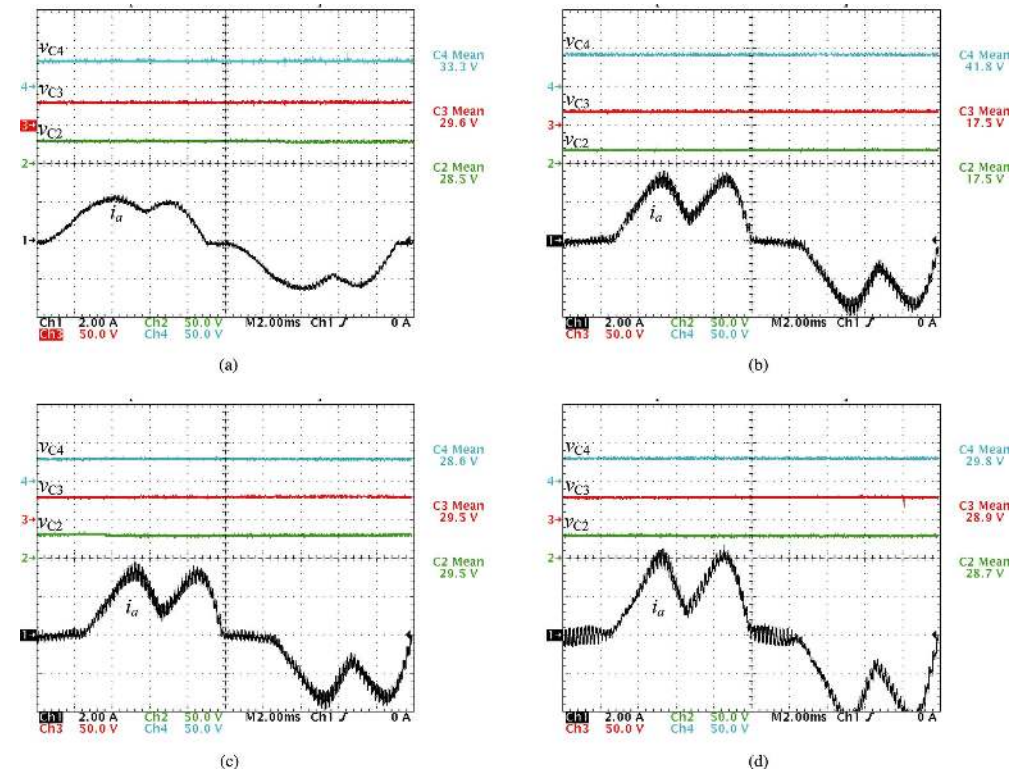

Fig. 13. Experimental results for v_{C2}, v_{C3}, v_{C4}, and i_a under the following conditions: $V_{dc} = 120$ V, $C = 155$ μF, $f_s = 5$ kHz, a nonlinear load consisting of a three-phase boost diode rectifier (with inductance L per phase), a capacitor (2 mF), and a resistor (33 Ω) connected across the rectifier dc side, and the same prototype in Fig. 12 operated with the proposed VV PWM. (a) $m = 0.75$, $L = 12.5$ mH, balancing control off. (b) $m = 0.75$, $L = 2.5$ mH, balancing control off. (c) $m = 0.75$, $L = 2.5$ mH, balancing control on. (d) $m = 0.95$, $L = 2.5$ mH, balancing control on.

TABLE I
DESIGN RANKING

Feature	Design A	Design B	Design C
Component count	2	3	1
PWM algorithm computation time	2	3	1
THD	2	1	3
Semiconductor device losses in the multilevel converter	2	1	3

Key: 1—best, 2—middle, 3—worst.

an Altera EPF10K70 programmable logic device in charge of generating 24 switch control signals.

Fig. 12 shows that the NTV PWM used as a reference for comparison leads to the collapse of the middle capacitor voltages v_{C2} and v_{C3}. The same would occur with any other NTV PWM at this operating point. On the other hand, with the proposed VV PWM all four capacitor voltages are fairly balanced in the absence of a closed-loop control.

The balancing properties of the proposed VV PWM have been therefore experimentally verified for linear loads at operating points beyond the limits specified in [16] and [17] for NTV PWMs, in the case of a three-level converter [15], four-level converter [30], and five-level converter (see Fig. 12). However, the proposed VV PWM strategy guarantees a capacitor voltage balance only if phase currents are approximately constant over a switching cycle. This assumption is not verified under certain operating conditions: load transients, transients under closed-loop phase-current control, certain nonlinear loads, and especially under high phase-current ripple. In general, if high phase-current time derivatives occur, the per-switching-cycle balancing effect of the proposed open-loop modulator is lost. In these cases, the addition of the balancing control proposed in [31] is essential to maintain the balance. In [34], this has already been verified for a three-level converter under a closed-loop output current control. The multilevel dc–ac converter operates in inverter mode, injecting energy into the ac mains. The dedicated balancing control effort is minimal during a steady-state operation and transients.

Fig. 13 presents experimental results under a nonlinear load. Fig. 13(a) shows that the capacitor voltage unbalance is negligible under a small phase-current ripple. In Fig. 13(b), a significant capacitor voltage unbalance appears under a higher current ripple. The activation of the balancing control [31] in Fig. 13(c) allows recovering the capacitor voltage balance. Finally, Fig. 13(d) shows that a balanced operation is also possible under high modulation index values and high current ripple with the proposed VV PWM and the balancing control. The balancing control effort in Fig. 13(c) and (d) is small. The control introduces a variation in the duty ratios lower than 0.01 (i.e., 1%). This control is also necessary in practice to guarantee the balance under unequal switching behavior, leakage currents, etc.

V. CONCLUSION

The definition of VVs guaranteeing the capacitor voltage balance in every switching cycle, even under nonlinear loading conditions, can be extended to any multilevel diode-clamped converter. This paper has presented the definition of these vectors for an n-level three-leg diode-clamped converter and the guidelines for designing practical VV PWMs. These guidelines take into consideration the number of switching transitions, the output voltage distortion, and the simplicity of the final implementation.

The leg duty-ratio expressions that allow a simple implementation of these PWMs have also been presented. These PWMs (patent pending) guarantee capacitor voltage balance even for high modulation indexes, enabling the use of multilevel diode-clamped converters with passive front-ends.

The performance of an n-level three-leg diode-clamped converter operated with a VV PWM (design A) has been compared with the performance of two alternative designs: an n-level three-leg diode-clamped converter replacing the dc-link capacitors with regulated dc voltage sources and operated with a conventional NTV PWM (design B), and a two-level converter operated with a conventional space vector modulation (design C). Table I presents their ranking in terms of different performance items.

Designs A and B offer a good alternative to design C because of their superior performance in terms of output voltage harmonic distortion and converter losses, as expected. In applications with no stringent filtering requirements, design A might be the best solution, since it will probably present a lower total component cost and higher overall efficiency than design B.

Therefore, VV PWMs lead to a competitive design solution that may allow, with the addition of other recent technical advances [37], [38], highly integrated and compact converter designs based on diode-clamped topologies.

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