JPE 16-2-11

http://dx.doi.org/10.6113/JPE.2016.16.2.498
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

PWM Control Techniques for Single-Phase Multilevel Inverter Based Controlled DC Cells

Mahmoud A. Sayed†, Mahrous Ahmed*, **, Maha G. Elsheikh*, and Mohamed Orabi*

†Electrical Engineering Department, Faculty of Engineering, South Valley University, Qena, Egypt
*APEARC, Faculty of Engineering, Aswan University, Aswan, Egypt
**Electrical Engineering Department, Faculty of Engineering, Taif University, Taif, Saudi Arabia

Abstract

This paper presents a single-phase five-level inverter controlled by two novel pulse width modulation (PWM) switching techniques. The proposed PWM techniques are designed based on minimum switching power loss and minimum total harmonic distortion (THD). In a single-phase five-level inverter employing six switches, the first proposed PWM technique requires four switches to operate at switching frequency and two other switches to operate at line frequency. The second proposed PWM technique requires only two switches to operate at switching frequency and the rest of the switches to operate at line frequency. Compared with conventional PWM techniques for single-phase five-level inverters, the proposed PWM techniques offer high efficiency and low harmonic components in the output voltage. The validity of the proposed PWM switching techniques in controlling single-phase five-level inverters to regulate load voltage is verified experimentally using a 100 V, 500 W laboratory prototype controlled by dspace 1103.

Key words: Multilevel inverter, PWM, Single-phase inverter, Voltage control

I. INTRODUCTION

Recently, the applications of power electronic inverters have become increasingly important. Pulse width modulation (PWM) inverters have the ability to control their output voltages and frequencies simultaneously. Therefore, PWM inverters are considered excellent candidates in industrial applications, such as renewable energy sources, electrical machine drives, uninterruptible power supplies, and power conversion applications. With the rising importance of high efficiency and low harmonic contents, new requirements for the switching techniques and circuit topologies of PWM inverters have developed. The most important issues include the output voltage levels and limitations of switching devices [1], [2].

Multilevel inverters are now considered for power electronic applications due to their ability to operate at high output voltages while producing low levels of harmonic components in switched output voltages because of the great availability of voltage levels [3]-[9]. In addition, output voltages can be filtered using small reactive components. The switching frequencies of devices can be reduced, and more sinusoidal-shaped output voltage waves can be obtained [10], [11]. Multilevel inverters are now preferred in high power medium voltage applications due to the reduced voltage stresses on devices. Neutral point clamped inverters [12], [13], flying capacitors [14]-[16], and cascaded H-bridge inverters [17]-[19] are popular topologies of multilevel inverters. However, these multilevel inverter topologies require a large number of power semiconductor switches and thus suffer from high switching power losses. Although low voltage rate switches can be utilized in multilevel inverters, each switch requires a gate drive circuit. This requirement increases the cost and complexity of the overall system. Therefore, in practical implementation, the reduction of the number of switches and gate driver circuits is an essential research topic [20].

Recently, many topologies of single-phase multilevel inverters and PWM switching techniques have been proposed. In [20], combinations of series and parallel switches were used to implement multilevel inverters. However, this topology uses a large number of power switches. In [21], a multilevel inverter was implemented by using two switches and two power diodes

Manuscript received Jul. 28, 2015; accepted Oct. 28, 2015
Recommended for publication by Associate Editor Lixiang Wei.
†Corresponding Author: mahmoud_sayed@ieee.org
Tel: +201121380066, South Valley University
*APEARC, Faculty of Engineering, Aswan University, Egypt
**Electrical Engineering Department, Faculty of Engineering, Taif University, Saudi Arabia

with an H-bridge single-phase inverter. These two systems can generate only five output voltage levels. In [22], a conventional single-phase inverter was converted to a single-phase five-level inverter by adding one switch and four power diodes to the conventional H-bridge single-phase inverter. In [23], a modular inverter that can produce any required voltage levels was presented. In [24], a single-phase five-level inverter was proposed using only six power switches in addition to two coupled inductors and one dc supply. However, the size of the coupled inductors is large. In [25], a new topology of a single-phase five-level inverter was presented using only six power switches in addition to two floating dc power supplies. However, the control scheme was designed based on a lookup table. In [26], a new topology of a single-phase five-level inverter was presented based on a minimum number of power switches. This topology adopts a full-bridge configuration with a single-pulse control technique based on a switching angle calculation method. The harmonic components of the output voltage are determined by the load inductance in addition to the filter. Therefore, their harmonic reduction is limited to a certain degree. Furthermore, the switching angle calculation method requires off-line calculations of the switching angles and a lookup table. The same technique was modified in [27] by using bidirectional switches, which increase the number of power switches used in the cascaded controlled dc cells. In [28], the same technique was used to obtain a single-phase multilevel inverter using conventional power switches. However, each dc supply was controlled by two switches. To overcome these limitations, the authors in [29] proposed a new PWM switching technique for controlling single-phase five-level inverters based on high efficiency and low harmonics.

Motivated by the aforementioned issues, the present work proposes two novel control techniques based on PWM switching for controlling a stand-alone single-phase five-level inverter. The structure of the inverter uses two power switches that control the dc input voltage of a conventional H-bridge inverter. In both control schemes, some switches operate at high switching frequency, whereas others operate at fundamental line frequency to reduce switching power losses. A proportional–integral (PI) controller is used to achieve load voltage to be same as the reference one. Theoretical analysis, numerical simulation, and laboratory prototype with several experimental results are presented to investigate the capability of the proposed PWM switching schemes in controlling load voltage and to confirm the characteristics of the proposed inverter.

II. Configuration and Operational Principle of the Proposed Inverter

The proposed structure of the single-phase multilevel inverter is shown in Fig. 1. It consists of *n*-cells connected in series; one cell is a dc supply and the other cells have dc supply controlled by two switches (S_{k1}, S_{k2}), where ($k = 1, 2, , n$). The switch (S_{k2}) is connected in series with the dc voltage source, and the other switch (S_{k1}) is connected in parallel to the dc voltage source and the series switch (S_{k2}). According to the proposed configuration shown in Fig. 1, each cell controlled by two switches features two output voltage states: zero voltage and the dc voltage source associated with the considered cell. Given that cell-n only has a dc voltage source, it has only one state voltage, which is the value of its dc supply. Therefore, the dc bus voltage has (n) states according to the values of ($V_1, V_2, \ldots, V_n$), as shown in Fig. 2. The dc bus shown in Fig. 1 clearly lacks zero state voltage. Therefore, cell-n is the basic cell that must be included in any multilevel inverter based on the proposed topology.

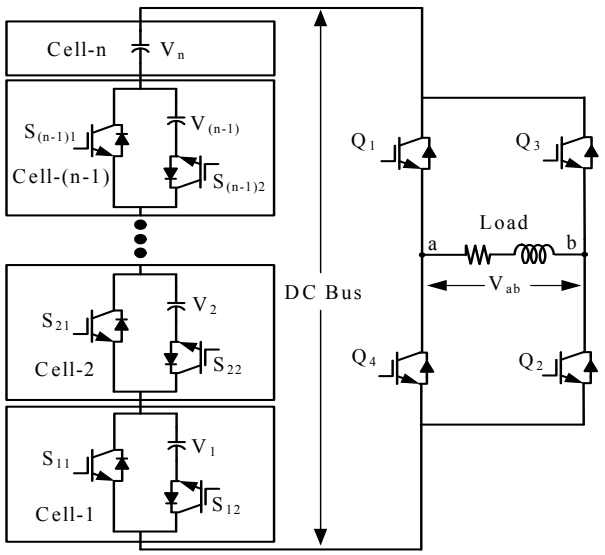


Fig. 1. Configuration of a single-phase multilevel inverter.

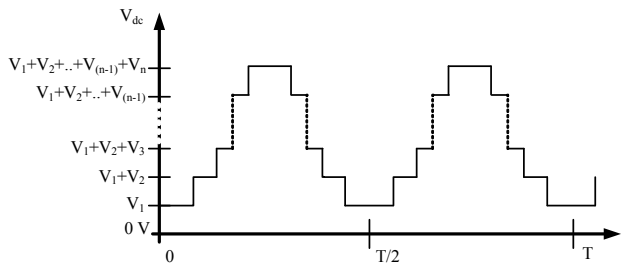


Fig. 2. Voltage levels of the dc bus.

A conventional H-bridge inverter is connected to the dc bus terminals to convert the dc voltage to the switched bipolar voltage limited by the value of the dc voltage at the dc bus. The H-bridge inverter consists of four switches ($Q_1, Q_2, Q_3,$ and Q_4), as shown in Fig. 1. The main function of the H-bridge inverter is to obtain a zero state voltage on the ac load by considering the switches Q_1 and Q_3 or Q_2 and Q_4 to be in the ON state simultaneously. Moreover, the H-bridge inverter is used to obtain a positive half cycle by considering the switches Q_1 and Q_2 to be in the ON state and a negative half cycle by considering the switches Q_3 and Q_4 to be in the ON state.

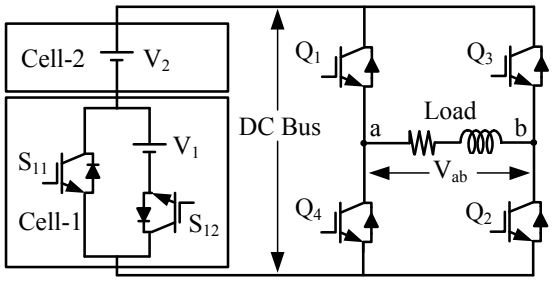


Fig. 3. Model of a single-phase five-level inverter.

TABLE I
SWITCHING STATES OF THE SINGLE-PHASE FIVE-LEVEL INVERTER

States	V_{ab}	i_o	ON switches
a	$2V_{dc}$	+	$Q1$, $Q2$, and $S12$
b	$2V_{dc}$	−	$D1$, $D2$, and $S12$
c	V_{dc}	+	$Q1$, $Q2$, and $S11$
d	V_{dc}	−	$D1$, $D2$, and $S11$
e	0	+	$Q1$ and $D3$ or $Q2$ and $D4$
f	0	−	$Q3$ and $D1$ or $Q4$ and $D2$
g	$-V_{dc}$	+	$D3$, $D4$, and $S11$
h	$-V_{dc}$	−	$Q3$, $Q4$, and $S11$
i	$-2V_{dc}$	+	$D3$, $D4$, and $S12$
j	$-2V_{dc}$	−	$Q3$, $Q4$ and $S12$

Unlike conventional topologies, the new structure can reduce the number of switches for single-phase multilevel inverters without affecting inverter performance since the zero state voltage can be generated using either the upper or the lower switches of the H-bridge inverter.

III. PROPOSED SINGLE-PHASE FIVE-LEVEL INVERTER

Two cascaded cells (n = 2) are required to generate five levels of the proposed inverter shown in Fig. 1. One cell has a dc supply controlled by two switches, and the other cell only has a dc supply.

Fig. 3 shows the configuration of the proposed single-phase five-level inverter. Two switches are added to the conventional single-phase H-bridge inverter to realize a single-phase five-level inverter. To achieve balanced output voltage levels, the dc voltage sources in both cells are typical: $V_1 = V_2 = V_{dc}$. The dc bus voltage V_{bus} comprises two states: (V_{dc} and $2V_{dc}$). The load output voltage V_{ab} comprises five states: ($2V_{dc}, V_{dc}, 0, -V_{dc},$ and $-2V_{dc}$). The zero state of the load voltage can be generated by simultaneously switching either the upper switches or the lower switches of the H-bridge inverter. The other four states can be generated from the dc bus voltage V_{bus}.

As the load current is bi-directional regardless of the load voltage, the operation of the proposed single-phase five- level inverter involves 10 switching states, as illustrated in Fig. 4 and Table I. The switching patterns of the proposed inverter are shown in Fig. 4, whereas the load current directions at each load voltage level state according to ON-OFF switch conditions are shown in Table I. The conventional freewheeling states (zero voltage states) are shown in Figs. 4 (e) and (f). The other output voltage levels + or − can be achieved by switching the conventional H-bridge inverter with the control of cell-1 switches (S_{11} and S_{12}). The PWM switching technique is required to control the single-phase five-level inverter and achieve the reference load voltage based on the 10 switching patterns shown in Fig. 4 and Table I.

IV. SWITCHING ALGORITHMS FOR THE PROPOSED PWM SWITCHING TECHNIQUES

Switching frequency and the ON-OFF terminal voltage of power semiconductor devices are the main factors that affect inverter power loss and harmonic contents. On the basis of these factors, two PWM switching techniques are proposed to control the single-phase five-level inverter. Switching loss and harmonic distortion are considered in both techniques by operating certain switches at high frequency and others at fundamental line frequency.

A. Technique-I

The first PWM switching technique proposed for the single-phase five-level inverter basically depends on the generation of gate signals by comparing rectified reference waveforms with two in-phase triangle carriers having the same frequency and peak-to-peak voltage but different offset voltages. Fig. 5 shows the switching patterns of the single-phase five-level inverter using PWM Technique-I. The intersection points between carrier A and carrier B with the reference waveform determine the inverter output voltage level. The first level of the inverter output voltage $\pm V_{dc}$ is generated at the intersection points of the reference voltage waveform and the lower carrier signal (carrier A), whereas the second level of the output voltage $\pm 2V_{dc}$ is generated at the intersection points of the reference voltage waveform and the upper carrier signal (carrier B). The positive half cycle of the reference voltage waveform is responsible for generating positive dc voltage levels (V_{dc} and $2V_{dc}$) in the output voltage, whereas the rectified half cycle is responsible for generating negative dc voltage levels ($-V_{dc}$ and $-2V_{dc}$). According to the reference voltage, the intersection of the reference waveform may occur with the lower carrier only resulting in a modulation index between 0 and 0.5 or with both carrier signals resulting in a modulation index between 0.5 and 1. Therefore, if the modulation index is less than or equal to 0.5, then the output voltage of the inverter comprises only three levels (V_{dc}, 0, and $-V_{dc}$). By contrast, if the modulation index is greater than 0.5, then the output voltage of the inverter comprises five levels ($2V_{dc}$, V_{dc}, 0, $-V_{dc}$, and

$-2V_{dc}$). According to the amplitude of the reference voltage, its period can be divided into five intervals based on four modes (Mode A, Mode B, Mode C, and Mode D). On the basis of the related displacement phase angles ($\theta_1,\ \theta_2, \theta_3,$ and θ_4) shown in Fig. 5, the operational modes can be defined as follows:

$$\left.\begin{array}{ll} Mode\ A & 0 < \omega t < \theta_1, \quad \theta_2 < \omega t \leq \pi \\ Mode\ B & \theta_1 < \omega t \leq \theta_2 \\ Mode\ C & \pi < \omega t < \theta_3, \quad \theta_4 < \omega t \leq 2\pi \\ Mode\ B & \theta_3 < \omega t \leq \theta_4 \end{array}\right\} \quad (1)$$

The modulation index (MI) of the proposed single-phase five-level inverter is defined as follows:

$$MI = \frac{A_M}{2A_C} \quad (2)$$

where A_M is the peak value of the reference modulating waveform and A_C is the peak-to-peak value of the carrier. The frequency ratio (m_f) is defined as follows:

$$m_f = \frac{f_c}{f_m} \quad (3)$$

where f_C is the frequency of the carrier signals and f_m is the frequency of the modulating signal.

Fig. 5 shows that the displacement phase angles ($\theta_1, \theta_2, \theta_3,$ and θ_4) are affected by MI. If MI is less than or equal 0.5, then the displacement phase angles are defined as follows:

$$\theta_1 = \theta_2 = \frac{\pi}{2}, \qquad \theta_3 = \theta_4 = \frac{3\pi}{2} \quad (4)$$

If MI is greater than 0.5, the displacement phase angles are defined as follows:

$$\left.\begin{array}{l} \theta_1 = sin^{-1}\left(\frac{A_C}{A_M}\right) \\ \theta_2 = \pi - \theta_1 \\ \theta_3 = \pi + \theta_1 \\ \theta_4 = 2\pi - \theta_1 \end{array}\right\} \quad (5)$$

According to the intersection between the modulation waveform and carrier signals, the period of the reference voltage (2π) is divided into six time intervals defined as ($P_1, P_2, P_3, P_4, P_5,$ and P_6), as shown in Fig. 5. The signals C_A and C_B, shown in Fig. 5 result from the comparison between the modulation waveform and the lower and upper triangle carriers, respectively. The gate signals of the proposed inverter switches can be calculated based on the resultant signals C_A and C_B in addition to the six time intervals ($P_1, P_2, P_3, P_4, P_5,$ and P_6). The resultant gate signals of the inverter six switches can be formulated as follows:

$$\left.\begin{array}{l} Q_1 = P_1 + P_2 + P_3 \\ Q_2 = \left((P_1 + P_2 + P_3)\,.\,C_A\right) + \left((P_4 + P_6)\cdot \overline{C_A}\right) \\ Q_3 = \left((P_1 + P_3)\cdot \overline{C_A}\right) + \left((P_4 + P_6 + P_5)\cdot C_A\right) \\ Q_4 = P_4 + P_5 + P_6 \\ S_{11} = \left(\left((P_1 + P_3) + (P_4 + P_6)\right)\cdot C_A\right) + \left((P_2 + P_5)\cdot \overline{C_B}\right) \\ S_{12} = (P_2 + P_5)\cdot C_B \end{array}\right\} \quad (6)$$

As shown in Equ. (6) and Fig. 5, the inverter power switches ($Q1$ and $Q4$) are complementary switches that operate at fundamental line frequency (i.e., 50 Hz). The power switches (S_{11} and S_{12}) cannot be switched ON simultaneously. However, their switching signals are determined based on the basis of Equ. (6) and operate at switching frequency. Moreover, the power switches (Q_2 and Q_3) are complementary switches that operate at switching frequency.

B. Technique-II

The second proposed technique presents a simple control of the single-phase five-level inverter. Technique-II uses only two switches operating at switching frequency and the other four switches operating at fundamental line frequency. Fig. 6 shows the switching patterns of the single-phase five-level inverter using PWM technique-II. This technique basically depends on the generation of gate signals by comparing the rectified reference waveform with two in-phase triangle carriers that feature the same frequency and zero offset voltage; however, the peak-to-peak voltage of carrier B is twice that of carrier A. The intersections between the reference voltage waveform and carrier A generate the first level ($\pm V_{dc}$) at the output of the inverter, whereas the intersections between the reference voltage waveform and carrier B generate the second level ($\pm 2V_{dc}$). Similar to technique-I, the zero voltage level at the inverter output can be generated using the upper or lower switches of the H-bridge. In addition, positive dc output voltage levels (V_{dc} and $2V_{dc}$) are generated by the positive half cycle of the reference waveform, whereas negative voltages ($-V_{dc}$ and $-2V_{dc}$) are generated by the rectified half cycle of the reference waveform. As the two carriers have zero offset voltage, the reference waveform has intersection points with both carriers simultaneously. However, MI is defined to be 0.5 at the peak voltage of carrier A. Therefore, if MI is less than or equal to 0.5, then the output voltage of the inverter comprises only three levels ($V_{dc}, 0,$ and $-V_{dc}$), similar to technique-1. Alternatively, if MI is greater than 0.5, then the output voltage of the inverter comprises five levels ($2V_{dc}$, $V_{dc}, 0, -V_{dc},$ and $2V_{dc}$), as shown in Fig. 6.

The results of the comparison of the reference waveform with carrier A and carrier B are shown in Fig. 6 as signals C_A and C_B, respectively. Similar to technique-I, period (2π) is divided into six time intervals ($P_1, P_2, P_3, P_4, P_5,$ and P_6) on the basis of the peak value of the reference voltage waveform, as shown in Fig. 6.

According to the resultant signals C_A and C_B, in addition to the six time intervals ($P_1, P_2, P_3, P_4, P_5,$ and P_6), the resultant gate signals of the inverter six switches can be formulated as follows:

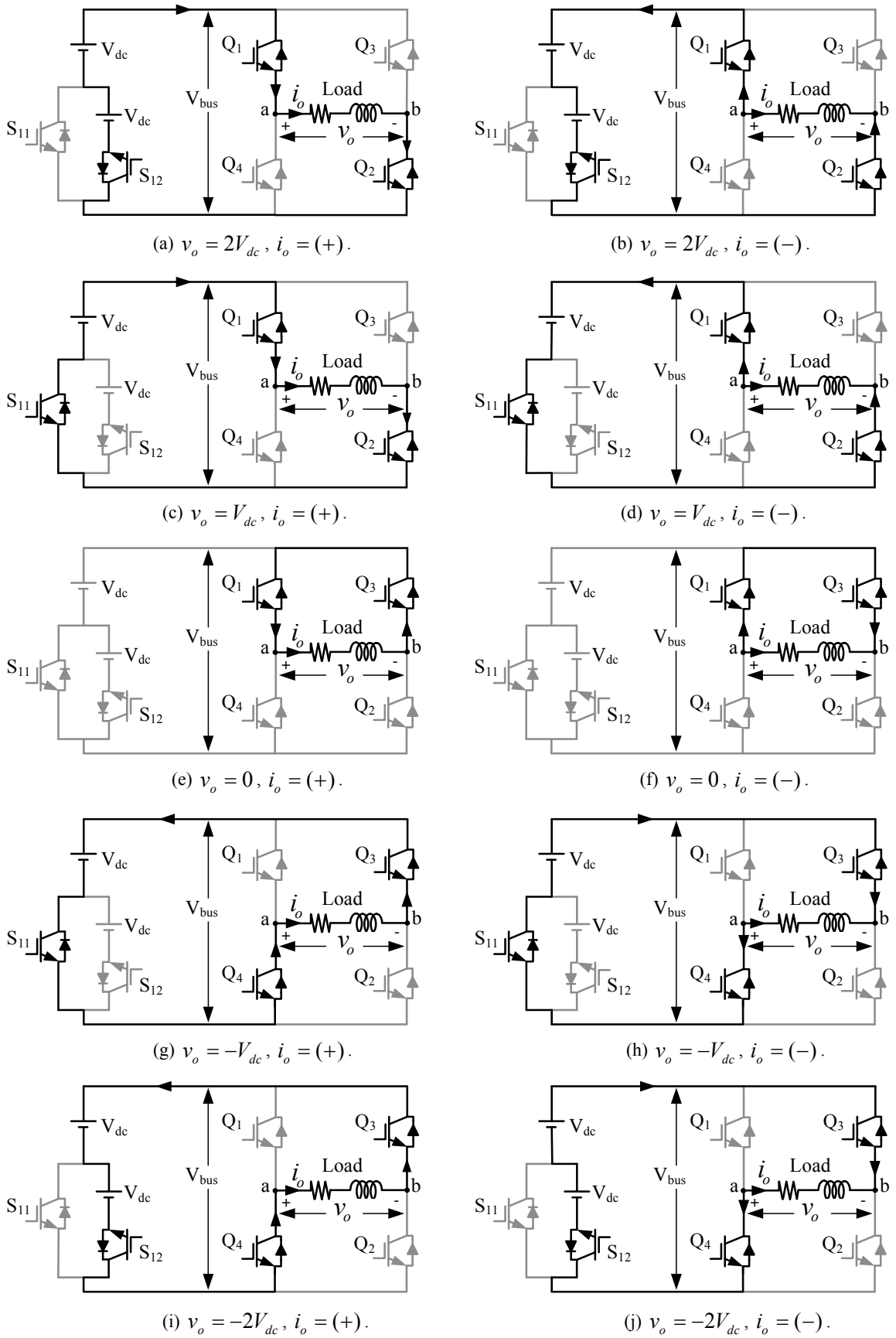


Fig. 4. Operational switching states of the proposed single-phase five-level inverter and the direction of load current.

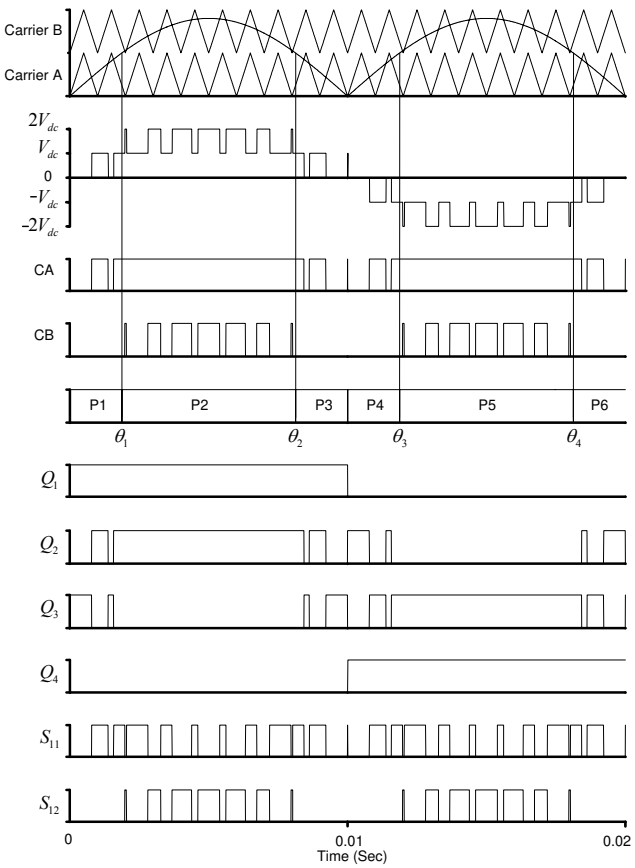


Fig. 5. Switching pattern of PWM technique-I for the proposed single-phase five-level inverter.

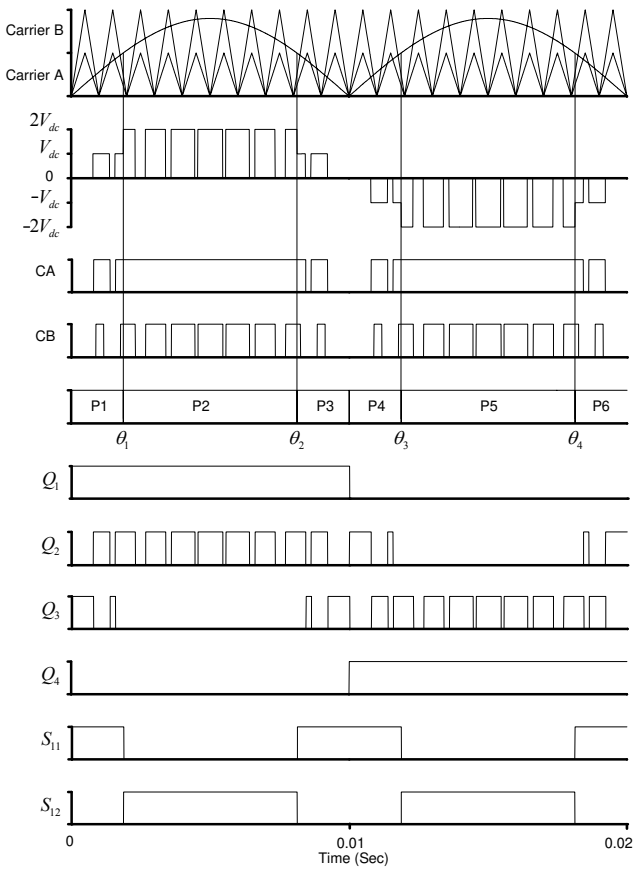


Fig. 6. Switching pattern of PWM technique-II for the proposed single-phase five-level inverter.

$$\left.\begin{aligned} Q_1 &= P_1 + P_2 + P_3 \\ Q_2 &= \Big(\big((P_1 + P_3)\cdot C_A\big) + (P_2 \cdot C_B)\Big) + \Big((P_4 + P_6)\cdot \overline{C_A}\Big) \\ Q_3 &= \Big(\big((P_4 + P_6)\cdot C_A\big) + (P_5 \cdot C_B)\Big) + \Big((P_1 + P_3)\cdot \overline{C_A}\Big) \\ Q_4 &= P_4 + P_5 + P_6 \\ S_{11} &= P_1 + P_3 + P_4 + P_6 \\ S_{12} &= P_2 + P_5 \end{aligned}\right\} \quad (7)$$

The switching pattern of Technique-II, shown in Fig. 6 indicates that the cell switches (S_{11} and S_{12}) are complementary and thus prevent short circuit on the dc voltage supply. Moreover, the switches operate at a double line frequency. Two switches of the H-bridge inverter ($Q_1$and Q_2) operate complementarily at line frequency. Therefore, Technique-II provides PWM switching for six power switches with only two switches operating at high frequency.

Therefore, the two PWM techniques provide output voltages with five levels. The voltage difference during switching of any power switch in Technique-I is V_{dc} at any time. By contrast, the inverter output voltage in Technique-I changes from zero to $2V_{dc}$ at the time interval period P_2 or from zero to $-2\,V_{dc}$ at period P_5. Hence, switching occurs at a higher voltage than that given by Technique-I. As a result, technique-II suffers from higher switching losses and harmonics compared with Technique-I.

V. Harmonic Analysis of the Proposed PWM Patterns

The harmonic components and total harmonic distortion (THD) of the output voltages in the proposed techniques are presented here. Fig. 5 shows that the output voltage waveforms of both techniques feature an odd quarter-wave symmetry ($a_n = 0$).

Therefore, the Fourier series of the waveforms for technique-I and technique-II can be expressed according to the following assumptions:

- M_1 and M_2 are the number of pulses resulting from the intersection of the modulating signal with carrier A and B, respectively.
- α_k and β_k , $(k = 1, 2, \ldots)$ are the start and end angles for pulses M_1 and M_2, respectively.

A. THD of Technique-I

The Fourier series of the inverter output voltage waveform based on Technique-I can be expressed as follows:

$$\mathrm{f(wt)} = \frac{4V_{dc}}{n\pi}\Big[\sum_{k=1}^{M_1}\sum_{n=1}^{\infty}(-1)^{k+1}\cos(n\alpha_k)\sin(n\omega t) + \sum_{k=1}^{M_2}\sum_{n=1}^{\infty}(-1)^{k+1}\cos(n\beta_k)\sin(n\omega t)\Big] \quad (8)$$

where

$$n = 1, 3, 5, \ldots$$

$$90° = \alpha_{M1} > \ldots > \alpha_3 > \alpha_2 > \alpha_1$$
$$90° = \beta_{M1} > \ldots > \beta_3 > \beta_2 > \beta_1$$

The fundamental frequency amplitude at n = 1 is formulated as follows:

$$B_1 = \frac{4}{\pi}\sum_{k=1}^{M_1}(-1)^{k+1}\cos(\alpha_k) + \frac{4}{\pi}\sum_{k=1}^{M_2}(-1)^{k+1}\cos(\beta_k) \quad (9)$$

Therefore, the THD of the output voltage waveform can be formulated as follows:

$$THD = \frac{4}{\pi B_1}\left(\sum_{n=3}^{\infty}\left(\frac{1}{n}\right)\left[\sum_{k=1}^{M_1}(-1)^{k+1}\cos(n\alpha_k) + \sum_{k=1}^{M_2}(-1)^{k+1}\cos(n\beta_k)\right]^2\right)^{0.5} \quad (10)$$

where n is odd orders (n = 3, 5,…).

B. THD of Technique-II

The Fourier series of the inverter output voltage waveform based on Technique-II can be expressed as follows:

$$f(wt) = \frac{4V_{dc}}{n\pi}\left[\sum_{k=1}^{M_1}\sum_{n=1}^{\infty}(-1)^{k+1}\cos(n\alpha_k)\sin(n\omega t) + 2\sum_{k=1}^{M_2}\sum_{n=1}^{\infty}(-1)^{k+1}\cos(n\beta_k)\sin(n\omega t)\right] \quad (11)$$

The fundamental frequency amplitude at n = 1 is formulated as follows:

$$B_1 = \frac{4}{\pi}\sum_{k=1}^{M_1}\cos(\alpha_k) + \frac{8}{\pi}\sum_{k=1}^{M_2}\cos(\beta_k) \quad (12)$$

where

$$n = 1,3,5,\ldots$$
$$90° = \alpha M\,1 > \ldots > \alpha 3 > \alpha 2 > \alpha 1$$
$$90° = \beta M\,1 > \ldots > \beta 3 > \beta 2 > \beta 1$$

Therefore, the THD of the output voltage waveform can be formulated as follows:

$$THD = \frac{4}{\pi B_1}\left(\sum_{n=3}^{\infty}\left(\frac{1}{n}\right)\left[\sum_{k=1}^{M_1}(-1)^{k+1}\cos(n\alpha_k) + 2\sum_{k=1}^{M_2}(-1)^{k+1}\cos(n\beta_k)\right]^2\right)^{0.5} \quad (13)$$

where n is odd orders (n=3, 5,. . .)

By using (10) and (13), the THD of the proposed PWM techniques is calculated and then compared with the simulation and experimental results.

VI. Control Scheme

The single-phase five-level inverter employing an LC filter is applied to control the voltage at a resistive load. Fig. 7 shows the control scheme of the single-phase five-level inverter for regulating the resistive load voltage (v_L). A simple LC filter is used to obtain a sinusoidal voltage waveform at the load. Given that the inverter output voltage has five levels, the parameters of the LC filter are smaller than those used in conventional three-level inverters.

The implemented control scheme shown in Fig. 7 is used to investigate the ability of the proposed PWM techniques (Technique-I and Technique-II) to drive the single-phase five-level inverter. A conventional PI controller is used to regulate the load voltage to be the same as the sinusoidal reference voltage (v_L^*), as shown in Fig. 7. Therefore, the actual load voltage (v_L) is compared with the reference voltage (v_L^*), and the error is minimized using the PI controller. MI is the output of the PI controller. Moreover, MI is compared with the two carriers in each technique to generate pulses ($C_A, C_B, P_1, P_2, P_3, P_4, P_5,$ and P_6). Then, Equs. (6) and (7) are used to generate inverter switch pulses for technique-I and technique-II, respectively.

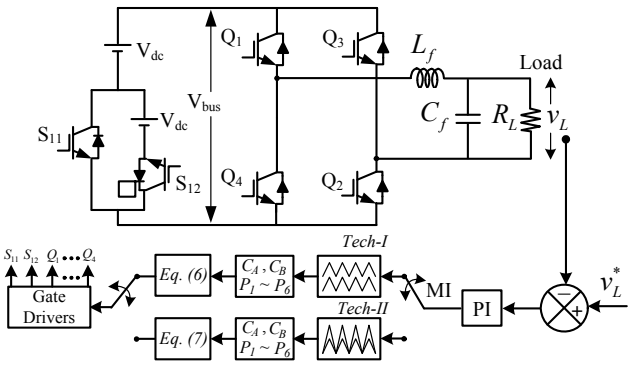


Fig. 7. Proposed control technique of the single-phase five-level inverter.

VII. Simulation Results

The single-phase five-level inverter and the two proposed PWM switching techniques are implemented using Matlab/Simulink to verify the validity of the topology. The simulated system is controlled using a conventional PI controller as shown in Fig. 7. Ideal power switches are used to simulate the inverter circuit. The parameters of the simulated system are shown in Table II. Based on MI, the inverter output voltage can have three or five levels. Low and high MI values are used to verify the validity of the proposed two PWM techniques in controlling the load voltage. The reference load voltage (v_L^*) is set to 43 V (RMS) with MI of about 0.4 to investigate the three-level output voltage, whereas (v_L^*) is set to 100 V (RMS) with MI of about 0.9 to investigate the five-level output voltage.

A. Simulation Results Using Technique-I

Fig. 8 shows the simulation results of the inverter output voltage (v_{inv}), actual and reference load voltage (v_L, v_L^*), and load current (i_L) for the three-level output voltage control. The inverter output voltage clearly comprises only three levels of (0, ±80). In addition, the reference and actual load voltages coincide well. The load voltage and current are sinusoidal waveforms with low ripples. Fig. 9 shows the simulation results of the five-level output voltage when controlled to be equal to 141 V (RMS). The inverter output voltage clearly comprises five levels of (0, ±80, and ±160), and the reference and actual load voltages appear identical. Moreover, the ripples in the sinusoidal waveforms of the load

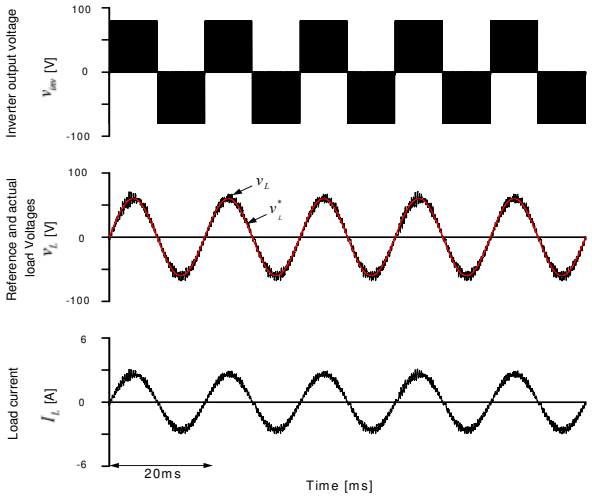


Fig. 8. Simulation results of the single-phase five-level inverter at $v_L^* = 42.4$ V (RMS) using PWM technique-I.

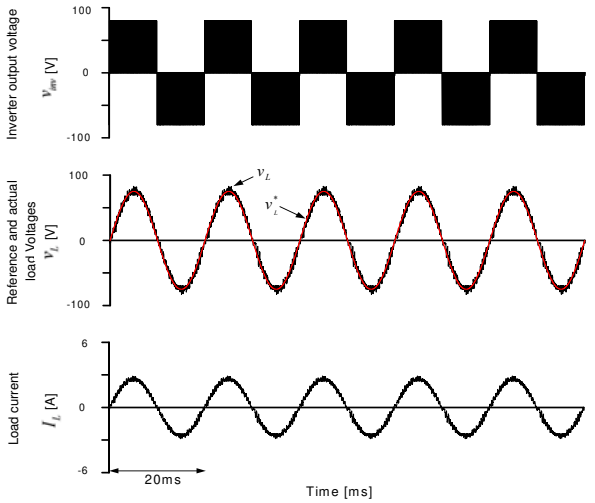


Fig. 10. Simulation results of the single-phase five-level inverter at $v_L^* = 42.4$ V (RMS) using PWM technique-II.

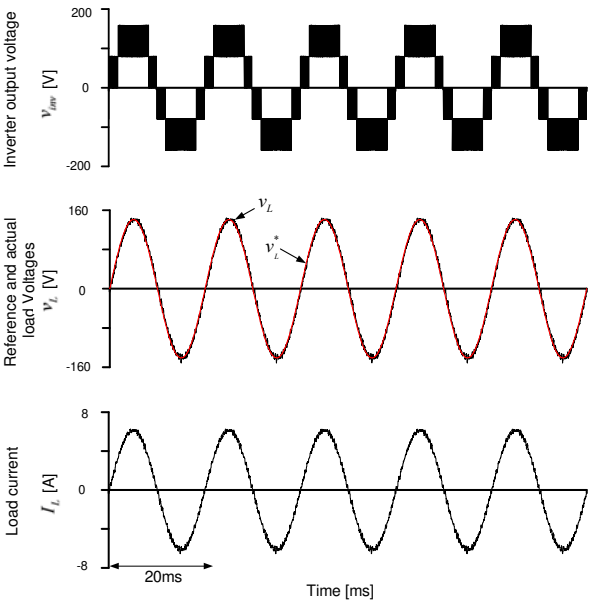


Fig. 9. Simulation results of the single-phase five-level inverter at $v_L^* = 100$ V (RMS) using PWM technique-I.

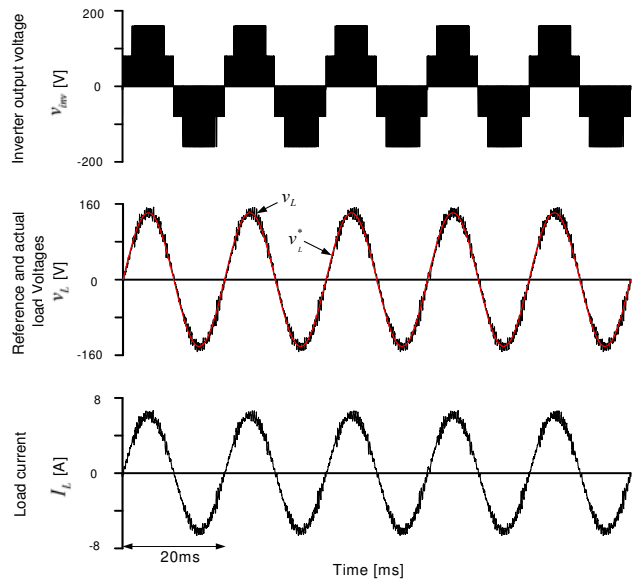


Fig. 11. Simulation results of the single-phase five-level inverter at $v_L^* = 100$ V (RMS) using PWM technique-II.

voltages and currents are reduced because of the increase in the inverter output voltage levels.

B. Simulation Results Using Technique-II

Figs. 10 and 11 show the simulation results of the system when the reference load voltage is set to 43 V (RMS) and 100 V (RMS), respectively, using PWM technique-II. Both figures show that the reference and actual load voltages agree well and that the sinusoidal waveforms of the load voltage and current exhibit low ripples. The inverter output voltage shown in Fig. 10 comprises only three levels of (0, ±80) because *MI* is less than 0.5, whereas the inverter output voltage in Fig. 11 comprises five levels of (0, ±80, and ±160) because *MI* is greater than 0.5.

The three-level output voltage obtained using PWM

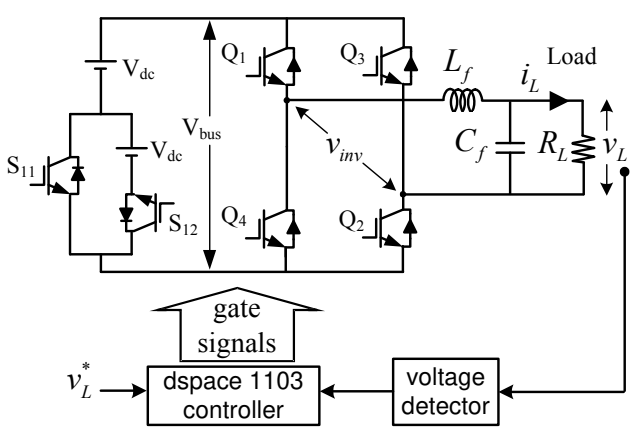


Fig. 12. Experimental system configuration.

technique-II is similar to that obtained using PWM technique-I, given that the power switches are ideal. However, the ripples of the load voltage and currents in Fig. 11 are higher than those obtained from the other cases because the five levels obtained using PWM technique-II are always a step from zero. This condition in turn increases load voltage harmonics and voltage stress on power switches.

VIII. Experimental Results

Laboratory prototype systems have been carried out to demonstrate the effectiveness of the single-phase five-level inverter in controlling the load voltage. The proposed PWM techniques are used to confirm their capability of driving the inverter. The experimental waveforms of the load currents, load voltages, and inverter output voltages for both techniques are captured. The harmonic components and THDs for both techniques are also measured and compared with theoretical values to demonstrate the accuracy of the experimental system and the proposed control schemes.

A. Experimental System Configuration

Fig. 12 shows the laboratory prototype of the single-phase five-level inverter with its two dc supplies in the input, LC filter at the output, resistive load, and digital controller. Fig. 13 shows a photo of the laboratory prototype system. The dspace 1103 is selected as the controller for the single-phase five-level inverter. This inverter is built with MOSFET IRFP31N50L as the power device. The switching frequency for inverters is 10 kHz. The parameters of the whole system are listed in Table II. The captured experimental waveforms of the inverter output voltage, in addition to the load voltage and current, are measured using Tektronic MSO2000 oscilloscope. The efficiency of the inverter and the harmonic components of the inverter output are measured using a Yokogawa digital power analyzer WT1800. The main function of the single-phase five-level inverter employing an LC filter is to control the load voltage (v_L) to be the same as the reference sinusoidal voltage (v_L^*) using a conventional PI control technique. Therefore, only one voltage sensor is needed to detect the actual load voltage, which is compared with the reference voltage inside the controller to obtain all the switch gate signals based on the generated *MI* and two carriers.

Technique-I and technique-II are used to control the single-phase five-level inverter to demonstrate their effectiveness in controlling the load voltage and investigate their power quality. In each technique, two different voltage levels are confirmed to examine inverter behavior at different modulation indices. The reference load voltage is adjusted to 43 V (RMS) and 100 V (RMS) with *MI* of 0.4 and 0.9, respectively. At *MI* of 0.4 (less than 0.5), the behavior of the inverter is similar to that of a conventional full-bridge three-level inverter, whereas at *MI* of 0.8 (greater than 0.5), the inverter output voltage comprises five levels.

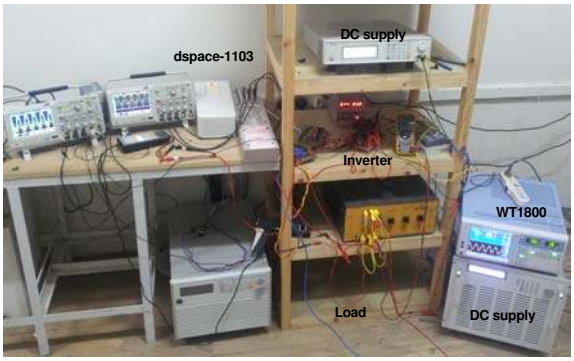


Fig. 13. Experimental system prototype.

TABLE II
Simulation and Experimental System Parameters

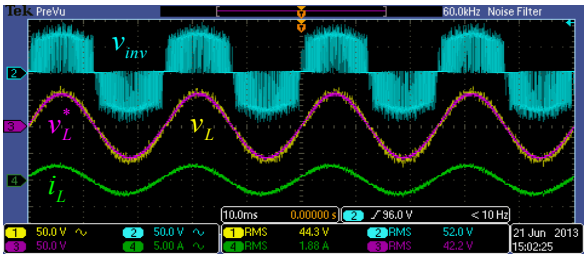
Source voltage V_{inv}	80 V
Load R_L	23 Ω
Filter L_f	1.0 mH
C_f	470 μF
Switching time T_s	100 μs
Main PI gains K_P, K_I	0.01 A/V, 0.005 A/V.s

B. Load Voltage Control Using Technique-I

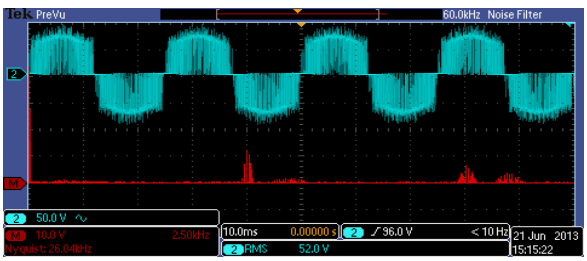
The laboratory prototype shown in Fig. 12 is implemented using PWM technique-I to control the single-phase five-level inverter that supplies an AC resistive load. Fig. 14 shows the experimental results of the system given a load reference voltage of 43 V (RMS) with *MI* of about 0.4 and the inverter output voltage with three levels. Fig. 14(a) shows the inverter output voltage (v_{inv}), reference and actual load voltages (v_L^*, v_L), and load current (i_L). The reference and actual load voltages appear identical.

Figs. 14(b) and (c) show the inverter output voltage and load voltage after the LC filter, with their fast Fourier transform (FFT) showing their harmonic contents. The LC filter clearly removes the harmonics of the inverter output voltage and provides the load with a sinusoidal voltage waveform. The THDs of the inverter output voltage and load voltage are 75.1% and 5.9%, respectively. Fig. 14(d) shows the power analyzer results of the load voltage, current, and inverter voltage in addition to system efficiency. The efficiency of the system is 77.9%. Fig. 15 shows the experimental results of the system for a load reference voltage of 100 V (RMS) with *MI* of about 0.9 and the inverter output voltage with five levels.

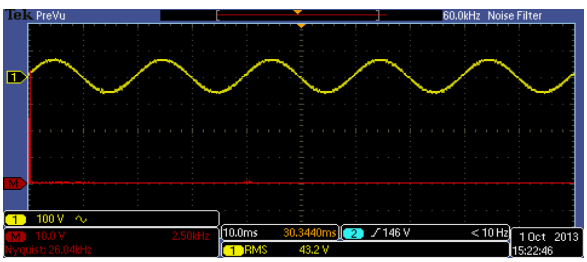
The actual load voltage clearly coincides with the reference voltage. The harmonic components of the inverter output voltage shown in Fig. 15(b) are less than those shown in Fig. 14(b) because of the increase in the output voltage levels (target operation). The THDs of the inverter output voltage and load voltage are 39.6% and 3%, respectively. Moreover,



(a) Inverter voltage, reference and actual load voltage, and load current.



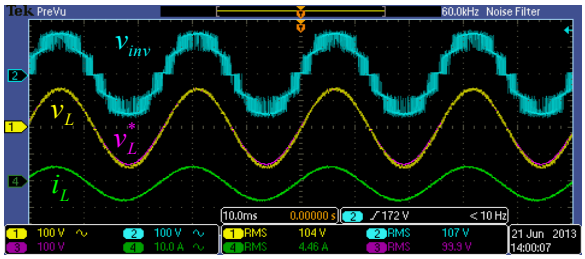
(b) Inverter voltage and harmonic distortion FFT.



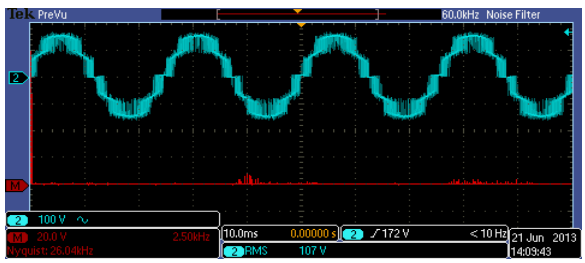
(c) Load voltage and harmonic distortion FFT.

(d) Inverter and load waveforms with system efficiency.

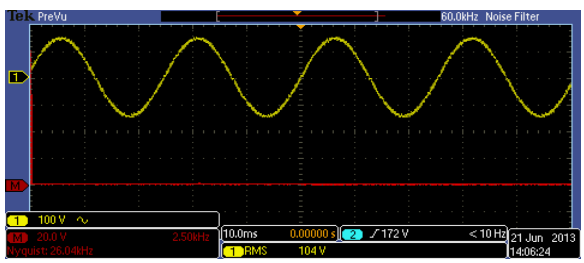
Fig. 14. Experimental results of the single-phase five-level inverter at $v_L^* = 42.4$ V (RMS) using PWM technique-I.



(a) Inverter voltage, reference and actual load voltage, and load current.



(b) Inverter voltage and harmonic distortion FFT.



(c) Load voltage and harmonic distortion FFT.

(d) Inverter and load waveforms with system efficiency.

Fig. 15. Experimental results of the single-phase five-level inverter at $v_L^* = 100$ V (RMS) using PWM technique-I.

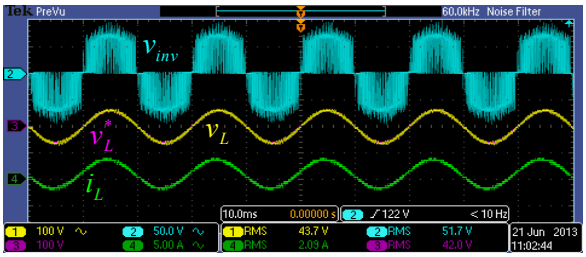
the efficiency of the system operating at the five-level mode is higher than that operating in the three-level mode because of harmonic reduction. The measured efficiency of the system is 90.7%.

C. Load Voltage Control Using Technique-II

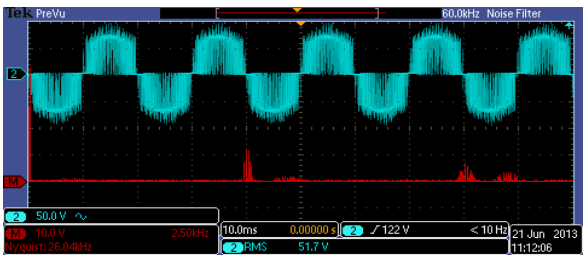
The laboratory prototype is implemented to investigate the effectiveness of the proposed PWM technique-II under the same conditions of technique-I.

The reference voltage is adjusted using the same two voltages used in technique-I (43 and 100 V) to compare the power quality of the proposed techniques.

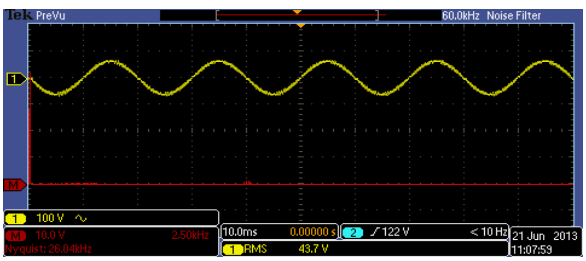
Fig. 16 shows the experimental results of the single-phase five-level inverter controlled with PWM technique-II to control the AC load voltage to 43 V (RMS) with *MI* of less than 0.5. The reference and actual load voltages coincide well, as shown in Fig. 16 (a). The harmonic contents of the inverter output voltage and load voltage using FFT are shown in Figs. 16(b) and (c). The THDs of the inverter output voltage and load voltage are 74.4% and 5.6%, respectively. System efficiency is measured using a digital power analyzer, as shown in Fig. 16(d). System efficiency is 78.5%.



(a) Inverter voltage, reference and actual load voltage, and load current.



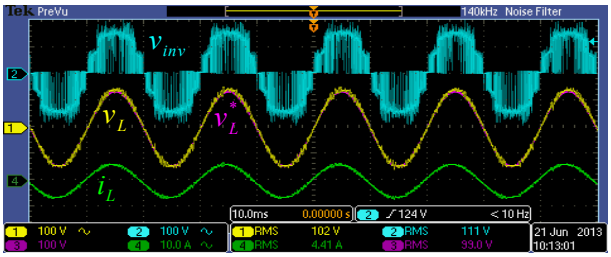
(b) Inverter voltage and harmonic distortion FFT.



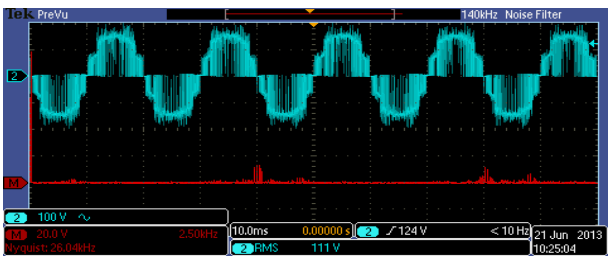
(c) Load voltage and harmonic distortion FFT.

(d) Inverter and load waveforms with system efficiency.

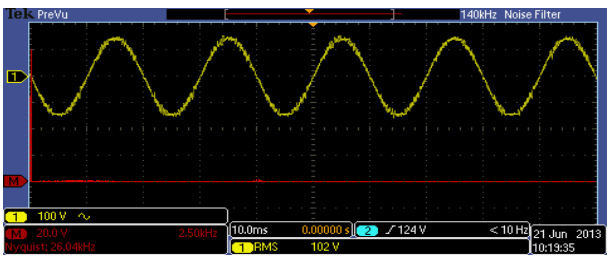
Fig. 16. Experimental results of the single-phase five-level inverter at $v_L^* = 42.4$ V (RMS) using PWM technique-II.



(a) Inverter voltage, reference and actual load voltage, and load current.



(b) Inverter voltage and harmonic distortion FFT.



(c) Load voltage and harmonic distortion FFT.

(d) Inverter and load waveforms with system efficiency.

Fig. 17. Experimental results of the single-phase five-level inverter at $v_L^* = 100$ V (RMS) using PWM technique-II.

Fig. 17 shows the experimental results of the system using PWM technique-II with a load reference voltage of 100 V (RMS) and MI ($0.5 < MI \leq 1$). The actual load voltage clearly coincides with the reference voltage. The inverter voltage level is changed from 0 to $\pm Vdc$ during the intersection between the modulation waveform and carrier A and from 0 to $\pm 2Vdc$ during the intersection with carrier B. As a result of the increase in voltage levels to five, the harmonic components of the inverter output voltage shown in Fig. 17(b) are less than those shown in Fig. 16(b). Fig. 17(c) shows the load voltage harmonics. The THDs of the inverter output voltage and load voltage are 52% and 3.6%, respectively. Moreover, system efficiency under the five-level mode is higher than that under the three-level mode because of harmonic reduction. The efficiency of the system is 88.3%.

Fig. 18 shows a comparison of the simulation and experimental results of the THD of the inverter output voltage V_{inv} controlled with PWM technique-I with the variation of MI.

Fig. 19 shows the same comparison but for the case in which the THD is controlled with PWM technique-II. Both techniques exhibit almost the same THDs when MI is less than 0.5 ($0.0 < MI \leq 0.5$) because the inverter output

voltages are almost the same, that is, they both have the conventional three levels. However, when MI is higher than 0.5 ($MI > 0.5$), the THD of the inverter output voltage controlled with PWM technique-I is less than that obtained with PWM technique-II. This difference is due to the consistent change in the inverter voltage controlled by technique-II during the switching process from 0 V to $\pm V_{dc}$ or $\pm 2V_{dc}$; by contrast, in technique-I, the inverter voltage changes from 0 V to $\pm V_{dc}$ and from $\pm V_{dc}$ to $\pm 2V_{dc}$.

Fig. 20 shows a comparison of system efficiencies using the proposed PWM techniques. System efficiency under technique-II is slightly higher than that under technique-I when MI is less than 0.5 ($0.0 < MI \leq 0.5$) because technique-II only has two high frequency switches, whereas technique-I uses four switches operating at high frequency. The difference in efficiency is not significant because of the small current flowing in the switches. However, the difference in the efficiencies of the two techniques is noticeable when MI is higher than 0.5 ($MI > 0.5$) because of the high current flowing in the switches. System efficiency under technique-I is clearly higher than that under technique-II when MI is higher than 0.5 ($MI > 0.5$), although technique-II uses only two high frequency switches. This result can be explained as follows. The reduction in switching loss in technique-II as a result of the few high frequency switches used is less than the increase in the switching loss caused by switching at a high voltage difference (from 0 V to $\pm 2V_{dc}$), in addition to the losses caused by increased harmonics. As indicated by the experimental results on the efficiency and THD of the single-phase five-level inverter system, using PWM technique-II is better than using PWM technique-I when ($0.0 < MI \leq 0.5$), whereas using PWM technique-I is better than using PWM technique-II when ($MI > 0.5$).

IX. Conclusion

This paper presents two control schemes for controlling a single-phase five-level dc-ac inverter. The THD and efficiency of the inverter are the key points in designing PWM switching techniques. PWM technique-I uses only four switches operating at switching frequency and two switches operating at fundamental line frequency. PWM technique-II uses only two switches operating at switching frequency, two switches operating at double line frequency, and two switches operating at line frequency.

The effectiveness of the proposed PWM techniques is verified theoretically and experimentally using laboratory prototypes. The experimental results prove that both techniques have the ability to control inverter output voltage such that it matches the reference voltage. The experimental results of the THD show good agreement with the theoretical results. The efficiency of the inverter and the THD of its output voltage vary with MI depending on the reference output voltage. Technique-II is preferable when ($MI \leq 0.5$) because of its high efficiency, whereas PWM technique-I is preferable when ($MI > 0.5$) because of its high efficiency and low THD.

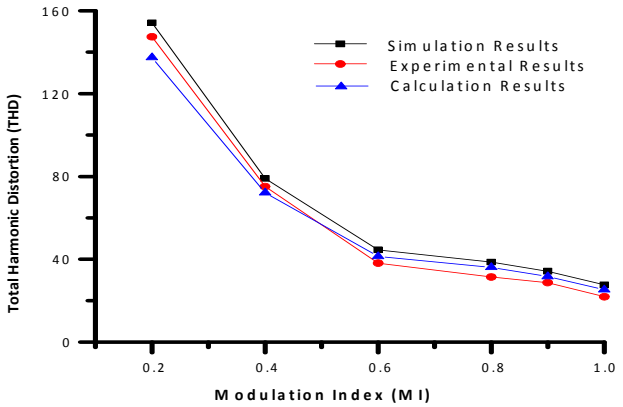


Fig. 18. Comparison of simulation and experimental results of the THD of the inverter using PWM technique-I.

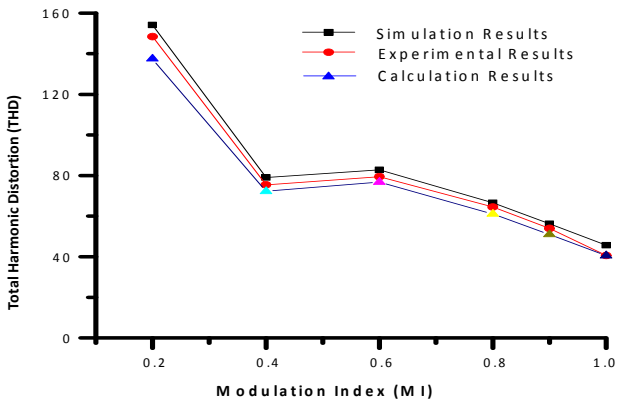


Fig. 19. Comparison of the simulation and experimental results of the THD of the inverter using PWM technique-II.

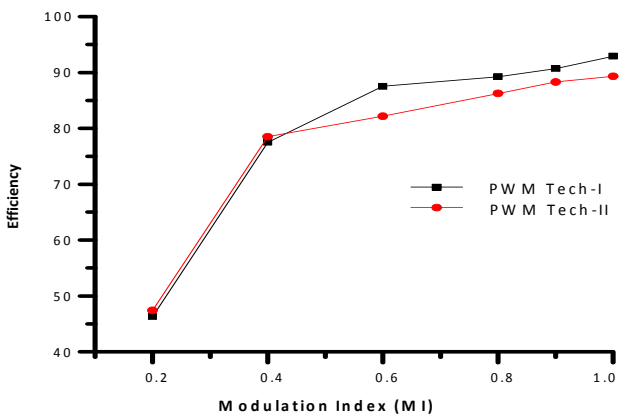


Fig. 20. Efficiency of the system using both PWM techniques.

Acknowledgment

This work is sponsored in part by the Egyptian Science and Technology Development Funds (STDF). Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the funding agencies.

REFERENCES

[1] P. Chan, H.-H. Chung, and S. Hui, "A generalized theory of boundary control for a single-phase multilevel inverter using second-order switching surface," *IEEE Trans. Power Electron.*, Vol. 24, No. 10, pp. 2298-2313, Oct. 2009.

[2] Y.-H. Liao and C.-M. Lai, "Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources," *IEEE Trans. Power Electron.*, Vol. 26, No. 9, pp. 2386-2392, Sep. 2011.

[3] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 4, pp. 724-738, Aug. 2002.

[4] J. Wen and K. Smedley, "Synthesis of multilevel convertersbased on single- and/or three-phase converter building blocks," *IEEE Trans. Power Electron.*, Vol. 23, No. 3, pp. 1247-1256, May 2008.

[5] I. Pharne and Y. Bhosale, "A review on multilevel inverter topology," in *International Conference on Power, Energy and Control (ICPEC)*, pp. 700-703.

[6] J.-S. Lai and F. Z. Peng, "Multilevel converters – A new breed of power converters," in *IEEE Thirtieth IAS Annual Meeting, IAS '95*., Vol.3.pp. 2348- 2356.

[7] S. Sirisukprasert, J.-S. Lai, and T.-H. Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 4, pp. 875-881, Aug. 2002.

[8] P. Rodriguez, M. Bellar, R. Munoz-Aguilar, S. Busquets-Monge, and F. Blaabjerg, "Multilevel-clamped multilevel converters (mlc2)," *IEEE Trans. Power Electron.*, Vol. 27, No. 3, pp. 1055-1060, Mar. 2012.

[9] F. Zare and G. Ledwich, "A hysteresis current control for single-phase multilevel voltage source inverters: PLD implementation," *IEEE Trans. Power Electron.*, Vol. 17, No. 5, pp. 731-738, Sep. 2002.

[10] X. Zhang and J. Spencer, "Study of multisampled multilevel inverters to improve control performance," *IEEE Trans. Power Electron.*, Vol. 27, No. 11, pp. 4409-4416, Nov. 2012.

[11] J. Salmon, A. Knight, and J. Ewanchuk, "Single-phase multilevel PWM inverter topologies using coupled inductors," *IEEE Trans. Power Electron.*, Vol. 24, No. 5, pp. 1259-1266, May 2009.

[12] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, Vol. IA-17, No. 5, pp. 518-523, Sep. 1981.

[13] B. McGrath and D. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 4, pp. 858- 867, Aug. 2002.

[14] S. Priyan and K. Ramani, "Implementation of closed loop system for flying capacitor multilevel inverter with stand-alone photovoltaic input," in *International Conference on Power, Energy and Control (ICPEC)*, pp. 281-286, 2013.

[15] K. Corzine and X. Kou, "Capacitor voltage balancing in full binary combination schema flying capacitor multilevel inverters," *IEEE Power Electronics Letters*, Vol. 1, No. 1, pp. 2-5, Mar. 2003.

[16] X. Kou, K. Corzine, and Y. Familiant, "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, Vol. 19, No. 4, pp. 979-987, Jul. 2004.

[17] H. Liu, L. Tolbert, S. Khomfoi, B. Ozpineci, and Z. Du, "Hybrid cascaded multilevel inverter with PWM control method," in *IEEE Power Electronics Specialists Conference, PESC 2008*, pp. 162-166, 2008.

[18] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 11, pp. 4399-4406, Nov. 2009.

[19] S. Mekhilef and M. Kadir, "Novel vector control method for three-stage hybrid cascaded multilevel inverter," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 4, pp. 1339-1349, Apr. 2011.

[20] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel dc voltage sources," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2643-2650, Aug. 2010.

[21] V. Agelidis, D. Baker, W. Lawrance, and C. V. Nayar, "A multilevel PWM inverter topology for photovoltaic applications," in *IEEE International Symposium on Industrial Electronics, ISIE '97.*, Vol. 2, pp. 589-594, 1997.

[22] S.-J. Park, F.-S. Kang, M. H. Lee, and C.-U. Kim, "A new single-phase five-level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron.*, Vol. 18, No. 3, pp. 831-843, May 2003.

[23] G.-J. Su, "Multilevel DC-link inverter," *IEEE Trans. Ind. Appl.*, Vol. 41, No. 3, pp. 848-854, May/Jun. 2005.

[24] Z. Li, P. Wang, Y. Li, and F. Gao, "A novel single-phase five-level inverter with coupled inductors," *IEEE Trans. Power Electron.*, Vol. 27, No. 6, pp. 2716-2725, Jun. 2012.

[25] K. Gupta and S. Jain, "Multilevel inverter topology based on series connected switched sources," *IET Power Electron.*, Vol. 6, No. 1, pp. 164-174, Jan. 2013.

[26] E. Beser, B. Arifoglu, S. Camur, and E. Beser, "A novel topology for single-phase five-level inverter," in *5th WSEAS/IASME conference on electric power systems*, pp. 314-319.

[27] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, Vol. 23, No. 6, pp. 2657- 2664, Nov. 2008.

[28] M. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, Vol. 28, Vol. 2, pp. 625-636, Feb. 2013.

[29] M. Ahmed, M. Elsheikh, M. Sayed, and M. Orabi, "Single-phase five-level inverter with less number of power elements for grid connection," in *Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1521-1527, 2012.

Mahmoud A. Sayed was born in Qena Prefecture, Egypt, in 1974. He received his B.Sc. and M.Sc. degrees in Electrical Engineering from Minia University, El-Minia, Egypt, in 1997 and 2001, respectively, and his Ph.D. degree from the Nagoya Institute of Technology, Nagoya, Japan, in 2010. Since 1999, he has been with the Department of Electrical Engineering, Faculty of Energy Engineering, Aswan University, Aswan, Egypt, first as an Administrator and then as a Research Assistant starting in 2001. Currently, he is an Associate Professor in the Department of Electrical Engineering, Faculty of Engineering, South Valley University, Qena, Egypt. His research interests include series and shunt compensation of electrical distribution systems for voltage regulation and loss reduction using series and shunt PWM converters, as well as PWM switching techniques of the direct

ac-ac matrix converter for three-phase and multiphase applications, in addition to renewable energy applications and machine drives. Dr. Sayed is a member of the IEEE Power Electronics Society.

Mahrous Ahmed was born in Sohag, Egypt. He received his B.S. and M.Sc. degrees in Electrical Engineering from Assiut University, Assiut, Egypt, in 1996 and 2000, respectively, and his Ph.D. degree in Electrical Engineering from University of Malaya, Kuala Lumpur, Malaysia, in 2007. Since 2007, he has been an Assistant Professor in the Aswan Faculty of Engineering, Aswan University, Aswan, Egypt. In 2008, he joined Aswan Power Electronics Applications Research Center, where he participated in five research projects in power electronic and renewable energy applications. Currently, he is an Associate Professor in the Faculty of Engineering, Taif University, KSA. His research interests include power conversion techniques and real-time control systems.

Maha G. Elsheikh was born in Aswan, Egypt. She received her B.S. and M.S. degrees in Electrical Engineering from Aswan University. She currently works as an Assistant Researcher at Aswan Power Electronics Applications Research Center (APEARC), Aswan University. She has several publications in international conferences. Her research interests include power electronics, multilevel inverters, PWM techniques, control of power converters, and renewable energy applications.

Mohamed Orabi received his Ph.D. degree from Kyushu University, Fukuoka, Japan, in 2004. He is currently a Professor in the Department of Electrical Engineering, Faculty of Engineering, Aswan University, Aswan, Egypt. He is the Founder and the Director of the Aswan Power Electronics Application Research Center (APEARC), Aswan University. From June 2011 to July 2014, he was with Enpirion Inc. and Altera Corp. as the Senior Manager of the Altera-Egypt Technology Center. His research interests are power electronics applications, including switched power supply dc–dc and ac–dc power-factor-correction converters, integrated power management, the modeling and analysis of nonlinear circuits, and power converter design and analysis for renewable energy applications. Dr. Orabi is an Associate Editor of the IET Power Electronics Journal. He is an Editorial Board member of the "Electric Power Components and Systems Journal (EPCE), Taylor & Francis" and the "Advances in Power Electronics Journal," and he previously served as an Editorial Board member of the "International Journal on Advanced Electrical Engineering." Dr. Orabi was the recipient of the 2002 Excellent Student Award of the IEEE Fukuoka Section, the Best Paper Award of the 28th Annual Conference of the IEEE IES (2002), the IEEE-IES Student Grant from the 2003 IEEE International Symposium on Industrial Electronics, and the Best Young Research Award from the IEICE Society, Japan, in 2004. he also received the South Valley University Encouragement Award in 2009 and the National Encouragement Award in 2010 for his great achievements in engineering science.