Quasi-2D Compact Modeling for Double-Gate MOSFET

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ABSTRACT

This paper presents an approach to model the characteristics of undoped Double-Gate MOSFETs without relying on the charge-sheet approximation. Due to the extremely thin silicon film used, the inversion charge thickness becomes comparable to the silicon film thickness and cannot be ignored. Together with volume inversion and quantum effect, the carriers are distributed along the vertical direction perpendicular to the direction of current flow. Therefore, a 2-D modeling approach considering vertical current distribution and lateral carrier transport is required. To simplify the 2-D problem, the quasi-Fermi potential has been taken as a reference to develop a quasi 2-D DG MOSFET model.

Keywords: CMOS Device, Double-gate MOSFET, Circuit Simulation, Device model, SPICE, BSIM

1 INTRODUCTION

Double-gate (DG) MOSFETs have been a topic of interest recently due to its scalability beyond the limit of convention technology in the sub-50nm gate length [1]. The short-channel effect (SCE) of DG MOSFET is controlled by the thin silicon film that enables strong gate coupling to the channel and elimination of sub-surface leakage paths. The physics that govern the operation of DG MOSFETs, however, also become more complicated. A number of effects that are considered as secondary become dominant in DG MOSFETs. Traditional approaches in MOSFET modeling usually based on charge-sheet approximation [2] to simplify the current expression in different bias regions. This approach ignores the vertical carrier distribution, which maybe valid in bulk MOSFETs, cannot fully account for the behaviors observed in DG MOSFETs such as volume inversion and quantum confinement by the dielectric barriers. A more rigorous 2-D approach that includes the vertical carrier distribution and lateral transports is required to predict the characteristics of DG MOSFETs.

As a full 2-D modeling of DG MOSFET is extremely difficult, we proposed a quasi-2D framework to model the performance of DG MOSFETs. The model is based on the exaction solution of Poisson's equation along the vertical direction. Quantum effects are included based on the result of 2-D quantum simulation using a self-consistence Schrodinger and Poisson solver taking wavefunction penetration into account. The model has been verified with extensive 2-D/3-D device simulations and limited device data available.

2 MODELING STRATEGY

A flexible DG MOSFET model should be able to handle different mode of operations, including symmetric DG (SDG) MOSFETs and asymmetric DG (ADG) MOSFETs. The ADG mode also includes a wide range of devices such as ground plate MOSFETs and ultra-thin-body (UTB) MOSFETs. To simplify the 2-D modeling, we assumed that the quasi-Fermi level along the vertical direction (or x) remains constant. This assumption implies that the current only flows in the lateral (or y) direction and no carrier exchange in the x direction. That is the current density at any location (x, y) is given by.

$$J(x,y) = J(x) \tag{1}$$

Under this assumption, a generic expression for current can be obtained [3] as given below:

$$I_{DS} = \frac{\mu_{eff} W_{eff}}{L_{eff}} C_{ox} \left(\frac{kT}{q}\right)^2 \left[\frac{Q_S^2 - Q_D^2}{2} + (Q_S - Q_D)\right] \tag{2}$$

Expression in (2) is a very powerful expression because it implies that as long as the source charge and drain charge are know, the I-V expression can be obtained easily. The same expression applied to SDG, ADG and ground plane MOSFETs. The next task in the model formulation is then to find the source/drain charge, and the mobility.

3 GENERIC CHARGE FORMULATION

The formulation of DG MOSFETs starts from undoped body as it is more meaningful in the regime that requires DG MOSFETs. The detail formulation of source and drain charges for undoped SDG MOSFETs has been derived in detail by another paper in the same conference [4]. However, a more

generic expression is required from a modeling perspective to account ADG and ground-plane MOSFET. The cost for going for more generic solution is the more complicated boundary conditions resulting in more complex solution. The generic solution can be obtained with a similar method as in [4], but using the minimum potential point in the channel rather than the middle of the channel as a boundary condition. Starting from

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q\psi}{kT}} \tag{3}$$

we perform integration with the reference to the location of the minimum potential at $x=x_0$ where $\psi(x_0) = \psi_{\min}$. We consider a few special cases here to simplify the discussion. In SDG case, $x_0=T_{Si}/2$. In UTB case, $x_0=T_{Si}$. In ADG case, if we assume the device has n+/p+ gates with workfunction difference of 1V, and V_{DD} is less than the workfunction difference in ultra-small devices, then $x_0=T_{Si}$ in all operation regions similar to the UTB case. By integrating (3) up to x_0, a generic solution is obtained:

$$\frac{d\psi}{dx} = -\sqrt{\frac{2kTn_i}{\varepsilon_{si}}\left(e^{\frac{q\psi}{kT}} - e^{\frac{q\psi_{\min}}{kT}}\right) + \left(\frac{d\psi}{dx}\Big|_{x=x_0}\right)^2} \tag{4}$$

Letting

$$A = \frac{2kTn_i}{\varepsilon_{si}} \quad \text{and} \quad B = A\exp\left(\frac{q\psi_{\min}}{kT}\right) - \left(\frac{d\psi}{dx}\Big|_{x=x_0}\right)^2 \tag{5}$$

and integrating (4) again, we obtain the potential as a function of spatial coordinate in the x direction.

$$\psi(x) = \frac{2kT}{q}\ln\left[\sqrt{\frac{A}{B}}\cos\left(\frac{q\sqrt{B}}{2kT}(x_0 - x) + \cos^{-1}\left(\sqrt{\frac{B}{A}}e^{-\frac{q\psi_{\min}}{kT}}\right)\right)\right] \tag{6}$$

relating electron density and potential using (6) we got

$$n(x) = \frac{n_i\left(\frac{B}{A}\right)}{\cos^2\left[\frac{q\sqrt{B}}{2kT}(x_0 - x) + \cos^{-1}\left(\sqrt{\frac{B}{A}}e^{-\frac{q\psi_{\min}}{kT}}\right)\right]} \tag{7}$$

The total inversion charge is then obtained by integrating (7) from $x=0$ to $x=x_0$ giving

$$Q_{inv} = \frac{2kTn_i\left(\frac{B}{A}\right)}{\sqrt{B}}\left[\tan\left(\frac{q\sqrt{B}}{2kT}(x_0 - x) + \cos^{-1}\left(\sqrt{\frac{B}{A}}e^{\frac{-q\psi_{\min}}{2kT}}\right)\right) - \tan\left(\cos^{-1}\left(\sqrt{\frac{B}{A}}e^{\frac{-q\psi_{\min}}{2kT}}\right)\right)\right] \tag{8}$$

By using this inversion charge term, and following similar derivation as in [4], the I-V equation can be derived. One difficulty in this formulation is the dependent of the solution in term of the boundary condition of x_0 and ψ_{min} which the analytical expression in term of device structure and bias condition is not yet formulated besides the special cases as described before. The general solution with arbitrary device structures and bias conditions requires some fitting function or extrapolation to find x_0 and $\psi_{\min}$.

4. EFFECTIVE MOBILITY FORMULATION

The mobility formulation follows the charge formulation for consistency. For devices with relatively thick silicon film, some experimental results show that the electron effective mobility (μ_{eff}) agrees well with the universal mobility when the inversion layers at both sides of the silicon film weakly interact. In this case, the current transport can be represented by two channels in parallel [5]. When the T_{si} is reduced, the inversion electrons are confined by the two oxide barriers and the form factor increases. Therefore, the phonon limited electron mobility decreases with reducing T_{si} [6-8]. As the T_{si} is scaled below 5nm, most of the electrons are populated in the unprimed subband, featuring a higher μ_{eff} due to its lower conductivity mass [6-8].

While many mechanisms that affect the mobility has been proposed, the most of them can be modeled by the constant term μ_0 in the universal mobility model. A more important part of the model, which is not as widely addressed, is the bias dependent of the mobility. The impact of bias towards the mobility is mainly through the effective vertical field (E_{eff}). Recent experimental results show that the bias dependent of the mobility still more or less follows the universal mobility model. Even if not, it is likely that the direct link between mobility to E_{eff} still exist. With these assumptions in mind, an analytical expression of E_{eff} as a function of device geometry and bias is the most important bridge to model the bias dependence of carrier mobility in DG MOSFETs.

Following the classical approach, E_{eff} is defined as [9-10]

$$E_{eff} = \left[\int_0^{x_0} |E(x)| \cdot n(x)dx\right] \Big/ \left[\int_0^{x_0} n(x)dx\right] \tag{9}$$

It can be interpreted as the average electric field experienced by the carriers in the inversion layer towards the surface of the channel. As the E_{eff} increases, the carriers in the inversion layer have a larger chances to interact with the Si/SiO_2 interface, which degrades the carrier mobility according to the universal mobility model [11].

$$\mu_{eff} = \frac{\mu_o}{1 + \left(E_{eff}/E_o\right)^v} \tag{10}$$

To calculate the E_{eff}, the Poisson's Equation is solved along the vertical direction in the silicon channel, considering only the mobile charge (electron) density as the body is undoped. From equation (7) and Guass Law, the electric field as a function of position can be found and the expression is

$$E(x) = \frac{2kTn_i\left(\frac{B}{A}\right)}{\varepsilon_{si}\sqrt{B}}\left[\tan\left(\frac{q\sqrt{B}}{2kT}(x_0 - x) + \cos^{-1}\left(\sqrt{\frac{B}{A}}e^{\frac{-q\psi_{\min}}{2kT}}\right)\right) - \tan\left(\cos^{-1}\left(\sqrt{\frac{B}{A}}e^{\frac{-q\psi_{\min}}{2kT}}\right)\right)\right] - \frac{d\psi}{dx}\Big|_{x=x_0} \tag{11}$$

By substituting equation (11) and (7) into (9) and using equation (8) to simplify the expression, we obtain a simple generic expressions of the E_{eff}

$$E_{eff} = \frac{Q_{inv}}{2\varepsilon_{si}} - \frac{d\psi}{dx}\Big|_{x=x_0} \tag{12}$$

It should be noted that the expression for SDG with symmetrical boundaries eliminate the second term in equation

(12) and double the inversion charge with the second channel. It results in an even simpler expression of

$$E_{eff} = \frac{Q_{inv}}{4\varepsilon_{si}} \tag{13}$$

To verify the validity of the formulation of E_{eff}, extensive numerical simulations with and without quantum effect have been performed. Fig. 1 illustrates the E_{eff} against the Q_{inv} with different T_{Si} (without quantum effect) for SDG and UTB MOSFETs. The ADG case is very similar to that of UTB except for the different $-\frac{d\psi}{dx}\Big|_{x=T_{Si}}$ term used in equation (12). It shows good agreement between the analytical solution and the simulation result. Also, it is interesting to notice that the $1/4\varepsilon_{si}$ relationship in SDG and the $1/2\varepsilon_{si}$ relationship in UTB device are independent of the T_{Si}.

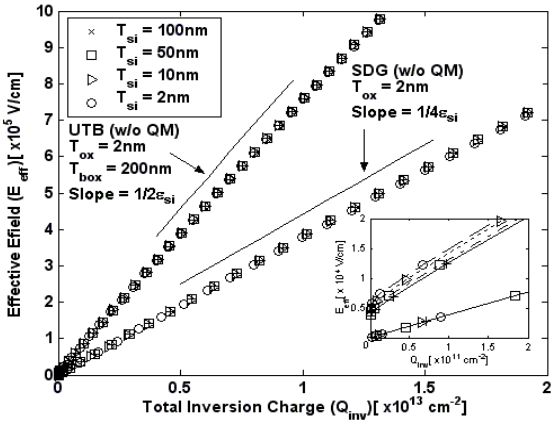

Fig. 1: The plots of the E_{eff} against the Q_{inv} with different T_{Si} for SDG and UTB MOSFETs without quantum effect. The insert magnifies the low inversion charge region showing the offset due to $d\psi/dx$

The plots of E_{eff} versus Q_{inv} including quantum effect for SDG and UTB devices with different T_{si} are shown in Fig. 2. It shows that the functional dependence of $1/4\varepsilon_{si}$ and $1/2\varepsilon_{si}$ with Q_{inv} in both SDG and UTB is not influenced by the quantum effect. We can, in general model the quantum effect only through a correction to the zero-field mobility (μ_o) rather than the E_{eff} term.

Fig. 3 shows the μ_{eff} against the Q_{inv} for a SDG and an UTB MOSFETs with same T_{si}. When the SDG and the UTB device have the same amount of Q_{inv}, the SDG case has a much smaller E_{eff} than the UTB or ADG devices according to equation (12) and (13), which allows it to have a significantly higher μ_{eff}. Therefore, SDG is a more optimal structure for small devices when current drive and speed are considered.

Recently, experimental results show that the mobility in SDG is higher than that in UTB device when the Q_{inv} of UTB device is half of the Q_{inv} of SDG MOSFETs especially when the amount of inversion charge is relatively low. This effect is not fully explained in previous studies [9]. According to equation (12) and (13), when the Q_{inv} of UTB devices is half of the Q_{inv} MOSFETs, the E_{eff} of UTB devices is larger than the that of SDG MOSFETs due to the finite electric field ($-\frac{d\psi}{dx}\Big|_{x=T_{Si}}$) at the backside Si/SiO_2 interface of UTB (and also ADG) MOSFETs. This also explained the higher μ_{eff} in SDG MOSFET at low inversion charge as shown in Fig. 4.

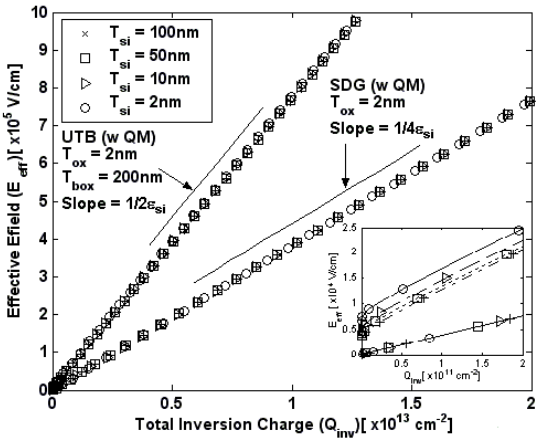

Fig. 2: The plots of the E_{eff} against the Q_{inv} for SDG and ADG MOSFETs with different T_{si} including quantum effect.

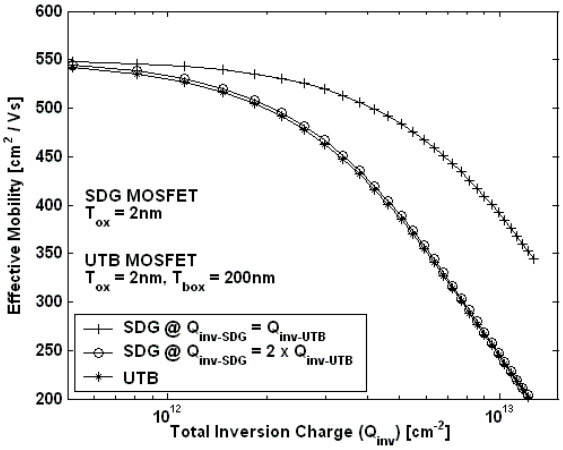

Fig. 3: The plot of the μ_{eff} versus the Q_{inv} for SDG and UTB MOSFETs with T_{si} = 5nm. Less mobility degradation in SDG MOSFET at the low inversion charge region when Q_{inv_UTB} is half of the Q_{inv_SDG}.

Fig. 4 illustrates the electric field at the backside Si/SiO_2 interface ($-\frac{d\psi}{dx}\Big|_{x=T_{Si}}$) of UTB MOSFETs as a function of Q_{inv} with different T_{si}. It shows that the backside electric field is relatively constant with respect to Q_{inv}. As the amount of inversion charge increases, the contribution of the $-\frac{d\psi}{dx}\Big|_{x=T_{Si}}$ term in the UTB device becomes smaller, which

makes the E_{eff} of UTB devices behave more like E_{eff} of SDG MOSFETs under the $Q_{inv\_UTB} = Q_{inv\_SDG} / 2$ condition. Therefore, as the Q_{inv} is increased, the μ_{eff} becomes essentially the same in both SDG and UTB device (Fig. 4) when the $Q_{inv\ UTB}$ is half of the $Q_{inv\ SDG}$.

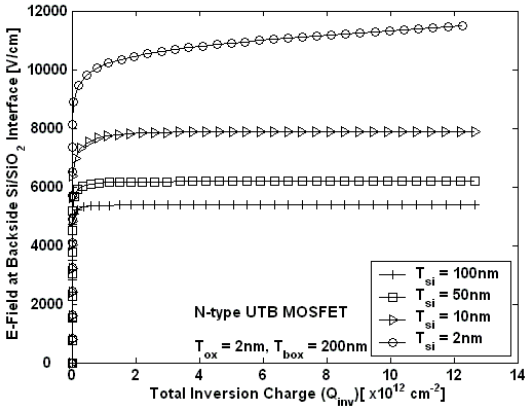

Fig. 4: Simulated electric field at the backside Si/SiO_2 interface of UTB MOSFETs as a function of Q_{inv} with different T_{si}.

5 MODELING CHANNEL ELECTRIC FIELD OF SDG MOSFET IN THE SATURATION REGION

The modeling of DG MOSFETs so far has been focused on the linear region. The modeling of the saturation characteristics is through the introduction of the saturation charge Q_{Dsat} at the end of the gradual channel region, which is independent of the detail physics in the velocity saturation region (VSR). In most cases, the approach is sufficient in giving reasonable I-V characteristics of a DG MOSFET. However, to have more detail understand in the operation inside the VSR such as channel length modulation, a more detail analysis in the velocity saturation region is required. As an initial trial to model the electric field in the velocity saturation region, we first focus on SDG MOSFET due to its simpler boundary condition. The model will be extended to the ADG case in the future.

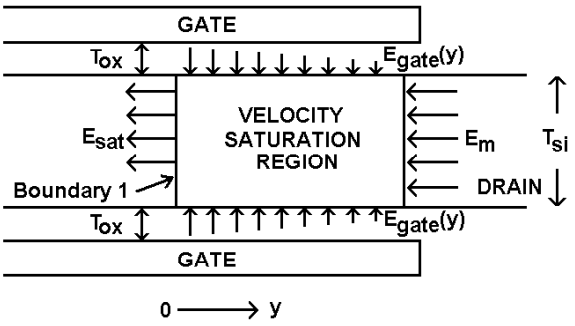

Fig. 5: The velocity saturation region of the undoped SDG MOSFET where Gauss's Law is applied.

For the device operating in saturation regime, the channel of the DG MOSFET can be divided into gradual channel approximation (GCA) region and VSR. A schematic cross-section of the VSR of a SDG MOSFET with undoped body is shown in Fig. 5. "Boundary 1" in the figure indicates the location in the channel where the velocity of carriers just saturates.

The model is developed based on the pseudo two-dimensional approach proposed by Elmansy [12] and Ko [13]. When Gauss's law is applied to the VSR (Fig. 6), we have

$$\varepsilon_{si}\int_{-\frac{T_{Si}}{2}}^{\frac{T_{Si}}{2}} E_{sat}\cdot dx-\varepsilon_{si}\int_{-\frac{T_{Si}}{2}}^{\frac{T_{Si}}{2}}\frac{\partial V}{\partial y}\cdot dx-2\varepsilon_{gate}\int_{0}^{y}E_{gate}(k)\cdot dk = -q\int_{-\frac{T_{Si}}{2}}^{\frac{T_{Si}}{2}}\int_{0}^{y}Q_{inv}(x,k)\cdot dkdx \tag{14}$$

where ε_{gate} are the dielectric coefficient of the gate insulator. The integral can be performed with surface potential, but channel voltage (which differs with the surface potential only by a constant) is used in this case to link the result directly to the external voltage. To account for the non-uniform distribution of the lateral electric field and allow the problem to be solved analytically, it is assumed that the ratio of average lateral electric field to the surface lateral electric field in the VSR is independent of position y and is equal to the value at boundary 1 [12]. We can then write

$$\int_{-\frac{T_{Si}}{2}}^{\frac{T_{Si}}{2}}\frac{\partial V}{\partial y}\cdot dx = A\cdot T_{Si}\cdot\frac{dV_{sur}}{dy} \tag{15}$$

where V_{sur} is the voltage at the silicon/oxide interface. The value of A at boundary 1 can be calculated using the vertical potential profile proposed by Taur [14]

$$V(x) = -\frac{2kT}{q}\ln\left[\cos\left(B\cdot x\right)\right]+V_o \tag{16}$$

where V_o is the potential at the center of the film and $B=\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\cdot e^{\frac{qV_o}{2kT}}$. For simplicity, the potential profile is approximated by a parabolic function with a parameter K

$$V(x)\approx K\cdot x^2+V_o \tag{17}$$

Since the parameter K will be eliminated in the calculation of A, the exact value of K is not shown in the following calculations. The value of A is calculated by substituting (17) into (15), giving

$$A=\frac{1}{3}+\frac{2}{3}\cdot\frac{\partial V_o}{\partial V_{sur}} \tag{18}$$

The partial derivative in (18) is calculated using equation (16) giving

$$A=\frac{1}{3}+\frac{2}{3\left(1+\frac{B\cdot T_{Si}}{2}\cdot\tan\left(\frac{B\cdot T_{Si}}{2}\right)\right)} \tag{19}$$

Substituting (15) into (14) and differentiating both sides with respect to y, we get

$$\varepsilon_{si} \cdot A \cdot T_{Si} \cdot \frac{d^2 V_{sur}}{dy^2} = q \int_{-\frac{T_{Si}}{2}}^{\frac{T_{Si}}{2}} Q_{inv}(x,y)dx - 2\varepsilon_{gate} \cdot E_{gate}(y) \quad (20)$$

Using similar approach as [13], the integrated mobile charge term in (20) can be replaced by the gate electric field at boundary 1 with the assumption that GCA still holds at that location. Equation (20) becomes

$$\varepsilon_{si} \cdot A \cdot T_{Si} \cdot \frac{d^2 V_{sur}}{dy^2} = 2\varepsilon_{gate} \cdot \left[E_{gate}(0) - E_{gate}(y)\right] \quad (21)$$

where the gate electric field $E_{gate}(y) = \frac{V_G - V_{FB} - V_{sur}(y)}{T_{gate}}$, V_G and V_{FB} is the gate and flat band voltage, respectively. T_{gate} is the gate insulator thickness. (T_{ox} is not used as high-k material are allowed in the formulation) Equation (21) is rewritten to

$$\frac{d^2 V_{sur}}{dy^2} = \frac{\left[V_{sur}(y) - V_{sur}(0)\right]}{\lambda^2} \quad (22)$$

where $\lambda = \sqrt{\frac{A \cdot \varepsilon_{si}}{2\varepsilon_{gate}}} \cdot (T_{Si})^{\frac{1}{m}} \cdot (T_{gate})^{\frac{1}{n}}$ (23)

with $m = n = 2$. Using the conditions at boundary 1 that $V(0) = V_{Dsat}$ and $\frac{dV_{sur}(y)}{dy}|_{y=0} = E_{sat}$, the solution of (22) is given by

$$E_{sur}(y) = E_{sat} \cdot \cosh(\frac{y}{\lambda}) \quad (24)$$

and $$V_{sur}(y) = V_{Dsat} + \lambda \cdot E_{sat} \cdot \sinh(\frac{y}{\lambda}) \quad (25)$$

It can be shown that the maximum lateral electric field (E_m) at the end of the channel is

$$E_m = \sqrt{\frac{(V_D - V_{Dsat})^2}{\lambda^2} + E_{sat}^2} \quad (26)$$

where V_D is voltage at the end of the channel.

To verify the result, a 50nm SDG NMOSFET with mid-gap work function gate-electrode simulated by MEDICI and compared with the model. 2-D simulation results show that the parameter m in equation (23) should be linearly from 2.03 to 1.97 as the T_{Si} increasing from 5nm to 20nm. Fig. 6 compares the results calculated from the model with the results obtained from MEDICI for the SDG device with T_{ox} =2nm, T_{si} = 10nm and E_{sat} = 3.5x10^4 V/cm [15]. Good agreement, is obtained between the model and the 2D simulation result especially near the peak E-field region.

Fig. 7 shows E_m as a function of T_{Si} with different T_{ox} under the same biasing condition. The results from the model, again, show good agreement with the simulation results. As predicted by the model, the maximum electrical field increases with the reduction of T_{si} and T_{ox}. The impact of geometry scaling is included through λ which does not have an obvious scaling trend. However, there is a minimum value of λ which can be obtained by replacing the parameter A with its minimum value, giving $\lambda_{\min} = \sqrt{\frac{\varepsilon_{si}}{6\varepsilon_{gate}}} \cdot (T_{si})^{\frac{1}{m}} \cdot (T_{gate})^{\frac{1}{n}}$. This λ_{min} is an important parameter to calculate the maximum E_m and evaluate the worst-case impact ionization for a given SDG structure and biasing condition, which has been shown to take place even at a low V_D < 1V [16].

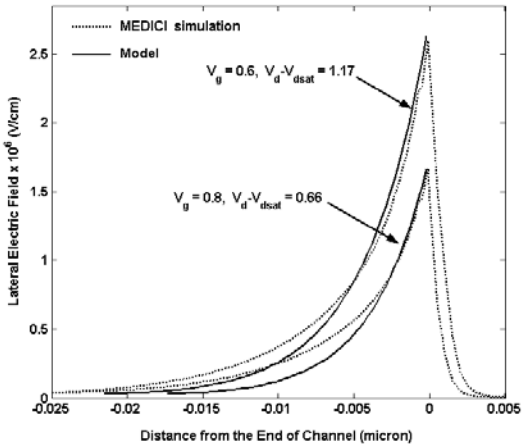

Fig. 6: Comparison of the results calculated from the model with the results obtained from the simulations for the SDG device with T_{ox} = 2nm, T_{si} = 10nm and E_{sat} = 3.5x10^4 V/cm.

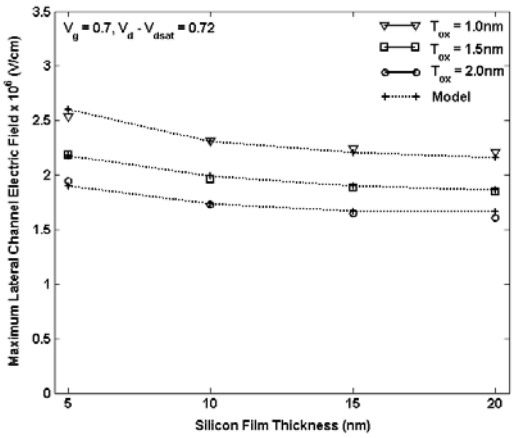

Fig. 7: The plot of the maximum lateral channel electric field (E_m) against the silicon film thickness (T_{si}) with different gate oxide thickness.

Fig. 8 shows the lateral electric field for two SDG devices with same I_{off} and V_T, but different T_{ox} and T_{Si} with value shown in the figure. The I_D-V_G characteristic of those SDG devices are shown as an insert in Fig. 9. The results show that the SDG devices have similar DC characteristic, but different E_m. Although scaling either the T_{Si} or the T_{ox} can give the same performance, peak channel E-field is more seriously affected by the scaling of T_{ox}.

The current formulation of channel E-field does not include quantum effects for simplicity. However, its effects in the VSR region is not serious because the transverse electric field is relative small. For the solution of the Poisson equation,

it can be coupled to the exponential relationship between lateral electric field and position for the VSR region with continuous current flow.

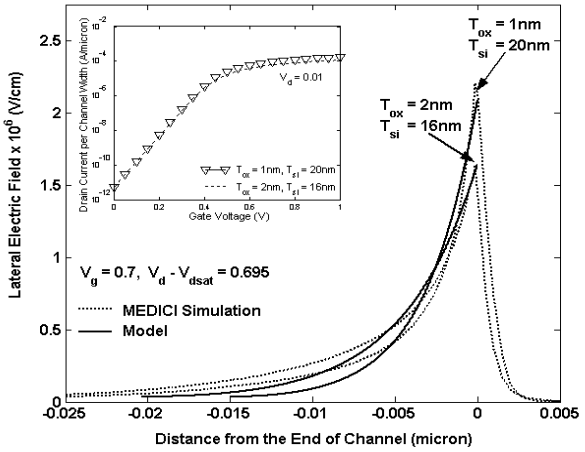

Fig. 8: Comparisons of the E_y for two SDG MOSFETs with same I_{off} and V_T with different T_{ox} 1nm, T_{Si} = 20nm and T_{ox} = 2nm, T_{Si} = 16nm.

In extremely short channel devices, velocity over-shoot (VOS) allows the carriers have a higher velocity than the classical saturation velocity (e.g. $7x10^6$ cm/s). In other words, the velocity of the carriers inside the VSR is not a constant, but increasing with the channel position. Since the current is continuous within the entire channel, the higher the carrier velocity, the lower the lateral electric field inside the VSR. Although the purposed model cannot predict the lateral electric field with VOS, the proposed model can still provide an upper bound on the trend on the maximum lateral electric field with vertical dimension scaling.

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