Radiation Effects in Advanced and Emerging Nonvolatile Memories

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***Abstract*— Despite hitting major roadblocks in 2-D scaling, NAND flash continues to scale in the vertical direction and dominate the commercial nonvolatile memory market. However, several emerging nonvolatile technologies are under development by major commercial foundries or are already in small volume production, motivated by storage-class memory and embedded application drivers. These include spin-transfer torque magnetic random access memory (STT-MRAM), resistive random access memory (ReRAM), phase change random access memory (PCRAM), and conductive bridge random access memory (CBRAM). Emerging memories have improved resilience to radiation effects compared to flash, which is based on storing charge, and hence may offer an expanded selection from which radiation-tolerant system designers can choose from in the future. This review discusses the material and device physics, fabrication, operational principles, and commercial status of scaled 2-D flash, 3-D flash, and emerging memory technologies. Radiation effects relevant to each of these memories are described, including the physics of and errors caused by total ionizing dose, displacement damage, and single-event effects, with an eye toward the future role of emerging technologies in radiation environments.**

***Index Terms*— Emerging memory, magnetic memory, nonvolatile memory (NVM), phase change memory, radiation effects, resistive memory.**

I. Introduction

MEMORY is a key ingredient in computing. The other key ingredient, logic, relies on one device—the transistor, and one circuit primitive, complementary metal–oxide–semiconductor (CMOS), to carry out all computations. Unfortunately, a single universal memory device does not exist, and, therefore, most modern computing systems rely on multiple memory technologies having different devices, circuits, and functional properties. At the dawn of computing, Von Neumann [1] had already recognized the need for a memory hierarchy which organizes memory into categories to meet the needs of each section of the computing system—and became engrained in the von Neumann architecture. Fig. 1 illustrates this hierarchy for a modern microprocessor-based computer. A major component of modern computer architecture research, development, and design is focused on minimizing the effect of these memory technologies which each have significantly different latency, bandwidth, and density [2].

Manuscript received November 17, 2020; revised March 30, 2021 and April 8, 2021; accepted April 8, 2021. Date of publication April 29, 2021; date of current version May 20, 2021. This work was supported in part by the Laboratory Directed Research and Development program at Sandia National Laboratories.

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TNS.2021.3074139.

Digital Object Identifier 10.1109/TNS.2021.3074139

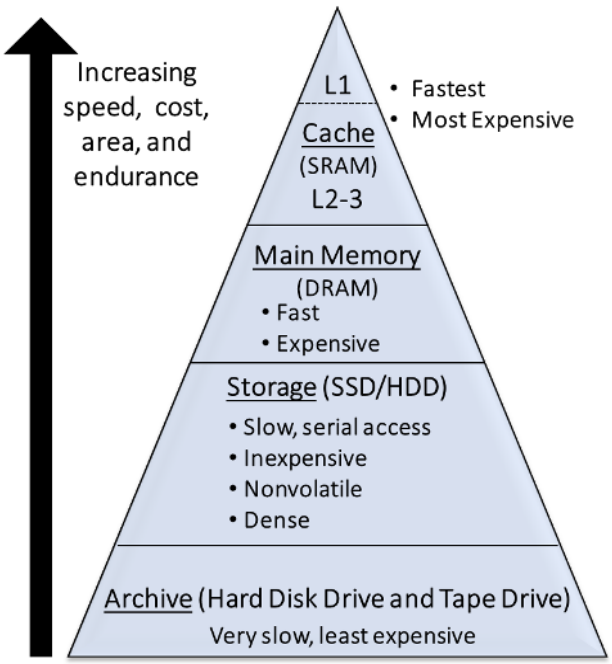

Fig. 1. Modern memory hierarchy.

Although the hierarchy illustrated in Fig. 1 represents a microprocessor-based computer architecture, such as that found in a smartphone or laptop, it applies to most modern systems, from embedded microcontrollers to cloud systems with minor differences. Memory is arranged from the highest performance and lowest density at the top of the pyramid through the lowest performance, lowest cost, highest density, at the bottom. At the top of the hierarchy is cache. Level 1 (L1) cache is typically integrated directly in the logic chip, runs at or near the speed of the processor core (typically >1 GHz), and is ultimately responsible for feeding data to the registers connected to the arithmetic logic unit (ALU) or similar execution unit. Higher level L2 and L3 cache provide a buffer between L1 cache and the much slower main memory and may be shared across multiple processor cores.

The majority of modern caches store each bit in a static random access memory (SRAM) cell, which typically consists of six transistors. These transistors can be optimized for speed or density depending on the application and utilize the same CMOS process technology as the logic core. The requirement for six transistors per bit is a major density limiter for SRAM. A modern 7-nm FinFET-based processor integrated circuit (IC, also referred to as a "chip" or "die") can have up to about 50 billion transistors, but even if half of the area is

devoted to SRAM cache and supporting circuitry, this only allows for a maximum of about 10–80 MB of SRAM on a chip. Clearly there is a limited set of applications which are fully functional using only the on-chip cache, which is why the next level down the hierarchy, main memory, is a necessary workhorse.

Most of a program's working data is stored in main memory and only requested by the cache when it is needed for an operation. Main memory typically employs dynamic random access memory (DRAM), most commonly located on a separate chip. DRAM is slower than SRAM, with an access time, or latency of about 10–50 ns. The memory state is physically stored in an array of capacitors, which are each individually controlled by a series access transistor. DRAM has a denser cell size than SRAM and is less expensive to manufacture on a per-bit basis. Therefore, modern personal computing systems often contain a few to hundreds of GB of DRAM memory, enabling large programs and data sets to be loaded in the working memory.

DRAM capacitor structures require a different silicon process flow than standard CMOS logic transistors and hence they are typically fabricated on separate die than the microprocessor. Typically, DRAM dies are arranged in dual inline memory modules (DIMMs) which communicate with the microprocessor through standard electrical interfaces, such as double data rate (DDR). DDR has contributed to a latency bottleneck and energy inefficiency between SRAM and DRAM in modern systems, and this memory communication path has become a more significant performance limitation than the computation itself. From the energy perspective, it only takes about 1 pJ per bit to program a DRAM bit, but 10–100 pJ per bit to transfer the information to and from the processor.

Another drawback of DRAM is that the bit cell will lose most of the capacitor charge and memory state over a relatively short period of time ($<$1 s) through the access transistor. For this reason, DRAM must be periodically refreshed with a period of tens of microseconds to milliseconds depending on the specific design standard, with the most common refresh period being 64 ms.

SRAM and DRAM are volatile, meaning that their state cannot be retained without an active power source. Many systems are not continuously powered and require a persistent, nonvolatile data storage capability. Furthermore, it would be inefficient to store all of a system's data on the main memory, due to the relatively high cost of DRAM. These considerations define the requirements for the third level on the hierarchy: storage. The operating system, program files, and data are stored in a nonvolatile storage medium, from which they are loaded during the system boot-up process. The most common modern storage memory is NAND-flash, the physics of which is discussed in detail below. Nonvolatile memory (NVM) is of low cost and high density, allowing typical personal computing systems to utilize GBs to terabytes (TB) of persistent storage. This data can still be accessed with latencies on the order of 10–1000 μs for a modern solid state drive (SSD), depending on the specific details. Magnetic hard disk drives (HDDs) which rely on electromechanical elements to read disks offer even lower cost storage at the expense of even greater latency ($>$1 ms) and higher power. Sometimes a smaller SSD will be used in tandem with a large HDD to speed up operations such as operating system loading. For data that will be accessed rarely, slow serial access magnetic tape systems are still used, due to the very low cost per GB of storage.

Embedded Internet of Things (IoT), and some edge systems, which are based on microcontroller units (MCUs) or field programmable gate arrays (FPGAs), may follow a simplified version of this hierarchy. Many of the electronic systems used in radiation environments such as space and aviation fall in the class of embedded systems. In these systems, it is often the case that a small to moderate data and program storage are required, and the main program and data memory may utilize an embedded NVM on the same IC as the execution unit. In this case, the main memory and storage are compressed to a single level in the hierarchy. In practice, this embedded floating gate (FG) or charge trapping memory (CTM) is the most common form of on-board NVM embedded in an MCU or FPGA. In this case, an FG or charge trapping cell is integrated in the same process technology as the MCU logic transistors, creating a more complicated process technology. Emerging resistive memories, such as redox random access memory (ReRAM), have also been explored as a possible embedded memory. These have the advantage that they can be integrated into the back end-of-line (BEOL) of an existing CMOS logic process, suggesting that embedded memory may be an important application for these emerging technologies [3].

A. NVM Basics

Before discussing the individual NVM technologies, it is useful to review the associated basic concepts and terminology. This brief introduction can be complemented by comprehensive sources, including [4] and [5].

NVMs are typically arranged in arrays which are read and written using orthogonal wordlines (WLs) and bitlines (BLs). The wordline typically activates a group of storage cells and the orthogonal bitline connects each cell on an active wordline to the read circuitry, such as a sense amplifier. Different memory device technologies use different array topologies. For example, three-terminal charge-based devices such as FG and CTMs are typically arranged in the NAND and NOR flash topologies discussed below. Two-terminal resistive memories are more commonly arranged as random access arrays similar to DRAM, allowing for selective read and write operation on single cells.

Terms used to indicate reading and writing to NVMs often depend on the technology being discussed. For charge-based memories, the terms write or program are used to indicate injecting charge into the storage element (FG or trapping layer), whereas erase typically refers to the process of removing charge. In resistive memories such as ReRAM or phase change memory (PCRAM), the terms set and reset are commonly used to indicate writing a low- and high-resistance state, respectively, to the resistive cell.

Endurance is the number of times that data can be written to an NVM cell before it begins to register errors. Whereas SRAM and DRAM can effectively change memory state an

TABLE I
COMPARISON OF MODERN EMBEDDED NVM TECHNOLOGIES AND EDRAM. DUE TO THE RANGE OF VALUES IN THE LITERATURE, NUMBERS SHOULD BE CONSIDERED APPROXIMATE

	eDRAM	eFlash (NOR)	STT-MRAM	ReRAM	CBRAM	PC-RAM
2021 Commercial Maturity	Production (14nm)	Production (28nm)	Production (22nm)	Pre-Production (22nm)	Pre-Production (28nm)	Production (28nm)
Min device size (nm)	~100	>28	<16	<10	<10	<10
Density (F^2)	~10	~10	~8-20	4	4	4
Read Time (ns)	< 10	~10	~10	~10	~10	~10
Write Time (ns)	< 10	10^6	13	2	2	50
Write Voltage (V)	~1	~10	<1	1-3	1-3	1-3
Endurance (W/E Cycles)	$>10^{16}$	10^5	10^{12}	10^{12}	10^{10}	$>10^9$
Retention	>64 ms	> 10 y	> 10 y	> 10 y	> 10 y	> 10 y
BE Mask Layers	FE	FE	4	4	4	4

unlimited number of times, and NVMs usually have a limited number of endurance cycles. As seen in Table I, endurance ranges from about 10^5 in modern embedded flash [6] to $>10^{11}$ in spin-transfer torque magnetic random access memory (STT-MRAM) [7]. Endurance in some technologies can also be improved or sacrificed as a tradeoff for other properties, such as reduced retention or longer program times.

NVMs will hold a state for a finite amount of time without being rewritten, known as retention. Retention is often an Arrhenius function, where the amount of time a device can retain a memory state decreases exponentially with increasing temperature. For this reason, retention is typically specified at a maximum temperature. Modern NVM technologies are expected to have retention of at least 10 years at 85 °C for most commercial applications. For more demanding applications such as automotive and aerospace, 10 years at 125 °C is required. Retention is typically determined by accelerated testing, most commonly using temperature or voltage acceleration models.

Read and write parameters are also important attributes of an NVM technology. These include write voltage, write time, write current, and read time. Many of these properties are factors of both the memory cell and the array configuration. For example, NAND flash is faster to write but slower to read than NOR flash. Resistance change memories typically demonstrate very fast switching at the cell level (<10 ns), but have slower array access times, due to array circuitry and error correction. A comparison of key properties of embedded DRAM (eDRAM) and major embedded NVM technologies is given in Table I (values from [6]–[12] and references therein).

A single NVM chip can have billions of bits, and the read and write functions for that memory will occur millions of times per second. Often the memory is designed, assuming that not every bit will be read or written correctly during routine operation. The number of incorrect bits over a given period is known as the bit error rate (BER). At the system level, the term failure in time (FIT) is used to specify the number of errors where one FIT is equivalent to one bit failure over 10^9 h of operation [13]. Error correction codes (ECCs) and error correction circuitry are required in modern high-density scaled NAND flash to ensure accurate output [14].

B. Radiation Effects Relevant to NVMs

NVMs can be affected by cumulative radiation exposure over time, including total ionizing dose (TID) and displacement damage. Effects of single transient energized particle strikes, known as single-event effects (SEEs), are the other fundamental result of exposing a memory to radiation. The dominant type and levels of radiation that an NVM will experience depend on the mission environment and duration. For example, TID for satellite missions can be on the order of tens to hundreds of krad, with a strong dependence on the orbit location. Details of radiation environments can be found in reviews such as [15].

TID affects the state of charge storage devices by altering the charge levels stored in the cell. All modern NVM technologies require CMOS peripheral circuitry, which is subject to threshold voltage shifts and subthreshold leakage paths due to TID that can cause the read and write circuitry to function incorrectly. The common unit of absorbed ionizing dose in electronic devices is the rad. Comprehensive discussions of the effects of TID in microelectronics can be found in [16] and [17]. Displacement damage from charged particles interacting with the device structure can also permanently alter the atomic structure of the material they strike. In this case, some atoms forming the bit are displaced, which can cause it to remain permanently stuck or lose memory functionality.

Displacement damage is often characterized by the fluence in particles per unit area, such as ions/cm^2. In some cases, displacements per atom are also used to quantify the damage.

Several types of SEEs are observed in NVMs, due to heavy-ion or high-energy charged particle strikes. Common SEE phenomena include nonpermanent or soft errors known as single-event upsets (SEUs). These include single bit upsets (SBUs) and multibit upsets (MBUs). An SBU in an NVM cell refers to a state change in a single bit due to a transient particle strike, typically as a result of charge deposition. In some cases, it is possible for a charged particle to upset the state of more than a single NVM bit, in which case an MBU occurs. A single-event functional interrupt (SEFI) occurs when the functionality of the memory controller circuitry, such as a microcontroller controlling the read and write operation sequence, is disrupted by the particle strike. For example, a write-SEFI may occur during the programming of a NAND-flash, because the write sequence was executed during the ion strike. This may require that the program routine is restarted, or in some cases, a complete power cycle is required [18]. In addition to transient effects, heavy ions can also cause potentially permanent SEEs such as single-event latchup (SEL), and permanent, destructive effects such as single-event burnout (SEB). Destructive SEEs are less common in NVM arrays and not detailed in this article.

Further detailed discussion of the fundamentals of single-event radiation effects in microelectronics can be found in numerous reviews such as Dodd and Massengill [19] and Baumann [20].

C. Organization and Scope

The remainder of this article will cover the fundamentals, current state of technology, and radiation effects of the most prevalent advanced and emerging NVMs. An excellent overview of radiation effects in NVM was given 10 years earlier in the 2010 review by Gerardin and Paccagnella [18]. This work should be considered a complementary reference, providing special attention to topics which have progressed significantly over the past decade. This includes results in highly scaled and 3-D flash, as well as emerging memory technologies and radiation effects in these devices—topics of significant interest in recent years [21].

II. Charge Storage Memories (Flash)

Charge storage memory in the form of NAND flash remains the most prominent nonvolatile technology in the market as of 2020. As discussed below, the term "flash" refers to an array architecture which is most commonly implemented using either of two charge storage device structures: FG or CTMs. Charge storage memories are often referred to as flash memory due to these array architectures, and these terms will be used interchangeably in this article.

Flash memory is one of the most common embedded NVM options at foundries and has been integrated in scaled embedded CMOS technologies as small as 28 nm [6]. It is used in standalone memories with nodes as small as 16 nm [22]. Flash is used for an array of applications, including storage

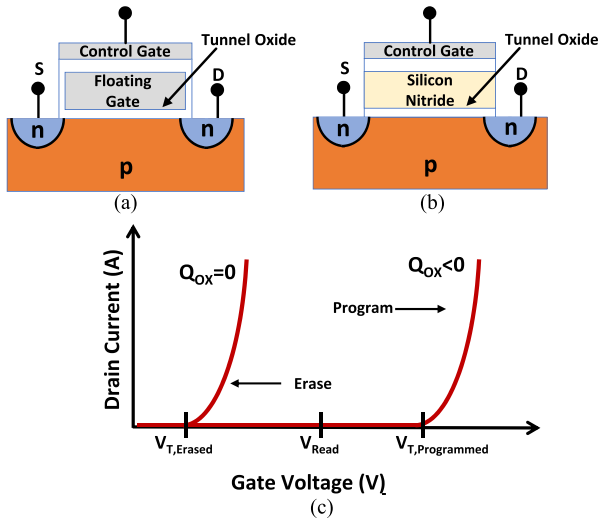

Fig. 2. (a) FG and (b) semiconductor–oxide–nitride–oxide–semiconductor cells. (c) Drain current versus gate voltage when there is no charge and negative charge on the gate.

ICs, such as SSDs, embedded memory for MCUs found in automotive, industrial, and consumer electronics, as well as IoT. Embedded flash scaling has progressed slowly at nodes below about 28 nm, whereas standalone flash has moved to 3-D due to scaling challenges. Charge-based memories are more sensitive to ionizing radiation than noncharge-based memories, and scaled FG is particularly sensitive to radiation-induced data loss, posing challenges for future use in systems that will encounter radiation.

The remainder of this section covers basic device physics, array organization, and state-of-the-art scaled and 3-D NAND topologies and the radiation effect mechanisms in these devices.

A. Charge Storage Devices

Charge storage devices represent a memory state using charge stored permanently between the gate and the channel in a MOSFET structure modified for this purpose. A simplified, planar three-terminal FG memory structure is shown in Fig. 2(a). This device resembles an n-channel MOSFET (nFET) with an important modification to the gate-stack: an electrically conducting structure, such as polysilicon or metal tab, is inserted in the gate oxide such that it is electrically insulated from all terminals due to the oxide—and is known as an FG. Fig. 2(b) shows an analogous nFET structure, except that the gate-stack has an insulating nitride charge trapping layer (CTL) inserted, in which trapped charge is stored to represent the memory state. This device is known as CTM. This is the gate-stack layers of the example structure in Fig. 2(b) are semiconductor–oxide–nitride–oxide–semiconductor, and this device is referred to as SONOS. Charge can be injected through the lower oxide and stored on the FG or CTL through the mechanisms described below. This lower oxide between the FG or CTL and MOSFET channel is referred to as the tunnel oxide (TO) and sometimes the upper oxide is referred to as the interpoly oxide. The top electrode is referred to as the control gate.

The threshold voltage (V_T) of the MOSFET in Fig. 2(a) is proportional to the amount of charge in the FG or silicon nitride (SiN) in Fig. 2(b). The physics of the threshold voltage shift can be understood by considering a charge sheet in the gate oxide region of a conventional MOSFET. If a sheet of charge Q_{ox} is inserted somewhere in this oxide, the V_T shift will be set by the position of the charge sheet with respect to the gate electrode and the channel. As the charge sheet is moved closer to the channel, and further from the gate electrode, the V_T shift for a given charge Q_{ox} is proportionally increased. Analogously, in a charge trapping or FG device, as the ratio of the lower to upper oxide thickness is reduced, a given Q_{ox} in the storage layer will more significantly shift V_T. In practice, it is desired to have a thin lower (tunnel) oxide to maximize the V_T shift given by the charge in the FG. The minimum TO thickness is constrained by that needed to reliably retain charge in the FG over many program and erase cycles. Furthermore, while a thicker upper oxide will increase the V_T shift for a given charge and TO thickness, this will also increase the required voltage to achieve a given field in the TO (and decrease the overall capacitance of the stack), ultimately increasing cell write voltage. Clearly, the layer thicknesses must be carefully chosen to optimize the desired traits of the memory cell, which include long retention, high speed write, and low write voltage.

The memory is programmed by injecting charge into the gate, through the mechanisms discussed below. In the case of electron injection into an nFET FG, the resulting V_T shift is positive. The memory is erased by removing the electrons. The cell can be read simply by grounding the gate, biasing the drain, and measuring the current. The current through a device with a programmed or written (high V_T) state will be significantly lower than a device in the erased (low V_T) state. The memory state is read by examining the MOSFET drain current (I_D) versus control gate voltage (V_{CG}) behavior [Fig. 2(c)].

Programming the cell occurs by two possible mechanisms: Fowler–Nordheim (FN) tunneling, or hot carrier injection (HCI). These processes can be explained considering the case of an electron storage FG cell based on an nFET. When programming via FN tunneling, the source and drain of the MOSFET are grounded, and a high positive voltage is placed on the control gate. Electrons tunnel from the channel into the FG under the high electric field, as depicted in the band diagram of the control gate to the substrate in Fig. 3(a). Following this process, the band diagram of a programmed FG cell retaining charge is given in Fig. 3(b).

In the case of programming with hot electron injection, both the gate and drain are positively biased, such that the MOSFET channel is conducting current. When sufficient vertical field is created by a high positive gate voltage and sufficient lateral field is created by a high drain voltage, carriers will gain enough energy to overcome the TO barrier and enter the FG. The HCI write mechanism is faster than FN tunneling and requires a lower gate bias. However, hot carriers can degrade the TO during each program cycle.

Both program mechanisms are applicable to CTMs, such as SONOS. An important difference between the CTM and FG is

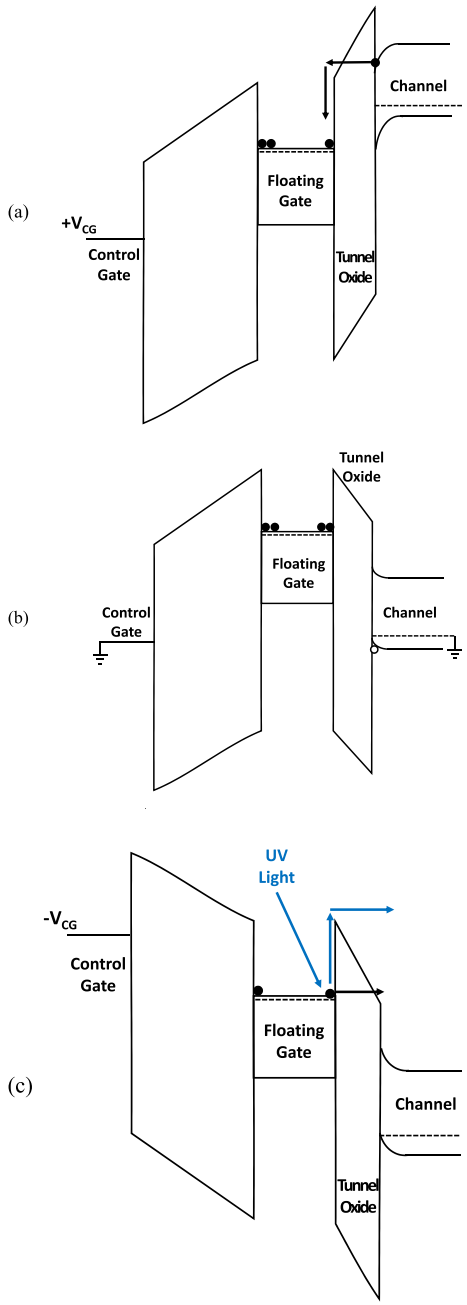

Fig. 3. Band diagram of an FG cell in (a) FN tunnel programming, (b) retention of the programmed state, and (c) erasure by FN tunneling (black) and UV light (blue).

that in the former, the charge is localized in traps through the CTL following injection. Conversely, the FG is a conductor, and charge will spread out evenly on the surface. When hot electron injection is used to program a CTL, the carriers will remain localized in traps near the drain. If the cell is reversed by positively biasing the source and grounding the drain, hot electrons will be injected close to the source. This property can be used to create a two-bit cell, where the bits are differentiated by storage of charge either near the drain or near the source and is the basis of the nitride read only memory (NROM) cell [23].

Charge removal from the FG or CTL is achieved with FN tunneling in all modern flash technologies. In the case of FN

tunneling, a high negative field is placed on the gate and either: 1) the p-well is positively biased and the source and drain are grounded or 2) the source is positively biased and the substrate and drain are grounded. Electrons are forced to tunnel from the FG to the channel in case 1) or to the n-type source in case 2) [see Fig. 3(c)]. In early FG technologies, an ultraviolet (UV) light source was used to stimulate electron emission over the barrier rather than tunnel through it. The biasing is similar to that used for FN tunnel erasure, but a significantly lower field across the gate oxide is required, which was important for early device structures which had oxides that were too thick for tunneling. UV light is used with energy high enough to allow electrons under a field to overcome the barrier between the gate and oxide and exit the gate. Stimulated electron emission over the TO barrier is also one of the key mechanisms of memory state change due to ionizing radiation.

Once programmed, a properly designed flash memory will retain its state for years. As noted above, a nonvolatile cell must retain its state for 10 years typically at 85 °C and up to 125 °C, depending on the application. The programmed state, with a band diagram in Fig. 3(b), is more difficult to maintain than the unprogrammed state due to the high field on the TO which causes charge at the edge of the TO too slowly tunnel back through to the channel. In order to minimize this leakage current, the TO cannot be thinner than about 8 nm, even in highly scaled devices, otherwise unacceptable charge loss will occur [24]. Leakage paths or pinholes in the TO are most problematic for FG devices because the charge will easily find to the weakest point in the oxide and exit the FG. This leakage through the TO is reduced in CTMs because the charge is spatially spread out and confined to local traps in the CTL. Therefore, even when a defect in the oxide occurs, the charge lost is confined to charge near the defect. Improved charge loss characteristics of CTMs have enabled the TO to be scaled somewhat thinner than state-of-the-art FG devices, to about 5 nm [24].

B. Flash Memory Basics

Charge storage devices can be arranged with individual read and write access to every three-terminal device. However, wiring this array with individual connectivity to each bit creates significant complexity and inefficient use of chip area. Flash memory was invented to efficiently organize these NVM arrays. Two flash architectures are commonly used: NOR and NAND.

A NOR array can be described with reference to Fig. 4. The bitline is connected to the drains of each cell in the column and the wordlines are connected to the gates of each row. The cell sources are tied together to a common ground. Cells can be read individually by positively biasing a WL and BL, enabling a true random access read. The NOR cell is written individually using the HCI process described above. NOR still must be erased in blocks, by placing a high voltage on the gates (WL) and using FN tunneling to remove charge. NOR arrays require an area of about $9–11F^2$ per bit, where F is the technology feature size.

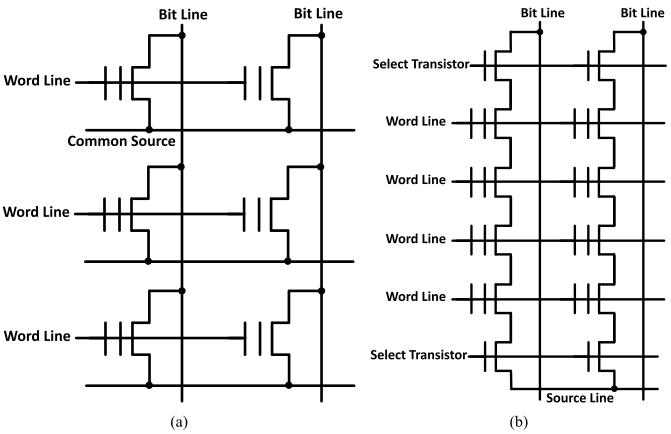

Fig. 4. (a) NOR flash array and (b) NAND flash array as described in the text.

NAND arrays arrange the cells in strings, with shared source and drain contacts, as illustrated in Fig. 4(b). This is more area-efficient than NOR, requiring about $4–6F^2$ per bit. NAND arrays require a more complex addressing architecture, with slower serial read than NOR arrays. In NAND flash, both write and erase operations utilize FN tunneling.

NOR is significantly faster to read (in terms of random access time) and has higher endurance than NAND. NAND has a higher write speed and greater density, resulting in a lower cost per bit. NAND is commonly used in storage applications, such as solid-state hard drives, smartphones, and thumb-drives. NOR is ideal for applications where low read latency, random access read, and higher endurance are needed, such as in embedded controller code storage [4].

Flash memory can have thousands to millions of cells in an array, with variations in cell properties occurring across the array. Ideally, all programmed cells will have identical charge levels and threshold voltages, and the same would be true for each erased cell. For real devices, the program and erase operations result in a distribution of threshold voltages centered around a target level. Therefore, cells in an array are characterized by distributions of threshold voltages, commonly plotted as the number of cells in a V_T range versus the target V_T. Fig. 5 plots this V_T distribution for a single-level cell (SLC) flash array, illustrating behavior which typically follows a Gaussian distribution [25]. The voltage at which V_G is biased during a read operation is indicated in Fig. 5 as V_{Read}.

If V_T for the tail bits of the programmed and erased populations cross V_{Read}, the offending bits will register as errors. During the retention mode, charge will leak out of the programmed cells at different levels, spreading the distribution [24], [26], [27]. When the programmed bits at the low end of the V_T distribution start to cross the read threshold voltage, these bits will register as errors. This distribution shift is illustrated in Fig. 5, with the red curve representing bits following charge loss. When characterizing the effects of radiation on a flash array, the V_T distribution is important in understanding bit error behavior.

Distributions are further complicated in modern flash cells, which utilize the multilevel cell (MLC) scheme to achieve greater density. An MLC is programmed to hold two bits (four levels) by programming cells to multiple V_T targets

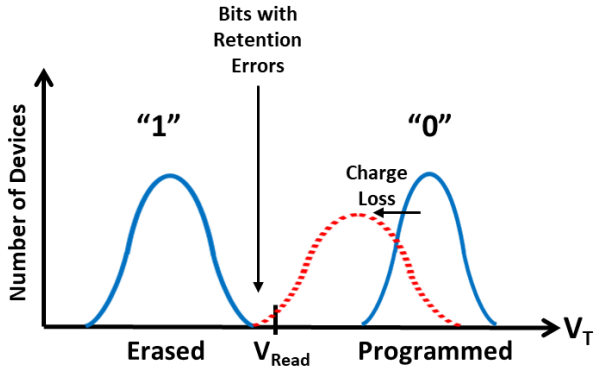

Fig. 5. Threshold voltage versus the number of devices, showing the V_T distribution of flash cells in the initial programmed and erased states (blue) and the shift in distribution of the programmed state due to charge loss retention loss (red).

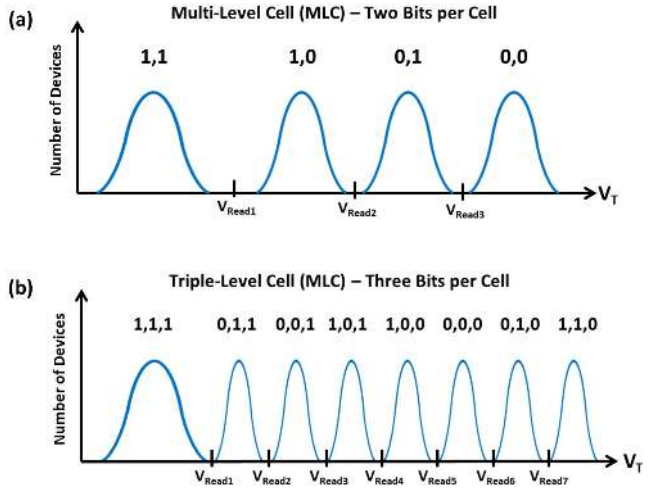

Fig. 6. Qualitative distribution of devices versus V_T for (a) MLC and (b) TLC schemes.

to represent each of the four memory states, resulting in distributions as illustrated qualitatively in Fig. 6(a). When V_T distributions of any of the four levels overlap, read errors will occur. For a given flash technology node, the overall physical threshold voltage range for MLC devices is not significantly different than that for SLC, and hence tighter V_T distributions are required to achieve four levels without increasing the error rate. This tighter V_T band tolerance and reduction in memory window for each level results in a lower endurance and retention for cells programmed with MLC than those using an SLC scheme in the same physical device technology [25]. The MLC concept can be extended to a three-bit (eight level) scheme known as triple-level cells (TLCs), as illustrated in Fig. 6(b). This requires even tighter distributions to avoid overlap between the eight levels and further challenges the reliability.

C. Modern Flash Memory

In the early 2000s, until the saturation of 2-D flash around 2015, flash was leading Moore's law scaling—implementing smaller critical dimension more aggressively than logic transistors. Around 2010, it was recognized that 2-D planar NAND was starting to reach physical and lithographic limits. The timeline of flash technology progress in the decade

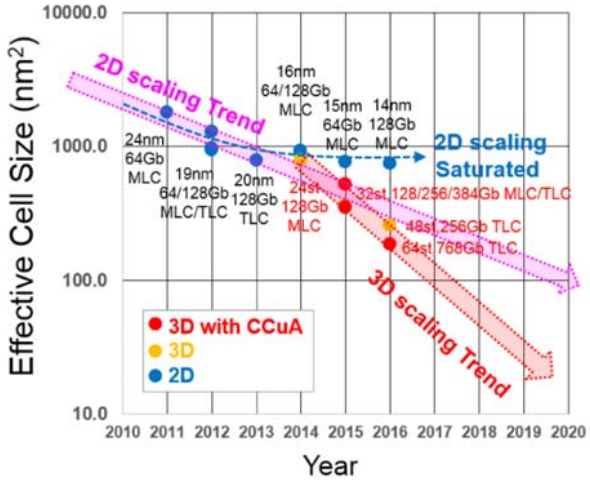

Fig. 7. Effective cell size versus year, illustrating trends in 2-D and 3-D flash between 2010 and 2020 (© 2017 IEEE. Reprinted, with permission, from [31]).

between 2010 and 2020 is illustrated in Fig. 7. By the 25-nm node, the FG had about 50 electrons [Fig. 8(a)] [28]. Severe cell crosstalk at the 25-nm node required innovations in the FG cell process. Integrating an air-gap in the bitline reduced crosstalk and enabled the 25-nm node, and this air-gap technique was extended to a process known as the "planar cell," which enabled the 20- [29] and 16-nm [22] nodes. Challenges at the cell level included cell-to-cell variation in V_T due to random dopant fluctuation, which increased the programmed V_T spread [Fig. 8(b)], as well as electronic random telegraph signal (RTS) noise which significantly alter the measured current and V_T of the cell between consecutive read operations [Fig. 8(c)] [28]. In addition to physical degradation due to cell scaling, these nodes hit the limits of double patterning (DP) and finally the limits of quadruple patterning (QP) lithography [24], [30], [31]. By this point around 2014, it was clear that 2-D flash scaling was becoming unsustainable. During this period, interest in the emerging memories such as ReRAM, STT-MRAM, and PCRAM peaked as possible NAND-flash replacements.

However, the NVM industry ultimately mitigated the 2-D challenges by migrating to 3-D flash structures, drawing from the development of innovative vertical processes that commenced years earlier [32]. These processes allowed relaxation of the physical feature size while maintaining a high density of bits on a single IC and reduced the number of lithography steps and cost associated with each bit.

Samsung was the first to release a vertically stacked 3-D NAND product in 2014 [33] based on a charge trapping cell, such as SONOS or TaN–AlO–SiN–SiO_2–Si (TANOS) [34]–[36]. FG cells have also been integrated into 3-D NAND flash architectures, starting with the stacked surrounding gate transistor (S-SGT) circa 2001 [37] and serve as the basis of Micron's current 3-D-NAND products [38]. For 3-D NAND, it is useful to define an "effective cell area," which is the entire number of bits in the vertically stacked structure divided by the silicon area the array covers. This effective density is typically much smaller than the physical area of the vertical cell.

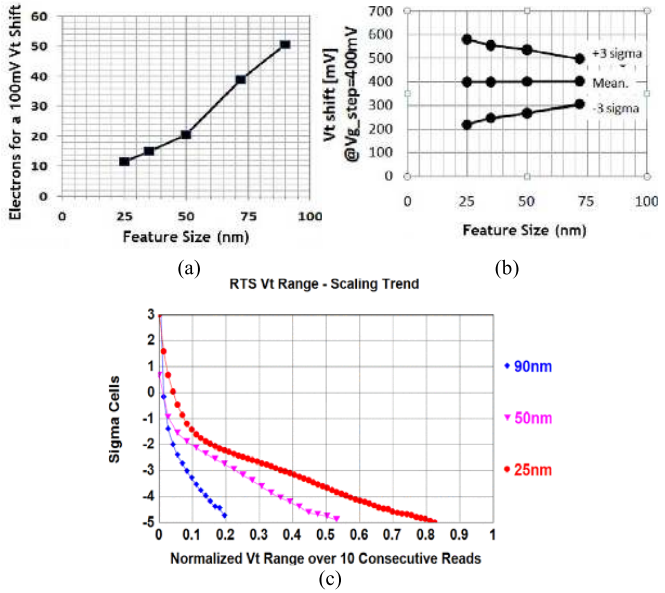

Fig. 8. (a) Number of electrons to cause a 100-mV V_T shift in an FG cell versus technology node. (b) Program V_T variation. (c) Read variation in 25-nm FG cells (© 2010 IEEE. Reprinted, with permission, from [28]).

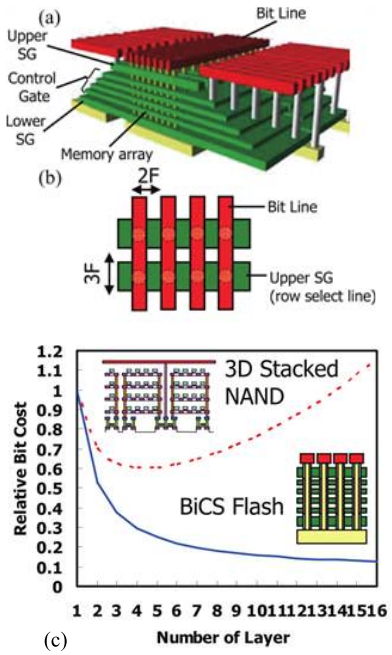

Fig. 9. (a) 3-D BiCS NAND flash array architecture and (b) process and (c) comparison of bit cost versus the number of layers between the earlier stacked NAND and BiCS flash (© 2007 IEEE. Reprinted, with permission, from [32]).

There are several 3-D NAND-flash array architectures and processing schemes. One early architecture that had significant impact was known as bit cost scalable (BiCS). This was based on a vertical SONOS cell, presented by Toshiba, Yokohama, Japan, in 2007 [32], which was later extended to pipe-shaped BiCS [39]. The terabit cell array transistor (TCAT) is built on the BiCS concept, solved some of the process and device challenges [40] and went to become the basis of Samsung's production V-NAND technology [33].

The BiCS physical array architecture and device layout are illustrated in shown in Fig. 9(a) and (b), respectively [32].

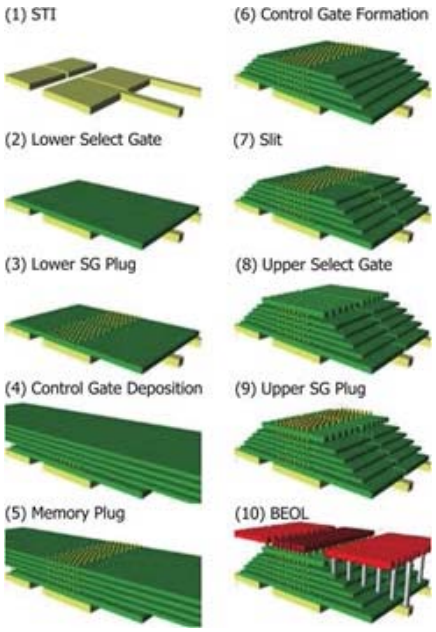

Fig. 10. 3-D BiCS NAND flash process flow (© 2007 IEEE. Reprinted, with permission, from [32]).

Prior to BiCS, NAND flash was being extended to 3-D arrays by repeating the same process steps for each layer. This repetitive stacking process enabled vertical NAND but was not commercially viable because of two issues. The main drawback was that each memory layer repeated the same set of lithography and etch steps and therefore after a few layers, the cost per bit will be similar to a 2-D process. The second drawback is that the repeated complex lithographic processes reduce yield with each layer. The combined effect is that for 3-D NAND made through layer duplication, a higher cost per bit than the 2-D baseline occurs after about three layers [see Fig. 9(c)]. The innovation of the BiCS process was to avoid a full set of lithography and etch steps for each memory layer, but rather amortize a special high-aspect ratio etch over many layers. In this case, the number of lithographic steps is constant with the number of memory layers—and therefore, the cost per bit will decrease as the number of layers increases. This cost advantage led to significant commercial interest BiCS and related fabrication techniques. As seen in the simplified process flow of Fig. 10, the memory bits cells for many layers are deposited by alternating poly-Si (gate electrode) and SiN cap layers. Then a high-aspect-ratio hole is etched and the CTLs are deposited, followed by the poly-Si body. The BiCS architecture results in an effective cell area of $6F^2/n$, where n is the number of layers.

BiCS utilized a charge trapping cell, which localized charge under each gate without having to separately define CTLs, which simplified processing. The BiCS SONOS NAND flash string is illustrated in Fig. 11(a), with a close-up view of the vertical SONOS transistor with a poly-Si both and gate [Fig. 11(b)] and the poly-Si select transistor in Fig. 11(c). Each SONOS cell in the 3-D-NAND string is programmed, erased, and read in a similar manner to the planar version, where program and erase are accomplished through the FN processes described above. The 3-D poly-Si body SONOS

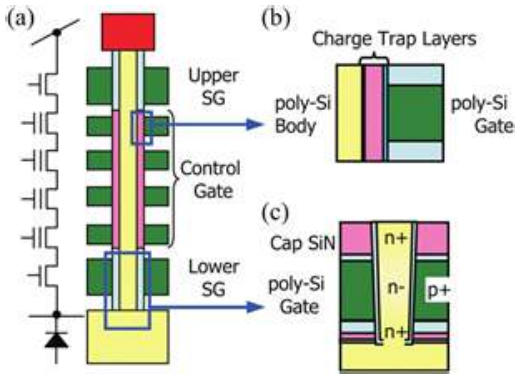

Fig. 11. (a) Vertical flash string. (b) Corresponding SONOS cell. (c) Select gate cell (© 2007 IEEE. Reprinted, with permission, from [32]).

devices do have operating challenges and reliability concerns beyond those in planar devices, such as reduced channel mobility and trapping at grain boundaries [31]. However, the cell reliability of 3-D NAND was generally improved when compared directly to planar technologies with the same effective cell area, because the 3-D has larger physical cell dimensions and therefore more total charge representing a given memory state.

Although CTMs such as SONOS were the first form of 3-D NAND, FG-based 3-D NAND flash has also been developed and is in commercial production. The 3-D conventional floating gate (C-FG) architecture utilizes pillars of NAND strings formed by FG cells with a vertical poly channel similar to BiCS [31]. The 3-D FG cell requires a somewhat more complicated cell and process than 3-D CTM due to the need for separately defined and isolated FGs. C-FG 3-D NAND was the basis of the Intel/Micron 256GB MLC/384GB TLC NAND platform [41] and later of the 768-GB Micron platform [38].

D. Radiation Effects in Charge Storage Memories

Charge storage memories are sensitive to TID. The fundamental physical mechanisms by which TID can alter charge stored on the FG cell, first described over three decades ago, are still largely relevant to modern devices [42], [43]. These are described with reference to Fig. 12 [42]. In the first case, the FG cell is in the programmed (or "0") state and is retaining charge. This state is more susceptible to TID than the erased state due to three mechanisms. Mechanism (1) is the generation of charge in the oxides surrounding the FG. The direction of the electric field in a programmed FG cell sends generated carriers into the FG which have the opposite charge as those currently stored within it, effectively reducing the amount of stored charge.

The second mechanism (2) is charge being trapped and remaining in the field effect transistor oxides on both sides of the FG, which can shift V_T. This mirrors the case where charge trapped in a standard MOSFET gate oxide causes the V_T to shift. In this case, the charge in the TO has the greatest effect, because it is closest to the channel. However, the TO is thin (∼8 nm) in modern flash and this thickness is essentially constant with area scaling. Hence, this effect tends to be minor.

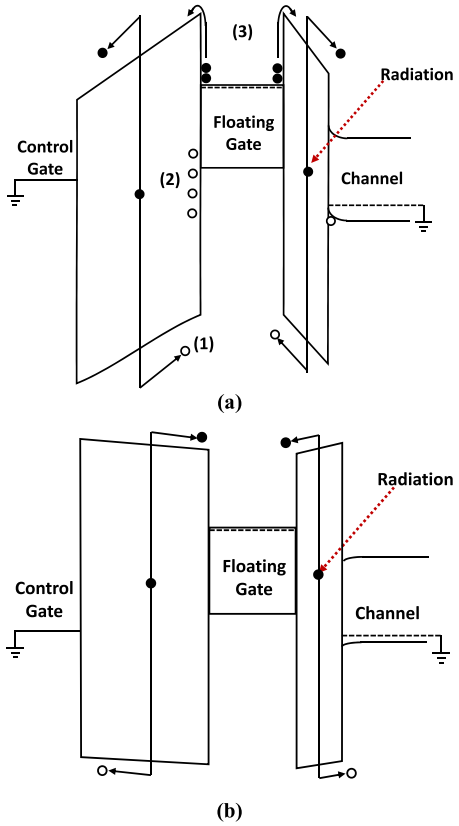

Fig. 12. Basic mechanisms of threshold shift due to ionizing radiation in FG memory in (a) programmed or "0" state and (b) erased or "1" state (based on [42]).

Mechanism (3) occurs when carriers in the FG gain energy from the incident radiation that is higher than the gate to oxide barrier. The FG charge is retained at the edge of the conducting FG, which is subject to the field illustrated in Fig. 12(a), and carriers are photoemitted over the TO. Note that this emission occurs at much lower fields than are required for erasure through FN tunneling. This is analogous to the UV erase band diagram in Fig. 3(c), except that it is without external bias, so the field is not as strong. TID reduces the charge on the FG most when in the programmed state because more charge is stored and a greater field is acting to remove the charge when stimulated by ionizing radiation.

Mechanisms (1) and (3) are dominant in modern FG cells due to the thin TOs. Both effects require a charge on the FG and the resulting field in the TO. In the case of the erased (or "1") device state [Fig. 12(b)], very little charge is stored on the FG, and the field across the oxide is low and in the opposite direction of the programmed state. Therefore, ionizing radiation tends to have much less effect on this erased state than the programmed state as illustrated by the distribution plot in Fig. 13. As described in Fig. 5, errors will occur for the bits with V_T that cross V_{Read}. Errors caused by shifts in the charge storage during retention mode in the FG cell are referred to as "retention errors."

CTMs are also susceptible to TID-induced shifts, due to somewhat different physical mechanisms, related to the behavior of radiation in the insulating CTL. The basic physics of ionizing radiation in CTMs was originally described by

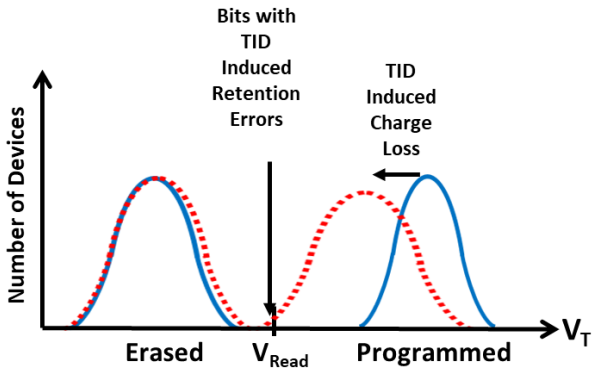

Fig. 13. Qualitative threshold voltage distribution shift due to TID comparing impact of programmed and erased states.

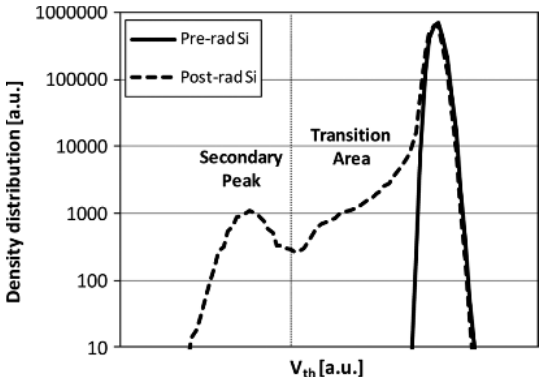

Fig. 14. Threshold voltage distribution of the programmed state illustrating the V_T shift of a portion of the cells due to 121-MeV Si ion strikes (© 2010 IEEE. Reprinted, with permission, from [46]).

McWhorter *et al.* [43] and remain relevant to scaled devices. An electric field exists throughout the CTL (nitride), unlike the FG where the field only exists at the border of the FG and surrounding insulator. In the nitride, electron–hole pairs are generated and in the programmed state, holes are preferentially captured in the nitride. Electrons are likely to be emitted over the reduced energy barrier under the strong internal field of the programmed state. Both effects reduce the V_T. In the erased state, the charged trapping layer continues to preferentially trap holes, but the electric field also assists the emission of holes, a process which increases V_T. Hence, the V_T reduction will be less than the programmed state, and in some cases can be in the same (negative) direction as the shift in the programmed state [44], [45].

Heavy ions also affect the charge state distributions of charge storage memory arrays. Ion strikes cause loss of charge from the FG cell(s) in the path of the ion, affecting the distribution in an array. As with TID, ions have a greater effect on memory states programmed to higher V_T, which have a higher field. For example, Fig. 14 shows the change in V_T distribution of 65-nm FG cells due to 121-MeV Si ion bombardment for the highest V_T state in an MLC bit array [46]. The "secondary peak" represents the group of cells which have been subject to the greatest charge loss. The fine details of charge loss due to ion strikes are the subject of continued research. Models that have been proposed are: 1) the temporary existence of a conducting path that shorts the FG to the substrate [47] and 2) a very fast flux of hot carriers out of the FG [48]. MLCs tend to be more sensitive to ion strike-induced upsets due to the tighter distributions [49]–[51].

In addition to effects of radiation directly on the FG and CTM devices, it is important to consider the effect of radiation in the peripheral circuitry required by a flash memory. A key peripheral block in a flash memory is the charge pump, which is needed to generate the high required program and erase voltages. TID-induced error in NAND flash has been attributed to disrupting the charge pump operation [52], [53]. During the read operation in NAND flash, data must be transferred from the block to a CMOS buffer, which utilizes SRAM. If a heavy-ion strike occurs which upsets the CMOS buffer, this error will be reflected in the read. Further discussion of peripheral errors relevant to FG flash is given in [18] and [54]. As CMOS dimensions have decreased, the effect of TID on transistors has been reduced, and the major source of TID-induced errors in modern flash memory is more commonly the charge storage devices themselves.

1) TID in Advanced FG Memories: Scaled FG flash remains highly sensitive to the effects of TID, although there is not a strong effect of area scaling on the TID response of the FG cell. Several competing effects influence the FG V_T shift in response to TID, which continue to follow the basic mechanisms outlined above (Fig. 12). First, although critical cell dimensions have decreased significantly to increase density, the TO thickness of flash devices has remained around 8 nm to avoid excessive leakage current which would degrade retention [24]. Since the TO is thin, the V_T shift due to trapped charge in the TO (mechanism (2) in Fig. 12) remains negligible. When insulator thicknesses and other factors are equal, reducing the area of the FG cell decreases the ΔV_T for a given TID level [55].

However, experimentally, the opposite was observed when comparing a 65- and 90-nm FG, as illustrated in Fig. 15(a)—ΔV_T was more sensitive to TID for the smaller 65-nm cell. This was attributed to a higher absolute V_T for the programmed 65-nm cell and hence higher TO field, which strongly affects the rate of charge loss under ionizing radiation. In the TID range investigated in Fig. 15(a), ΔV_T is linear with dose, but in general this relationship depends on the nonlinear factors described above and so will not necessarily hold for other programmed V_T levels and other TID ranges [46].

It has become very common in modern flash cells to utilize MLCs and TLCs to improve density. These multibit per cell schemes require tighter V_T distributions, which create reliability challenges, and make the cell more sensitive to TID-induced V_T shifts. As illustrated in the 90-nm device in Fig. 15(b), the higher levels represented by higher absolute V_T values are subject to greater TID-induced shifts due to their increased TO field [46].

The effect of TID on storage and operation of a highly scaled 34-nm SLC and 25-nm MLC NAND flash were comprehensively investigated by Gerardin *et al.* [51], under Co-60 irradiation. As expected, 34-nm SLC cells exhibited a higher TID threshold for retention errors (defined as 1% of bits in error), typically at <80 krad(Si) than 25-nm MLC cells, which were just above 20 krad(Si), given by the green bar in Fig. 16.

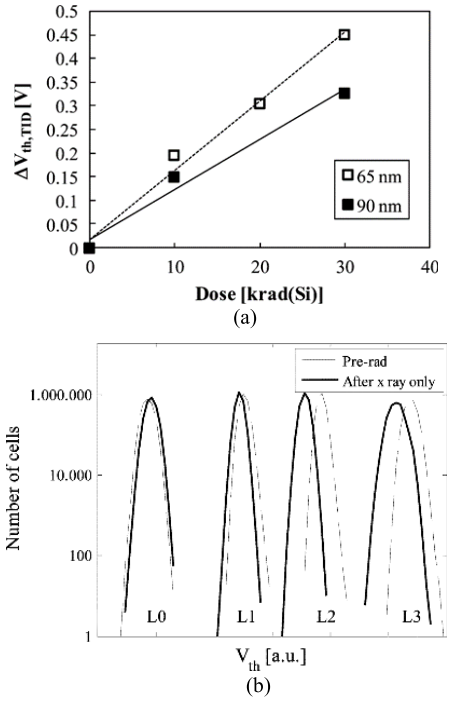

Fig. 15. (a) ΔV_T versus dose for 65- and 90-nm FG cells and (b) V_T distributions for the 90-nm array before and after 20 krad(Si) (© 2010 IEEE. Reprinted, with permission, from M. Bagatin, et al, *IEEE Trans. Nuclear Sci.,* vol. 57, no. 6, pp. 3407–3413, 2010).

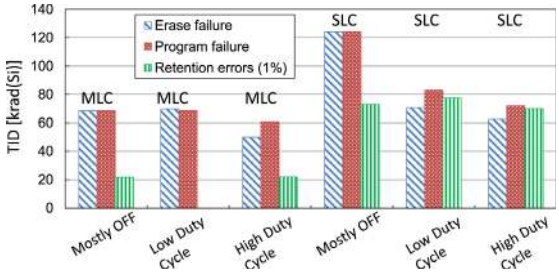

Fig. 16. Summary of 25-nm NAND flash SLC and MLC TID results (© IOP Publishing. Reproduced with permission. All rights reserved. From [49]).

For a given technology, a lower TID level is required to upset an MLC than an SLC, due to the tighter V_T distributions required by an MLC (as in Fig. 6). This is consistent with the finding by Irom *et al.* [56] that such low TID levels were required to upset Micron 25-nm TLC (eight states) die that experiments were discontinued. Later, Gadlage *et al.* [57] showed that this TLC product is so sensitive that the onset of bit errors can be found in following X-ray conditions of a computed tomography (CT) inspection, with a dose of less than 1 krad(Si) (Fig. 17).

It was also found in 25-nm SLC cells that TID errors can occur in both the programmed and erased states [51]. This was unexpected because TID typically affects the programmed state more significantly for reasons described above. The mechanisms by which the erased state was affected were not fully clear. It was suggested that the internal programming scheme might change the stored values of the cell, such that the 0 and 1 states are not represented physically by the usual programmed and erased cells, obfuscating the physical meaning of these results.

Modern high-density flash is increasingly based on the 3-D architectures described above. Radiation effects in 3-D NAND

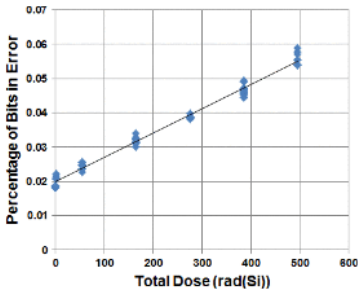

Fig. 17. Bit errors observed in 25-nm NAND technology at less than 1 krad(Si) (© 2013 IEEE. Reprinted, with permission, from [57]).

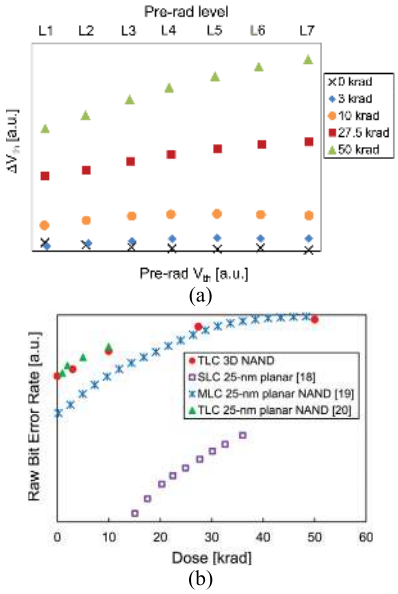

Fig. 18. (a) V_T shift distributions for different levels of Co-60 irradiation for 3-D NAND. Comparison of TID-induced (a) V_T shifts and (b) bit errors between 3-D and scaled planar NAND flash (© 2019 IEEE. Reprinted, with permission, from [58]).

flash is the subject of several recent studies [58], [59]. For example, TID was investigated in the Micron 3-D NAND chip with TLC (8-bit) cells, with the vertical C-FG architecture discussed above [58]. The 3-D cells were irradiated up to 50 krad(Si), and V_T shifts across the seven levels were recorded. The results in Fig. 18(a) illustrate, consistent with 2-D flash, that the magnitude of the V_T shift depended on the quantity of charge stored in the device subject to TID. The greatest V_T shifts occurred on cells with the highest prerad V_T, as these cells had the most charge and greatest TO field.

A major factor determining the sensitivity to TID-induced upsets continues to be the number of bits per cell, with TLC being common in 3-D NAND. As indicated in Fig. 18(b) [58], 3-D NAND has a similar raw BER versus TID as 25-nm planar TLC NAND, despite having a cell area around 50 nm [41]. This corroborates the fact that the effect of TID is significantly more affected by the bits per cell than cell area.

2) SEEs in Advanced FG Memories: FG flash has become significantly more sensitive to SEUs with decreased cell area. This is due to the following reasons. First, the amount of charge required to shift V_T is proportional to the cell area. Hence, a highly scaled cell can be altered by manipulating a smaller quantity of charge than a larger cell to achieve

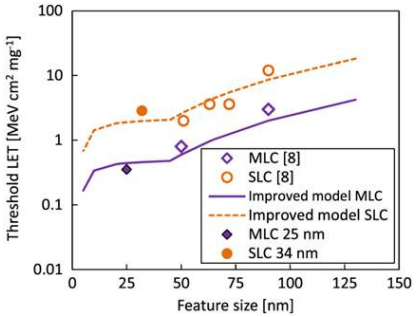

Fig. 19. Upset threshold LET versus feature for several flash technologies (© 2014 IEEE. Reprinted, with permission, from [60]. Includes data from ref [61]).

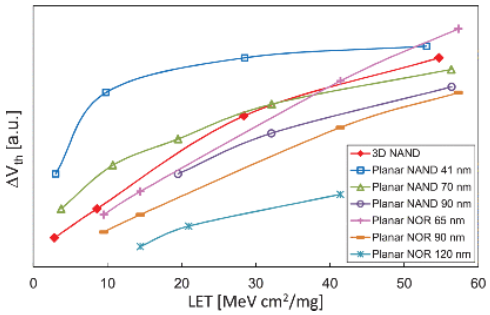

Fig. 20. Upset threshold LET versus feature for comparing 3-D with planar flash technologies (© 2018 IEEE. Reprinted, with permission, from [62]).

an equal V_T shift. However, the absolute V_T range used by memory cells and V_T shift needed to alter the bit state and cause an upset remains relatively constant with scaling. Furthermore, the charge that can be affected by a given linear energy transfer (LET) remains relatively constant. Hence, the minimum or threshold LET (LET_{TH}) to cause a V_T shift great enough to upset the cell decreases. Fig. 19 plots this trend LET versus upset for SLC and MLC technologies for feature sizes ranging from 25 to 90 nm, demonstrating a broad downward trend in LET_{TH} for more scaled devices, with planar, 25-nm MLC cells upsetting at <1 MeV·mg/cm^2 [60]. This trend also demonstrates that, similar to the case with TID, MLCs are more susceptible to upset than a similar SLC. This is further confirmed by the observation by Irom *et al.* [56] that upsets in planar 25-nm TLC occur with more than an order of magnitude higher cross sections at the lowest LET (0.1 MeV · mg/cm^2) tested than the 25-nm MLC cells.

SEEs in 3-D FG products have also been recently investigated [59], [62]. Bagatin *et al.* [62] reported an in-depth heavy-ion study on the Micron 384-Gbit chip using a TLC scheme, specifically studying the V_T distributions of the level 5 (L5) bit, which has a high TO field and is expected to be sensitive to upset. The L5 was chosen rather than the most sensitive bit (in this case, L7) to make a better comparison to the most sensitive bit previously investigated in a 2-D, four-level flash array [62]. A key observation from these studies was that 3-D-NAND SEU sensitivity was reduced significantly from planar cells with areal densities (Gb/mm^2 of silicon) around the 3-D-NAND's equivalent areal density. Although 3-D cells have an equivalent areal density greater and effective cell dimensions smaller than found in highly scaled 2-D flash (<20 nm), the true physical vertical FG dimensions are relaxed and the charge in a single bit cell is increased. The exact gate dimensions and charge

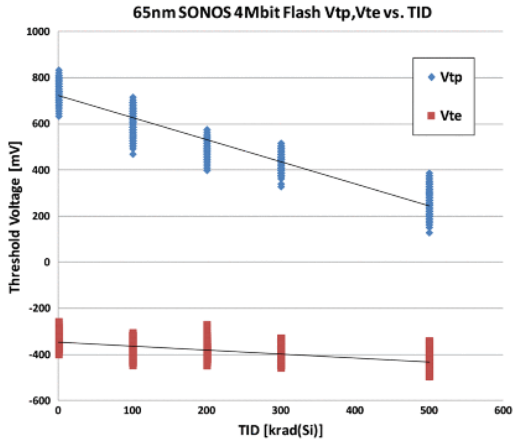

Fig. 21. Effect of TID on threshold voltage of written and erased 65-nm planar SONOS NOR flash (© 2014 IEEE. Reprinted, with permission, from [45]).

volume of the Micron 3-D FG cell are not given, but the number of electrons for a 100-mV V_T shift put the vertical cell in the range of 50-nm technology, despite an equivalent areal density feature size of ~13 nm [41]. The V_T shift for a given LET is significantly lower than that of the 41-nm planar NAND and somewhat better than 70-nm planar technologies, as illustrated in Fig. 20. For additional detail regarding the radiation effects in scaled FG-based NAND flash, the reader is referred to reviews [49] and [54].

3) Radiation Effects in Advanced CTMs: Scaled 2-D SONOS cells exhibit a shift in V_T distributions qualitatively similar to earlier generations, with a significantly greater effect on the programmed distribution than that of the erased cells [44], [45]. As with FG memory, the relationship between ΔV_T and TID is not strongly dependent on the area of the charge trapping cell, but will be affected by other factors that differ between generations such as the programmed V_T and corresponding TO field. The effects of Co-60 on the programmed and erased V_T distributions of the Cypress 65-nm SONOS device are plotted Fig. 21. These results can be explained by the mechanisms described above, with more significant charge lost from the programmed state. Hole trapping rather than emission of holes appears to dominate the erased state response because even in the erased state the ΔV_T occurs in the negative direction. As with earlier generations, CTMs continue to exhibit a significantly lower sensitivity to TID than their FG counterpart at the same node. Following 500 krad(Si), the SONOS distribution of the programmed cells have shifted about 500 mV whereas, in contrast, the 65-nm FG [plotted in Fig. 15(a)] shifts nearly 500 mV after about 30 krad(Si).

Cypress recently presented results on radiation testing of their 40-nm embedded NOR SONOS cells [63]. The programmed cell distribution exhibited an average ΔV_T shift of about 1 V following a TID of 500 krad(Si) and only a slight decrease in the erase distribution [Fig. 22(a)]. This suggests that data storage is possible at 500 krad(Si) with minimal error correction. Furthermore, heavy-ion testing revealed a tail distribution for the programmed state (similar to that of FG) starting at an LET of 20 MeV·cm^2/mg [Fig. 22(b)], higher than for similar 65-nm FG NOR devices, which start to experience upsets at ~10 MeV · cm^2/mg (Fig. 20).

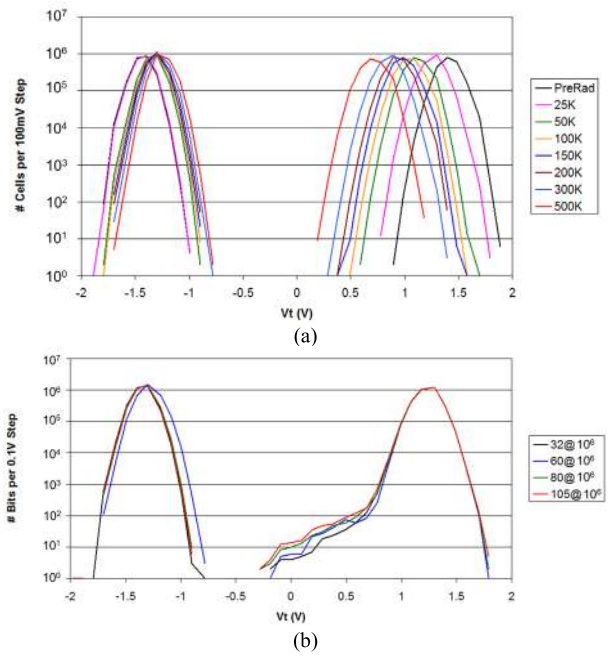

Fig. 22. (a) TID response and (b) heavy-ion response of a 40-nm embedded NOR SONOS cell. © 2020 Helmut Puchner, used with permission, from [63].

TID has also been investigated in a prototype 3-D SONOS structure that was developed by Imec, Leuven, Belgium, with 45-nm polysilicon channels [Fig. 23(a) and (b)] [64]. Consistent with 2-D SONOS and FG cells, the average V_T of the erased state is shifted less than that of the programmed state [Fig. 23(c)]. However, in the erased state, there is a slight increase in V_T due to TID, indicating that the preferential trapping of holes is slower than the emission of holes from the nitride, similar to the SNOS device studied by McWhorter *et al.* [43].

Chen *et al.* [65] investigated SEU behavior in a 128-Gb Hynix 3-D CTM product. The SEU susceptibility was found to be much lower in the SLC mode than in the MLC mode, as with other flash technologies. The SEU cross section of the 3-D Hynix array in the MLC mode was compared with the Micron 16-nm 128-Gb FG MLC planar product and found to be similar despite the differences in both scale and physical storage mechanisms. Without the information on the physical cell size, threshold voltage levels, or distributions, it is difficult to speculate if this result implies a difference in the cell-level susceptibility of the charge trapping and FG devices. The 3-D memory had a reduced susceptibility to MBUs, and a strong dependence on angle as compared to the planar array—requiring careful testing at different angles to fully understand the susceptibility. Continued work is needed to investigate commercial high-density vertical charge trapping storage technologies, such as Samsung V-NAND, for suitability in environments with significant ionizing radiation.

III. Emerging Memory Technologies

Although flash continues to dominate the commercial market, emerging memories offer significant advantages in scalability, endurance, write speed, write voltage, and energy. Foremost among these are STT magnetic memory (STT-MRAM),

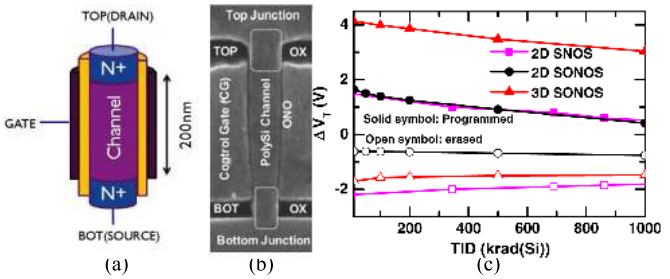

Fig. 23. (a) Illustration and (b) cross section of a scaled 3-D SONOS cell. (c) Comparison of the V_T shift in response to TID for the 3-D SONOS versus earlier 2-D generations (© 2014 IEEE. Reprinted, with permission, from [64]).

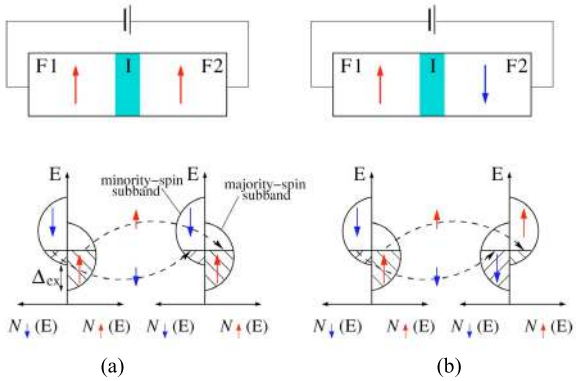

Fig. 24. (a) P and (b) AP MTJ band diagrams (Reprinted figure with permission from [69] Copyright 2004 by the American Physical Society).

oxide-based resistive memory (ReRAM), conducting bridge memory (CBRAM), and phase change memory (PCRAM), which are the topic of the remainder of this review.

A. STT Magnetic Memory

STT-MRAM is a low-voltage, resistance change memory technology that is compatible with BEOL CMOS processing. Embedded STT-MRAM (eMRAM) is currently in production at nodes as small as 22 nm [66] and standalone at 28 nm [7]. Currently, there is interest in using STT-MRAM technology for an array of applications including industrial and automotive embedded systems, IoT, industrial and broad consumer electronic products. Due to the low power and high speed, there is interest in using STT-MRAM as an embedded cache memory [67]. STT-MRAM is relatively insensitive to radiation and hence is considered promising for future radiation-hard electronics [68].

Magnetic memory is based on a structure known as a magnetic tunnel junction (MTJ), comprised of two ferromagnetic conductive layers separated by a thin insulator that acts as a tunnel barrier (see Fig. 24). In order to understand the MTJ physics, it is useful to consider the two cases of the device illustrated in Fig. 24(a) and (b). In the first case, both ferromagnetic layers F1 and F2 are oriented in the same direction. When current passes through the first ferromagnetic layer (F1), the electron spin is preferentially polarized in the direction of this layer's magnetization [Fig. 24(a)]. If the second ferromagnetic layer (F2) is polarized in the same direction as F1 [parallel (P)], an abundance of states exist for

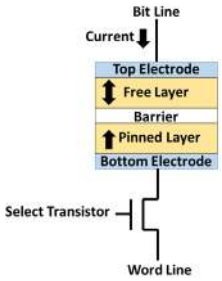

Fig. 25. MTJ-based memory cell with select transistor.

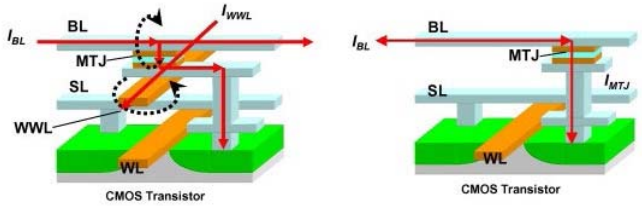

Fig. 26. (a) Toggle MRAM and (b) STT-MRAM device structures (Reprinted from [73], © 2012 with permission from Elsevier).

the electron to transfer to after it tunnels through the insulator. In the second case, the F2 layer is has a magnetization direction opposite to F1 [antiparallel (AP)] [Fig. 24(b)]. This time, when current passes from F1 through the insulator, there are fewer states in F2 for it to travel. Hence, the current flowing in the second AP case is lower than that of the first P case. In terms of AP resistance (R_{AP}) and P resistance (R_P), it can be stated that $R_P < R_{AP}$. For details of the physics of this process, the reader is referred to reviews [69]–[72].

The most important metric of an MTJ is the tunnel magnetoresistance (TMR) ratio, which is calculated from R_P and R_{AP} as follows:

$$\text{TMR} = \Delta R/R = (R_{AP} - R_P)/R_P.$$

Early MTJs had TMR below 100%, but significant improvements in TMR helped advance magnetic technology in the early 2000s [73]. Parkin *et al.* [74] demonstrated 220% TMR in a CoFe/MgO/CoFe MTJ, where all three layers were (100) oriented following careful annealing. Shortly after this in early 2005, Djayayprawira *et al.* [75] demonstrated 230% TMR in CoFeB/MgO/CoFeB, where the MgO layer became (001) oriented after deposition on the amorphous CoFeB substrate. MTJs can have two orientations of magnetization: in-plane magnetoanisotropy (IMA or iMTJ), where the magnetization is oriented in the direction of the MTJ layer plane (as in Figs. 24 and 27) and perpendicular magnetoanisotropy MTJ (PMA or pMTJ), where it is perpendicular to this plane, as shown in Fig. 25 [76]. PMA has advantages of lower switching current and hence greater scalability. However, practical realization of PMA MTJ was elusive until 2010, when Ikeda *et al.* [76] demonstrated a PMA Ta/CoFeB/MgO/CoFeB/Ta structure with reasonable TMR (120%) that was scalable to 40 nm. This remains the basic material stack utilized in modern scaled MRAM cells.

An MTJ can be used as the storage element of a memory by manufacturing one of the layers (such as F2 in Fig. 24)

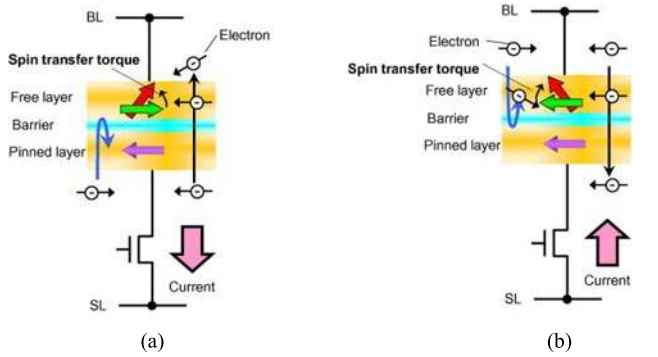

Fig. 27. (a) AP to P and (b) P to AP switching with the STT effect (Reprinted from [73], © 2012 with permission from Elsevier.).

such that the magnetization does not change during normal operation of the device. This is referred to as the pinned layer (PL). The other ferromagnetic layer is manufactured such that it is free to change the magnetization from P to AP, which is known as the free layer (FL) (Fig. 25). When the magnetization of pinned and reference layers are P, the resistance is low and the memory state is "0," and when they are AP, the resistance is high, and the memory state is "1." The MTJ memory element always has a select transistor, which isolates it from the surrounding devices in an array (Fig. 25).

The first mainstream memory based on the MTJ element was programmed using a magnetic field generated by an electric current via ampere's law, known as field switched MRAM. The bit is read by measuring the resistance across the MTJ. One of the challenges of this early field switched MRAM device is the tendency for the high field write line to disturb unselected devices along this line during the write operation. An improved version of structure (shown in Fig. 26) known as toggle MRAM was invented by Motorola, Chandler, AZ, USA, in 2003, which addressed this issue and reduced the half-select write challenges [77], [78]. The toggle MTJ employs synthetic antiferromagnet (SAF) free and PLs to enable a write scheme which only programs the bit if it is determined it needs to be switched. Commercial products based on toggle MRAM have been produced since 2006 [79], originally by Freescale and more recently by their spinoff, Everspin. The toggle-switched MRAM is also the basis of radiation-hardened MRAM products [80].

Field-switched MRAM (including toggle MRAM) require large currents to produce the magnetic field required to switch the cell, limiting their power efficiency and scalability. The industry has overcome this problem by harnessing the STT effect, which was discovered by Berger [81] and Slonczewski [82] in 1996. In the case of the STT effect, current is passed directly through the MTJ to change the state of the FL [Fig. 26(b)].

Fig. 27 illustrates the physic of STT switching. We first consider the case where the FL and PL start in the AP state and switch to the P state. In this case, illustrated in Fig. 27(a), current is applied such that electrons are injected from the PL to the FL. These electrons with spin opposite to the PL are filtered, hence, only the electrons with the same spin

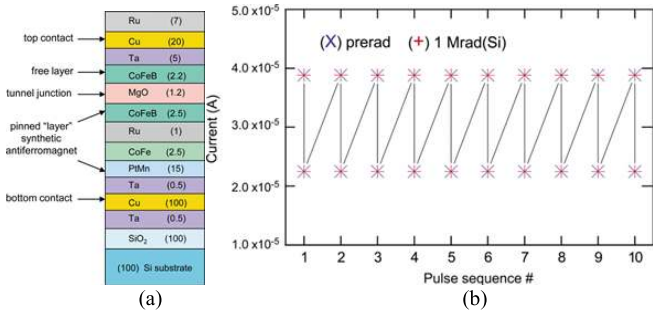

Fig. 28. (a) MTJ stack and (b) pre- and post-TID Co-60 exposure resistance switching curves for in-plane STT device structures (© 2012 IEEE. Reprinted, with permission, from [86]).

orientation as the PL enters the FL. The STT exerted in the FL by these polarized electrons causes the FL to align to the spin of the electrons, which is P to the PL. Now consider the case where the state is changed from P to AP illustrated in Fig. 27(b). In this case, current is applied such that electrons flow from the FL to the PL. As they pass through the FL, those with the opposite spin from the PL are reflected back into the FL at the boundary. These reflected electrons exert an STT on the FL which will causes it to change to the opposite magnetization as the PL and increase the magnetic tunnel resistance of the junction.

STT-MRAM has been under commercial development for over a decade by several major foundries including IBM, NY, USA, Samsung, Hwasung, South Korea, Intel, Hillsboro, OR, USA, and Motorola (transitioning to Freescale and later Everspin, all in Chandler, AZ, USA). Excellent performance, scalability, and reliability have been demonstrated. For example, at IEDM 2019, Everspin detailed their 1-Gbit STT-MRAM chip capable of $>10^{11}$ cycles and 10-year retention at 85 °C, integrated with 28-nm CMOS [7]. Prototypes have been demonstrated with switching times of <3 ns [83] as well as switching currents <35 μA and voltages <200 mV [84].

The MTJ is relatively insensitive to radiation effects because, unlike charge-based storage devices, there is not a known mechanism of interaction between an MTJ and ionizing radiation. Field-switched MRAM has been used in radiation-hardened memory products [80], [85]. Fewer studies have been performed in the modern STT cell, especially the most scalable technology which utilizes perpendicular magnetic anisotropy (PMA or pMTJ). SEEs such as SEFIs are observed in commercial MRAM but are most often attributed to peripheral circuitry rather than the memory device itself. However, as discussed below, there have been reports of device level bit flips in highly scaled pMTJ-based STT-MRAM.

Ren *et al.* [87] demonstrated the relative insensitivity of STT-MTJ to TID by assessing the field coercivity (H_c) and TMR of an in-plane STT-MTJ stack based on MgO tunnel barrier and CoFeB FM layers. There was no perceptible change in TMR or coercivity (H_C) following 10 Mrad(Si) of Co-60 gamma irradiation. Hughes *et al.* [86] investigated the effects of Co-60 and 2- and 200-MeV protons on in-plane magnetic anisotropy STT-MTJ structures with MgO tunnel barriers which were not integrated with CMOS. The report concluded that there was no effect in switching characteristics, retention, current-in-plane tunneling, or ferromagnetic

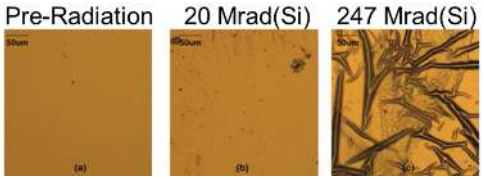

Fig. 29. MTJ stack preradiation and following 20- and 247-Mrad(Si) gamma exposure (© 2019 IEEE. Reprinted, with permission, from [89]).

resonance as a result of up to 10-Mrad(Si) Co-60 gamma and proton fluence of 1×10^{12} protons/cm^2 (2- and 220-MeV protons), as illustrated in Fig. 28(b). A very slight decrease in resistance of the FL resistivity was noted following 2-MeV proton exposure, possibly due to displacement damage. An avalanche 55-nm commercially available STT-MRAM product was also evaluated for TID up to 2 Mrad(Si), with no failures observed, although a slight increase in standby power occurred due to the peripheral transistors [88].

Wang *et al.* [89] investigated higher levels of gamma irradiation in CoFeB/MgO perpendicular MTJ, with total dose as high as 475 Mrad(Si) in order to simulate deep space mission conditions. At the highest levels of 247 and 475 Mrad(Si), the films effectively lost their ferromagnetic nature and even started physically cracking (see Fig. 29). However, at levels of 10 and 20 Mrad(Si), the magnetic coercivity was degraded only slightly.

Displacement damage on modern STT-pMTJ arrays was studied recently by Xiao *et al.* [90], by subjecting set of about 25–70 MTJs without transistors, with dimensions of 80–115 nm to 3-MeV Ta fluences ranging from 10^9 to 10^{14} ions/cm^2. Following exposures of 10^{11} ions/cm^2 and less, no effect was observed in the switching properties before and after exposure. Following 10^{12} ions/cm^2 exposure, minor degradation of switching functionality is observed, which would not preclude normal memory functionality. At fluences of 10^{13} ions/cm^2 and above, switching functionality is lost due to severe damage in the interface, FL, or PLs, with the exact nature of the degradation still under investigation [90].

Heavy-ion effects were on 256-Mbit commercial STT-MRAM arrays without supporting circuitry were studied by Honeywell, Plymouth, MN, USA [68]. These were observed to be free of permanent errors up to as high as 84 MeV $\cdot$ cm^2/mg [68]. This was found to be an improvement over the field-switched toggle MRAM, which did exhibit some permanently shorted bits following strikes with LET >70 MeV $\cdot$ cm^2/mg [85].

Damage and bit upsets induced by heavy ions were studied by Kobayashi *et al.* [91], specifically investigating the effect of 15-MeV silicon atoms on the CoFeB/MgO/CoFeB pMTJ devices with a diameter of 70 nm and did not find resistance change. Later, the same group found that single-event bit flips can occur in an MTJ cell resulting from heavy-ion exposure, depending on both the LET and properties of the bit [92]. In this second study, MgO/CoFeB pMTJ with diameters between 40 and 80 nm were subject to heavy-ion bombardment. It was found that bit flips occur at a threshold LET of about 15 MeV $\cdot$ cm^2/mg [with 400-MeV Fe; see Fig. 30(a)]. Following a bit flip, some permanent heavy-ion

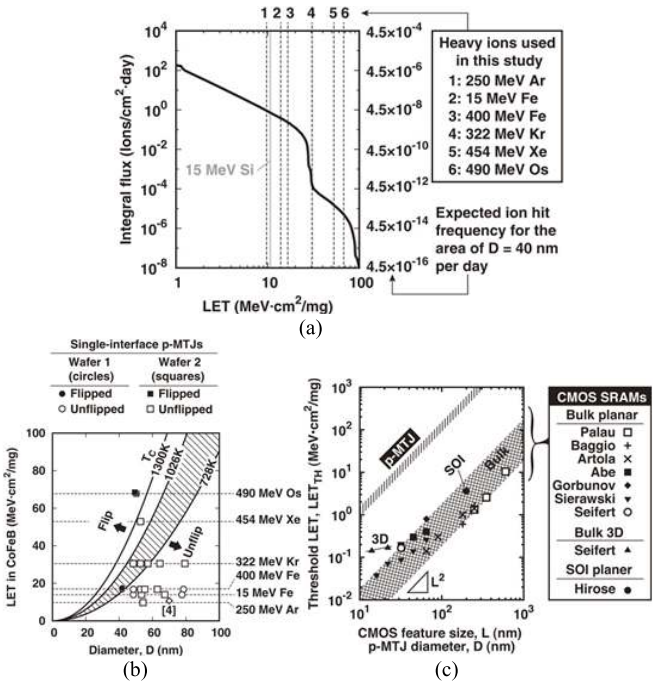

Fig. 30. Single-event bit flips for p-MTJs: (a) Integral flux versus LET for ions used in experiment. (b) LET in CoFeB versus diameter of the p-MTJ. (c) Summary of LET versus feature size/bit diameter for the experiment described in the text. Copyright (2017) The Japan Society of Applied Physics. Reprinted with permission, from [92].

damage appeared as a minor distortion of the magnetic hysteresis loop, but the cell was rewritable. In addition to LET, the response depended on the area of the MTJ. The likely cause was speculated to be heating imparted on the FL by the ion, which is a function of area and LET. The behavior is plotted as a function of LET versus bit diameter in Fig. 30(b). The area-dependent model is used to extrapolate the sensitivity of pMTJs scaled down to 10 nm [Fig. 30(c)].

SEE has also been studied in the avalanche 55-nm pMJT-based MRAM product. Following exposure to a range of heavy ions, SEFIs were observed when the product was struck during the read or write operations [88]. It was found that all bit errors could be cleared by restarting, and no permanent errors occurred. The SEFI cross sections during read and write versus LET were consistent between NSWC Crane and NASA, plotted in Fig. 31 [88], [93].

B. Oxide-Based Resistive RAM

Oxide-based resistive switching RAM (OxRAM), often abbreviated ReRAM, RRAM, or OxRAM, is a two-terminal resistive device which uses the electrically induced resistance modulation due to vacancy motion in metal oxides as the basis of memory. ReRAM is a scalable, low-voltage bit cell technology being developed in the 22- [94], 28- [10], 40-nm [95] nodes for embedded applications such as automotive, IoT, and less traditional applications such as neuromorphic computing and hydrogen sensing [95]. As discussed below, it is also relatively insensitive to radiation effects [21] and holds promise for future radiation-hard NVM.

The typical ReRAM cell is an electrode/oxide/electrode stack, where the most common oxides are tantalum oxide (TaO_x) [96], [97], hafnium oxide (HfO_x) [98], tungsten

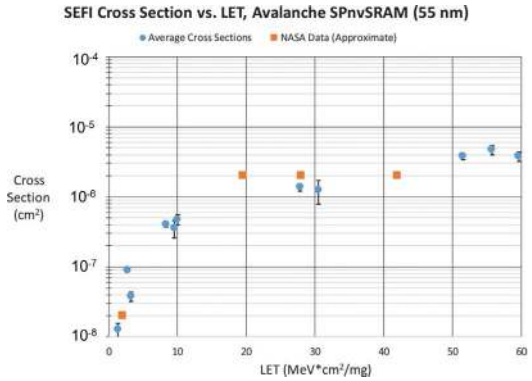

Fig. 31. SEFI cross section versus LET in a 55-nm avalanche STT-MRAM (© 2019 IEEE. Reprinted, with permission, from [88]).

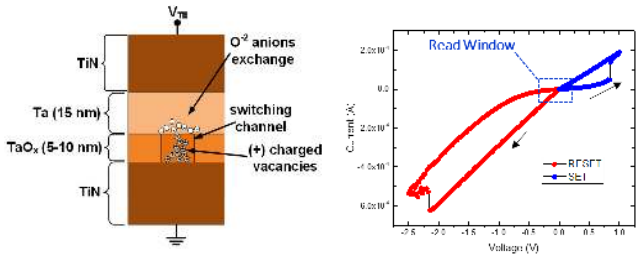

Fig. 32. (a) Sandia TaO_x ReRAM cell and (b) typical ReRAM cycling.

oxide (WO_x) [99], and titanium oxide (TiO_2). However, resistance switching has been demonstrated in a large variety of materials, including oxynitrides and nitrides [100]. It is desirable for the metal oxide to be substoichiometric, such that the oxide has a significant number of vacancies. In some cases, these oxides are deposited substoichiometrically using reactive sputtering [101]. In other cases, a stoichiometric oxide is deposited and one of the electrodes is used to get oxygen vacancies from the oxide. In bipolar ReRAM, one of the electrodes is reactive with the metal oxide, such that the metal to oxide barrier is reduced and an ohmic contact is formed. This "ohmic electrode" is commonly made of Ta, Ti, or Hf. The second electrode is typically inert and forms an interface with a Schottky barrier. Common Schottky electrodes include TiN and Pt, the former being most common in CMOS-compatible processes.

The forming and switching processes can be explained with reference to Sandia's TiN/Ta/TaO_x/TiN ReRAM shown in Fig. 32. In this device, the ohmic electrode is Ta and the Schottky electrode is TiN. Both materials were chosen to be compatible with a standard CMOS fab.

When the ReRAM cell is first fabricated, it is typically at a high-resistance state. Prior to nonvolatile resistance switching functionality, the oxide must undergo a soft electrical breakdown, referred to as electroforming. Electroforming is typically done by applying a positive voltage pulse, ramp, or repeated positive pulse on the reactive electrode [Ta in Fig. 32(a)]. The voltage must be of sufficient magnitude and duration such that oxygen anions are mobilized and removed from the oxide. When oxygen starts to leave the switching oxide in a local area known as the switching channel, the resistance rapidly drops, more current flows, and a positive

feedback event occurs where this region quickly becomes conductive [see the switching channel in Fig. 32(a)]. It is important to control the duration and maximum current of the forming process; otherwise, it is possible to quickly cause permanent damage to the switching channel, rendering it impossible to switch the cell.

Following the electroforming process, it is possible to return some of the oxygen anions or remove some of the oxygen vacancies from the channel by applying a negative voltage ramp or pulse to the ohmic electrode. This shift from low to high resistance is known as the reset process. It should be noted that this reset process does not return the device to the as-manufactured state, but a state that is higher in resistance than the low-resistance electroformed state. As with electroforming, ionic motion is facilitated by a combination of joule heating which increases the ionic mobility and ion drift in the electric field. Thermal effects such as the Soret effect may also play a role in switching [102]. Upon the next application of a positive voltage, oxygen is again removed, and the device returns to a low-resistance state. This is the set process. The resistance can be read by applying a voltage well below the set or reset voltages and measuring the current.

ReRAM has many favorable memory properties. Unlike STT-MRAM, the typical resistance ratio of reset to set resistance is routinely an order of magnitude or more. Endurance of up to 10^{12} cycles has been recorded in individual TaO_x ReRAM cells [103]. The switching voltages are on the order of 1–3 V. Switching times of less than 10 ns are common; switching can occur in sub-1-ns timescales [104]. Scalability down to <10 nm has been demonstrated [98], which could enable very dense memory arrays. Samsung has developed a 3-D ReRAM process which would enable many layers without additional photolithography steps, potentially providing a path to cost-per-bit that is competitive with NAND [105]. Several major foundries have developed prototypical ReRAM processes, including Samsung, Hwaseong, South Korea [105], TSMC, Hsinchu, Taiwan [106], and Intel, Hillsboro, OR, USA [94]. ReRAM is not in wide-scale product use as of 2020, although the technology may be available to general foundry users in the near future. While early work studied a variety of switching oxides, currently the field has coalesced to focus largely on TaO_x- and HfO-based cells.

ReRAM is one of the newest memory technologies that has entered the mainstream. The detailed physics of operation is still the subject of active research and debate. Reliability remains a major challenge, especially regarding differences in electrical properties in cells in an array and even variation between set and reset cycles in the same cell. This is further confounded by the fact that there are multiple switching oxide materials; in some cases, the same material can have different properties (such as amorphous versus polycrystalline) all of which can affect the switching properties.

Now we consider the effects of TID, displacement damage, and SEE in ReRAM. Being a newer technology, there are some inconsistencies in the literature, and there is not a complete understanding of radiation effects in ReRAM. In addition, early radiation effects studies often used prototypical devices fabricated at a university or research laboratory, where

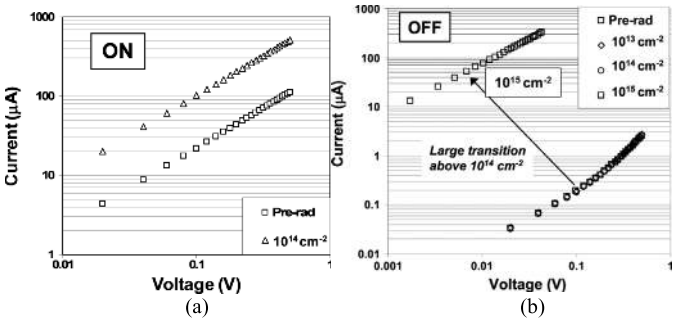

Fig. 33. (a) Change in state for a TiO_2 ReRAM (memristor) in the (a) "ON" (low resistance) and (b) "OFF" (high resistance) states, following listed doses of 1-MeV alpha particles. (© 2011 IEEE. Reprinted, with permission, from [113]. In (b), the 10^{15} cm^{-2} curve is indicated by the box.)

robust reliability and fabrication consistency were not always possible. However, as with MRAM, there is not a direct mechanism of interaction of ReRAM with radiation, and therefore ReRAM is generally insensitive to radiation effects. For a very comprehensive literature review of detailing radiation effects in ReRAM and CBRAM, the reader is referred to [21].

The earliest radiation effects studies tended to focus on TiO_2-based devices, as this was initially a material of technological interest. However, TaO_x- and HfO_x-based devices demonstrated improved properties and subsequently became the materials of primary technological relevance, which is still true today.

Regarding TID, as a general trend, ReRAM cells typically do not show significant changes in switching properties following exposure, although subtle effects have been observed. As with STT-MRAM, this is expected because there is not a significant mechanism by which ionizing radiation can alter the resistance of the oxide cell, which would require displacing or moving oxygen atoms to alter the switching channel. In one of the first studies of radiation effects in ReRAM, TiO_2 devices were exposed to an effective dose of 45 Mrad(Si) of Co-60 gamma irradiation and 23 Mrad(Si) of 941-MeV Bi, where the latter was calculated to be predominantly ionizing dose and not displacement damage [107]. The high- and low-resistance states were not found to change due to the exposure, and cycling was possible following the experiment.

The first TID study in TaO_x showed some effect at low levels of X-ray irradiation, but this was attributed to variability in the cells and not observed with gamma irradiation at similar levels [108] or seen in later X-ray experiments up to 18 Mrad(Si) [109]. Bi *et al.* [110] studied the effect of 10-keV X-ray irradiation on Imec's 55-nm HfO_2/Hf devices, observing no changes up to 7 Mrad(SiO_2). Later, Weeden-Wright *et al.* [111] of the same research group found that no change occurred in cycling characteristics after exposing a CMOS-integrated HfO_x cell to 1 Mrad(Si) from 10-keV X-ray irradiation, despite some effect on the CMOS transistor itself. Fang *et al.* [112] studied the effects of 5.2 Mrad(HfO_2) of Co-60 gamma irradiation on HfO_x resistive memory cells and found no significant change in switching properties, but observed some degradation of high-resistance state retention, which was attributed to the breaking of Hf–O bonds.

ReRAM is also relatively insensitive to moderate levels of displacement damage, beyond which it is possible to

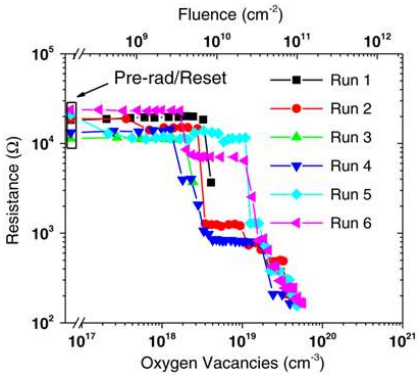

Fig. 34. Change in resistance for the OFF-state of a TaO_x ReRAM device structure following listed doses of 800-MeV alpha particles (© 2013 IEEE. Reprinted, with permission, from [109]).

reduce the device resistance. In 2011, Barnaby *et al.* [113] demonstrated a drop in the low-resistance (ON) state and a larger drop in the high-resistance (OFF) state following alpha ion bombardment of 10^{14} ions/cm^2, as illustrated in Fig. 33. Cycling between the states was still possible even after an exposure of 10^{15} ions/cm^2. The decreased resistance was hypothesized to be the result of additional oxygen vacancy creation, increasing the doping concentration and lowering the resistance in the switching region.

This was consistent with results showing that displacement damage caused by 800-keV Si atoms on a TaO_x ReRAM device was observed to cause a drop in resistance proportional to the fluence [108]. This was also attributed to an increase in oxygen vacancies in the switching region. Later results from the same group demonstrated a resistance drop in the OFF-state in similar TaO_x devices under 800-keV Ta ion irradiation, starting at a fluence of about 10^{10} ions/cm^2, which was calculated to create 10^{18}–10^{19} vacancies per cm^{-3} in the oxide (see Fig. 34) [109]. Following the resistance drop, the devices could be reset to recover the high-resistance state, although the maximum resistance that the device could reach was reduced. This is consistent with the hypothesis that an increase in vacancies due to displacement damage increases the conductivity when the damage exceeds a material-dependent threshold.

SEEs in ReRAM cells and early products have also been investigated. Bennett *et al.* [114] studied and modeled SEEs in a 1T1R Hf/HfO_2-based ReRAM cell with bit dimensions of 105 nm × 120 nm, as illustrated in Fig. 35(a). The cell was subject to heavy ions and biased with increasing voltages at each LET until state changes occurred. The ReRAM was found to switch from the high-resistance state (∼100 kΩ) to flip to the low-resistance state (∼10 kΩ), only under biases of greater than 0.65 V. As plotted in Fig. 35(b), the bias voltage required for a single-event-induced bit flip decreased with increasing LET. The 1T1R cell in Fig. 35(a) illustrates that the bias across the ReRAM bit necessitates a bias across the drain of the connected transistor. This suggests the increasing bias across the transistor enabling an increased current pulse on the bit during the strike. Another interesting finding was that a bit can experience multiple upsets, each with a small resistance change. The cumulative result was the gradual switching of the high-resistance to the low-resistance state. Due to the

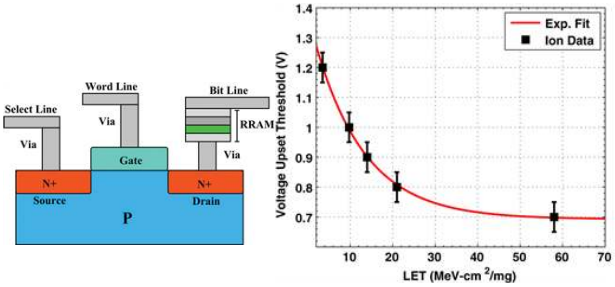

Fig. 35. (a) Imec 1T1R ReRAM bit cell and (b) plot of LET required for an SEU in the biased ReRAM bit versus bias (© 2014 IEEE. Reprinted, with permission, from [114]).

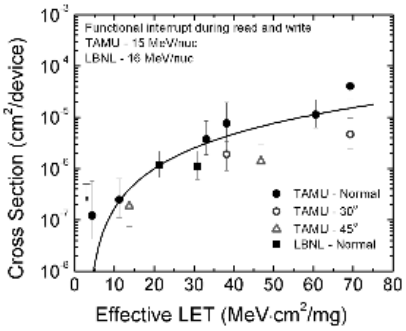

Fig. 36. Panasonic commercial ReRAM MCU SEU cross section versus LET (© 2014 IEEE. Reprinted, with permission, from [116]).

relatively small time in which a ReRAM bit is biased during operation, the work concluded that bit upsets in a real product are unlikely.

The conclusion that bit-level upsets are unlikely is supported by several other findings. Alayan *et al.* [115] that a TiO_2/HfO cell experienced no upsets for changes following unbiased heavy-ion irradiation exposure to LET of 59 MeV · cm^2/mg. The authors' modeling does suggest that a read bias may enable an upset to occur. This was consistent with an investigation of SEE in the commercially available Panasonic ReRAM-based microcontroller product reported by Chen *et al.* [116]. In this work, the microcontroller was subject to heavy ions (using the Texas A&M University Cyclotron) and laser pulses [116]. No static memory bit flips were observed under either case, with ion LET as high as 70 MeV · cm^2/mg. As with the avalanche STT-MRAM, SEFIs were observed during the read and write processes with cross sections plotted in Fig. 36. Additional experimentation targeting the array verified that bit upsets could be attributed to effects in the CMOS periphery, and the ReRAM bits themselves did not switch.

C. Conducting Bridge RAM

CBRAM, also known as the programmable metallization cell (PMC) or electrochemical metallization cell (EMC), is a two-terminal resistive memory. The memory state is written by forming and removing a metallic filament through a dielectric. This low-voltage, BEOL CMOS-compatible scalable memory device was originally invented and developed in the late 1990s at Arizona State University, Tempe, AZ, USA [117] and has matured to the point where high-density CMOS-integrated CBRAM arrays have been demonstrated [118]. Commercial

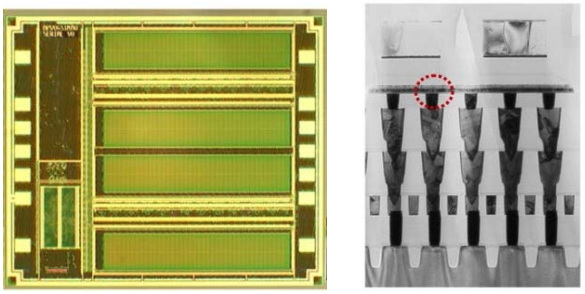

Fig. 37. Adesto Ag/GeSe CBRAM integrated in 130-nm BEOL process (Reprinted from [119], © 2011 with permission from Elsevier).

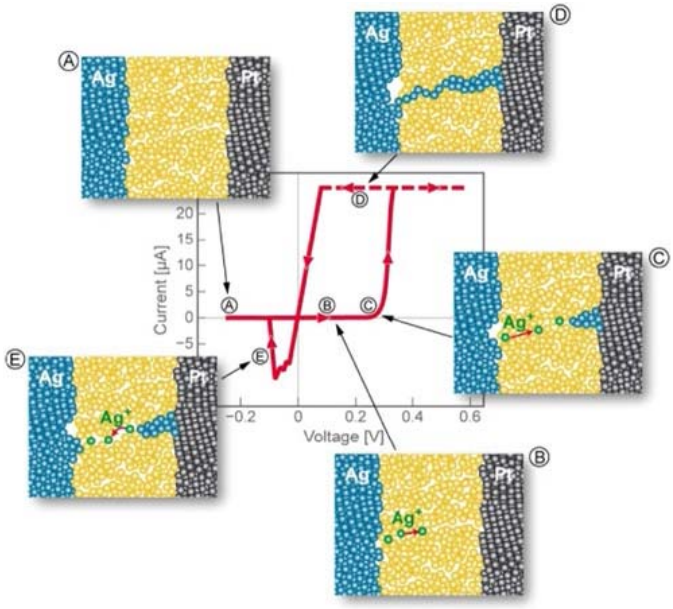

Fig. 38. CBRAM cell operation as described in the text (© IOP Publishing. Reproduced with permission. All rights reserved. From [123]).

products have been available since 2012 from Adesto (now Dialog Semiconductor, Santa Clara, CA, USA), such as the die and cross section shown in Fig. 37 [119], [120]. As with other resistive memories, CBRAM is relatively insensitive to radiation effects and may be a future radiation-hard memory candidate. As we will see, this memory element has some similarities and marked differences from the oxide ReRAM device, as discussed above.

The CBRAM structure is similar to ReRAM, with two conductors surrounding an insulating dielectric. However, CBRAM typically utilizes Ag or Cu as one of the electrodes and an inert metal as the other. The dielectric can be an oxide, such as SiO_2 or Ta_2O_5, but is also commonly a chalcogenide such as GeSe or GeS [121]. A comprehensive list of materials can be found in [122]. As with ReRAM, CBRAM is bipolar, where a positive bias pulse or ramp is used to switch to a low resistance and vice versa.

An example Ag/dielectric/Pt cell and current–voltage (*IV*) curve is presented in Fig. 38 [123]. Device operation can be described with reference to Fig. 38, where the yellow is a generic dielectric. Initially, the two metal electrodes are smooth, and the resistance is high. Upon application of a positive voltage to the Ag electrode, an Ag atom can now react with an available electron and ionize to the Ag^+ state (B). The

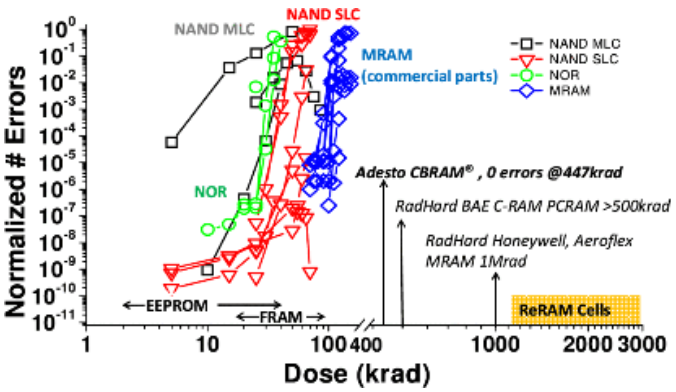

Fig. 39. TID effect on the retention errors of Adesto CBRAM versus other NVM technologies (© 2014 IEEE. Reprinted, with permission, from [122]. References for other TID data provided therein).

Ag^+ ion is now free to drift under the electric field toward the Pt electrode. When the ion reaches the electrode, it will lose the positive charge and start to form a solid agglomeration of Ag on the Pt electrode, which is the start of a filament (C).While the Ag electrode is positively biased, the Ag^+ ions continue to drift and attach to the Ag filament, until eventually a complete connection is formed, and the conductivity rises dramatically. The device is now in the low resistance or SET state. It can be returned to a higher-resistance state (which is typically lower than the fresh device resistance) by reversing the polarity. The Ag atoms in the filament become ionized and drift back to the Ag electrode, returning the cell to a high-resistance state.

The conducting bridge switching process has been demonstrated to have significant potential as a scalable, low-energy memory. Endurance as high as 10^{10} has been demonstrated in Ag/GeSe research devices [124]. Early commercial development by Infineon, Munich, Germany, demonstrated Ag/GeSe cells with scalability down to 20 nm with a prediction of 10-year retention at 70 °C based on accelerated testing, and over 10^6 cycles of endurance [125]. Adesto released the first commercial product in 2012, a 1-Mbit EEPROM chip based on an Ag/GeSe cell, capable of 10-year retention at 70 °C (Fig. 37) [119], [120]. Later, Adesto demonstrated high-temperature data retention in their second-generation Cu-based devices, compatible with brief 10-μs solder reflow processes at 260 °C [120]. Very low write power (19 μW) and energy have been demonstrated, showing promise for low-power electronics applications [126].

As with STT-MRAM and ReRAM, CBRAM devices are generally robust to TID effects [121]. The possibility that ionizing radiation can affect the properties of the chalcogenide dielectric with photodoped Ag was an initial consideration. Gonzalez-Velo *et al.* [127] investigated this possible interaction by exposing Ag/$Ge_{30}Se_{70}$ cells to Co-60 gamma radiation at levels as high as 10 Mrad(Si). The resistance distributions did not change during exposure, but upon cycling, the average high-resistance state of the cell was found to increase slightly following exposure. This is attributed to the effect of the dielectric exposure, as this can explain the effect when there is no filament (high-resistance state) and would not be changed when a filament exists (low-resistance state). A follow-up

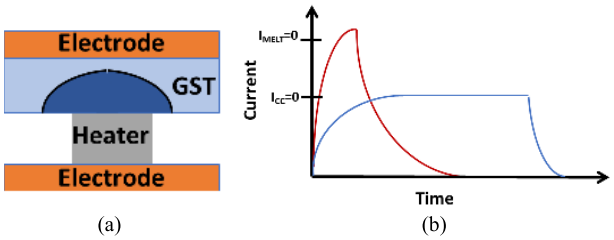

Fig. 40. (a) Phase change memory cell and (b) SET and RESET current transient plot.

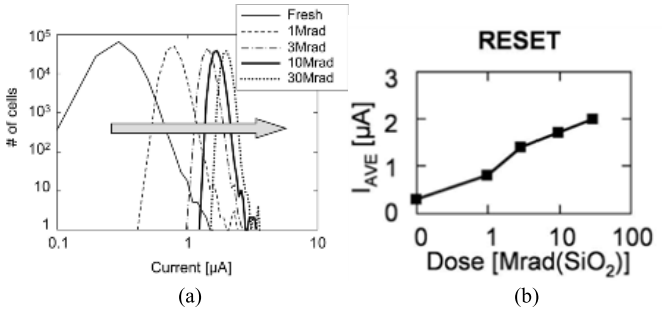

Fig. 41. (a) TID-induced current distribution shifts and (b) shifts versus dose in an STMicro 4-kbit test chip in the reset state (© 2007 IEEE. Reprinted, with permission, from [141]).

study by the same group confirmed for the same device type, no radiation-induced bit flips occurred after 5 Mrad($Ge_{30}Se_{70}$) and there was not a significant effect on retention up to 2.8 Mrad($Ge_{30}Se_{70}$) [128]. Endurance was not affected up to 10^4 cycles following 4.6 Mrad($Ge_{30}Se_{70}$), after which point the unirradiated devices would start to degrade [128].

TID effects were also studied for Adesto's first-generation Ag/GeS_2 CBRAM 128-kb serial memory (part no. RM24EP128KS) [119], [122]. No increase in standby current and no increase in bit errors were observed at a dose of 447 krad(Si). This is an improvement over commercial NAND flash and commercial (unhardened) MRAM, as plotted Fig. 39.

Initial heavy-ion studies revealed that in a 1T1R Ag/GeS_2 cell, bit flips occur when the high-resistance state experiences a resistance decreases [129], similar to that observed in ReRAM by Bennett *et al.* [114]. This is attributed to current resulting from an ion striking drain of the select transistor. Later, SEE experiments in the Adesto RM24C EEPROM product yielded upsets that flipped both the high-resistance state to low-resistance state and vice versa with a threshold LET of ~10–20 MeV·cm^2/mg [130]. Bit errors were reported to occur only during the static bias and dynamic read/write tests in a standby mode or during a read-only operation, indicating the CBRAM bit itself was not the source of the upset. As with ReRAM and STT-MRAM arrays, the primary failure during heavy-ion testing was due to SEFIs. In this case, read, write, and static SEFIs were observed and in a few cases were not corrected by power cycling.

D. Phase Change Memory

Phase change memory (PCM or PCRAM) is another CMOS BEOL-compatible resistance change memory, currently in production by STMicro, France, at the 28-nm node [11], targeting automotive and other embedded applications. As with other resistive memories, PCRAM is relatively insensitive to radiation and has served as the basis of previous radiation-hardened memory development efforts [131]. Although previous generations of PCRAM have struggled with high-temperature retention, recent devices have overcome this, perhaps suggesting that the technology will be viable for future radiation applications.

PCRAM uses the difference in electrical properties of amorphous and crystalline phases of a chalcogenide to store a memory state. When the chalcogenide is in the amorphous phase, the resistance is significantly higher than when it is in the crystalline phase. This reversible, electrically inducted resistive switching, which results in a stable (nonvolatile) phase change, was first described by Ovshinsky [132] in 1968. Optical reflectance is also modulated by chalcogenide phase change, which can be triggered by the heat from a laser. The optical phase change effect has been widely used as the basis of optical information storage systems for decades, in technologies such as compact disks and Blu-ray disks.

A simplified PCRAM NVM cell structure is illustrated in Fig. 40(a). Electrodes surround a chalcogenide thin film, which is most commonly $Ge_2Sb_2Te_5$ (GST) in modern systems [133]. Typically, a resistive heating element is fabricated immediately below the GST film to facilitate state change. Electrically programming the cell into a low-resistance state (set operation) is achieved by applying a relatively long, current-controlled bias near the crystallizing temperature (~350 °C in GST [133]), as plotted qualitatively in Fig. 40(b). The GST film can then be amorphized and returned to the high-resistance state (reset) by applying a shorter, higher current pulse, in which the film reaches the melting temperature of ~610 °C in GST [133].

Although phase change materials have been widely used for optical memory for several decades, the first results of commercial PCRAM development were presented around 2001 [131], [134]. Subsequently, many semiconductor companies have developed PCRAM processes including STMicro [11], Intel, Hillsboro, OR, USA, Micron, Boise, ID, USA, Samsung, Seoul, South Korea, Numonyx, Switzerland, and IBM, NY, USA.

Phase change memory has advantages of high endurance, scalability, and reasonable retention. Cycling endurance of 10^{12} and individual bits cells with up to 10^{13} cycles were discussed in the early work by Lai and Lowrey [134] in 2001. However, this appeared to be based on individual (perhaps "hero") devices, and subsequent papers demonstrating arrays typically have lower endurance numbers from 10^5 to 10^9 [135], [136]. Wearout mechanisms have been reported including set-stuck cell (low-resistance state) attributed to the GST itself, and reset-stuck (high-resistance state), which was related to delamination of the cell [135]. The physical origin of the set-stuck failure endurance was a function of the reset time, related to the thermal cycling of the cell, and if this is optimized, endurance of $>10^{10}$ is achievable [137]. Comprehensive overviews of phase change memory technology are given in [13] and [138].

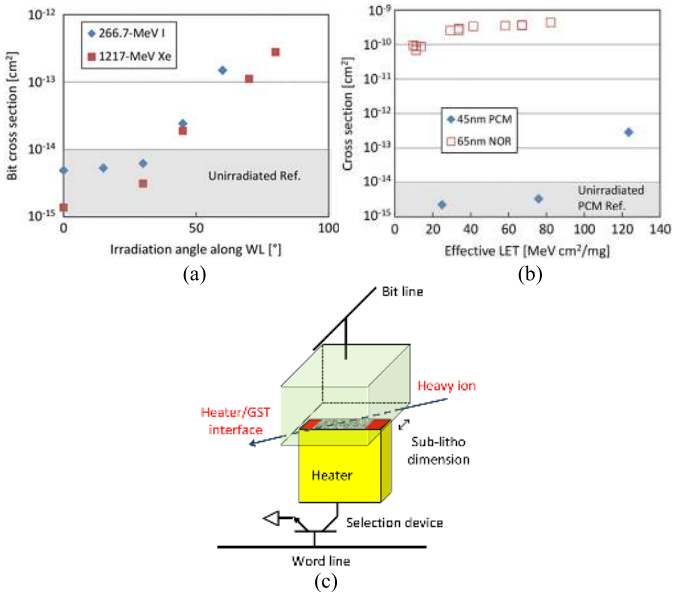

Fig. 42. Upset cross section versus (a) angle and (b) LET for upsets observed at the cell level in a 45-nm Micron array, and (c) possible bit upset mechanism (© 2014 IEEE. Reprinted, with permission, from [139]).

A primary interaction mechanism between the PCRAM chalcogenide switching layer and ionizing radiation is not known. Hence, as with other resistance change memories, most radiation-induced errors that have been observed are attributed to the peripheral circuitry (although recent exceptions have been observed with heavy ions on scaled devices [139]).

The first TID studies carried out in 2000 by Raytheon, Sudbury, MA, USA, reported on a pore-based 0.25-μm GST cell [140]. No change in electrical properties was observed after devices were subjected to 100 krad(Si) and 1 Mrad(Si) of Co-60 gamma irradiation [140]. Additional early TID studies were carried about by the BAE-Ovonyx collaboration on 64-kbit test arrays of GST bits. Similarly, changes in electrical characteristics did not occur following Co-60 gamma irradiation with a TID up to 2 Mrad(Si) [131].

In 2008, the effect of TID was examined on the more advanced STMicro 4-Mbit NVM test chip integrated with 0.18-μm CMOS [141]. The chip was subject to an 8-MeV electron beam up to 30 Mrad(SiO_2). The average high-resistance state (reset) current distributions were observed to increase as a function of dose (Fig. 41). In this case, the larger shifts relative to the small overall current high-resistance state current were attributed to increased leakage in the unselected bitline transistors in the array. Minor low-resistance state (set) distributions were observed (relative to the much higher total magnitude of the set or "ON" current), attributed mainly to leakage current caused by the selected bitline transistor V_T shift. Similar behavior was observed following exposure of STMicro PCRAM test chips to a dose of 30 Mrad(SiO_2) of 2-MeV protons when arrays with MOSFET selectors were used [142].

Early SEE experiments on the BAE, Manassas, VA, USA, test chip with 64-kbit GST arrays showed no static errors effect up to an LET threshold of 98 MeV $\cdot$ cm^2/mg [131]. Write errors occurred above 60 MeV $\cdot$ cm^2/mg during the SET process, attributed to a false triggering of the write circuitry. Read errors occurred were attributed to the sense amp [131]. None of the errors that occurred were attributed to the GST cell. In 2011, Gerardin *et al.* [143] investigated heavy-ion effects on a high density, 128-Mbit, 90-nm Numonyx test chip. The cell did not show cell upsets at the highest LET of 58.2 MeV $\cdot$ cm^2/mg, although SEFIs and latch-up occurred in the peripheral circuitry. Further analysis predicted that heavy-ion cell upsets at the cell level would not be observed until 32 nm.

More recently, in a high-density 1-Gbit Micron chip based on 45-nm GST cells, SBUs at the cell level were reported [139]. At LET of about 60 MeV $\cdot$ cm^2/mg, upsets are observed in "1" (low-resistance state crystalline) bits when the ions are incident at an angle starting at about 45° to the WL [Fig. 42(a)]. The cross section increased with increasing incidence angle up through about 80° to the WL. The cross section and LET_{th} are still quite low when compared to a modern NOR flash memory, as illustrated in Fig. 42(b). The mechanism is thought to be GST amorphization due to the heavy-ion energy transfer, which results in a transient temperature increase near the interface of the heater and the GST film [Fig. 42(c)]. Hence, cell-level upsets cannot be ruled out in scaled PCRAM, and, considering the continuing technological relevance, further investigation of bit-flips in scaled GST cells is warranted.

E. Other Emerging NVM Technologies

So far, this tutorial has focused on the most prominent emerging technologies—those which are currently being developed in major foundries at scaled nodes, and which are found in mainstream or prototype products. However, it is truly difficult to predict which technologies will dominate future markets, and numerous other emerging NVM technologies are the subject of research and development. Although it is beyond the scope of this tutorial to comprehensively cover all of these technologies, it is worthwhile to briefly mention some of the most prominent emerging memory technologies. The IEEE International Roadmap for Devices and Systems (IRDS) provides an overview of the emerging memory landscape [12], and references for further reading about each technology are provided below.

1) Ferroelectric Memories: Ferroelectric materials such as lead zirconate titanate (PZT) strontium bismuth tantalate (SBT) retain an internal electric field with a polarity that can be changed through the application of a field. When not subject to a field, the polarization can retain its state. Hence, a ferroelectric film, either sandwiched between two electrodes or integrated in another device, can be used as a memory. The use of this ferroelectric switching effect to create a semiconductor memory has a long history, starting in the 1955s ferroelectric transistor concepts were patented by Bell Labs, Murray Hill, NJ, USA [144]. The first demonstration of a metal–ferroelectric–semiconductor transistor (MSFT) occurred in 1974 [145]. In this device, illustrated in Fig. 43(a), a bismuth titanate ferroelectric film was integrated into the dielectric of an n-type silicon MOSFET. Switching the polarization of the ferroelectric film would change the state of the MOSFET surface, from accumulation to inversion, and hence

the V_T would change, and the memory state could be read in a similar manner to an FG cell. The modern version of this device referred to as the ferroelectric field effect transistor (FeFET). Another common implementation of ferroelectric memory is known as ferroelectric random access memory (FRAM). In this case, a ferroelectric capacitor is integrated in series with a transistor similar to a DRAM cell, and a DRAM-style read and write circuit is used.

During the 1980s, startups Ramtron, Colorado Springs, CO, USA, and Krysalis, Albuquerque, NM, USA, produced memories based on ferroelectric capacitors integrated with transistors in an SRAM configuration [147], as well as FeFET-based memory [148]. Another surge of interest occurred when Samsung demonstrated a prototype FRAM integrated with 0.6-μm CMOS was developed and demonstrated in 1999, in part due to the near unlimited cyclability [149]. Around this time, interest was also generated in aerospace community due to insensitivity to ionizing radiation and SEUs, as well as high endurance [150].

However, due to limited scalability, CMOS-fab material compatibly, and retention challenges, memories based on traditional ferroelectrics such as PZT and SBT have not been not integrated with highly scaled CMOS technologies. In 2011, ferroelectricity in HfO_x films was discovered [151], [152]. This led to a new, ongoing wave of interest in ferroelectric memories due to the significantly improved scalability and CMOS-fab compatibly, in part because nonferroelectric HfO_2 is already integrated into the gate-stack of standard CMOS transistors to reduce static gate leakage starting at the 28–45-nm node. Shortly after this discovery, ferroelectric $HfO_2$was integrated into the gate-stack of a 28-nm high-k metal gate (HKMG) process to demonstrate a FeFET with NVM functionality [see Fig. 43(b)] [146]. Furthermore, ferroelectric HfO_2 without a memory effect was integrated into a FinFET gate-stack to produce a steep subthreshold slope "negative-capacitance" logic device [153]. Ferroelectric memory based on HfO_2 is an area of continuing research, and we may see significant additional progress in the next decade. Müller *et al.* [154] provide a review of work utilizing ferroelectric HfO_2 in scaled memory devices.

Another ferroelectric memory device of recent interest is the ferroelectric tunnel junction (FTJ), which is a two-terminal ferroelectric resistance change device that can be thought of as a ferroelectric version of the MTJ [155], [156]. The FTJ-based memory device, which experiences a nonvolatile barrier height shift and resistance change depending on the ferroelectric polarization, was experimentally realized in 2012 [157] and continues to be investigated as a nonvolatile resistive memory device [158].

2) Other Resistive Memories: Several other emerging resistive memories have been invented and remain the topic of ongoing research. Resistive memories based on forms of carbon have had periods of significant interest, including amorphous carbon [159], graphene (2-D) [160], and carbon nanotubes (1-D) [161]. Each of these memories take the form of a two-terminal resistance switching device which retain a given resistance value until written using a higher bias and current. Hence, these are forms of resistive memory, but

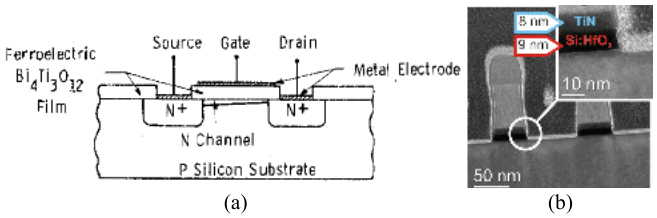

Fig. 43. (a) MSFT demonstrated by Westinghouse in 1974 (© 1974 IEEE. Reprinted, with permission, from [145]). (b) Cross section of a 28-nm FeFET integrated in an HKMG process (© 2012 IEEE. Reprinted, with permission, from [146]).

with different proposed physical switching mechanisms, which are described in [159]–[161]. Shortly after its invention in the early 2000s, NVM based on carbon nanotubes (known as NRAM) was of interest for space applications due to its radiation resilience [162], and work was done to integrate with radiation-hard CMOS [163].

Another class of NVM is known as polymer or organic memories. This wide class of memories can include many of the classes of memory discussed above, such as resistive, ferroelectric, and even FG devices [164]. The major distinguishing characteristic of polymer memories are that organic materials play a role in the switching mechanism and are integrated in the switching material. Resistive switching memories based on polymers (as opposed to oxides described above) remain of interest to the research community, especially for applications where a mechanically flexible device is required [165].

Perhaps, the most recently invented NVM device is known as the electrochemical random access memory (ECRAM). This is a three-terminal nonvolatile device which utilizes principles of ionic transport found in batteries to create a highly tunable analog resistance state required by neuromorphic computing applications [166]. The first prototype of this device functioned by linearly modulating the conductivity of the lithium cobalt oxide (LCO) cathode as a structure analogous to a lithium ion battery is charged and discharged [166]. This resistance-change concept was extended to proton-based [167], [168] and most recently to oxygen vacancy-based devices [169], the latter of which has interesting analogies to oxide-based ReRAM discussed above, but with significantly improved analog switching properties.

IV. Conclusion

The effects of TID and SEEs on advanced and emerging memories are summarized in Table II. From the perspective of radiation effects, technologies can broadly be split into two categories based on their storage mechanisms: charge-based storage and resistance-based storage devices.

FG memories tend to be sensitive to relatively low radiation doses due to the direct interaction of ionizing radiation with their stored charge. TID causes bit upsets at the cell level at 10–50 krad(Si) and is relatively unaffected by scaling. However, as MLC and TLC become more prominent in scaled cells, these advanced cells become more prone to errors caused by TID and SEUs. Single-event upsets occur readily in the floating cell at LETs of less than 10 MeV·cm^2/mg. FG memory has become more sensitive to bit upset devices with scaling,

TABLE II
SUMMARY OF TID AND SEES ON ADVANCED AND EMERGING MEMORIES

Technology	Radiation Tolerance	Approximate Total Ionizing Dose Static Error Threshold	Total Ionizing Dose: Description of Effects	Approximate Single Event Upset Threshold LET	Single Event: Description of Effects
2D Floating Gate (90 nm, SLC)	Low	<50 krad(Si) [46]	Programmed states: V_T significant distribution shift toward less programmed state. Erased states: slight V_T distribution shift toward neurtral state.	<10 MeV·cm^2/mg [46]	Programmed V_T distribution bifurcation, with secondary peak toward less programmed state.
2D Floating Gate (25nm, SLC)	Low	< 20 krad(Si) [44]		<2 MeV·cm^2/mg [53]	
2D Floating Gate (25nm, TLC)	Very Low	< 10 krad(Si) [49],[50]		<0.5 MeV·cm^2/mg [49]	
3D Floating Gate NAND (TLC)	Very Low	< 10 krad(Si) [51]		<2 MeV·cm^2/mg [55]	Programmed V_T distribution bifrication with peaks depending on ion angle of incidence [55]
Charge Trapping (40nm SONOS)	Moderate	300-500 krad(Si) [57]	Programmed state: V_T distribution shift toward less programmed state. Erased state: slight V_T distribution shift depending on stack.	20 MeV·cm^2/mg [57]	Programmed V_T distribution bifurcation, with secondary peak toward less programmed state. [57]
Toggle MRAM	High	1 Mrad(Si) [77]	No device-level effects reported.	69 MeV·cm^2/mg [77]	Some hard bit shorting failures for LET > 70 MeV·cm^2/mg [77]
STT-MRAM	High	>10 Mrad [78]	Film structural degradation at > 247 Mrad(Si) [81]	F=150nm: LET > 84 MeV·cm^2/mg [76] F=40-80nm: LET=15 MeV·cm^2/mg [82]	Bit flips for scaled MTJs, in the range of 40-80nm, LET ≥15 MeV·cm^2/mg [83]
ReRAM	High	TaOx: > 18 Mrad(Si) [100] HfOx: > 7 Mrad(Si) [101]	Charge trapping in the oxide [101]	TaOx, Unbiased in Product: >70 MeV·cm^2/mg [106] HfO2, 1T1R, with bias: ~10 MeV·cm^2/mg [105]	No static mode (device) upsets due to TaOx bit observed [105] High res to low resistance switch in 1T1R HfO_2 when biased [105]
CBRAM	High	>2.8 Mrad(GeSe) [119]	Slight endurance and retention degradation following 2.8 Mrad(GeSe) [119]	>60 MeV·cm^2/mg [121]	No static mode (device) upsets (due to bit) up to LET >60 MeV·cm^2/mg [121]
PC-RAM	High	> 2 Mrad(Si) [125]	No device-level effects reported.	F≥90nm: LET > 58 MeV·cm^2/mg [134] F=45nm: LET ≥38 MeV·cm^2/mg [130]	45nm GST devices show low resistance changing to high resistance at approx LET ≥38 MeV·cm2/mg [130]

due to the decrease in charge stored for the programmed state. Advanced CTMs, such as scaled SONOS, are significantly more resilient, withstanding TID levels of 300–500 krad(Si) and upset cross sections starting at an LET of about 20 MeV · cm^2/mg.

Emerging resistance change memory technologies such as MRAM, ReRAM, CBRAM, and PCRAM are relatively insensitive to ionizing radiation, SEEs, and displacement damage, as there is not a direct mechanism for interaction between radiation and the storage mechanism. When radiation-induced errors do occur, it most often a result of interaction with the select device or supporting CMOS peripheral circuitry. However, there are some reports of device-level SBUs in highly scaled STT-MRAM bits (MTJs) [92] and PCRAM bits [139] which merit further investigation.

Each of these emerging resistive memory technologies are under continued development at highly scaled nodes by major foundries for next-generation electronics. Commercial advancements in these emerging technologies may pave the way for future high-density radiation-hard NVM.

ACKNOWLEDGMENT

The author would like to particularly thank T. P. Xiao, K. Galloway, and the TNS reviewers and editors for reading this article closely and providing valuable feedback. In addition, gratitude is due to many for useful discussions on memories, semiconductor devices, and radiation effects. Matthew J. Marinella is grateful to his advisor, the late Prof. D. K. Schroder, and many colleagues, including H. J. Barnaby, D. R. Hughart, C. Bennett, R. Jacobs-Gedrim,

A. A. Talin, M. L. McLain, M. Esposito, D. Garland, T. Meisenheimer, B. Draper, Y. Gonzalez-Velo, S. Agarwal, M. N. Kozicki, S. Dasgupta, P. Dodd, M. Shaneyfelt, N. Nowlin, A. Mitchell, K. Raby, J. Schwank, F. Mancoff, S. Aggarwal, J. Hasler, E. Fuller, M. P. King, J. A. Incorvia, R. Schrimpf, D. Fleetwood, and many others. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under Contract DE-NA0003525. This article describes objective technical results and analysis. Any subjective views or opinions that might be expressed in this article do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

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