Radiation Hardening by Design Techniques for the Mutual Exclusion Element

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ABSTRACT

Circuits in advanced CMOS technology are increasingly more sensitive to transient pulses caused by radiation particles that strike vulnerable circuit components, specially turned off transistors, often generating multiple voltage upsets. Towards mitigating these issues, this paper presents a novel Radiation Hardened by Design (RHBD) mutual exclusion element (mutex) that incorporates multiple RHBD techniques with reduced area overhead.

We compared our proposed circuit to the baseline and the state-of-the-art designs, in terms of resiliency to Single Event Transients (SET) and Single Event Upsets (SEU), request to grant latency, and area overhead. Results shows that the proposed circuit mitigates SET and prevents SEU events incurring in 1.42x performance and 5.1x transistor area overhead compared to the baseline (unhardened) design. On the other hand, the proposed mutex circuit improves SEU resiliency at outputs, achieving 0.58x transistor area and 0.62x latency compared to the state-of-the-art RHBD mutex that uses modular redundancy.

CCS CONCEPTS

• **Hardware** → **Asynchronous circuits**; **Circuit hardening**.

KEYWORDS

Mutual exclusion element, Mutex, radiation hardening by design, Asynchronous circuits, Metastability filter, C-elements, Guard Gates, Arbitration

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1 INTRODUCTION

Submicron CMOS circuits are severely degraded under radiation exposure partially because the continuous scaling of transistor sizes and decreasing supply voltage values that increase their sensitivity to interference from radiation sources [4]. In particular, a radiation strike can be induced when a highly energetic particle, such as a proton, neutron, alpha particle or heavy ion, impacts and interacts with the sensitive component inside CMOS transistors, inducing an electrical current between conducting terminals. A traditional means of radiation hardening involves altering the fabrication process and is called radiation hardening by process (RHBP). RHBP has the advantage of being very reliable, but it also suffers high manufacturing costs. In contrast, radiation hardening by design (RHBD) uses standard CMOS technologies. The hardening is implemented at system architecture, circuit design (topology and sizing of components), physical layout, or a combination of techniques and does not rely on the fabrication process itself. For sub-micron technologies, the primary concern is circuit level optimizations leveraged by layout and other possible hardening techniques [11].

The mutual exclusion element (mutex) [14], is the core component of arbiters in asynchronous circuits and multi-clock domain digital systems [12]. A mutex helps control the mutual exclusive access to a single resource from two or more independent requestors. If contention between requests occurs, metastability can occur within the mutex as it decides which request to grant. Before the mutex grants access any metastability must have resolved, which can take unbounded time. This unique behavior makes this circuit not suitable for a triple modular redundant (TMR) solution: after arbitration, two out of the three modules will agree, but an SET in any mutex node can change the decision agreement, momentarily or permanently, inducing a SEU. This change in decision does not happen in a typical TMR solution in which the module suffering an SET or SEU would always be outvoted. In the context of arbitration, this change in decision could lead to a system deadlock.

Naqvi's et al. in [17] proposed a RHBD arbiter cell that uses Yakolev's et al. tree arbiter cell (TAC) [22]. The RHBD arbiter uses modular redundancy on the mutex's surrounding handshaking circuitry, not to the mutex cell itself. Hence, the mutex is still susceptible to SET and SEU events. The RHBD arbiter's grant-request generator circuit has two variants: The first variant tolerates SETs at the handshaking C-elements, but they are susceptible to SEUs immediately after an arbitration event. The second variant implements multiple handshaking C-elements in a tree topology incurring in significant area overhead, but may be susceptible to deadlock under certain conditions.

Jang et al., proposed a mutex [20] using a dual interlocked Cell (DICE) [19] using modular redundancy that incurs significant area penalty. Set-Reset (SR) latches [8] are connected in a daisy-chain configuration, generating a double modular mutex arrangement. Any SET event will restore automatically to the correct previous state via the self correcting property of DICE.

In contrast, the proposed mutex circuit does not rely on modular redundancy. Rather, it incorporates noise-tolerant features of Schmitt-Trigger circuits, guard gates, and SR latch behavior control. The noise rejection helps prevent glitch propagation, the SR latch control prevents SEU events, and the guard gates prevents any SET

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(glitch) propagation. The proposed circuit is SET and SEU tolerant. Compared to the mutex, it has low area and performance overhead. However, compared to the state-of-the-art DICE mutex, it provides better area and performance with similar SET and SEU tolerance.

The rest of the paper is organized as follows. Section 2 provides general background in radiation effects in CMOS and radiation hardening at the circuit level as well as a review of the SR latch, metastability filters, and CMOS Schmitt triggers. Section 3 presents related work including the baseline and DICE mutex designs. Section 4 details our proposed RHBD mutex. Section 5 explains our simulation-based experimental setup and results, Section 6 discusses the design and experiments, and Section 7 concludes with a brief summary and description of possible future work.

2 BACKGROUND

2.1 Radiation Effects in CMOS Circuits

Figure 1.a depicts the interaction of a radiation particle striking the sensitive depletion regions or reverse-biased *p-n* junctions inside a transistor, generating a trail of electron-hole pairs. These free carriers can drift creating a transient current pulse which results in charge collection that generates a transient voltage at the drain node. The generated transient voltage is known as a Single Event Transient (SET), and depending on the induced voltage fluctuation and duration, can propagate to downstream logic. If the SET reach a state holding element at the right time and condition, it can induce the state to flip, a condition known as a Single Event Upset (SEU). An SET or SEU, both are non-destructive forms of Single Event Effects (SEE) [15].

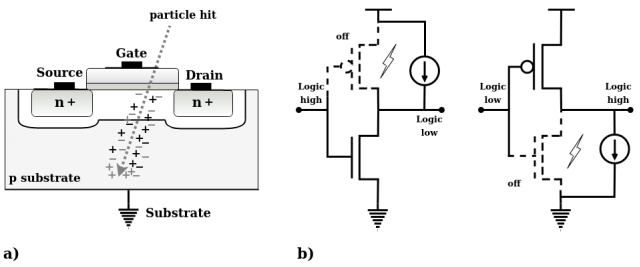


Figure 1: a) A radiation particle hit on a sensitive area. b) Radiation particle strike model.

Linear Energy Transfer (LET) is the the energy that is transferred into the material when an ionizing particle passes through it [9]. The LET event is traditionally represented in SPICE simulations as a independent current source, connected between drain and body transistor terminals. This current source has been traditionally implemented as a double exponential waveform [21], but different waveform implementations are explored in [1]. Depending on the logic state, the junctions of the off transistors in a gate are vulnerable to SETs. Figure 1.b depicts the independent current source connection of CMOS circuits. For a *n-hit*, or a hit on an off NMOS transistor, the direction of the independent current is from ground to drain. In contrast, for a *p-hit* or a hit on an off PMOS transistor, the direction of the induced current changes, from V_{dd} to drain.

2.2 Radiation Hardening By Design Techniques

The focus of this paper is RHBD techniques that introduce changes to a circuit design to mitigate non-destructive SEEs, namely SETs and SEUs events at critical circuit nodes; i.e., nodes where an SET event can impair the functioning of the circuit. Below are listed some of the RHBD techniques used in the proposed circuit.

Increasing node capacitance is the most common way to increase node robustness to SET. This can be achieved by adding a capacitor, increasing transistor sizing, or adding transistor redundancy to the node.

Spatial redundancy or modular redundancy (MR) usually doubles or triplicates (TMR) the circuit and implement a voting element at the output to filter the SET propagation.

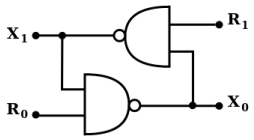
Temporal masking is implemented using glitch filters and guard gates [3] these are special circuits that relies on MR and increased node capacitance to filter out the SET propagation to downstream logic. Additionally, some enabling signals can act as temporal masking signals on glitch filters.

The above techniques, despite being effective, introduce significant area, power, and performance overheads. For this reason they must be used carefully to achieve the required robustness while not incurring unnecessary overheads in terms of power, area, or performance.

2.3 Mutex base cells

In this subsection, some of the cells used by related and proposed mutexes are described.

2.3.1 Set-Reset latch. The Set-Reset (SR) latch [8] is a state-holding element implementing two cross-coupled NAND gates and its States table is presented in Figure 2. For this application, we must consider all input conditions and transitions, even those that are traditionally considered illegal. For now, lets assume R_0 and R_1 input signals



State	R_0 R_1	X_0 X_1
a	0 0	1 1
b	0 1	1 0
c	1 0	0 1
d.1	1 1	0 1
d.2	1 1	1 0

Figure 2: SR latch 2-input NAND gates implementation. Shaded rows denote state-holding states.

remain stable until the circuit's outputs become stable. The idle state "a" has both inputs low. In turn this implies both outputs are high. From this state, the latch can go to state "b" or "c", implying that one of the outputs will flip to low correspondingly.

Furthermore, moving from state "b" to state "d.2" or from state "c" to "d.1" does not incur any change at the outputs. At "d.1" or "d.2" states, the SR latch behaves as a state-holding element, remembering the output values from the previous state. Conversely, moving from states "b" to "d.1" or "c" to "d.2" is not possible. Rather, from states "b" or "c" it is only possible to go back to state "a". Finally, from "d.1" it is possible to go to state "c" or "a" and from "d.2" it is possible to go to state "b" or "a". These behaviors are deterministic.

On the other hand, transitioning directly from state "a" when both inputs simultaneously causes the circuit to *non-deterministically*

choose between entering state "d.1" or "d.2" and this choice may depend on which way the internal metastability in the circuit is resolved (which may take an unbounded amount of time) [5]. We later call this *arbitration* as it provides mutually exclusivity to the outputs.

We emphasize, however, that electrical disturbances to the outputs can force the circuit to transition between states "d.1" and "d.2". This behavior is not expected during normal SR operation, but can be caused by an SEU.

2.3.2 Metastability filter. The 2-input metastability filter, illustrated in Figure 3.b, is comprised of two voltage-controlled inverters, namely $X_0 - G_0$ and $X_1 - G_1$ respectively. They are cross coupled where one's inverter input is connected to other's V_{dd} terminal. Input X_0 controlling the V_{dd} of the $X_1 - G_1$ inverter, guarantees that the output G_1 will only go high when the mutually exclusive logic condition at inputs X_0 low and X_1 high is guaranteed. Similarly, the complementary mutually exclusive condition holds for output G_0. More precisely, the voltage at output G_0 cannot be raised if the difference between the input voltages at X_0 and X_1 is below the PMOS threshold voltage. Consequently, when X_0 and X_1 voltages are metastable, near $V_{dd}/2$, the outputs remain zero.

We note that for applications where a voltage-controlled inverter is not available (e.g., an FPGA), an alternate is to replace the inverters with 4-input NOR gates with inputs tied together [23]. This is effective because the NOR gates have a relatively low switching threshold and thus still prevents metastable voltages from propagating.

2.3.3 CMOS Schmitt Trigger. The inverting Schmitt Trigger [10], depicted in Figure 3.a, is composed of a double-stacked NMOS (MN_0, MN_1) and PMOS (MP_0, MP_1) transistors at the input, followed by MN_2 and MP_2 feedback transistors that provide hysteresis; i.e., different input voltage thresholds for rise and fall transitions at the output. The hysteresis provides better noise-rejecting margins at the input with low capacitance overhead at the output.

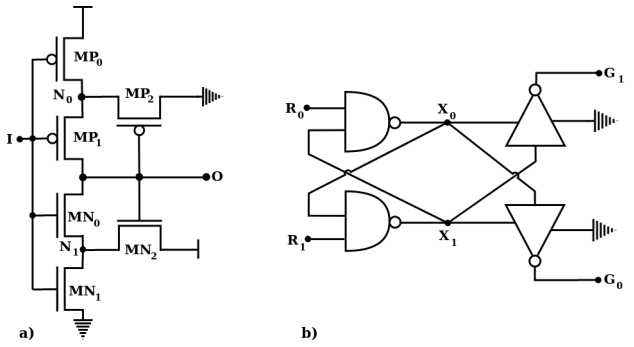


Figure 3: a) Inverting Schmitt Trigger. b) Baseline mutex consisting of an SR latch and a metastability filter.

The proposed mutex circuit is designed using novel 3-input NAND gates using a similar transistor topology. This will be discussed in Section 4.1.

3 RELATED WORK

This section reviews and analyzes the baseline [14] and DICE [20] mutexes. Excluded from a detailed analysis is Naqvi's work [17] because the underlying mutex cell is not RHBD.

3.1 Baseline mutual exclusion element

The 2-input mutual exclusion element (baseline mutex), illustrated in Fig. 3.b, consists of an SR latch and metastability filter [5]. The filter ensures that metastability in the SR latch does not propagate to downstream logic. The mutex controls access to a single resource from two independent requestors. If the time between requests (R_0 and R_1) is large, the mutex's decision is straightforward, granting access to the earlier request.

However, when the time between requests is shorter than the time needed for the SR latch stabilization, metastability may occur at the output of the SR latch, as it decides which request should be granted, but cannot propagate through the filter. The *critical nodes* of a mutex are along the paths R_0, X_0, G_0 and R_1, X_1, G_1 as they can impair the functioning of the baseline mutex if an SET event occurs. During a *request-grant* operation, the baseline mutex can exhibit two modes of operation. One is deterministic operation, comprising transition paths starting from state "a" to "b" or "c", then going back to "a". The second is the *arbitration* mode comprising transitions starting from state "a" to "d.1" or "d.2", then returning back to "a". These two modes are repeatedly executed, one or the other, returning to the idle state "a" after each *request-grant* operation.

3.2 DICE Mutex design

A DICE based mutex is presented in patent [20]. The core of their design is four SR latches arranged in a ring, as illustrated in Fig. 4, implements a form of modular redundancy. The input and output ports are replicated, creating two parallel request and grants for each logical input/output. Thus, the equivalent baseline mutex inputs R_0, R_1 become $R_{0a}, R_{0b}, R_{1a}, R_{1b}$ and the output nodes from the SR latch ring structure are now $X_{0a}, X_{0b}, X_{1a}, X_{1b}$.

Because of the redundant SR latch arrangement and increased capacitance at intermediate nodes, these nodes are considered SET tolerant compared to the baseline mutex. A R_0 (R_1) request is in the form of both R_{0a} and R_{0b} (R_{1a} and R_{1b}) rising. To grant R_0 (R_1), outputs X_{0a} and X_{0b} (X_{1a} and X_{1b}) need to go low exclusively.

Comprising the SR ring, the NAND gates labelled "n" have three instead of the normal two inputs and each is paired with a 2-input NAND gate labelled "p". Both drive a common node. This configuration avoids contention between pairs of latches, ensuring their output grants agree. In the case of an SET event, the arrangement allows the SET to propagate at most one downstream logic stage. But, the modular redundancy prevents this propagation from altering the mutex output. The metastability filter arrangement consists of four structures, one per output. Each structure includes two 2-input voltage controlled inverters that, in turn, drive a 2-input C-element that provides mutex's output nodes $G_{0a}, G_{0b}, G_{1a}, G_{1b}$. The metastability filters structures are not depicted in Figure 4. One concern with this design is that non-hardened C-elements used at outputs are susceptible to SETs that can generate an SEUs when their inputs differ. This can happen if there is some arbitration delay

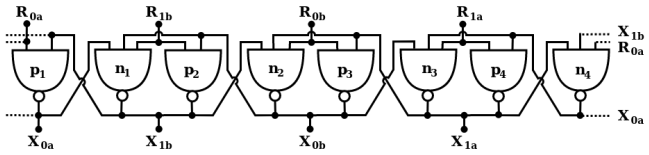


Figure 4: Arrangement of SR latches proposed in [20].

imbalance between cross-coupled mutexes. Thus, the DICE mutex *critical nodes* are found at outputs, namely nodes $G_{0a}, G_{0b}, G_{1a}, G_{1b}$.

4 PROPOSED RHBD MUTEX

The proposed RHBD mutex is shown in Figure 5. It is a modified baseline mutex at its core with surrounding circuits that provide RHBD. In particular, the SR latch implements special 3-input NAND gates and the metastability filter with Schmitt Trigger capabilities. We added a feedback path from each metastability filter output to the SR latch inputs. The purpose of these feedback structures is to provide SEU tolerance. In addition, a guard gate [3] is included after the output of each metastability filter, to avoid SET propagation to downstream logic. Because of the RHBD strategies applied, there are no nodes susceptible to SET or SEU events.

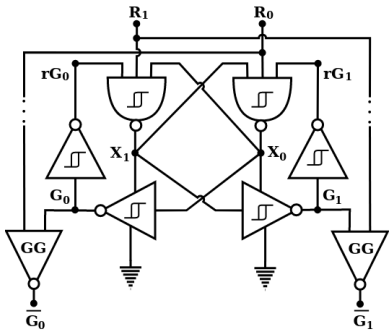


Figure 5: Proposed RHBD mutex.

4.1 3-input NAND gate implementing Schmitt Trigger circuitry

To take advantage of input noise rejection, a special 3-input NAND gate that includes Schmitt Trigger circuitry was developed. Noise margin at a node can be measured in terms of the node's critical charge defined to be the node capacitance time $V_{dd}/2$. Many previous works [10] assumed that SET amplitude over $V_{dd}/2$ crosses the noise margin of the subsequent gate. By incorporating ST circuitry to the output node of the 3-input NAND gate, the noise margin can exceed $V_{dd}/2$, and SET robustness is thus improved. As illustrated in Figure 6, the PMOS network of the NAND gate consists of three Inverting Schmitt Trigger PMOS networks, one for each input A, B and C. These include transistors MP_0 to MP_8. The NMOS network uses only one inverting Schmitt Trigger NMOS network. The key observation is that the single NMOS network can be controlled by both input A and B (transistors MN_0, MN_1 and MN_3). Inputs A and B requires higher noise rejection, for example, the $R_0 - X_0$ 3-input NAND, receives R_0 on input A, X_1 on input B and rG_1 on input C. A and B receive critical nodes on the standard mutex. In this case, they are susceptible only to SET events that reach the node's threshold switching voltage. In contrast, input C is located at the bottom of the NMOS stack (MN_2) receiving the inverted feedback path from G_1.

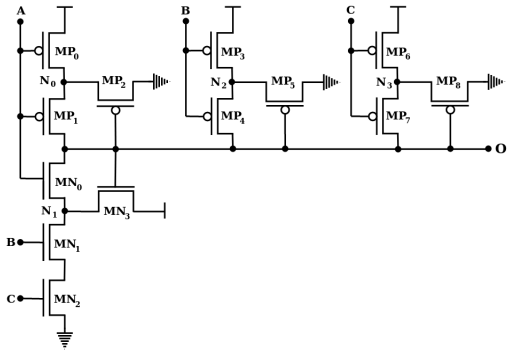


Figure 6: Special 3-input NAND implementing Schmitt Trigger circuitry.

4.2 Modified SR latch with feedback path control

The modified SR latch consists of two cross coupled 3-input NAND gates implementing Schmitt Trigger (ST) circuitry to increase noise margin at its inputs. In particular, the third input of each NAND ST is driven by the corresponding feedback output of the inverter Schmitt Trigger of the metastability filter. For example, in the case of the $R_0 - X_0$ 3-input NAND ST gate, the connected Inverter Schmitt Trigger originates at node G_1. These connections reinforce the NAND gate whose output is low such that an SET on any of the NAND-gate inputs has no effect, preventing any SEU event.

This topology provides the desired SR latch functionality with tailored noise rejection, SEU tolerance, and low area overhead.

4.3 Guard Gates

Guard gates (GG) were proposed in [3] and compared to 2-input inverting C-elements that have the same basic functionality in [13]. In particular, when both GG inputs are equal, the gate just acts as an inverter. But, unlike a C-element, a GG does not implement a back-to-back inverter (keeper) structure at the output.

Instead, it relies on output capacitance to hold state and provide the desired level of SET tolerance. This capacitance is achieved by means of transistor sizing or the addition of an explicit capacitor. GG gates synchronizes the request and grant signals after a *request-grant* operation. More precisely, R_0 (R_1) and G_0 (G_1) are fed into one GG to provide a latched and inverted G_0 (G_1) output signal. We add a second symmetric GG to drive the inverted G_1 (G_0) output. The delay in arriving inputs to the GG provides temporal masking. Moreover, to increase the temporal masking effect, the input R_0 (R_1) input path down to the GG gate may include buffers. Careful place and route and layout considerations are required to optimize this path delay.

5 EXPERIMENTAL SETUP AND RESULTS

Because our intent is to compare and contrast different mutex templates at the transistor level using SPICE simulations, a custom design flow using the PTM-MP 20nm HSPICE library models [16] based on BSIM-CMG modeling [7] was developed to synthesize the baseline, DICE, and the proposed mutexes. A common test setup was used during experiments with homogeneous transistor sizing of L=30nm, W=30nm for NMOS and L=30nm W=60nm for PMOS transistors was used on all designs. Additionally, $V_{dd} = 1V$ and the input R_0 (R_1) pulse amplitude was fixed to 0.95V at high and 0.05V at low. Period duration was variable, depending on the experiment. Rise and fall times were set to 10% of the period duration.

The methodology presented in flowcharts in [6] and the results presented in [2] where used to develop SET independent current sources for simulation [1] to imitate the strike effect on nodes and subsequent voltage transient. In addition, following the methodology described in [2], each SET current model was developed following proper boundary conditions to avoid over-voltage at the output of the CMOS gate.

Experiments using a chain of two inverters driving FO1 and FO5 circuits served as calibration setup to match results presented in [2]. In Figure 7, current shapes and transient voltages on the affected node for LETs with values 2, 4 and 7 MeV-cm^2/mg are shown. Considering SET events that propagate voltage disturbances into

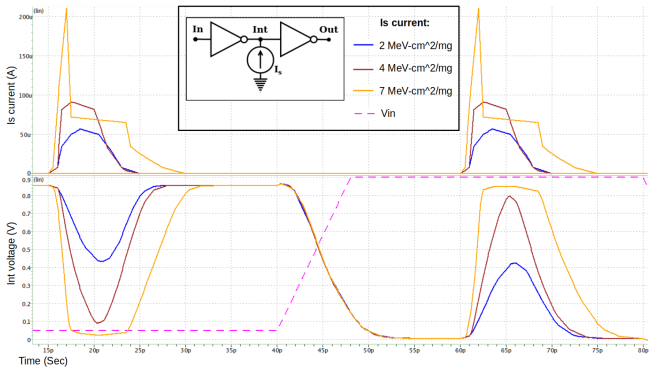


Figure 7: Top: Iset current model for LET values 2, 4 and 7 MeV-cm^2/mg. Bottom: Voltage upset at the intermediate node. Inset: Design under test.

the next downstream logic stage (were the voltage disturbance is greater than $V_{dd}/2$). Thus, all previous mentioned LET generate SET events driving FO1 fan-out structure. Only the SET generated by 7 MeV-cm^2/mg was able to generate a SET on a node that drives a FO5 fan-out structure. For this reason, this LET value is selected for further experiments. A testbench using two independent voltage sources implementing a 250 picoseconds (ps) period square wave, each driving a 2-stage inverter's chain that feed the inputs of the mutex under testing. At the output of the mutex FO5 fan-out circuits were connected to test different output loads. The independent current source (Is) SET for 7 MeV-cm^2/mg was selected to test SET mitigation. Simulation results on this experiment are shown in Table 1.

Table 1: Single 7 MeV-cm^2/mg LET event in nodes

Node	baseline [14]	DICE [20]	Proposed
R_0/R_1	SET	No *	No
X_0/X_1	SET	No **	No
G_0/G_1	SET	SET ***	No ****

Note: For DICE mutex:
* Input nodes are $R_{0a}, R_{0b}, R_{1a}, R_{1b}$.
** Intermediate nodes are $X_{0a}, X_{0b}, X_{1a}, X_{1b}$.
*** output nodes are $G_{0a}, G_{0b}, G_{1a}, G_{1b}$.
For Proposed, **** output nodes are $\overline{G_0}$, $\overline{G_1}$.

All nodes on the baseline and DICE's output nodes are susceptible to SETs and propagate the voltage disturbance. The opposite situation occurs on the proposed mutex. Moreover, the baseline is susceptible to SEU if an SET occurs on R_0 (R_1) input or X_0 (X_1) nodes. As an example on this, Figure 8 shows waveforms of SETs at the output nodes. For each mutex, voltage waveforms are superimposed. The continuous line represents the output mutex node and one subsequent FO5 node (dashed line) voltage. Note that the SET is clearly shown for baseline and DICE mutexes. For the proposal, the voltage disturbance was minimal and not propagated downstream.

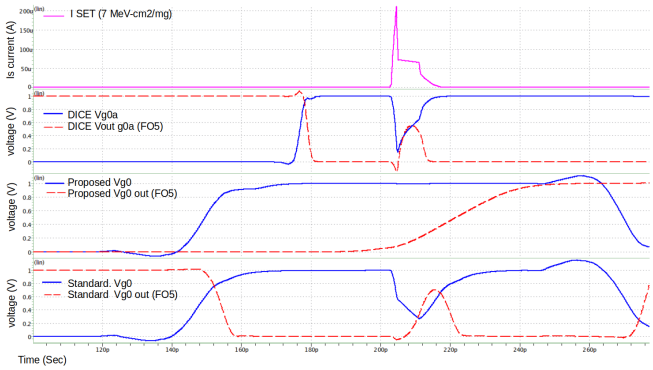


Figure 8: Waveforms for Iset (7 MeV-cm^2/mg). SET events at outputs and at the subsequent logic stage.

To test the proposed mutex against SEU, an SET event on node X_0 was generated after arbitration. For this specific case, the simulation resolved arbitration granting request R_0. The SET is mitigated at the input C at the $R_1 - X_1$ NAND gate. Although the controlling feedback path is slower by one logic stage, the SET at node X_0 was effectively contained and not propagated. Voltage node waveforms on R_0, X_0, G_0 and rG_1 (feedback G_0 to input C at $R_1 - X1$ NAND) are shown in Figure 9. Similar experiments were conducted on the baseline and DICE mutexes, showing that for baseline the SET at node X_0 is propagated downstream to node X_1. Note that X_0 and X_1 node voltages disturbed beyond $V_{dd}/2$ may lead to an SEU. On the other hand, DICE suffered voltage perturbation at X_0a but the subsequent X_1a node did not reach $V_{dd}/2$, thus no SET propagation occurred.

To further test SEU tolerance, an SET pulse with a 100 ps duration was applied (as 100ps is a typical SET duration for advanced

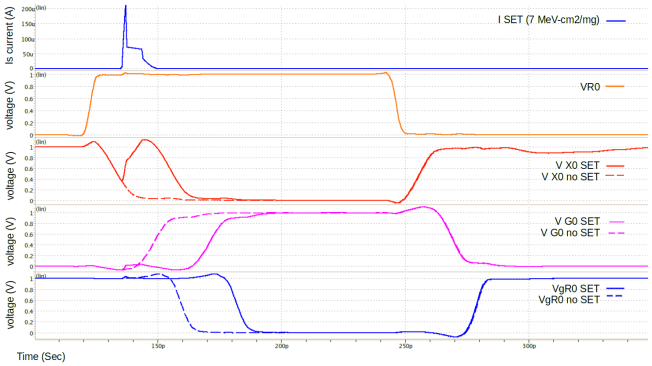


Figure 9: Waveforms for Iset 7 MeV-cm^2/mg. at proposed mutex's node X_0 after arbitration.

technologies [18]). The longer Iset was configured using a burst of consecutive 7 MeV-cm^2/mg LETs and the source (R_0) period was increased to 350ps. Figure 10 shows that the transition signal is delayed by the SET duration, and the SET was not propagated, yielding minimal voltage disturbance.

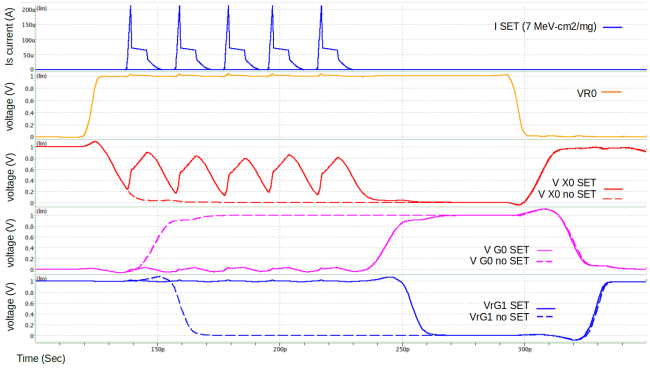


Figure 10: Proposed mutex waveforms for Iset of duration 100ps at node X_0 after arbitration.

6 DISCUSSION

A brief summary of our experimental results can be found in Table 2 that include measurements of the latency from request to grant raising signal, area, SET and SEU tolerance at different mutex nodes. The baseline design exhibit the shortest latency, due to low node capacitance, but also the lowest tolerance to SETs. The proposed circuit required 1.42 times longer to complete a request to grant event. But, this was expected and in fact is much shorter than the DICE mutex, which required more than twice of the baseline (2.28 times). These results show the tradeoff between node capacitance and SET resiliency, as the increased capacitance improves SET resiliency but slows down the circuit.

Transistor area was found to be 8.7 times greater for DICE than the baseline mutex. Thus, SEU tolerance can be provided by means of modular redundancy, with high area penalty.

In contrast, the area of the proposed circuit is 0.58 times the area of the DICE mutex, demonstrating that RHBD robustness can be achieved by focusing on the vulnerable circuit conditions. Moreover, the DICE mutex has an Achilles's heel on its outputs: the decision of driving the outputs using C-elements makes it vulnerable to SET and SEU events which can lead to system deadlock. Experimental results on the proposed mutex demonstrated that SETs are filtered at inputs and outputs and no SEU was generated even on the typical SET event duration.

Additionally, avoiding an SET on each node in the proposed mutex can mitigate multiple strikes of same intensity that in turn can generates multiple SET events on the baseline implementation. Finally, although the power was not measured, it can be estimated to be proportional to transistor area.

Table 2: Comparison to baseline and state-of-the-art circuits

	baseline[14]	**DICE[20]**	**Proposed**
Request-to-grant latency(ps)	25.6	58.5 (2.28x Std.)	36.5 (1.42x Std.)
Transistor Area μm^2	16.2	140.4 (8.7x Std.)	82.8 (5.1x Std.)
SET tolerant at internal nodes	No	Yes	Yes
SET tolerant at outputs	No	No	Yes
SR latch SEU tolerant	No	Yes	Yes
SEU tolerant at outputs	No *	No	Yes

Note: * Does not apply

7 CONCLUSION AND FUTURE WORK

An SET and SEU tolerant mutex has been presented. We compared our proposed circuit to the baseline and state-of-the-art mutex, in terms of SET and SEU resiliency, request to grant latency and area overhead. Results shows that the proposed circuit mitigates SET and prevents SEU events, incurring 1.42x performance and 5.1x transistor area overheads compared to the baseline (unhardened) mutex.

Compared to the state-of-the-art RHBD mutex that uses modular redundancy, on the other hand, the proposed circuit improves SEU resiliency at its outputs and and yields 0.58x the transistor area and 0.62x the latency.

In summary, this circuit avoids the modular redundancy area penalty and keep the performance overhead low. However, to increase radiation robustness, the final implementation also requires careful attention to place and route and radiation hard layout techniques, including spacing and shielding of critical nodes to minimize the effect of an SET affecting multiple nodes.

Our future includes investigating this strategy on other critical asynchronous control elements (i.e QFlops) and performing additional TCAD simulations to better guide transistor sizing.

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