Radiation-Tolerant Digitally Controlled Ring Oscillator in 65-nm CMOS

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***Abstract*— This article presents a radiation-tolerant digitally controlled complementary metal–oxide–semiconductor (CMOS) ring oscillator design suitable for all-digital phase-locked loop (ADPLL) implementations. To address the challenges presented by harsh radiation environments, a wide tuning range oscillator architecture is presented with superior single-event effect (SEE) tolerance. The proposed oscillator circuit is characterized experimentally in a 65-nm technology and shown to achieve a significant reduction in SEE sensitivity up to a linear energy transfer (LET) of 63.5 MeV mg^{-1} cm^2, remain free from harmonic oscillation errors under irradiation, and withstand a total radiation dose exceeding 1.5 Grad. At the design frequency of 1.28 GHz, the oscillator dissipates 7 mW of power while achieving a phase noise of −105 dBc/Hz at 1 MHz offset, corresponding to a figure of merit (FOM) of 159 dB.**

***Index Terms*— All-digital phase-locked loop (ADPLL), digitally controlled oscillator (DCO), oscillators, phase-locked loops (PLLs), radiation effects.**

I. Introduction

THE adoption of advanced technology nodes is well known to pose challenges to the analog circuit design process. This is true especially in the context of circuits designed for harsh radiation environments, where active devices are subject both to degradation from total ionizing dose (TID) effects as well as single-event effect (SEE). For the field of phase-locked loop (PLL) and carrier and data recovery (CDR) circuit design, a promising solution for both these challenges can be found in the adoption of all-digital PLL (ADPLL) architectures. A radiation-tolerant digitally controlled oscillator (DCO) is the key building block enabling their implementation. In applications where area constraints drive the design choices and larger phase noise can be tolerated, ring oscillators can be the preferred topology over *LC* tank oscillators. Being typically composed exclusively from active devices, ring oscillators have shown significantly stronger sensitivity to both SEE as well as TID degradation [1]. In order to fully exploit the area savings and radiation hardening opportunities offered by ADPLL architectures over their analog counterparts, there exists a need for radiation-tolerant digitally controlled ring oscillator (DCRO) designs, which has so far not seen widespread treatment in the literature.

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A. Radiation Effects in Ring Oscillator Circuits

Radiation effects in complementary metal–oxide–semiconductor (CMOS) ring oscillator circuits have been the subject of extensive studies in the past. The dominant radiation effects can be classified as either SEE or TID effects. In terms of TID effects in the dose regime above 100 Mrad, the dominant mechanism in submicrometer CMOS ring oscillator circuits is the increase of stage delay [2]. The resulting decrease of oscillation frequency eventually leads to failure of the oscillator to provide the frequency required by the application. When the amount of degradation over the device lifetime can be anticipated, a sufficient tuning margin can be foreseen during the design phase. Alternatively, layout techniques, such as enclosed layout transistor (ELT) geometries [3], can be used to reduce the amount of TID degradation. Considering SEEs, ring oscillators were found to be susceptible to transient frequency and phase errors [4], missing pulses [5], and stimulation of harmonic oscillation modes [6]. The impact of these radiation responses on closed-loop PLL circuits has also been studied [7] and other components of conventional PLLs optimized to a point where the oscillator remains as the largest SEE sensitivity [8]. Hardening against these effects has been achieved by measures such as the replication of bias stages [4]; duplicating or triplicating larger parts of the oscillator [9], [10]; and oscillator stage design methodologies aimed at suppressing the propagation of harmonic modes [6].

B. Organization of This Article

In the following article, we propose a CMOS ring DCO design addressing the challenges of SEE and TID degradation. In Section II, we describe the proposed circuit architecture and discuss its operation and advantages related to radiation tolerance. Section III provides an insight into characteristics and tradeoffs of the design through theoretical modeling, while

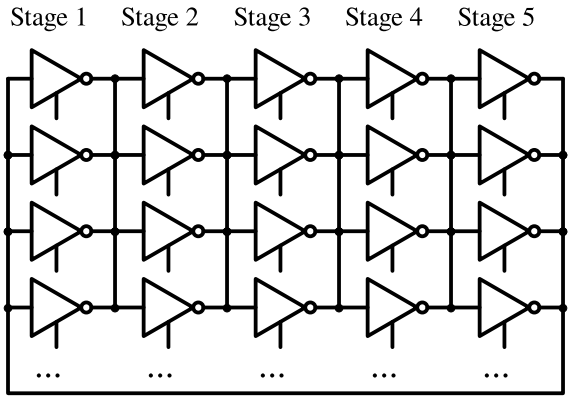

Fig. 1. Schematic representation of the adopted DCRO topology. Each stage of the oscillator is formed by an array of digitally controlled unit cells connected in parallel.

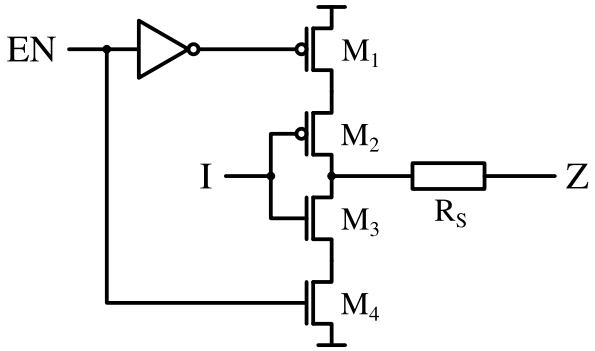

Fig. 2. Implementation of the RDUC for improved oscillator SEE tolerance. The output series resistor R_s decouples the individual output cells and reduces the impact of SET inside individual unit cells.

Section IV presents a practical design methodology using a 65-nm CMOS technology. In Section V, the SEE sensitivity of this design is analyzed using simulations and a design with improved SEE sensitivity is devised. Finally, Section VI presents the two manufactured ring oscillator designs and compares their performance and sensitivity to heavy-ion and X-ray radiation.

II. Circuit Description

The basic oscillator circuit topology adopted is the unit cell fill factor DCRO originally presented in [11] and shown in Fig. 1. In this circuit, each oscillator stage is composed of parallel tristate inverter unit cells of identical size. Individual cells, when enabled, increase the driving strength of a given stage and hence increase the oscillation frequency. Therefore, the control inputs of individual unit cells are used directly as a thermometric oscillator frequency tuning word (FTW). Since the load of each stage is constant but the driving strength increases proportionally with each additionally enabled unit cell, this DCRO topology achieves linear tuning over a wide frequency range, and the tuning is also inherently monotonous.

Multiple desirable properties for radiation hardness can be expected from this basic architecture. In the context of the large TID degradation expected from ring oscillators, the wide tuning range is beneficial since it increases the level of TID that can be tolerated before the oscillator becomes too slow to provide the oscillation frequency required in its application. The good linearity properties of the tuning characteristic reduce radiation-induced variations of the loop gain when the DCRO is used as part of a PLL circuit. Advantages in terms of SEE resilience can be expected from the unit cell segmentation of the oscillator. Both the oscillating and tuning nodes are segmented into independent, small devices. This is in contrast to conventionally used ring oscillator implementations. In voltage-tuned current-starved inverter ring oscillators, the oscillating node of each stage is driven only by a small number of active devices. For this reason, charge collection in these devices can disturb the oscillation waveform and result in phase errors [10]. Also, a single tuning node is often affecting all oscillator stages simultaneously and therefore causes a very high sensitivity to transient responses affecting the PLL control voltage. This makes such oscillators susceptible to frequency errors stimulated by SEE.

The unit cell approach addresses both these problems simultaneously: First, the oscillating node is driven by many small devices in parallel, compared to a small number of large devices contributing to all the charge in the oscillator. By additionally decoupling the individual cells from each other using resistive decoupling, this property can be further exploited to reduce the impact of single-event effects, as will be shown next. Second, the single tuning node present in voltage-tuned oscillators is distributed into many independent digital tuning nodes with small individual tuning gain. The presence of single-event transients (SETs) on any of the individual tuning bits, therefore, results in appreciably smaller frequency errors in the oscillator than when a single node with large sensitivity is affected.

The basic resistively decoupled unit cell (RDUC) used in the proposed oscillator is shown in Fig. 2. Four MOS devices form a basic tristate inverter, whose enable signal is used for frequency control of the oscillator. In order to decouple individual unit cells from one another, a series resistor R_s is added to the output of each unit cell. This resistive averaging technique has been more commonly used for analog circuit radiation hardening and was applied on a much smaller scale to the bias circuit of a voltage tuned ring oscillator in the past [4]. While charge collection in any of the active devices will still affect the local drain nodes of M_2 and M_3, the SEE current toward the common oscillation node will be limited by the resistor. Therefore, the main oscillation node will be protected by the resistor, while the collected excess charge is drained from the local node. The voltage perturbation at the gate nodes of the subsequent stage is therefore reduced and less phase error is stimulated in the oscillator.

An obvious drawback of introducing additional series resistance is a reduction of oscillation frequency since the unit cell output resistance is increased, while the load capacitance (composed of the input capacitance of the following stage and any interconnect parasitics) is not reduced, but potentially even increased by the resistor itself. This implies that the reduction of SEE sensitivity can be fundamentally traded off against an oscillation frequency penalty.

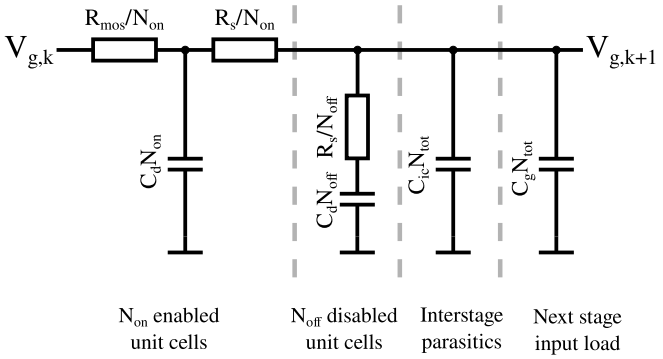

Fig. 3. Model of one oscillator stage used for Elmore delay-based oscillation frequency estimation. Enabled unit cells contribute to an increase of driving current, while disabled cells are assumed to load the common oscillation node with their drain capacitance.

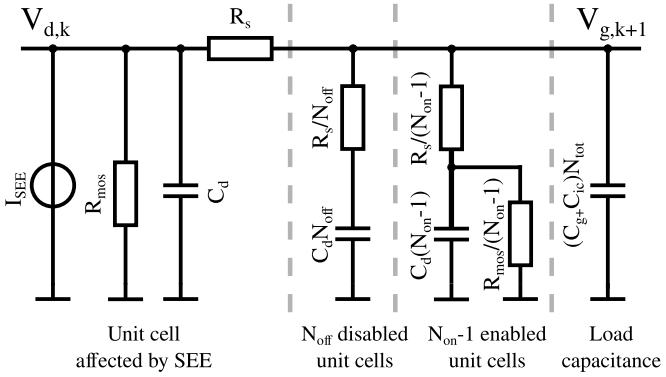

Fig. 4. Model of one oscillator stage for estimation of the SEE sensitivity. Charge is injected at the drain of an enabled unit cell (shown on the left), while all other unit cells are assumed to be unaffected.

III. Circuit Model

To better understand important design metrics of the fill factor DCRO design as well as the tradeoff between the oscillation frequency penalty and the achievable SEE sensitivity improvement, simple models will be derived first. Based on these simple models, an optimization is applied to obtain a range of values for the unit cell series resistance balancing both design aspects.

A. Oscillation Frequency Estimation

To qualitatively model the oscillation frequency, a simple equivalent circuit for a single oscillator stage based on the Elmore delay analysis [12] is proposed. The equivalent RC network for an oscillator stage consisting of N_{tot} parallel RDUCs can be seen in Fig. 3. Each of the N_{on} enabled unit cells contributes an effective parallel channel resistance of R_{mos}. Each cell is further modeled by a lumped drain capacitance C_d before the intentional cell series resistance R_s. The N_{off} disabled unit cells in each stage load the common oscillating node in addition to the N_{tot} gate capacitances C_g of the following stages and the parasitic interstage capacitance C_{ic}, which also grows linearly with the number of unit cells per stage. The resulting propagation delay of the RC network is approximated by

$$t_{\text{pd}} \approx C_d R_{\text{mos}} + \left(\left(C_{\text{ic}} + C_g\right)N_{\text{tot}} + C_d N_{\text{off}}\right) \times\left(\frac{R_s}{N_{\text{on}}} + \frac{R_{\text{mos}}}{N_{\text{on}}}\right). \quad (1)$$

To unify the resulting equations, we denote the ratio of enabled unit cells per stage by F (fill factor) and assume that F in each stage is identical

$$F = N_{\text{on}}/N_{\text{tot}} = 1 - (N_{\text{off}}/N_{\text{tot}}). \quad (2)$$

Rearranging (1) in terms of F, the oscillation frequency of a K-stage ring oscillator is obtained as

$$f = \frac{1}{2K t_{\text{pd}}} = \frac{F}{2K\left(C_d F + C_{\text{ic}} + C_g + C_d\right)R_s + 2K\left(C_{\text{ic}} + C_g + C_d\right)R_{\text{mos}}}. \quad (3)$$

Already from (3), it is obvious that for small values of R_s, the oscillation frequency of a given oscillator design depends very linearly on the fill factor F. A small nonlinear contribution is incurred for large R_s; however, the contribution of $2C_dF$ to the oscillator frequency remains below 10% for practical design values. Neglecting this nonlinear contribution, the oscillation frequency is conveniently expressed using

$$f = \frac{F}{2K\ \left(C_{\text{ic}} + C_g + C_d\right)(R_s + R_{\text{mos}})}. \quad (4)$$

It is noteworthy that the oscillation frequency is to first order independent of the number of unit cells N_{tot} in the oscillator since both the driving strength and the load of each stage increase proportionally with each cell. Instead, increasing N_{tot} improves the tuning resolution by providing more granular control over F. While this model is not entirely useful for estimation of the actual design frequency due to difficulties in determination of the included quantities, it adequately models many relevant effects, such as the independence of N_{tot} and the linearity of the tuning curve.

An important consideration is the dependence of the oscillation frequency on the value of R_s relative to R_{mos}. Rearranging (4) and disregarding constants, this relationship can be found to have the form shown in (5). This relationship will become relevant in the design optimization later on since it allows quantifying the tradeoff between oscillation frequency and SEE sensitivity

$$f \propto \frac{1}{1 + \frac{R_s}{R_{\text{mos}}}}. \quad (5)$$

B. SEE Sensitivity Reduction

As a second step, a model for the SEE sensitivity reduction provided by the addition of R_s to the unit cells is developed. For the following analysis, we consider a charge collection (as a result of irradiation) at one of the drain junctions connected to R_s, i.e., in M_2 or M_3. A circuit model for such an event is shown in Fig. 4. This small-signal model can give useful insight into the circuit behavior during irradiation. Following the established treatment of the impulse sensitivity

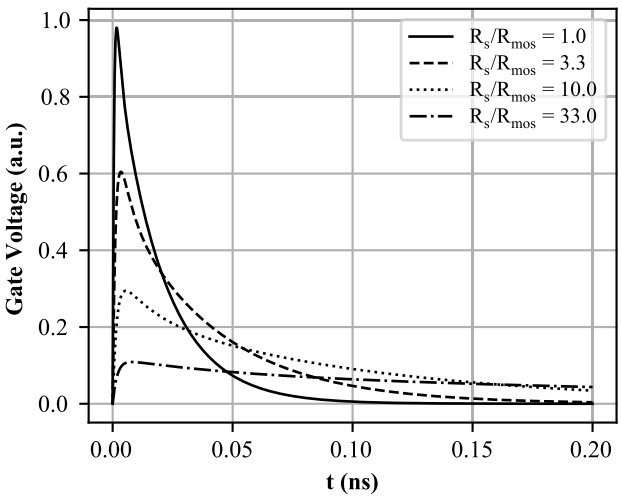

Fig. 5. Qualitative transient responses of the voltage at one oscillator stage gate node following a current impulse. Responses for different ratios of R_s to R_{mos} are shown, illustrating the lengthening and amplitude reduction of the voltage deviation.

function (ISF) of oscillator circuits [13], the stimulated voltage disturbance at the (common) gate node of the following ring oscillator stage $V_{g,k+1}$ is indicative of the resulting phase error of the oscillator at the maximum of the ISF. This quantity can be obtained by deriving the circuit transfer function

$$H_{\mathrm{SEE}}(s) = \frac{V_{g,k+1}(s)}{I_{\mathrm{SEE}}(s)}. \tag{6}$$

As a first-order estimate that allows retaining mathematical tractability, a Dirac impulse can provide a model for charge collection events during irradiation. We can therefore obtain the transient impulse response $V_{g,k+1}(t)$ by inverse Laplace transforming $H_{\mathrm{SEE}}(s)$ of the model in Fig. 4. Qualitative transient responses obtained for different values of R_s are shown in Fig. 5. It can be seen that as the ratio of R_s to R_{mos} increases, the stimulated voltage transient reduces in amplitude while at the same time lengthening in duration. In the ring oscillator circuit, this provides two benefits. The reduced voltage deviation at the common gate node results in less excess phase being regenerated by the next oscillator stage. The lengthening of the transient response will time-average the response of the SEE across a longer fraction of the period. Since the ISF is typically zero-mean, a significant lengthening across more than half of the oscillation period, therefore, contributes to a reduction of the sensitivity.

Since the full transfer function of the circuit in Fig. 4 is of fourth order, it provides little insight into the relevant parameters during the design process. To qualitatively assess the primary contributors that determine the peak SEE response generated in the circuit, we simplify this transfer function by retaining only the first-order terms and neglecting any insignificant contributors. Without sacrificing the qualitative behavior of the peak amplitude, we can in this way obtain a closed-form first-order estimate for the peak voltage deviation resulting from an impulse current injection with an area (charge) of 1 C

$$\mathrm{V}_{\mathrm{g,k+1(pk)}} = \frac{1}{\left(C_{\mathrm{ic}} + C_g + C_d\right) N_{\mathrm{tot}} \left(\frac{R_s}{R_{\mathrm{mos}}} + 2\right)}. \tag{7}$$

Equation (7) allows obtaining some intuitive properties of the circuit's SEE sensitivity. First, the sensitivity is inversely proportional to the number of unit cells in the oscillator and their capacitive parasitics. This is an intuitive relation since the voltage deviation resulting from injection of a fixed charge is inversely proportional to the capacitance it is transferred into, and the load of each stage increases linearly with the number of unit cells. However, it has to be considered that the circuit area (and therefore the area sensitive to radiation) also increases linearly with the number of unit cells. This implies that in a given radiation environment, the magnitude of phase errors can be traded off against their frequency of occurrence.

To motivate a choice of R_s, we can observe that the sensitivity of a given oscillator design with only R_s as the free variable follows the relationship:

$$\mathrm{V}_{\mathrm{max}} \propto \frac{1}{1 + \frac{R_s}{2R_{\mathrm{mos}}}}. \tag{8}$$

As expected from first principles, the sensitivity decreases significantly for values of R_s approaching or exceeding R_{mos}. In this regime, injected charge stops propagating to the common gate node and is dissipated locally in the unit cell. This shows the isolation behavior of the resistor for SEEs.

C. Design Tradeoff

Since the previous analysis has revealed that the oscillation frequency and SEE sensitivity follow simple relationships of R_s/R_{mos}, it makes sense to at least qualitatively assess the presence of optimal design points for this circuit. A favorable point would provide a significant reduction of the SEE sensitivity combined with an acceptable frequency reduction of the oscillator.

Since the ratios derived in (5) and (8) are simple enough to allow analytical optimization and range between zero and one, we can define a loss function as follows:

$$\lambda = -\mathrm{V}_{\mathrm{max}} \cdot (1 - f) \tag{9}$$

$$= -\frac{1}{1 + \frac{R_s}{2R_{\mathrm{mos}}}} \cdot \left(1 - \frac{1}{1 + \frac{R_s}{R_{\mathrm{mos}}}}\right) \tag{10}$$

$$= -\frac{2R_{\mathrm{mos}}R_s}{{R_s}^2 + 3R_{\mathrm{mos}}R_s + 2{R_{\mathrm{mos}}}^2}. \tag{11}$$

The dependence of the oscillation frequency, SEE sensitivity, and loss function on the ratio R_s/R_{mos} is shown in Fig. 6. The optimum is found by solving for the roots of the first derivative of (9), and the optimal value for R_s can be shown to be

$$R_s = \sqrt{2}R_{\mathrm{mos}}. \tag{12}$$

The identified optimum is rather shallow, so design points in its vicinity may also provide suitable compromises. The practical applicability of this optimization also requires consideration. One conceptual uncertainty of the proposed model lies

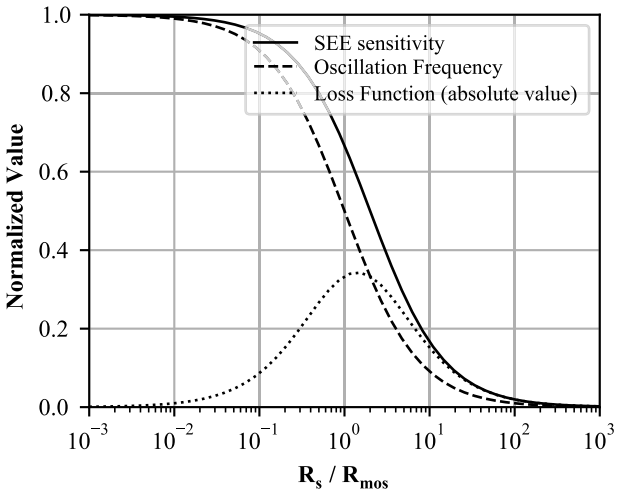

Fig. 6. Qualitative dependence of oscillation frequency, SEE sensitivity, and loss function chosen for optimization. All quantities are expressed as simple fractions of the ratio between the intentional series resistance and the effective unit cell ON-resistance.

in the definition of R_{mos}. The ring oscillator is a large-signal circuit by nature, defining that a single "effective" channel resistance has its limitations. Different values for R_{mos} might be appropriate for the analysis of oscillation frequency and SEE sensitivity, which may shift the position of the optimum. Another limitation is in the assumption made by modeling the charge collection event by a Dirac impulse. While this allows retaining mathematical tractability, typical current pulse shapes are more complex and extend over longer timescales approaching the oscillation period of high-speed oscillators.

IV. Design Procedure

In practice, the limitations of the simplified models are of little consequence since the circuit can be studied well using simulations. Using accurate models for active devices and interconnects, the oscillation frequency of this structure can be precisely estimated. With appropriate models for charge collection events during irradiation, the SEE sensitivity can be quantified in different charge regimes more precisely. An additional consideration for the design tradeoff is an increase of phase noise resulting from the additional series resistance R_s. To quantify this aspect together with the anticipated improvement in SEE tolerance, a parametric design study is carried out on a practical design. A five-stage ring oscillator composed of 100 unit cells per stage is designed in a 65-nm technology. Minimum transistor lengths are selected to maximize the oscillation frequency. Since TID degradation of the maximum drain current of pMOS devices dominates over nMOS devices in the chosen technology [14], the minimum width of pMOS devices is constrained based on their anticipated level of TID. The nMOS device widths are then obtained by determination of the $W_{\text{P}}/W_{\text{N}}$ ratio resulting in a symmetric oscillation waveform, which minimizes the contribution of flicker noise to the oscillator phase noise [15]. The impact of unequal degradation characteristics of pMOS and nMOS devices under irradiation and its impact on flicker noise upconversion can also be evaluated at this stage.

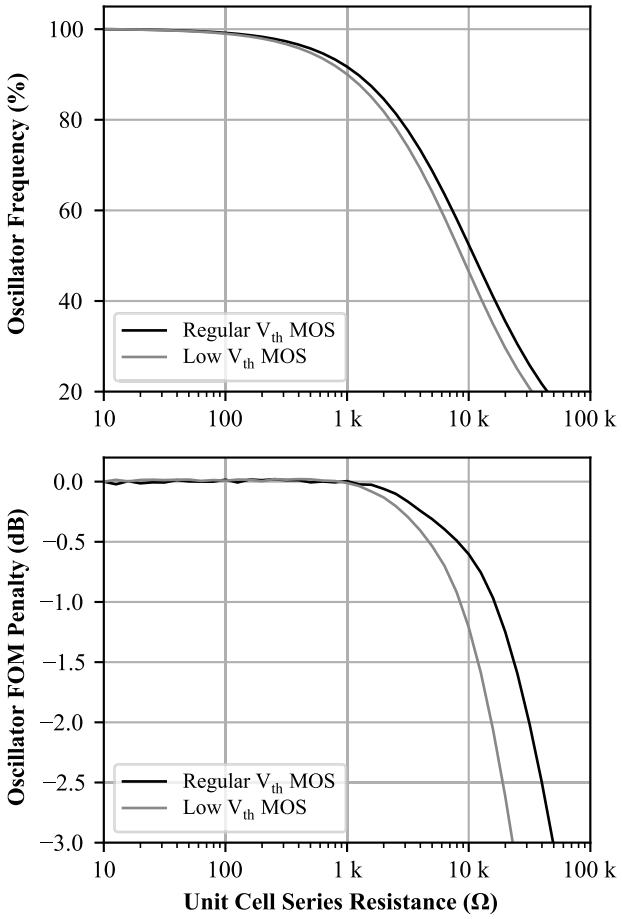

Fig. 7. Simulated dependence of the oscillation frequency and oscillator FOM on the unit cell series resistance. A strong roll-off is seen as the series resistance approaches the output resistance of the unit cell.

Following this sizing, the impact of additional unit cell series resistance on both the oscillation frequency and the oscillator figure of merit (FOM)[1] is obtained using simulations. In anticipation of the experimental validation later performed in Section VI, all simulations are performed for active device flavors with regular and reduced V_{th}. The results of this analysis are shown in Fig. 7, which compares these dependencies to the initial design. In line with the intuitions gained from the modeling, series resistances that are small compared to the unit cell output resistance have an insignificant impact on the oscillation frequency. With increasing series resistance, the frequency reduces and the FOM begins to degrade. A noise analysis based on periodic-steady-state simulations was performed, which confirmed that the thermal noise contributions of the added series resistance increasingly dominate the circuit noise. However, up to a frequency reduction of 50%, the oscillator FOM only reduces by about 1 dB. Therefore, phase noise performance is not significantly impaired as long as the frequency reduction can

[1] $\text{FOM}_{\text{DCO}} = -\mathcal{L}(f_{\text{offset}}) + 20\log_{10}(f_{\text{DCO}}/f_{\text{offset}}) - 10\log_{10}(P_{\text{DCO}}/1\,\text{mW})$.

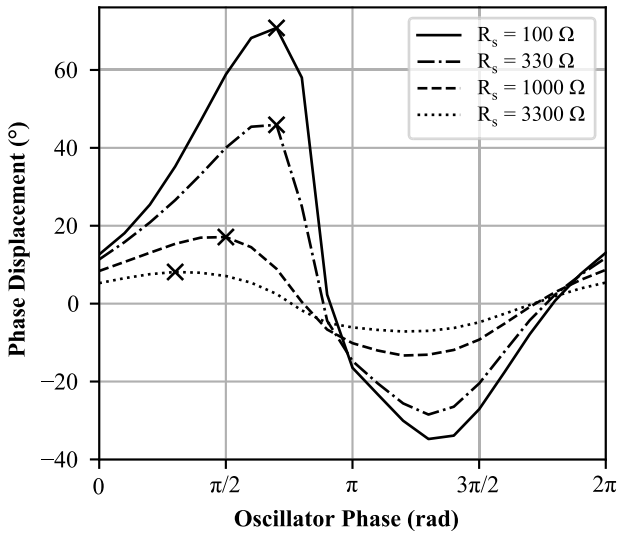

Fig. 8. Charge injection sensitivity functions obtained in the studied oscillator circuit. The maximum of the periodic, time-dependent sensitivity function (marked by the crosses) is extracted for each resistance value. The shown example data are obtained for 1 pC of injected charge on regular-V_{th} devices. Only the highlighted peak values of each sensitivity function are used in Fig. 9.

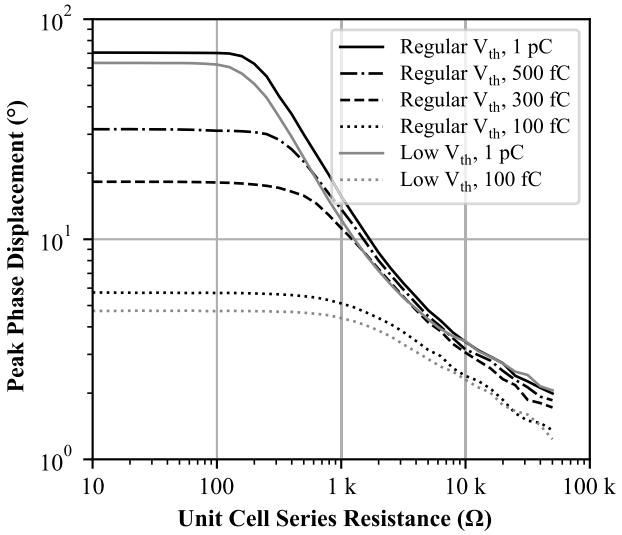

Fig. 9. Simulated worst case oscillator phase displacement for different values of unit cell series resistance. Simulations with different injected charge magnitudes are performed for comparison. The small difference between threshold voltage flavors of devices in the chosen technology is also shown.

be tolerated or recovered by other means (such as the use of low-V_{th} devices).

V. Radiation Effects Simulations

To enable optimizing the radiation hardness of this initial design by properly sizing the unit cell series resistor, the achievable reduction of SEE sensitivity is quantified using charge injection simulations. These parametric simulations cover multiple dimensions to adequately assess the circuit sensitivity.

1) As expected from the periodic, time-dependent nature of ISF of oscillators [13], SET responses of ring oscillator circuits were also shown to be time-dependent [16]. Therefore, charge injections need to be performed at multiple instants along the oscillation period to identify points of maximum sensitivity. In our simulations, twenty equidistant points along the oscillation period were chosen.
2) Because of the previously discussed circuit nonlinearity in the presence of large injected charges, the quantity of injected charge needs to be varied across the range expected from the circuit radiation environment. Charge quantities between 100 fC and 1 pC per transient were used in simulations, which corresponds to typical values stimulated by linear energy transfers (LETs) in the range from 10 to 100 $\text{MeV}\,\text{mg}^{-1}\,\text{cm}^2$ [17].
3) The dynamics of the current waveform used to simulate the charge injection influence the circuit response. To approximate the charge collection process in the chosen 65-nm technology, a double-exponential current pulse model was selected [18]. Time constants of $\tau_r = 15$ ps $\tau_f = 75$ ps were chosen for the performed simulations. These represent typical values in the chosen technology node, and the ratio of $\tau_f/\tau_r = 5$ is reported to be a good model for transients occurring in practice [19]. The sensitivity of the studied circuit to variations of these time constants was found to be small, implying that choosing a single value is adequate to reduce the number of simulation dimensions.

As charge is injected at multiple time instants of the oscillation period to account for the time-varying nature of the sensitivity, an individual sensitivity function of the oscillator is obtained for each pair of unit cell resistance and injected charge. A selection of example sensitivity functions obtained with 1 pC of injected charge is shown in Fig. 8. As a proxy for the worst case phase error stimulated by an SEE, the peak value of this sensitivity function is extracted for each parameter combination. These chosen points for sensitivity estimation are highlighted in Fig. 8. This reduction process allows summarizing the dependence of SEE sensitivity across the chosen range of collected charge and unit cell series resistance in Fig. 9.

These results are consistent with the findings from Section III. As long as the added series resistance remains small relative to the unit cell output resistance, no reduction of charge injection sensitivity is obtained. Above a threshold resistance, the stimulated oscillator phase error begins to reduce significantly. In this region, transients injected at the drain nodes of M_2 and M_3 are reduced at the common gate node, while the excess charge is drained away in the unit cell. Consequently, the propagation of the transient to the next stage of the ring oscillator is reduced, attenuating the resulting phase error stimulated.

While charge injection simulations are always subject to uncertainties due to the simplified current injection model used, they clearly indicate that significant reductions of the oscillator SEE response can be achieved by an appropriate choice of the unit cell series resistance. Suitable design points for a practical oscillator can be identified by combining the

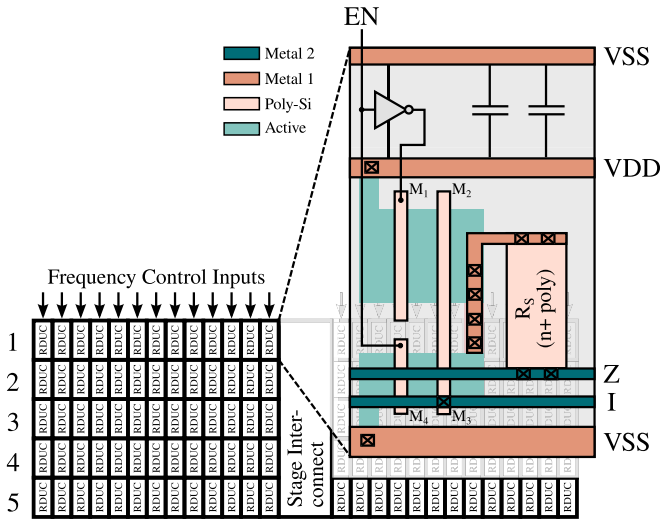

Fig. 10. Layout organization of the ring oscillator. The inset shows the layout of the abuttable RDUCs. For the design without R_s, the polysilicon resistor is replaced by metal, and however, the unit cell area is left unchanged.

results shown in Figs. 7 and 9. Since the SEE sensitivity improves monotonously with series resistance, the design is constrained by the frequency reduction and FOM penalty that can be tolerated. The area required for the implementation of large resistances in CMOS technologies might also place an upper bound to the resistance.

VI. Experimental Validation

To validate the findings obtained by simulations and quantify the improvements in SEE sensitivity experimentally, two DCROs were designed and manufactured in a commercial 65-nm CMOS technology with a nominal supply voltage of 1.2 V. One of the designed oscillators adopts the nonhardened architecture (without an additional series resistance), while the second design is composed of the proposed RDUCs promising increased radiation tolerance. Both oscillators were sized for an operation frequency of 1.28 GHz using the design procedure outlined in Section II. The digital frequency tuning range was sized over process, voltage, and temperature corners and also includes a TID degradation margin of 20%.

To fairly quantify the improvement obtainable using the RDUC approach experimentally, both oscillators need not only to operate at the same frequency but also to use an identical number of unit cells and fill factor. This constraint was fulfilled by compensating for the reduction of oscillation frequency by using active devices with reduced threshold voltage in the RDUC DCRO. The presented charge injection simulations confirm that the V_{th} flavor has very little influence on the SEE-related characteristics of the circuit. A unit cell resistance of 1.7 kΩ was chosen since it approximately equalizes the oscillation frequency of both oscillators and at the same time promises a significant reduction of the SEE sensitivity based on the preceding simulations. The unit cell resistor was implemented using an unsilicided polysilicon structure, which offers high sheet resistance and therefore occupies little

TABLE I
Summary of DCRO Design Variants

Design	Non-hardened	RDUC DCRO
Number of Stages	5	
Unit Cells per Stage	96 + 3 output buffers	
Unit Cell Series Resistance (Ω)	0	1700
MOS Threshold Voltage	Standard V_{th}	Low V_{th}
Minimum Frequency (GHz)	0.49	0.49
Maximum Frequency (GHz)	2.07	2.25
Power Dissipation (mW GHz^{-1})	5.7	5.8
Phase Noise[2] (dBc)	-104	-105
Oscillator FOM (dB)	158	159

circuit area. The resistor implementation increases the unit cell area by about 50%. Finally, both oscillators were implemented with identical physical layouts apart from the added polysilicon resistor. This was done to minimize differences in charge-sharing interactions of the unit cells, which will otherwise depend on their spacing [20]. The basic design parameters of both oscillators as well as performance figures obtained by postlayout simulations are summarized in Table I. The layout organization chosen for both designs is shown in Fig. 10.

Each oscillator occupies an area of 0.012 mm^2, which still makes the design a practical choice for area-constrained applications. Both manufactured designs dissipate 7 mW of power at the nominal operation frequency (1.28 GHz). Considering their identical power dissipation, the measurements confirm that both designs offer very similar levels of performance.

A. SEE Testing

To determine the difference in SEE sensitivity between the oscillator designs, both DCROs were integrated into identical integer-N bang-bang ADPLL circuits. In closed loop, the oscillators operate at a frequency of 1.28 GHz, phase-locked to a 40-MHz reference clock. Single-event effects in the digital PLL components (digital loop filter, frequency dithering, and feedback dividers) are mitigated by the implementation of triple modular redundancy (TMR), which leaves the DCO as the only block potentially exhibiting SEE sensitivities. The circuits were irradiated at the Cyclotron Resource Centre (CRC) Heavy Ion Facility in Louvain-la-Neuve, Belgium. Four types of ions ($^{36}Ar^{11+}$, $^{58}Ni^{18+}$, $^{84}Kr^{25+}$, and $^{124}Xe^{35+}$) with respective LETs between 9.9 and 63.5 MeV mg^{-1}cm^2 were used, while the circuits were irradiated using normal particle incidence. Fluences of at least 2×10^7 cm^{-2} were collected for each ion.

The experimental setup used during the irradiation test is shown in Fig. 11. Both PLLs present on the same die are provided with the same reference clock and use an identical loop configuration during the test. The depicted transient phase measurement system with a resolution of 4 ps was used to detect and record excursions from their nominal phase value relative to the reference clock. The detection threshold for SEE responses using this instrumentation setup was limited by the random PLL jitter of 3-ps rms. Using this setup, any excursion of the PLL phase from its nominal value of more than 16 ps for longer than 100 ns could be reliably detected and recorded.

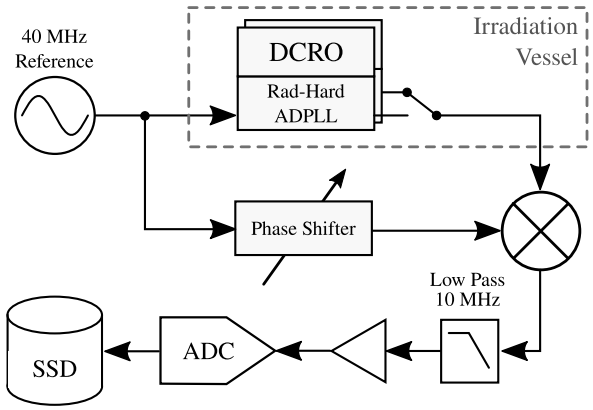

Fig. 11. Experimental setup for validation of SEE sensitivity improvement provided by the RDUC DCRO. A custom instrumentation setup is used for high-resolution, low-noise phase measurement.

TABLE II
EXPERIMENTAL DCRO PLL HEAVY-ION CROSS-SECTIONAL MEASUREMENTS

LET (MeV mg^{-1} cm^2)	Non-Hardened (cm^2)	RDUC DCRO (cm^2)
9.9 (Ar)	$\leq 5 \times 10^{-8}$	$\leq 5 \times 10^{-8}$
20.4 (Ni)	2.6×10^{-5}	$\leq 5 \times 10^{-8}$
32.4 (Kr)	5.6×10^{-5}	$\leq 5 \times 10^{-8}$
62.5 (Xe)	1.4×10^{-4}	9.4×10^{-6}

For both circuits, no SEE responses could be observed at and below 9.9 MeV mg^{-1}cm^2.

Aggregate cross sections for both circuits are summarized in Table II. Single-event effect responses were detected from the PLL containing the original DCRO design at LETs of 20.4 MeV mg^{-1}cm^2 and above, while the RDUC oscillator PLL did not show any transient responses below the highest LET of 63.5 MeV mg^{-1}cm^2. At this highest experimental LET, the cross section of the original design approaches the physical area occupied by the oscillator, while the proposed design improvement reduces the cross section by 15×. For all lower values of LET, the hardened DCRO ADPLL can be considered to be fully SEE hard.

Since the cross-sectional values presented in Table II give no insight about the magnitude of the SEE responses of the loop, Fig. 12 visualizes the observed distributions of stimulated peak phase error. It can be noted that for both oscillators, the phase errors generated in the loop are bounded below 100 ps. This value is in good agreement with the phase excursions obtained by simulations as presented in Fig. 9. At the highest values of charge collected from Xe heavy-ion irradiation, a peak phase displacement of about 60° would be anticipated, which corresponds to 120 ps for an oscillation period of 780 ps. For the nonhardened oscillator design, both the mean magnitude and the cross section scale with the heavy-ion LET. This is in agreement with the data presented in Fig. 9 since higher values of LET result in a larger amount of collected charge and therefore stimulate a larger phase error in the oscillator. For the improved oscillator implementation, it can be seen

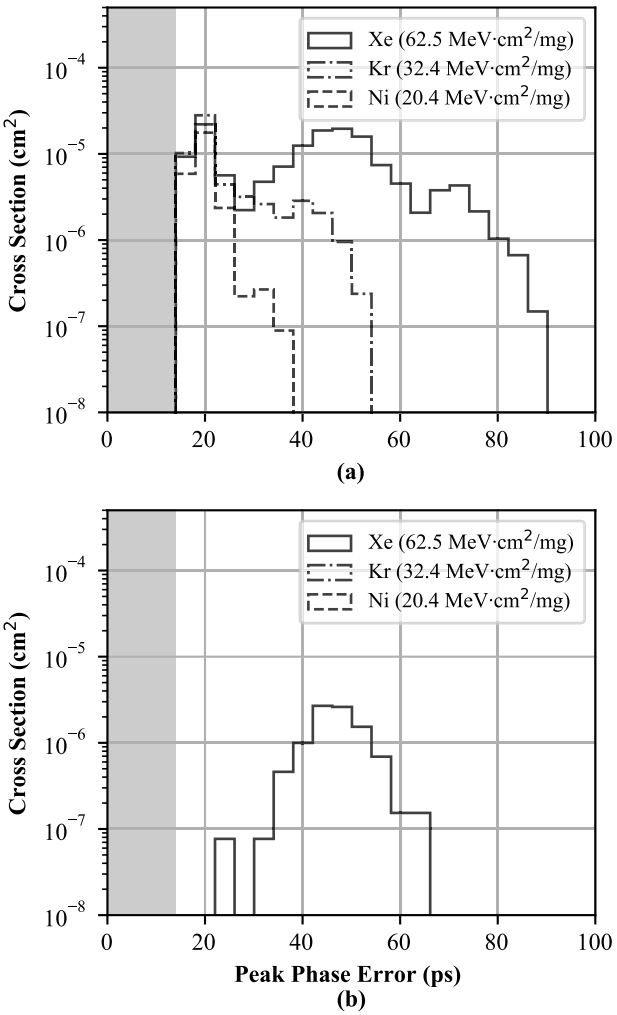

Fig. 12. Distribution of peak phase errors stimulated in the DCRO-ADPLL circuits with (a) nonhardened DCRO and (b) proposed RDUC oscillator. The improved design achieves a reduction of both the magnitude and the heavy-ion cross section. The shaded region corresponds to the PLL random jitter, inside which SEE responses cannot be detected.

that the total cross section is reduced significantly and the maximum phase error resulting from an SEE is typically only about 50 ps.

B. TID Testing

Finally, the TID tolerance of the circuit was experimentally studied using the CERN X-ray irradiation facility. The test chip was irradiated at a temperature of −10 °C, which is representative of application-specific integrated circuit (ASIC) environments in the high luminosity large hadron collider (HL-LHC) upgrade. Both oscillator designs were irradiated simultaneously over a period of 168 h at a dose rate of 8.94 Mrad h^{-1}, thus accumulating a TID of 1.5 Grad. During the irradiation process, all circuits were permanently under bias and the evolution of the oscillation frequency of both designs was monitored. Fig. 13 shows that qualitatively, the degradation behavior of both oscillators is essentially identical. The oscillation frequency degrades with a slope of approximately 1.5%/100 Mrad, which allowed the proposed oscillator design to operate at its design frequency of 1.28 GHz over a 10% supply voltage range up to 1.5 Grad. Since the oscillation

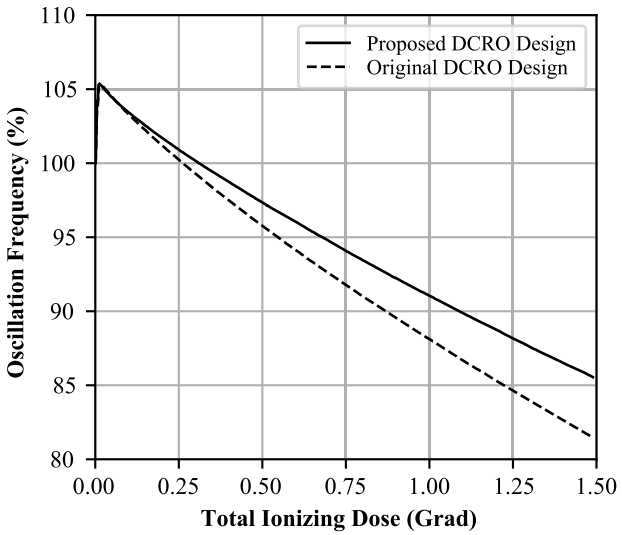

Fig. 13. Evolution of the oscillator frequency for both manufactured designs under X-ray irradiation at −10 °C. A similar degradation behavior of both oscillators was observed.

frequency of the proposed RDUC DCRO is determined by the series combination of the MOS channel resistance and the added series resistance R_s, which does not suffer from TID degradation, this design showed a slightly reduced rate of frequency reduction. The initial increase in oscillation frequency by about 5% is explained by a temporary enhancement of the $I_{d,\max}$ of nMOS transistors in the chosen technology [14]. The nMOS threshold voltage is slightly reduced by the fast build-up of oxide-trapped charge, which is compensated by slower interface trap buildup at higher doses [21]. A total dose of 1.5 Grad is the highest reported dose a ring oscillator achieves in the current state of the art.

VII. Conclusion

A DCRO with improved SEE sensitivity and high TID tolerance was presented. While TID tolerance is obtained by adoption of a wide tuning range oscillator topology, SEE immunity is achieved by implementing the oscillator from an array of unit cells. In addition, decoupling series resistors are added to each unit cell, which improves the isolation of drain nodes sensitive to charge collection from the gate nodes of the following ring oscillator stage. The combined effects of segmenting the oscillator tuning node and the oscillating nodes into small unit cells and their isolation from one another work in conjunction to provide a very high level of SEE suppression.

Incorporated in an ADPLL with TMR protection, the improved oscillator circuit remained unaffected by incident heavy-ion irradiation of LET up to 32.4 MeV mg^{-1}cm^2. Only at higher heavy-ion LET, phase transients of small magnitude were observed. Compared to an implementation without additional hardening, the LET threshold was significantly increased and the heavy-ion cross section reduced by more than one order of magnitude for the highest experimental LET. The circuit also demonstrated excellent degradation behavior when subjected to X-ray irradiation, maintaining operation at the design frequency up to a TID of 1.5 Grad.

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