Radio frequency analog electronics based on carbon nanotube transistors

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The potential to exploit single-walled carbon nanotubes (SWNTs) in advanced electronics represents a continuing, major source of interest in these materials. However, scalable integration of SWNTs into circuits is challenging because of difficulties in controlling the geometries, spatial positions, and electronic properties of individual tubes. We have implemented solutions to some of these challenges to yield radio frequency (RF) SWNT analog electronic devices, such as narrow band amplifiers operating in the VHF frequency band with power gains as high as 14 dB. As a demonstration, we fabricated nanotube transistor radios, in which SWNT devices provide all of the key functions, including resonant antennas, fixed RF amplifiers, RF mixers, and audio amplifiers. These results represent important first steps to practical implementation of SWNTs in high-speed analog circuits. Comparison studies indicate certain performance advantages over silicon and capabilities that complement those in existing compound semiconductor technologies.

The invention of the transistor in 1947 represents the birth of the solid state electronics age (1). The full scope of application possibilities began to emerge to the general public a few years later when researchers developed approaches to overcome the many scientific and technical challenges to implementing transistors in low-cost, handheld radios (2, 3). More advanced analog circuit systems and, ultimately, digital logic applications followed, thereby expanding the reach of transistors to virtually every form of modern technology. Although single-walled carbon nanotubes (SWNTs) have many remarkable properties, transistors based on them must go through a similar development sequence if they are to achieve important roles in advanced electronics. The high level of difficulty associated with this development is empirically clear from the history of the field. More than 15 years of worldwide research, beginning with the discovery of nanotubes, has failed, for example, to yield realistic demonstrations of even basic systems that provide power gain in the radio frequency (RF) range. Here, we describe some progress in the area of SWNT based RF analog electronics, including carbon nanotube power amplifiers that operate in the VHF frequency band. These results, together with integration of this technology in transistor radios that use nanotube devices for resonant antennas, fixed RF amplifiers, RF mixers and audio amplifiers, might represent important first steps in the development of SWNTs for RF electronics and other related applications.

The promise of SWNTs for electronics derives from their high mobilities and current carrying capacities (4, 5), together with their low intrinsic capacitances (6). Transistors and small-scale, simple digital logic devices that rely on individual SWNTs confirm this promise (7–9), through benchmarking studies conducted at low frequencies against single-crystal silicon (10). Scalable integration of SWNTs into digital circuits is challenging, although recent work with assembled individual tubes as active elements, or relatively dense, horizontally aligned arrays of tubes as thin film type semiconductors both show some promise (11–18). Nevertheless, the development of SWNTs for a digital electronics technology that could compete with silicon is daunting. Analog electronics (19–21), by contrast, represents a different and less well explored area of application of SWNTs. Analog devices share many of the same challenges associated with their digital counterparts, but they can be implemented at comparatively lower levels of integration density and in layouts that can better exploit the exceptional electronic and thermal properties of the SWNTs. Furthermore, analog devices require linearity, and it has been demonstrated that SWNTs have the potential to provide linearity well beyond what is possible with silicon or III–V semiconductors (22). Recent reports show some measurements of intrinsic high speed operation in transistors that use individual tubes or unaligned collections of tubes, and in a very recent case the use of a single tube device as a mixer in a radio (23), but without the sorts of layouts or performance that would be needed for realistic applications (20, 23–25). In particular, a critical part of an analog electronic circuit is the power amplifier, which converts small input signals to relatively high power outputs suitable for further processing. The ability to achieve power gain at high frequencies with 50 Ω termination is essential for applications in RF communication devices, global positioning systems (GPS), radar modules, and others. This paper presents direct measurements of RF power gain for narrow band amplifiers based on transistors that use horizontally aligned arrays of SWNTs as semiconductor thin films. The ability of these devices to drive standard 50 Ω termination systems leads to their straightforward use in analog electronics. Nanotube transistor radios in which nanotube devices provide all of the key functions demonstrate an important example of this capability.

Results and Discussion

For these systems, we developed advanced versions of basic layouts that we reported recently (11). In particular, horizontally aligned arrays of SWNTs with extremely linear configurations and high levels of alignment occupy the channel regions of transistor devices, where they act collectively as an effective thin film type semiconductor. Each of the several thousand SWNTs in a device provides an electrically continuous and independent pathway for charge transport. To achieve RF performance, we developed device designs that provide both high capacitance gate dielectrics (C_g) and low parasitic overlap capacitances (C_{gd}),

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with low resistance electrodes and probing pads. The electrodes define short gate lengths (L_g, down to 750 nm), precisely aligned to the source, drain (Ti, 1 nm; Pd, 10 nm; Au, 300 nm for source and drain; Ti, 10 nm; Au, 300 nm for gate), created either by electron beam (ebeam) lithography (Raith, eLine) or by contact mode photolithography (MJB8, Karl Suss). The alignment procedures provided an accuracy of ≈50 and ≈500 nm for the former and latter processes, respectively, as determined by the measured layouts of the electrodes. The lengths of the gate electrodes fabricated by ebeam lithography were somewhat smaller (≈100 nm) than the lengths of the channels (i.e., the separations between the source and drain electrodes). The gate dielectrics consisted either of a bilayer of HfO_2 (≈10 nm) deposited by atomic layer deposition, on top of a layer of benzocyclobutene (BCB, ≈20 nm Dow Chemical) spin cast on the SWNTs or a single layer of a HfO_2 (≈50 nm) deposited by electron beam evaporation (3×10^{-5} Torr; Temescal CV-8) directly onto the SWNTs. The thin film capacitance of the former and latter types of dielectrics were ≈160 nF/cm^2 and ≈210 nF/cm^2, respectively. Fig. 1*A* shows schematic illustrations of the device layouts, together with scanning electron (Fig. 1*B*) and optical (Fig. 1*C*) micrographs. The arrays of SWNTs had average densities of >5 SWNT/μm, with peak values as high as ≈25 SWNT/μm, in nearly ideal parallel, linear layouts, where >95% of the tubes span the source and drain electrodes and there are no tube/tube crossings or overlapping tubes. These devices and the performance enabled by them are major technical advances over previous results (11). Fig. 1*D* shows direct-current (DC) measurements of a representative device fabricated by ebeam lithography with an HfO_2 dielectric, L_g = 0.75 μm and a channel width (W) of 600 μm. This device and others like it show predominately *p* channel behavior; design and processing modifications can yield either *n* channel or ambipolar operation. In this example, g_m is as high as ≈17 mS at a drain bias of −1 V and gate bias of −0.5 V. The device is capable of current outputs up to tens of mA. The estimated average on-current per nanotube in these devices is ≈5 μA. The relatively low ratio of the currents in the on and off states results from the sizable populations (≈1/3) of metallic SWNTs in the channel. Although such low on/off ratios would preclude applications in digital logic, they can be acceptable in analog RF systems where the devices operate in a narrow range of voltages around a fixed bias point.

The large values of g_m together with small C_g, C_{gd}, lead to devices with good performance in the RF range. Fig. 2 *A* and *B* show two port *S*-parameter data (symbols) for a device with W = 300 μm and L_g = 8 μm and an HfO_2/BCB dielectric, for frequencies between 10 MHz and 10 GHz. Modeling results (solid lines) using a small signal equivalent circuit (Fig. 2B inset) with transconductance of g_m = 9.7 mS a small signal shunt resistance of R_0 = 220 Ω, a gate-drain capacitance of C_{gd} = 1.9 pF, and a drain resistance of R_d = 120 Ω, yields *S* parameters that match experimental results to within 1 dB over the 10 MHz to 1 GHz frequency range. This simple four-parameter model works well because R_d is large, allowing us to ignore C_{gs}, C_{ds}, and R_s. The values of R_d and C_{gd} are close to expectations based on the device geometry and materials. The product of g_m and R_0 is ≈2, consistent with a device that has ≈68% semiconducting nanotubes, if we assume that the conductance per tube of the metallic nanotubes is equal to the maximum transconductance per tube of the semiconducting nanotubes, a result that we find to be true empirically in our measurements of single SWNT devices (11, 20). Fig. 2*C* shows a plot of current gain ($|H_{21}|^2$) and maximum available gain (G_{max}) as a function of frequency for a device with W = 100 μm and L_g = 4 μm and an HfO_2/BCB dielectric. The maximum available power gain (G_{max}) for a transistor is (26)

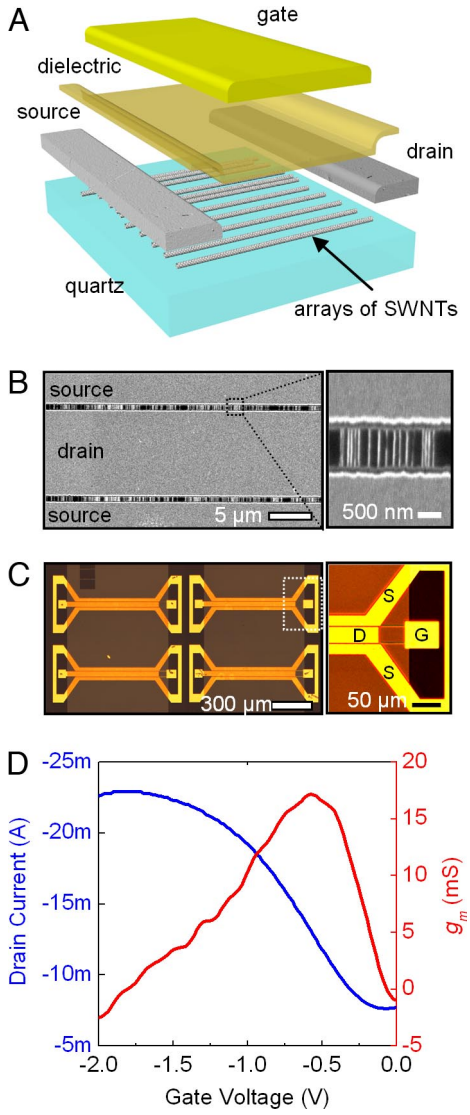

Fig. 1. Schematic illustrations, images, and electrical properties of RF carbon nanotube array transistors. (*A*) Schematic exploded view of a RF transistor that uses parallel, aligned arrays of SWNTs for the semiconductor. The critical design aspects include: (*i*) aligned source, drain, and gate electrodes to eliminate parasitic capacitance, (*ii*) short gate lengths and high capacitance gate dielectrics to maximize the transconductance, and (*iii*) low-resistance leads and contact pads. (*B*) Scanning electron micrograph of source/drain electrode pairs with bridging arrays of SWNTs. The average density of SWNTs is ≈5 SWNT per μm. (*Insets*) Magnified views. The devices used split gate layouts with probing pads in a ground–signal–ground configuration suitable for direct probing with a vector network analyzer. (*C*) Optical micrograph of an array of devices on a quartz wafer. (*Inset*) Magnified view. (*D*) Transfer characteristics of a representative device with channel length and width of ≈0.75 μm, and 600 μm, respectively, formed by electron beam lithography. The red and blue curves show the dependence of the transconductance (g_m) and drain current on gate voltage, both measured at a source/drain bias of −1 V.

$$G_{\max} = \left|\frac{S_{21}}{S_{12}}\right|, K < 1 \text{ or } \left|\frac{S_{21}}{S_{12}}(K - \sqrt{K^2 - 1})\right|, K > 1, \quad [1]$$

where the stability factor, K, is given by

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|}. \quad [2]$$

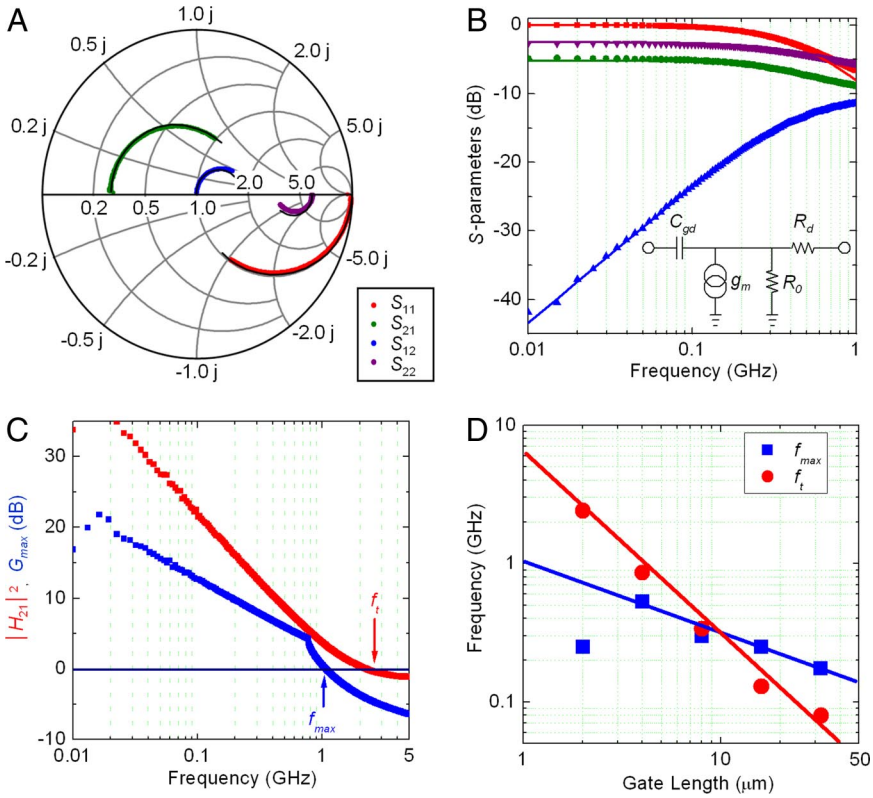

Fig. 2. Frequency response of RF carbon nanotube array transistors. (*A* and *B*) Smith chart and amplitude plot of measured (symbols) and modeled (lines) two-port *S* parameters for a device with channel length of 8 μm and width of 300 μm. (*Inset*) The four-parameter model used to simulate the device. (*C*) Current gain ($|H_{21}|^2$) and maximum available power gain (G_{max}) as a function of frequency for a device with channel length of 4 μm and width of 100 μm, showing f_T = 2.5 GHz and f_{max} = 1.1 GHz. (*D*) Plot of f_T and f_{max} as a function of gate-length devices with channel widths of 300 μm.

The extracted cutoff frequencies for current gain and power gain are f_T = 2.5 GHz and f_{max} = 1.1 GHz, respectively.

The scaling of these quantities with L_g, shown in Fig. 2*D*, provides additional insights. For diffusive transport, the intrinsic transconductance should be proportional to L_g^{-1}, whereas measurements show a weaker dependence on L_g. This difference arises from an effective transconductance, as extracted from the current-voltage curves, that is a function not only of the intrinsic transconductance, but also of the shunt resistance, R_0, associated with the metallic nanotubes, which is directly proportional to L_g. Fig. 2D shows the variation of f_T and f_{max} with L_g for photolithographically defined devices with bilayer dielectric, W = 300 μm and L_g between 2 μm to 32 μm. We find empirically, that f_T scales as L_g^{-1}, whereas f_{max} scales as approximately $L_g^{-0.5}$. The former scaling is relatively easy to understand, because f_T is proportional to g_m/C_{gd}, g_m is proportional to L_g^{-1} and C_{gd} is dominated by parasitic capacitance resulting from fringing fields, making this quantity essentially independent of L_g. (At frequencies near f_T, the capacitive reactance is much smaller than R_0 and dominates the device behavior.) The behavior of f_{max} is substantially more complicated. Simulations based on the small signal model in which g_m scales as L_g^{-1} and R_0 is proportional to L_g predict a nontrivial behavior for f_{max} that is consistent with, but not exactly the same as, a proportionality to $L_g^{-0.5}$.

We note that the peak mobilities (i.e., up to ≈2,500 cm^2/Vs for L_g = 32 μm), the intrinsic speeds (i.e., CV/I = 16 ps for L_g = 4 μm), and the intrinsic cutoff frequencies (i.e., up to 15 GHz for L_g = 4 μm) all show significant advantages compared with similarly scaled silicon MOSFETs (10). Conventional III–V technologies offer higher performance, but in *n*-channel operation. [For additional discussion, see supporting information (SI) *Text* and SI Table 1.]

SWNT Power Amplifiers. These devices are capable of producing power gain when the input and output are properly impedance matched, thereby providing the opportunity to build amplifiers that operate in the VHF range. Fig. 3*A* shows a schematic illustration of the measurement system for a narrowband amplifier, where a series inductor enables impedance matching. The inductor combines with the C_{gd} to form a resonator, stepping up the voltage on the input to a SWNT transistor that has a bilayer dielectric, W = 300 μm and L_g = 4 μm. These amplifiers provided power gains of 1–14 dB into a standard 50 Ω load for frequencies up to 125 MHz. Fig. 3*B* shows the power gain as a function of frequency for four different amplifiers. Modeling results (line in Fig. 3*B*), using the same values that reproduce the *S* parameters as discussed for Fig. 2 *A* and *B*, indicate that an additional ≈5 dB of gain could be obtained by properly impedance matching the output.

SWNT Transistor Radios. We fabricated a nanotube radio using these types of amplifiers and other SWNT transistor components to demonstrate several of the most important elements of analog electronics (Fig. 4*A*). Substrates with devices were diced into chips, each containing three SWNT transistors, and then wire bonded into a conventional ceramic DIP package. Fig. 4*B* shows the constructed circuit and packaged devices. The radio uses a heterodyne receiver design consisting of four capacitively coupled stages: an active resonant antenna, two fixed RF amplifiers, and an audio amplifier, all based on SWNT devices. The active resonant antenna uses a magnetic dipole antenna formed from 33 loops of wire on a 6-inch diameter form that has an inductance of 92.4 μH. The antenna is combined in parallel with a variable capacitor and the gate-drain capacitance of a SWNT transistor to from an LC tank circuit that steps up the voltage of the RF

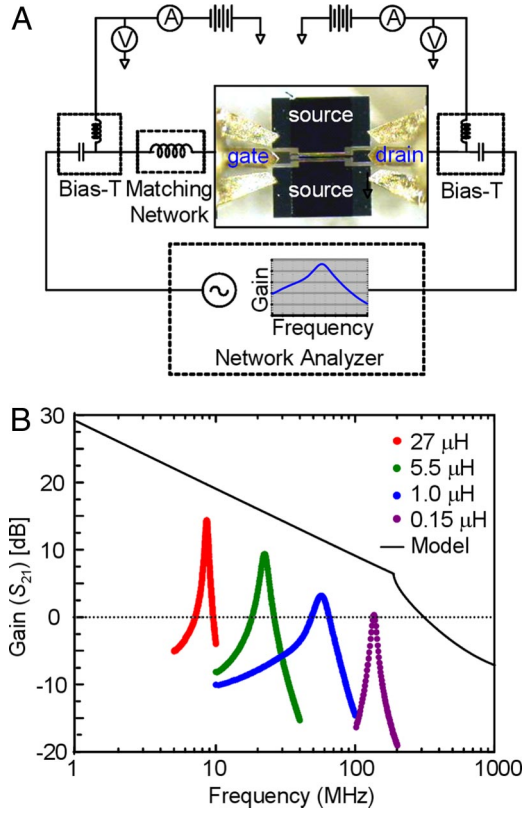

Fig. 3. Circuit schematics and frequency response of RF, amplifiers based on carbon nanotube array transistors. (*A*) Circuit schematic for an SWNT-based RF amplifier, with an illustration of the measurement system. (*B*) Plot of theoretical maximum stable gain calculated from *S* parameter data (line) and measured S_{21} data for narrow band amplifiers (symbols) with different matching inductors.

signal by a factor of 30 by stepping up the impedance. A SWNT transistor serves as a buffer to convert this high-impedance signal back to 460 Ω, resulting in a net power gain of 30 dB at the resonant frequency. For the purpose of testing, the antenna was designed to resonate at 1,090 kHz, corresponding to a local radio station in the Baltimore, MD, area. The two RF amplifiers were constructed using the same basic design shown in Fig. 3. A series inductor and shunt capacitor are used as an impedance transformer to step up the voltage to the gate of the FET. In this case, a 440-μH inductor was used and the gate-drain capacitance of the FET was supplemented with an external capacitor to provide a total capacitance of 48 pF. The first RF amplifier stage provides a signal gain of +20 dB at the resonant frequency. The second RF amplifier performed the dual function of providing gain and demodulating the signal. Biasing the gate voltage of the second amplifier slightly above the maximum gain point created a large second harmonic in the amplifier output. Applying the amplitude modulated input signal to this nonlinear amplifier produced a demodulated audio frequency signal with a conversion (mixer) gain of +8 dB. The audio amplifier design was similar to that of the RF amplifiers except the input was coupled with a transformer to produce audio frequency gain. Three SWNT transistors were connected in parallel to produce an effective transconductance of 20 mS. This was sufficient to provide 20 dB of power gain into a standard 16-Ω speaker at 1 kHz. An audio recording of a traffic report picked up by the nanotube radio is given in the SI Movie 1; a power spectrum of this output, which is dominated by frequencies in the range of the human voice, appears in Fig. 4*C*.

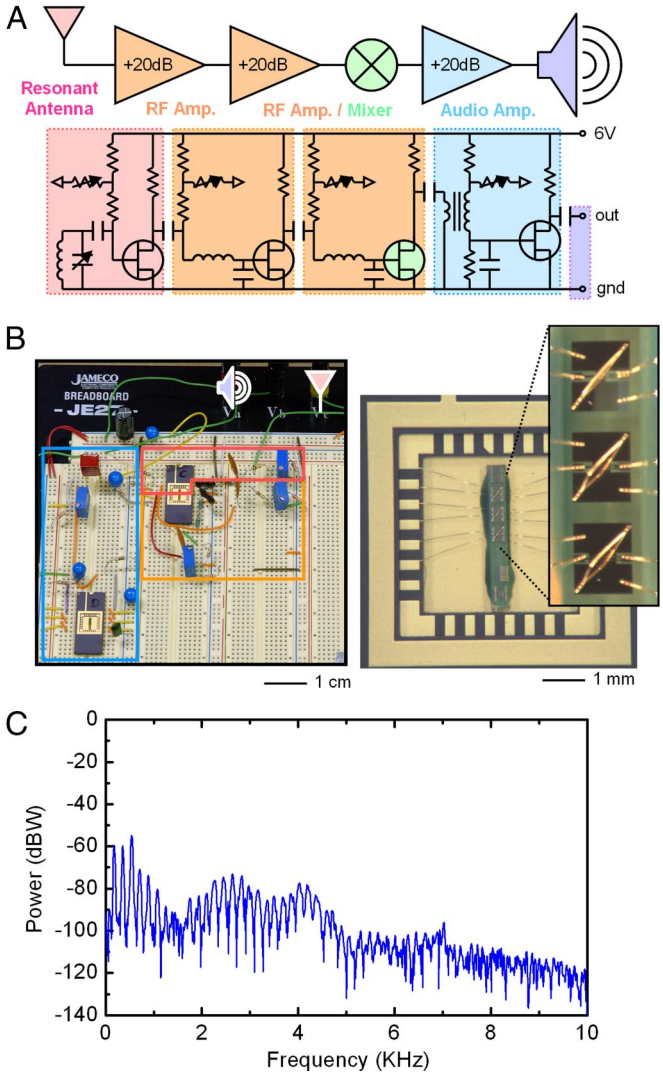

Fig. 4. Circuit schematics, images, and frequency response of a radio that uses carbon nanotube array transistors for all of the active components. (*A*) Block and circuit diagrams of a radio that uses SWNT transistors for the resonant antenna, two fixed RF amplifiers, an RF mixer, and an audio amplifier. (*B*) Image of the radio, with magnified views of SWNT transistors wire bonded into DIP packages. (*C*) Power spectrum of the radio output measured across a 16 Ω load, recorded during a commercial broadcast of a traffic report.

Conclusions

The results described here represent important first steps toward the implementation of SWNT materials in high speed analog electronics, in a manner that appears to have favorable scaling characteristics. Hundreds of devices, interconnected into desired planar layouts on quartz or even transferred to silicon are possible, thereby opening up the possibility of achieving systems with significantly more complex functionality. Straightforward downscaling of the dimensions of the types of devices introduced here should enable further improvements in performance. Benchmarking studies suggest that this class of device has the potential to provide a high performance *p* channel RF technology capable of complementing silicon and III–Vs in heterogeneously integrated systems. Keys to realizing the full potential of this technology include increasing the density of the tubes, eliminating the metallic tubes, and reducing the device dimensions in a way that retains high performance. These possibilities, as well as strategies to improve the density of the SWNTs in the arrays, are promising directions for future research.

Materials and Methods

Chemical Vapor Deposition of the Arrays of SWNTs. The growth of the arrays of SWNTs was accomplished by chemical vapor deposition growth on quartz. The process starts with cleaning of an ST-cut single crystal quartz wafers and then annealing them in air at 900°C for 8 h. 0.1–0.2 nm thick Fe film was deposited by electron beam evaporation (Temescal BJD1800, evaporation rate of 0.1 A/s) onto a photolithographically (standard UV photolithography) patterned layer of photoresist (AZ5214) on the quartz. Photoresist and photoresist residue were cleaned by acetone and stripper (AZ Kwik), respectively. To form isolated iron oxide nanoparticles, the samples were then annealed at 900°C for 1.5 h. The SWNT growth process began with flushing the chamber with a flow of Ar (3,000 sccm) for 2 min and then heating the furnace to 925°C while flowing H_2 (300 sccm). Ethanol vapor is used as a carbon source by passing gases (8 sccm H_2 and 8 sccm Ar) through an ethanol bubbler held a 0°C in a water bath chiller. Growth was terminated after 20 min, and the chamber was then cooled in H_2 and Ar flow. After the growth scanning electron micrograph (Raith e-LiNE) of the SWNTs were taken with 1kV acceleration voltage (SI Fig. 5).

Transistor Fabrication. ***Long channel-length devices.*** We have used standard UV photolithography to fabricate devices for long channel (2–32 μm) length. The fabrication process for long channel length devices began with fabrication of source/drain electrodes on SWNT array by UV photolithography (MJB8, Karl Suss) using AZ5214 photoresist. Metal for the source and drain electrodes (Ti:1 nm, Pd:30 nm) was deposited by e-beam evaporation (Temescal BJD1800; base pressure of 2e-6 torr). Liftoff was accomplished by rinsing in acetone for 10 min, and followed by rinsing with isopropanol and deionized water. Oxygen reactive ion etching (200 mT, 20 sccm O_2 flow, 100W RF power) removed SWNTs outside of the channel region, which was protected by a patterned layer of photoresist (AZ5214). Spin casting 2% BCB (20 nm) and atomic layer deposition of HfO_2 (10 nm) defined high capacitance bilayer dielectrics. Gate metal (Ti, 2 nm; Au, 30 nm ebeam evaporation Temescal BJD1800; base pressure of 2e-6 torr) is defined top of the dielectric by UV photolithography. After defining the gate metal, dielectric on the source/drain contact pads was removed by etching with concentrated HF acid.

Short channel-length devices. The fabrication of short channel-length devices (0.75 nm-2 μm) with these arrays of SWNT began with spin coating of a layer (400 nm) of electron beam (e-beam) resist (495PMMA-A6, Microchem) at 2,000 rpm for 30 s on the SWNT/quartz. The samples were then baked on a hot plate at 220°C for 2 min. To avoid charging during electron beam (e-beam) writing process, a uniform layer of Al (12 nm) was deposited by e-beam evaporation (Temescal BJD1800; base pressure of 2e-6 torr) onto the resist. The source-drain pattern was the defined with an e-beam lithography tool (Raith e-LiNE) using an accelerating voltage of 10 KV and a current dose of 140 μC/cm^2. After writing, the Al was removed with a KOH etching solution; the PMMA was developed by immersion in a solution of a 1:3 part solution of MIBK and IPA, for 45 s. Metal for the source and drain electrodes (Ti, 1 nm; Pd, 10 nm; Au, 300 nm) was deposited by e-beam evaporation (Temescal BJD1800; base pressure of 2e-6 torr). Liftoff was accomplished by rinsing in acetone for 10 min, and followed by rinsing with isopropanol and deionized water. Oxygen reactive ion etching (200 mT, 20 sccm O_2 flow, 100W RF power) removed SWNTs outside of the channel region which was protected by a patterned layer of photoresist (AZ5214). The gate dielectric (50 nm HfO_2) was deposited by e-beam evaporation (Temescal BJD1800, base pressure is 2e-5 Torr). After dielectric deposition, the gate pattern was defined by a second e-beam lithography step, using process conditions similar to those used for the source-drain layer. The gate electrode was aligned ($\pm$50 nm precision) to source and drain using previously patterned alignment markers. After defining the gate metal, the HfO_2 on the source/drain contact pads was removed by etching with concentrated HF acid.

Transistor Radio. For additional details, see *SI Text*.

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