Radio Frequency Digital to Analog Converter

by

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S.B., Massachusetts Institute of Technology (1997)
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Abstract

Dynamic performance of high speed, high resolution digital-to-analog converters (DACs) is limited by distortion at the data switching instants. Inter-symbol interference (ISI), imperfect timing synchronization and clock jitter are all culprits. A DAC output current controlled by an oscillating waveform is proposed to mitigate the effects of the switching distortion. The oscillating waveform should be a multiple ($k*f_s$) of the sampling frequency (f_s), where $k>1$. The waveforms can be aligned so that the data switching occurs in the zero regions of the oscillating output. This makes the DAC insensitive to switch dynamics and jitter. The architecture has the additional benefit of mixing the DAC impulse response energy to a higher frequency. An image of a low IF input signal can therefore be output directly at a high IF or RF frequency for transmit communications applications. A narrow-band sigma-delta DAC with eight unit elements is chosen to demonstrate the radio frequency digital-to-analog converter (RF DAC) concept. A sigma-delta architecture allows the current source transistors to be smaller since mismatch shaping is employed. Smaller current source transistors have a lower drain capacitance, allowing large high frequency output impedance to be achieved without an extra cascode transistor. Elimination of the cascode reduces transistor headroom requirements and allows the DAC to be built with a 1.8V supply. The RF DAC prototype is targeted to GSM transmit specifications and implemented in 0.18μm CMOS technology. Measured single-tone SFDR is -75dBc, SNR is 52dB, and IMD3 is -70.8dBc over a 17.5MHz bandwidth centered at 942.5MHz. Measured SNR has the predicted dependence on the phase alignment of the data clock and oscillating pulse.

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1 Introduction

One of the largest growth areas in electronics over the past five years has been in applications of wireless communications. High resolution analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are required in these systems to meet challenging signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), and distortion specifications in the presence of large nearby interferers. Additionally, recent trends have pushed towards higher speed data converters in pursuit of a "software radio" system, where receiver digitization is performed at an intermediate frequency (IF) or higher [1]. This permits channel selection filters and demodulation to be performed in the digital domain. Ideally, if the whole band can be digitized at a high speed, the band select filter can also be pushed to the digital domain. Reference [2] claims that converting to digital as early as possible in the receiver chain can result in overall size, weight and power reductions of over an order of magnitude. Similarly on the transmitter side, high speed, accurate DACs require fewer mixing and filtering stages before the antenna. The desirability of these programmable architectures has created a demand for high performance, high speed data converters.

Figure 1-1 shows conventional transmitter and receiver architectures. Both architectures typically include a low or zero-IF data converter and one or more mixing stages. The mixing stages may not be completely eliminated due to speed and resolution limitations of modern day data converters. Of particular interest for radio applications are ADCs whose sampling frequency is four times the carrier frequency, called $f_S/4$ bandpass converters. This ratio of IF to sampling frequency makes mixing down to baseband particularly simple in the digital domain, as depicted in Figure 1-1.

Jitter in the sampling/conversion clock is one of the main resolution limits of high speed data converters. Although there are many other noise sources, sampling jitter starts to dominate as input frequencies increase. Traditional approaches to mitigating the DAC clock jitter problem have focused on either building a high-power sampling clock with low jitter or using systems with oversampling to reduce the inband noise. This research initially concentrated on the limits of sampling jitter in converters and ultimately led to the development of a radio frequency (RF) DAC. This DAC trades sampling clock jitter for phase noise. It also has the additional benefit of mixing the DAC impulse response energy to a higher frequency. An image of a low IF input signal can

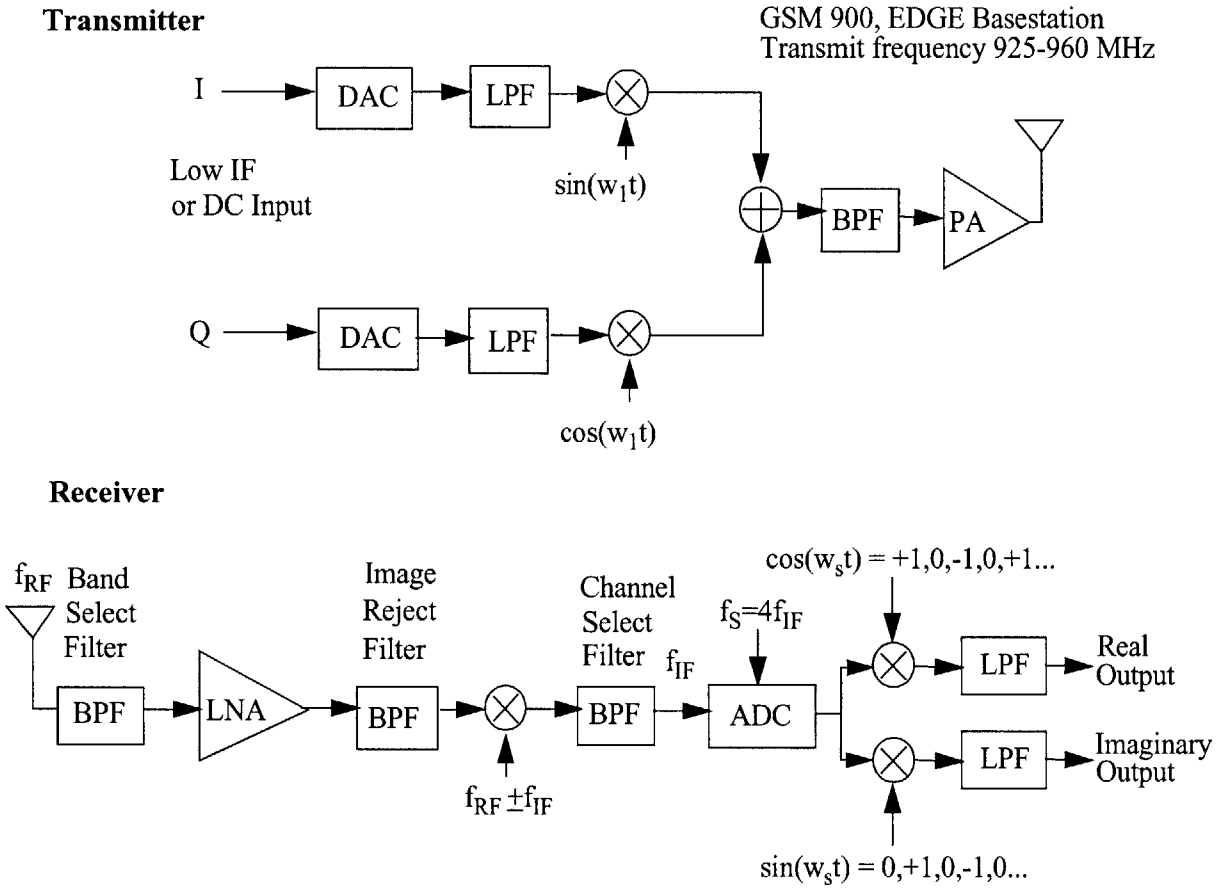

Figure 1-1: Conventional transmitter and receiver architectures.

therefore be output directly at a high IF or RF frequency for transmit communications applications to offer a lower noise, power, and area transmit solution. This saves power and hardware relative to a conventional transmitter architecture by eliminating the need for mixers and intermediate frequencies.

This section reviews state-of-the-art in data converters and the sampling jitter problem. Chapter 2 describes the new RF DAC concept. Chapter 3 is an analysis and comparison of the SNR of a square wave pulse used in conventional DACs and the cosine feedback pulse used in the RF DAC. Chapter 4 discusses trade-offs in the implementation of a prototype to demonstrate the new concept. Measurement results for the RF DAC prototype are presented in Chapter 5. Conclusions and areas for future work are detailed in Chapter 6.

1.1 State-of-the-art High Speed ADCs

State-of-the-art ADC architectures are dependent on the speed and resolution requirements of the converter. High speed (>1GHz) low resolution (6b) converters are driven by disk drive and high-speed Ethernet applications. These converters typically use a flash architecture, often with interpolation to save area and power or interleaving to increase speed [3]. They are currently limited by the speed and resolution of the sampling operation as well as by offsets and mismatches in interleaved paths [3] [5]. High resolution (>10b) converters typically utilize pipeline architectures and currently achieve as high as 100MSample/s rates. The resolution and speed of these converters are limited by device matching and the speed of closed-loop operational amplifiers respectively [6]. Digital calibration techniques can be used to ease the matching requirements in pipeline converters [7].

As the sampling frequency increases, continuous-time (CT) sigma delta modulators (ΣΔMs) have been preferred for narrowband applications because they do not have the op-amp settling-time constraints or the fast, high-precision sample and hold (S/H) requirements that limit the maximum clock rate in discrete-time (DT) ΣΔMs and upfront sampled ADCs. A block diagram of a typical current feedback CT ΣΔM is shown in Figure 1-2. The input is no longer sampled upfront. Instead the error signal at the output of the CT resonator is sampled. The CT resonator can be active g_m-C or passive LC, so no fast-settling op-amps are needed in the loop. This makes CT ΣΔMs particularly attractive for high speed, high bandwidth conversion. Indeed recent work has shown that sample rates of CT ΣΔMs have been steadily increasing and have surpassed those of their DT counterparts [2] [8] [9] [10] [12].

Unfortunately for their potential as high speed converters, the effect of clock jitter on the performance of CT ΣΔMs is worse than an upfront sampled system. The effect of clock jitter at the ADC is shaped by the feedback loop. The jitter in the DAC clock, however, is added directly to the input and does not benefit from loop shaping. Furthermore, this jitter on the DAC clock acts on the quantized DAC signal, which is a stepped version of the CT input. Thus, the CT ΣΔM ADC ends up with more SNR degradation due to jitter than the upfront sampled system, which samples the un-quantized input directly [21].

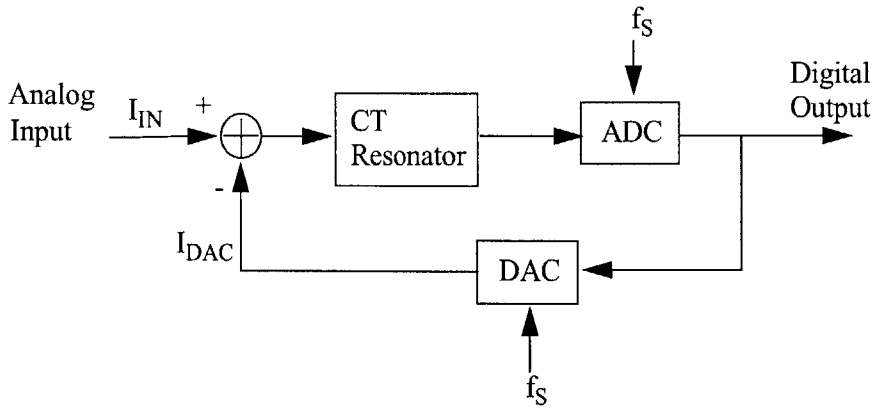

Figure 1-2: Typical CT ΣΔM block diagram.

Reference [10] concludes that most gigahertz CT ΣΔM ADCs are limited to an effective oversampling ratio (OSR) of about 16. Above this OSR, they are dominated by in-band white noise due to jitter rather than shaped quantization noise. Although DT ΣΔMs have been pushed to high speeds, their speed is limited due to the use of closed loop operational amplifiers [11]. Table 1-1 summarizes the performance of some of the best state-of-the-art high-speed ADCs.

Table 1-1 State-of-the-art high-speed ADCs

ADC Architecture	**SNDR (ENOB)**	**Power**	**Sampling Rate**	**Signal Bandwidth**
CMOS Flash [4]	33dB (5.5)	545mW	1.3GHz	650MHz
CMOS Interpolating Flash [3]	36dB (5.6)	300mW	900MHz	450MHz
CMOS Pipeline [6]	57dB (9.4)	180mW	100MHz	50MHz
SiGe HBT CT ΣΔM [10]	40dB (6.3)	450mW	4GHz	20MHz centered at 1GHz
AlInAs/GaInAs CT ΣΔM [2]	75.8dB (12) in 1MHz band 39dB (6) in 60MHz band	3.2W	4GHz	1MHz/60MHz centered at 180MHz
GaAs CT ΣΔM [12]	41dB (7) in 25MHz band 66d B (11) in 100kHz band	1.8W	3.2GHz	25MHz/ 100kHz band centered at 800MHz
CMOS DT ΣΔM [11]	87dB (14)	150mW	64MHz	2MHz

1.2 State-of-the-art High-Speed DACs

Communications applications are pushing the sampling speed and frequency domain performance requirements of high-speed DACs [14]. Direct digital synthesis (DDS) is another application demanding high speed DACs with good spurious performance [13]. Specifications of SNR, SFDR, and adjacent channel power ratio in a narrow bandwidth are becoming more important than static specifications such as integral nonlinearity (INL) and differential nonlinearity (DNL). Furthermore, third-order distortion (IMD3) is often the only significant harmonic that falls inband in narrowband communications applications. The SNR and SFDR performance of high-speed, high-resolution DACs is limited by dynamic errors at the switching instants [15] [17] [30]. This causes the SFDR performance to worsen as the input frequency increases. One source of dynamic degradation is inter-symbol interference (ISI). When ISI is present, the DAC output is dependent on the current data as well as the previous data, often in a nonlinear way. This problem is solved by using a return-to-zero (RZ) DAC output pulse, which essentially nulls the memory the DAC had of the previous data. However, this approach introduces large steps in the DAC output, thereby increasing jitter sensitivity and causing problems in the linearity of the output stage [21] [36]. The jitter problem will be studied further in Section 1.3.

Another source of DAC degradation is imperfect synchronization of the switch control signals between the elements of the DAC. This is especially troublesome in a multibit DAC, where glitches are created if the bits switch at different times. This has been solved by a combination of building a synchronization block in front of the switches and careful layout to match path delays [15] [30]. The accuracy of this method is still limited by the matching achievable in the synchronization blocks and layout routing.

The author has not been able to find any work on directly solving the clock jitter problem in DACs. DACs rely on a high-power sampling clock with low jitter and large oversampling ratios to reduce the inband noise. Return-to-zero (RZ) DACs have been shown to have worse jitter performance than non-return-to-zero (NRZ) DACs. A dual return-to-zero DAC has been proposed in [16] to alleviate the jitter problem in RZ DACs.

Table 1-2 State-of-the-art DACs

DAC Type	Resolution	Power	Sample Rate	Performance
Current Steering Nyquist [15]	10b	110mW	1GSample/s	SFDR = 61dB@ 500MHz output
Current Steering Nyquist [37]	16b	not given	400MS/s	SFDR~80dBc@300 MHz output, IMD3=-80dBc to 300MHz
Current Steering Nyquist [20]	14b	180mW 210mW	100MHz 200MHz	SFDR=72dBc @42.5MHz output with f_s=100MHz SFDR=50dBc @90MHz output with fs=200MHz
ΣΔ DAC [19]	13b	95mW	120MHz	DR=85dB SNDR=80dB both in 5MHz BW
ΣΔ DAC [18]	16b	290mW	96kHz	SNR=113dB in a 40kHz BW

Narrowband ΣΔ DACs with oversampling and mismatch shaping would seem useful in solving static and dynamic mismatch problems. Research in narrowband ΣΔ DACs has been driven by audio applications, which require high resolutions at relatively low speeds [18]. Multibit ΣΔ DACs are beginning to be investigated for MHz range-frequency applications [19]. Table 1-2 summarizes the performance of state-of-the-art high speed Nyquist rate and ΣΔ DACs.

1.3 Jitter Limits in Converters

Both the pipeline and flash converter ADC architectures utilize up-front samplers or track-and-holds. Resolution in these converters is not currently limited by jitter in the sampling process. However, resolution will become jitter-limited as technology improves the speed of converters as well as the other sources of converter noise.

In any up-front sampled ADC, sampling clock timing jitter creates an error in the sampled value. Regardless how much resolution the ADC has, it will never achieve better signal-to-noise ratio (SNR) than this sampling operation. The theoretical limit due to sampling a signal at frequency f_{in} with a jittered clock is [21], [22]

$$SNR = 20\log\frac{\sqrt{OSR}}{2\pi\sigma_t f_{in}} \tag{1.1}$$

where σ_t is the standard deviation of a Gaussian, white-noise random sampling jitter in seconds and OSR is the oversampling ratio, i.e. the ratio of the sampling frequency f_s to the Nyquist bandwidth of the signal $2f_b$. As the input frequency f_{in} increases, the achievable SNR due to a fixed amount of sampling jitter σ_t decreases. Plugging in $OSR = \frac{f_s}{2f_b}$ to Equation 1.1 gives

$$SNR = 20\log\frac{\sqrt{f_s}}{f_{in}}\frac{1}{2\pi\sigma_t\sqrt{2f_b}} \tag{1.2}$$

Equation 1.2 shows that even if the sampling frequency f_s is scaled with the input frequency f_{in}, the maximum achievable SNR still degrades as the square root of f_{in}.

The SNR for high speed DACs is similarly jitter limited. SNR for a RZ and an NRZ DAC are derived in Appendix A. For a RZ DAC, the SNR limit is shown to be

$$SNR = 20\log\frac{n}{2\sqrt{f_s f_b}\sigma_t} \tag{1.3}$$

where n is the fractional duration of the RZ pulse relative to the sampling period.

In the NRZ DAC case the SNR limit is shown to be

$$SNR = 20\log\left(\frac{y_{rms}}{\sqrt{2f_s f_b}\sigma_t y_{diffrms}}\right) \tag{1.4}$$

where y_{rms} is the rms value of the digital input and $y_{diffrms}$ is the rms value of the difference in input values. The jitter limited SNRs derived in Equation 1.2, Equation 1.3, and Equation 1.4 are plotted in Figure 1-3 versus the frequency of the input tone f_{in}. They are compared over a Nyquist bandwidth ($f_s=2f_b$) with f_s =1GHz and σ_t = 1psec. The RZ DAC pulse is half (n=0.5) the sampling period. Equation 1.4 is plotted for a 14-bit, 2-bit and 1-bit NRZ DAC.

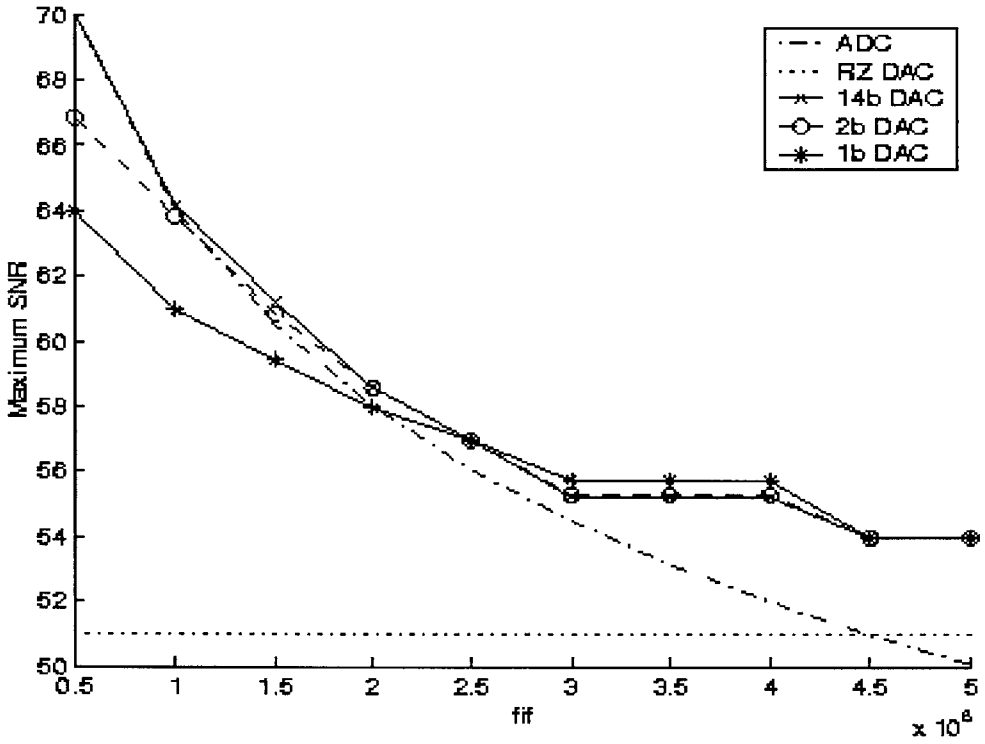

Figure 1-3: Jitter-limited SNR computed over a Nyquist bandwidth. All converters are sampling at f_s=1GHz with a clock jitter σ_t=1psec. In the RZ DAC the pulse is half the sampling period (n=0.5).

As expected, the RZ DAC has a jitter-limited SNR that is independent of the input frequency and the number of bits in the DAC. The RZ DAC pulse always has two edges with jitter, whereas the NRZ DAC has a random number of edges between 0,1, and 2. The number of transitions in the NRZ DAC increases as the input frequency increases, so the SNR decreases. The NRZ DAC curves depend on the number of bits at low input frequencies. For small f_{in}, the oversampling ratio is large and there are many samples per period. Many samples per period with a large number of bits translates to small step sizes. These small step sizes translate to less error and better SNR. As the number of bits increases, the low-frequency SNR limit approaches that of a sampler. At large input frequencies, however, the SNR limit becomes independent of the number of bits in the DAC. This case corresponds to fewer samples per period, or large transitions at every sampling instant. These transitions are so large that they become practically independent of how well they are quantized.

Near Nyquist sampling the NRZ DAC jitter-limited SNR is expected to be 3dB higher than the RZ DAC SNR. This is because the RZ pulse has an extra switching edge, causing a $\sqrt{2}$ larger error. The sampler SNR curve is lower near Nyquist sampling due to the lower signal power in the rms value of a sinusoid versus a square wave.

2 RF DAC Concept

2.1 Background

Zhang [23] recognized the problem of clock jitter in the feedback DAC waveform of a CT ΣΔ ADC. His thesis described the use of a sine wave to generate a RZ DAC output pulse, as illustrated in Figure 2-1. Figure 2-1 (a) shows an $f_s/2$ sine wave at the input to the mux, where f_s is the data update rate of the DAC. The mux switches at the zero crossings of the sinusoid, depending on the value of the input data. Figure 2-1 (b) shows the same concept implemented using a sine wave at frequency f_s with a DC offset. If the sine wave is noise free and perfectly locked to the data clock, first order jitter insensitivity is achieved in Figure 2-1 (a) due to the zero value of the control waveform at the switching instant. First and second order jitter insensitivity are expected from the waveform of Figure 2-1 (b) due to the zero value *and* zero slope of the control waveform at the sampling instants.

2.2 RF DAC Description

The RF DAC concept builds on Zhang's theoretical work by using multiple pulses per DAC output value. A harmonic of the DAC data clock (frequency f_s) is used as the DAC control waveform (frequency f_o). Figure 2-2 (a) shows the impulse response of a conventional DAC, while Figure 2-

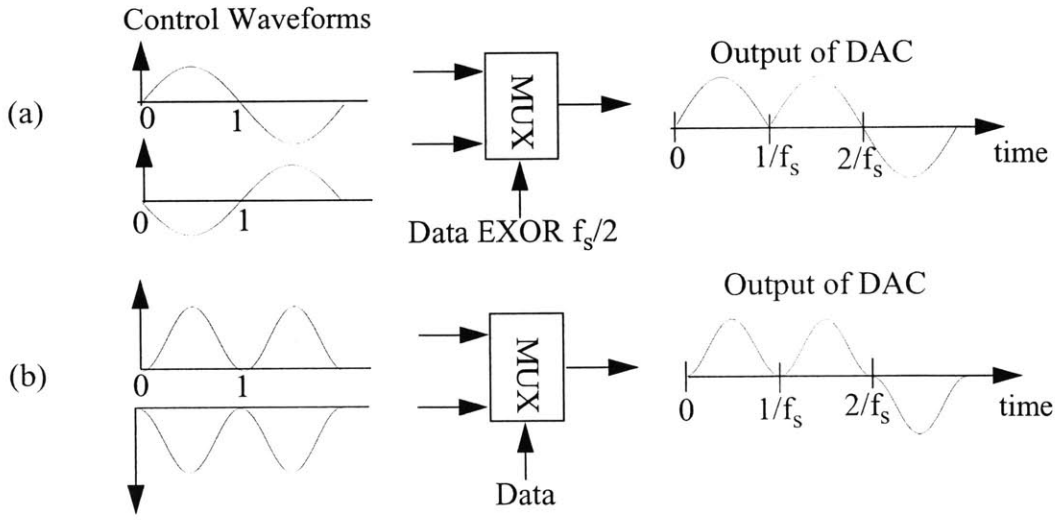

Figure 2-1: Binary DACs with jitter insensitive output [23].

2 (b), (c), (d), and (e) show possible DAC impulse responses using this RF DAC concept. The control waveform frequency f_o could be any multiple of the DAC data clock, $f_o=kf_s$. The RZ pulses do not have to be identical, as illustrated by the examples in Figure 2-2 (d) and (e).

The frequency domain impulse responses for the time domain waveforms of Figure 2-2 are shown in Figure 2-3. Cases (b)-(e) and the family of curves $f_o=kf_s$ implemented as in Figure 2-2 (b)-(e) have a high energy lobe at frequency kf_s. This allows an image of a low frequency DAC's input to be output with more energy at higher frequencies. This can also be thought of as a 'mixing DAC,' since the oscillating control waveform essentially mixes the DAC impulse response up to kf_s. Note that the control waveform does not have to be a perfect sinusoid to produce the high frequency lobe. Any distortion in the control waveform will cause a slightly different DAC impulse response and thereby a different inband gain, but the SNR at the output is not disturbed.

The concept of a DAC with an oscillating control waveform could be applied to Nyquist rate DACs, ΣΔ DACs, feedback DACs in ΣΔ ADCs, binary DACs, multibit DACs, current steering DACs, or resistor ladder DACs. The embodiments shown in Figure 2-2 are not the only possibilities. Any oscillating DAC control waveform with $f_o=kf_s$ can achieve a large high frequency lobe in the impulse response. The additional constraints $f_o=kf_s$ and switching at the zero crossings of the control waveform reduce ISI and improve noise performance.

2.2.1 RF DAC Advantages

The RF DAC has several advantages over conventional DACs. Some advantages are listed below:

- Ability to directly output a high frequency signal with large energy. This could be a high IF frequency or even a direct RF frequency in transmitters in communications systems. This can save power and hardware by eliminating the need for mixers, choppers, and filters in the additional intermediate frequencies currently present in state-of-the-art communication transmit systems. This concept is depicted in Figure 2-4. Noise and linearity requirements of the DAC are also relaxed, since there are fewer circuits before the antenna.

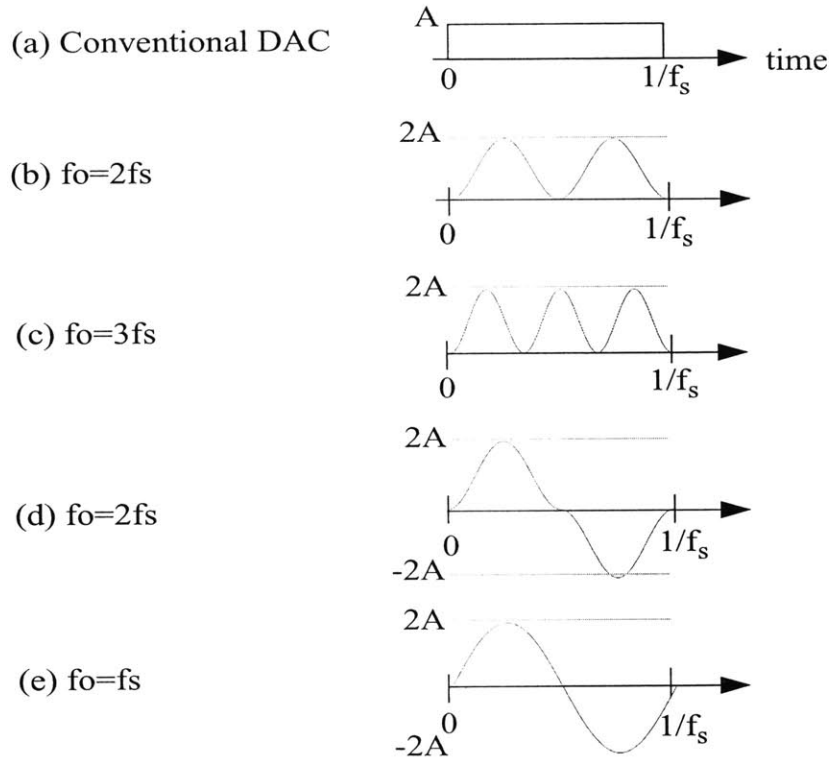

Figure 2-2: DAC impulse response with multiple pulses per sampling period.

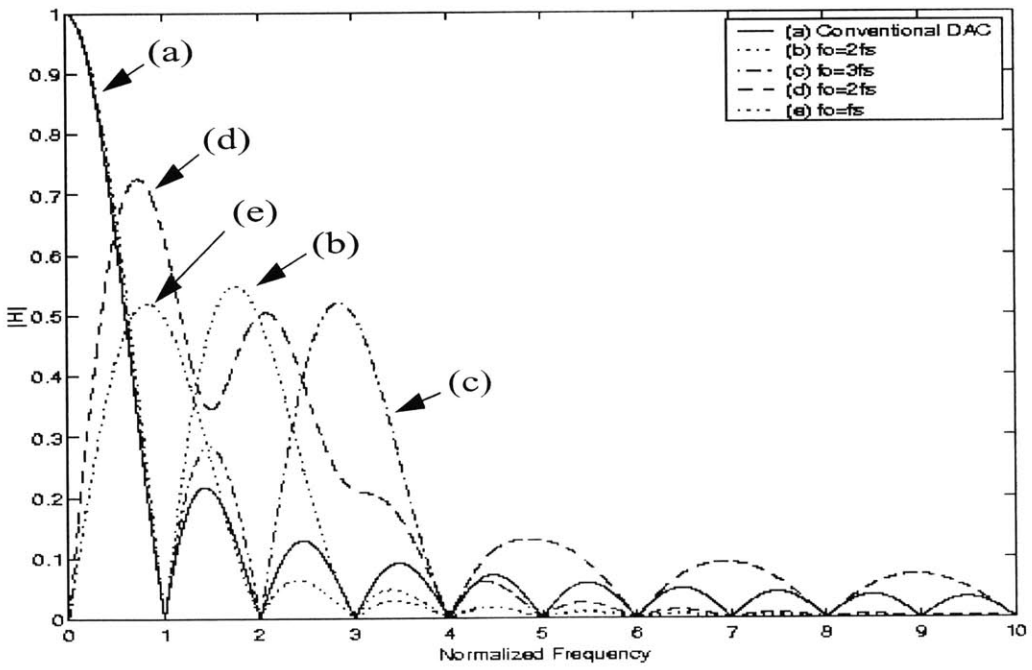

Figure 2-3: Frequency domain impulse response magnitude for the waveforms of Figure 2-2 normalized to f_s.

- Reduction of switch timing synchronization problems between the elements of the DAC. The burden of timing accuracy is placed on the control waveform. If the data clock is locked to the control waveform, it will switch at the zero value, zero slope points of the control waveforms of Figure 2-2 (a)-(d). Thus small mismatches in the data clock or control waveform distribution (relative to the period of the control waveform) will have little effect on the output.
- Reduced sensitivity to random jitter in the DAC data clock since the data clock switches when the control waveform is zero valued with zero slope. Performance is sensitive to the phase and amplitude noise of the oscillating control waveform. However, in practice it is easier to build a low phase noise sine wave than a low jitter clock or square wave. Thus improved jitter-limited SNR is expected over conventional square wave RZ and NRZ DACs. This point will be elaborated in Chapter 3.
- Reduced sensitivity to digital signal feed-through via the C_{gd} of the switch transistors. Conventional current steering DACs have solved this problem by using a reduced signal swing at the input to the switch transistors [24]. Reducing the switch transistor input swing, however, reduces the speed of the switching. In the RF DAC implementation, the output voltage is the same value at each switching instant. Thus the charge feed through is a disturbance proportional to the input that causes no distortion. Note that this constant output voltage at the switching instants is also an advantage present in any RZ DAC.
- Potential for reduced upconversion of 1/f noise. References [25] and [26] have shown that switching a MOS transistor between strong inversion and accumulation can reduce 1/f noise power. The best explanation for this effect is that the accumulation phase interferes with the long time constant associated with the 1/f noise trapping and detrapping process, and therefore with the long term memory that characterizes 1/f noise. Reference [26] has shown experimentally an 8dB improvement in upconverted 1/f noise. In a current steering RF DAC implementation, the current source transistor is turned on and off by the control waveform. If the transistor is driven into accumulation during the off state, the upconverted 1/f noise should be reduced, offering higher inband SNR than a conventional DAC.

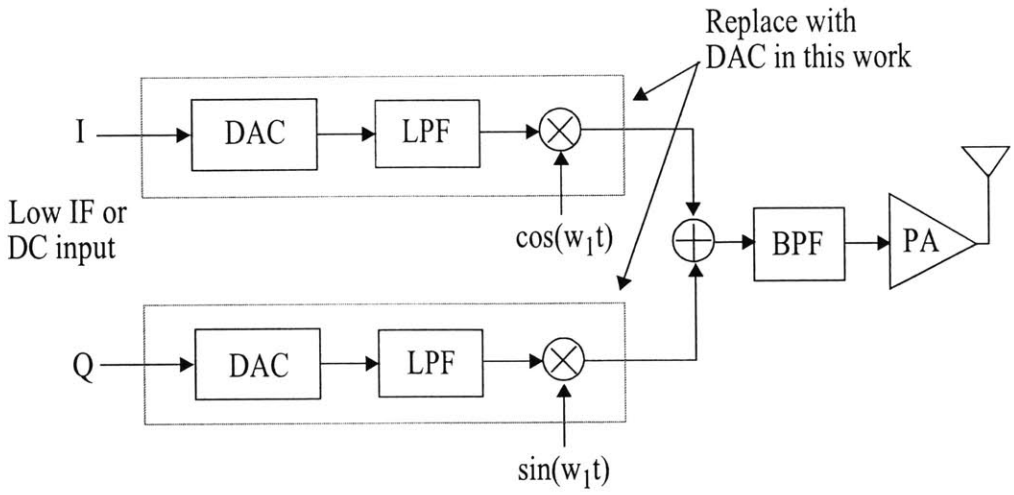

Figure 2-4: Conventional transmitter architecture shown with components that can be replaced by the RF DAC.

2.2.2 RF DAC Disadvantages

One disadvantage of using an image of the DAC output is illustrated in Figure 2-5. If the DAC output waveform has a DC component, the thermal or wideband noise from the primary image gets aliased inband for all of the subsequent images. If this thermal or wideband noise dominates, it could degrade the SNR of the images relative to that of the primary output. Similarly, thermal noise or any other source of noise in the DAC current will mix with the input and potentially alias out-of-band quantization noise back in-band.

Depending on the number of bits and frequencies used in RF DAC, the oscillator may have to drive a large capacitive load with a high-frequency signal. This can require large power consumption, specifically as the number of bits and frequencies increase.

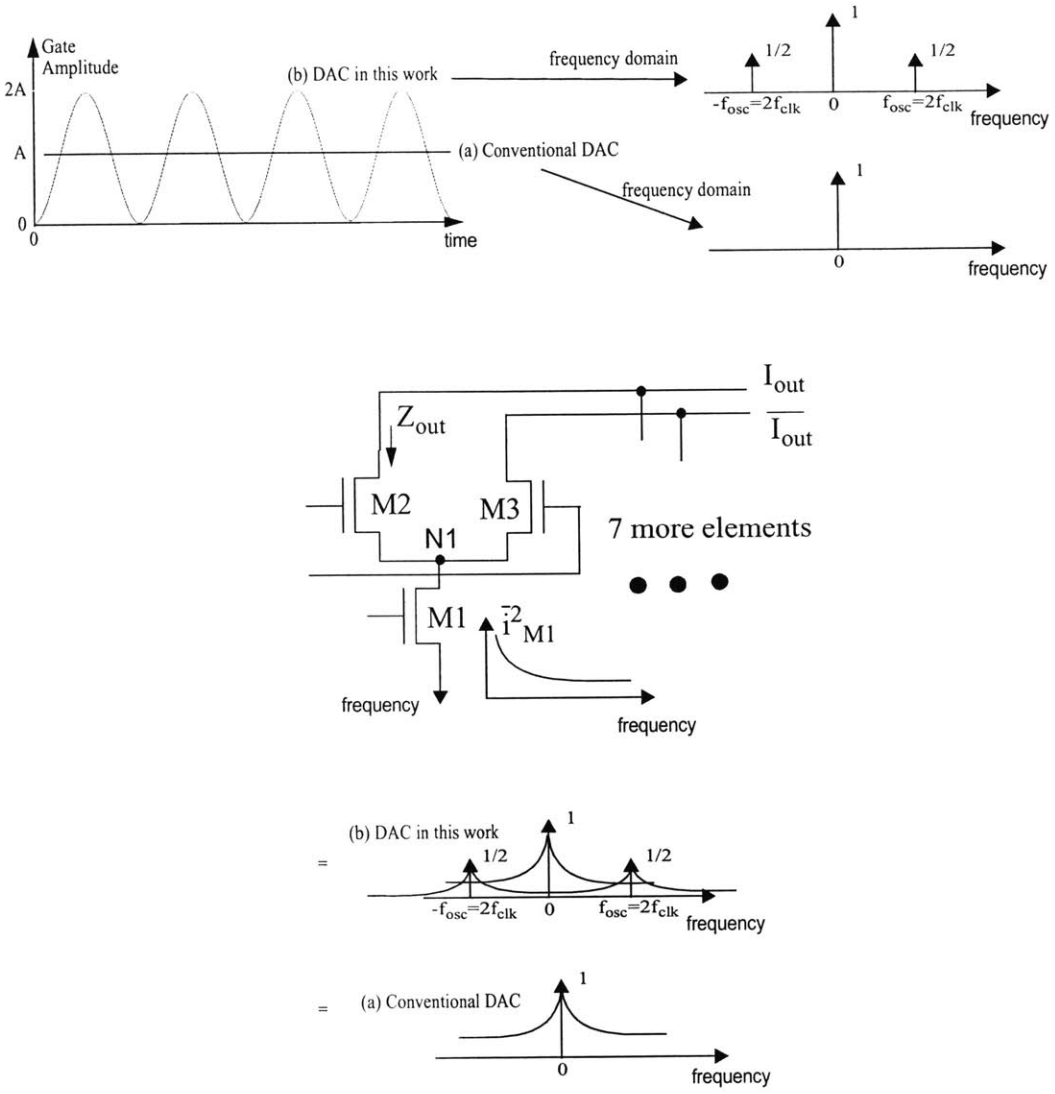

Figure 2-5: Illustration of noise aliasing of the thermal noise from the DC component to high frequencies.

3 Sources of Error in RF DAC

The RF DAC concept presented in the previous section changes the constraint from building a good data clock or DAC switching clock to building a low noise oscillating output waveform (or oscillator) that is accurately locked to a clock. These two waveforms are depicted in Figure 3-1. This chapter will explore the sources of error in the RF DAC system, including locking error, phase and amplitude noise [27]. The phase and amplitude noise will be compared both intuitively and analytically between the square waveform and the oscillating waveform. Since this chapter is relatively mathematical, quick intuitive arguments are first presented to explain the expected results.

Both waveforms in Figure 3-1 will be subject to uncertainties in the amplitude, also called amplitude noise. The amplitude noise of the voltage reference is expected to be the similar in both cases and set by the noise of a bandgap. The amplitude of the oscillating DAC is twice that of the square wave for the same amount of delivered charge. Thus the amplitude noise is expected to be worse in the oscillating waveform than in the square waveform.

A few quick hand-waving arguments can also be made about why the phase noise performance of an oscillating waveform is expected to be better than a square waveform with jitter. First, it is easier to practically build an oscillator with low phase noise than it is to build a clock with low jitter. An oscillating waveform can be filtered with passive components, whereas a square wave has harmonic frequency components that cannot be filtered as easily.

The second argument has to do with how the waveforms are used. In a DAC, the variation in the amount of charge delivered each cycle determines the SNR. Any timing jitter $\tau(t)$ on the switching edges of the square wave pulse of Figure 3-1 affects the amount of charge delivered. The

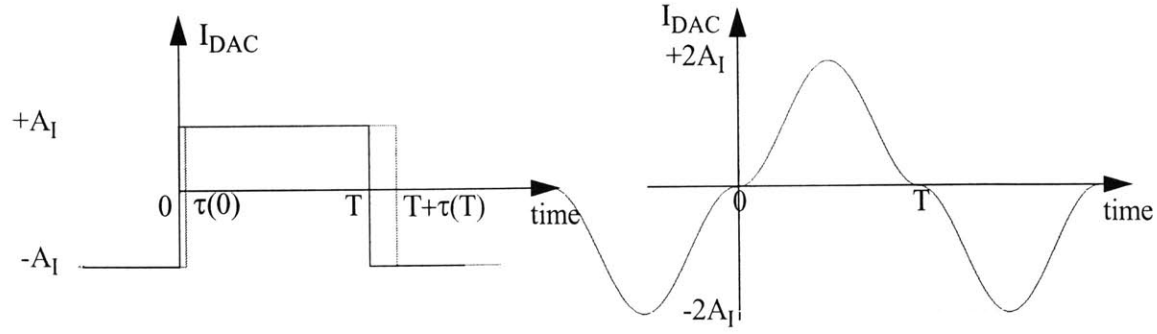

Figure 3-1: Square wave pulse with jitter on the switching edges (left). Oscillating pulse with phase noise not shown (right). Both waveforms will also be subject to amplitude noise.

instantaneous value of the timing jitter at the switching instants is important. However, in an oscillating DAC output waveform with phase noise the instantaneous value of the phase noise is irrelevant, only the integrated noise over a switching period contributes to SNR. This is equivalent to noise averaging or band-limiting the noise. Thus the phase noise performance in the oscillating case is expected to be better than the timing jitter performance of the square wave case. The remainder of this chapter will analyze and compare the sources of error in the DAC output waveforms of Figure 3-1. Ideal locking between the oscillating DAC output waveform and the data clock will be considered first. Then the case of non-ideal locking with jitter on the data clock will be analyzed. Finally phase and amplitude noise in the oscillating waveform will be discussed intuitively and analytically. The chapter will conclude with an example of a numerical comparison.

3.1 Ideal Locking

Suppose the cosine feedback pulse is ideal and perfectly locked to the DAC clock. The only source of error is then jitter in the feedback DAC clock. Integrating I_{DAC} over a period gives the amount of charge fed back in one cycle,

$$q_f = A_I \int_{\tau(t_0)}^{T+\tau(t_T)} (1 - \cos(w_s t))dt \tag{3.1}$$

Where $\tau(t_0)$ and $\tau(t_T)$ are the values of the clock jitter at times 0 and T respectively, and A_I is the amplitude of the cosine feedback pulse. The nominal value of the integral in Equation 3.1 is $A_I T$ when $\tau(t_0)$ and $\tau(t_T)$ are zero. Thus, the error in the fed-back charge of Equation 3.1 is given by

$$E_q = q_f - A_I T \tag{3.2}$$

Using Equation 3.1 and Equation 3.2 with simplification gives

$$E_q \approx \frac{A_I w_s^2}{3!}(\tau(t_T)^3 - \tau(t_0)^3) \tag{3.3}$$

The variance of the error E_q is given by

$$\sigma_e^2 = E[E_q^2] - E^2[E_q] \tag{3.4}$$

For simplification, assume $\tau(t_0)$ and $\tau(t_T)$ are zero-mean Gaussian uncorrelated random variables with variance σ_t^2. This is the same assumption used in Section 1.3 for deriving Equation 1.1. The variance of the error is found from Equation 3.4 and Equation 3.3 with simplification,

$$\sigma_e^2 \approx \frac{5A_I^2 w_s^4 \sigma_t^6}{6} \tag{3.5}$$

The SNR can be computed by approximating the input charge as half the value of the nominal feedback pulse $A_I T/2$. This is the same assumption used in [21], to which this analysis will be compared. This value is chosen to avoid modulator overload since [21] uses the DAC for feedback DAC in a CT ΣΔM.

$$SNR = 20\log\frac{A_I T\sqrt{OSR}}{2\sigma_e} \tag{3.6}$$

Substituting Equation 3.5 into Equation 3.6 and simplifying gives

$$SNR = 20\log\frac{\sqrt{OSR}}{7.3\pi^2 f_s^3 \sigma_t^3} \tag{3.7}$$

This third order jitter sensitivity (σ_t^3) is expected due to the zero value and zero slope of I_{DAC} at the sampling instants $\pm$kT. The SNR limit in Equation 3.7 is compared in Figure 3-2 to the SNR limits in an upfront sampled converter (Equation 3.1.1) and a conventional CT ΣΔM with a single bit, square wave, NRZ DAC pulse as derived in [21]. The standard deviation of the sampling jitter σ_t is assumed to be $0.7ps_{rms}$. The curves are plotted versus the input frequency for an $f_{in}=f_s/4$ bandpass (BP) CT ΣΔM. The input signal bandwidth f_b is 40MHz, but the relative comparison between the curves is the same no matter what f_b is used. It is clear that under ideal locking, jitter in the feedback DAC's clock will not be the limiting source of error in the SNR performance of the RF DAC.

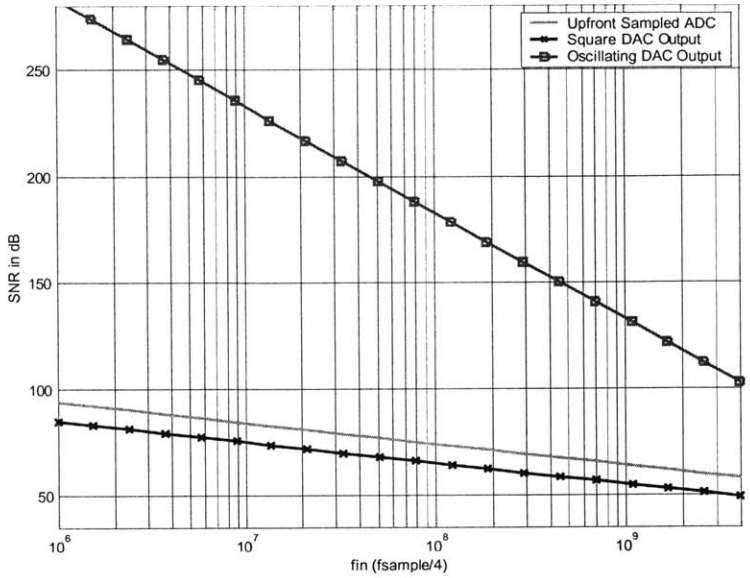

Figure 3-2: Comparison of jitter-limited SNR for an upfront sampled ADC, a DAC with square output pulse, and an oscillating output pulse. A signal bandwidth of 40MHz and sampling jitter standard deviation of $0.7ps_{rms}$ were used.

3.2 Locking Error

A locking error of t_o between the sampling clock edge and I_{DAC} is depicted in Figure 3-3. The feedback waveform is sampled at an offset of t_o from the zero crossings of the I_{DAC} waveform. This creates two sources of error that could degrade SNR. The first is the static offset, or "excess loop delay" in a CT ΣΔM [10]. The second is the data clock jitter acting on the nonzero I_{DAC} waveform.

3.2.1 Static Offset

Static offset between the sampling pulse and the DAC feedback pulse in a CT ΣΔM is the same as the "excess loop delay" discussed in [10]. If t_o is known, the loop can be designed with this delay, and the transfer function adjusted accordingly. If t_o is not known precisely, feedback coefficient tuning can be used to adjust the loop transfer function [10].

3.2.2 Dynamic Offset

Figure 3-2 indicates that clock jitter in the ideally locked case will not limit the SNR. However, if the feedback pulse and the clocking signal are not perfectly aligned as shown in Figure 3-3, the clock jitter will act on a nonzero DAC output with a nonzero slope. Suppose the clock is offset

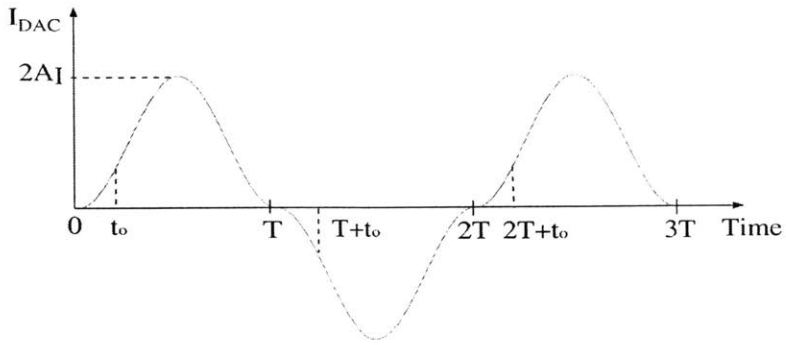

Figure 3-3: Static locking error.

from the feedback pulse by a constant value of t_o as shown in Figure 3-3. The fed-back charge is given by

$$q_f = A_I \int_{t_o+\tau(0)}^{T+t_o+\tau(T)} (1-\cos(w_s t))dt \tag{3.8}$$

Integrating, the error in the fed-back charge is

$$E_q \approx A_I(\tau(T)-\tau(0))(1-\cos(w_s t_o)) \tag{3.9}$$

Assuming that $\tau(0)$ and $\tau(T)$ are zero-mean Gaussian uncorrelated random variables with variance σ_t^2 the variance in the fed-back charge is

$$\sigma_e^2 \approx 2A_I^2\sigma_t^2(1-\cos(w_s t_o))^2 \tag{3.10}$$

Using Equation 3.6 and Equation 3.10,

$$SNR \approx 20\log\frac{\sqrt{OSR}}{2\sqrt{2}\sigma_t(1-\cos(w_s t_o))f_s} \tag{3.11}$$

Simplifying for $w_s t_o \ll 1$ or $t_o \ll T/6$ gives

$$SNR \approx 20\log\frac{\sqrt{OSR}}{56\sigma_t f_s\left(\frac{t_o}{T}\right)^2} \tag{3.12}$$

Given the fixed locking delay t_o and the standard deviation of the clock jitter σ_t, Equation 3.11 can be used to find the jitter imposed SNR limit.

In a conventional CTΣΔM with a square-wave feedback pulse, the jitter acts on a signal of height A_I when the output is switching. In the RF DAC case, the clock jitter acts on I_{DAC} with height $A_I(1-\cos(w_s t_o))$, giving the error in Equation 3.9. Although the output in the square wave pulse system is not always switching, the input to sampling frequency ratio may be low and the output will almost always be switching, especially in a single bit DAC case. Thus the SNR is expected to be better as long as $A_I(1-\cos(w_s t_o)) << A_I$ (i.e. $t_o < T/4$), or as long as the DAC switching does not occur near the peak of the cosine wave.

3.3 Phase and Amplitude Noise in the Oscillating Waveform

Timing jitter in the sampling clock is not the only source of error in the RF DAC. There are also nonidealities in the oscillating waveform itself. These nonidealities are expressed as amplitude and phase noise.

If the cosine pulse has phase noise $\phi(t)$, amplitude noise $A_m(t)$ in the DC level and $A_c(t)$ in the oscillator, the feedback current can be written,

$$I_{DAC} = A_I + A_m(t) - (A_I + A_c(t))\cos(w_s t + \phi(t)) \tag{3.13}$$

The charge transferred over one period can be written as

$$q_f = \int_0^T (A_I + A_m(t) - (A_I + A_c(t))\cos(w_s t + \phi(t)))dt \tag{3.14}$$

The nominal value of this feedback pulse is $\pm A_I T$ when there is no phase or amplitude noise. In the following analysis, the phase and amplitude noise will be analyzed separately. They are assumed to be uncorrelated and the total SNR degradation can be found by computing the sum of the squares of their error variances.

3.3.1 Phase Noise

The fed-back charge q_f with only phase noise in the cosine feedback pulse is given by

$$q_f = \int_0^T (1 - \cos(w_s t + \phi(t)))dt \tag{3.15}$$

The error in q_f due to phase noise is then

$$E_q = A_I \int_0^T -\cos(w_s t + \phi(t))dt \tag{3.16}$$

Expanding the sum and assuming $\phi(t) << \pi/2$ gives

$$E_q \approx -A_I \int_0^T \phi(t)\sin(w_s t)dt \tag{3.17}$$

3.3.1.1 Intuitive Analysis

Suppose there is a phase noise tone at frequency w_τ of amplitude Δ and phase θ given by

$$\phi(t) = \Delta\cos(w_\tau t + \theta) \tag{3.18}$$

Substituting Equation 3.18 into Equation 3.17gives

$$E_q \approx -A_I \int_0^T \Delta\cos(w_\tau t + \theta)\sin(w_s t)dt \tag{3.19}$$

Integrating and simplifying gives (for $w_\tau \neq w_s$)

$$\frac{E_q}{\Delta}(w_\tau) \approx -\frac{A_I w_s}{w_\tau^2 - w_s^2}(\cos(w_\tau t + \theta) - \cos(\theta)) \tag{3.20}$$

and for $w_\tau = w_s$

$$\frac{E_q}{\Delta} \approx -\frac{A_I T}{2}\sin(\theta) \tag{3.21}$$

Plotting the magnitude of the maximum value over θ (i.e. the envelope) of this transfer function as a function of the frequency of the tone ($f_\tau = w_\tau/2\pi$) with $f_s = w_s/2\pi$ gives the phase noise sensitivity curve shown in Figure 3-4. The envelope of the transfer function is scaled by A_I. This curve gives an intuitive feel for the frequencies of noise that cause large error in the delivered charge.

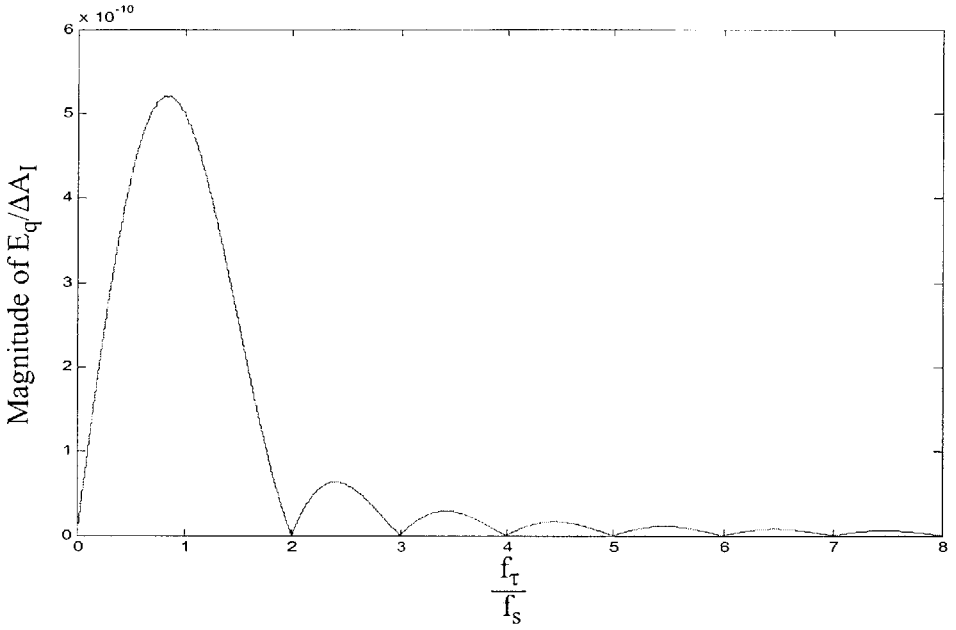

Figure 3-4: Envelope of $E_q/\Delta A_I$ versus f_τ for oscillating DAC waveform.

The curve can easily be multiplied by the measured magnitude Δ of the noise tones at different frequencies when used in a specific system to get the actual sensitivity plot.

It is interesting to note that the envelope is largest at $f_\tau=f_s$, and that $E_q/\Delta A_I$ with $f_s=w_s/2\pi$ approaches 0 as f_τ approaches 0 and as f_τ approaches ∞. $E_q/\Delta A_I$ is most sensitive to phase noise at frequencies near $f_\tau=f_s$. This corresponds to modulated phase noise at offset frequencies $f_\tau=f_s$ away from the carrier, i.e. near DC and $2f_s$. Thus, when designing a DAC with the cosine feedback pulse, it is advantageous to try to null out phase noise at DC and $2f_s$.

For comparison, the same analysis is performed with a conventional NRZ DAC square-wave feedback pulse. The square-wave pulse shown in Figure 3-1 has jitter on the clocked edges defined as τ(0) and τ(T). The charge in the fed-back pulse is given by

$$q_f = A_I \int_0^T (2u(t-\tau(0)) - u(t-T-\tau(T)) - 1)dt \tag{3.22}$$

The noise free value of this pulse is A_IT when τ(0) and τ(T) are both zero. This is the same nominal feedback charge in Equation 3.15. The error in the fed-back charge is

$$E_q = 2A_I(\tau(T)-\tau(0)) \tag{3.23}$$

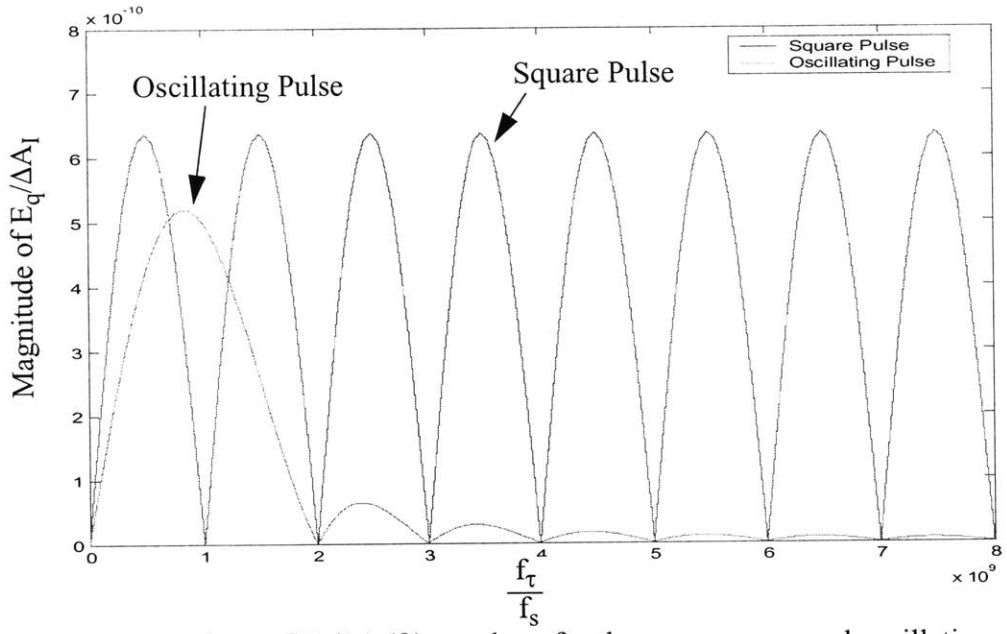

Figure 3-5: Comparison of $E_q/\Delta A_I(f_\tau)$ envelope for the square wave and oscillating wave DAC outputs.

To compare directly with the oscillating pulse, the timing jitter is defined analogously to Equation 3.18,

$$\tau(t) = \frac{\Delta}{w_s}\cos(w_\tau t + \theta) \tag{3.24}$$

This gives

$$\frac{E_q}{\Delta}(w_\tau) = \frac{2A_I}{w_s}(\cos(w_\tau T + \theta) - \cos(\theta)) \tag{3.25}$$

The envelope is compared in Figure 3-5 with the oscillating pulse envelope from Figure 3-4. This plot is also normalized to A_I and plotted versus f_τ.

The envelope of $E_q/\Delta A_I(w_\tau)$ for the square-wave pulse is sensitive to noise at all frequencies except at multiples of f_s. Thus, for broadband noise, the oscillating pulse should have better SNR performance. Additionally, if the noise at offsets of f_s can be nulled, the oscillating pulse has the potential for even better noise tolerance.

3.3.1.2 Analytical Analysis

The preceding analysis gives an intuitive view of which phase noise frequencies will cause large errors in the fed-back charge. It does not, however, give an analytical means of calculating the maximum achievable SNR. An analytical SNR expression is desired so that it can be compared to the SNR of upfront sampled ADCs and CT ΣΔMs with square-wave pulses.

To find the SNR degradation, the variance of the feedback charge error σ_e^2 is needed. From Equation 3.17,

$$\sigma_e^2 \approx E\left[\int_0^T A_I \phi(t)\sin(w_s t)dt \int_0^T A_I \phi(t')\sin(w_s t')dt'\right] \tag{3.26}$$

Simplifying gives

$$\sigma_e^2 \approx A_I^2 \int_0^T\int_0^T R_{\phi\phi}(t-t')\sin(w_s t)\sin(w_s t')dtdt' \tag{3.27}$$

where $R_{\phi\phi}(t\text{-}t')$ is the auto-covariance function of the phase noise. $R_{\phi\phi}(t\text{-}t')$ can be written in the frequency domain as a function of the power spectral density of the noise

$$R_{\phi\phi}(\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_{\phi\phi}(w)e^{jw\tau}dw \tag{3.28}$$

Simplifying gives

$$R_{\phi\phi}(\tau) = \frac{1}{\pi}\int_0^{\infty} S_{\phi\phi}(w)\cos(w\tau)dw \tag{3.29}$$

Once $S_{\phi\phi}(w)$ is known or measured, $R_{\phi\phi}(\tau)$ can be found from Equation 3.29. Then σ_e^2can be found from Equation 3.27 and used in Equation 3.6 to find the exact value of the SNR.

For the sake of comparison, assume $S_{\phi\phi}(w)$ is a constant value of A over the frequency range w_H to w_L and zero elsewhere. The previous analysis indicates that the phase noise at offset frequencies w_S will end up contributing most to the error in the fed-back charge. Indeed for such large offset frequencies from the carrier, a flat thermal noise limit is expected. Using this assumption gives

$$R_{\phi\phi}(\tau) = \frac{A}{\pi\tau}(\sin(w_H\tau) - \sin(w_L\tau)) \tag{3.30}$$

Substituting Equation 3.30 into Equation 3.27,

$$\sigma_e^2 \approx \frac{AA_I^2}{\pi}\int_0^{TT}\int_0 \frac{1}{t-t'}(\sin(w_H(t-t')) - \sin(w_L(t-t')))\sin(w_s t)\sin(w_s t')dtdt' \tag{3.31}$$

Carrying out this integration over a small band of frequencies $w_H \approx w_L \approx w_\tau$ gives the same phase noise sensitivity plot as in Figure 3-4. This corroborates that σ_e is dominated by the phase noise at w_s away from the carrier.

Integrating Equation 3.31 in the limit $w_H \to \infty$ to $w_L \to 0$

$$\lim_{w_H \to \infty,\, w_L \to 0} \int_0^{TT}\int_0 \frac{1}{t-t'}(\sin(w_H(t-t')) - \sin(w_L(t-t')))\sin(w_s t)\sin(w_s t')dtdt' = \frac{\pi T}{2} \tag{3.32}$$

This gives

$$\sigma_e^2 \approx \frac{AA_I^2 T}{2} \tag{3.33}$$

Using Equation 3.6 and OSR=$f_s/2f_b$ with simplification,

$$SNR \approx 20\log\frac{1}{2\sqrt{Af_b}} \tag{3.34}$$

This result indicates that the SNR limit due to phase noise in the pulse is not dependent on f_{in} or f_s. It is only dependent on the amplitude of the phase noise A and the bandwidth of the signal f_b. The only assumption made was that the phase noise spectrum was flat with an amplitude A at frequencies near an offset of w_s away from the carrier.

Figure 3-6 compares the jitter limited SNR in an upfront sampled signal (Equation 1.1), a conventional CT ΣΔM with a square feedback pulse [21], and a CT ΣΔM with the cosine-shaped feedback pulse (Equation 3.34). The SNR is plotted for a $f_{in}=f_s/4$ BP converter with a bandwidth f_b=40MHz. The phase noise amplitude, A, is -150dBm with a 7dBm carrier, and the standard

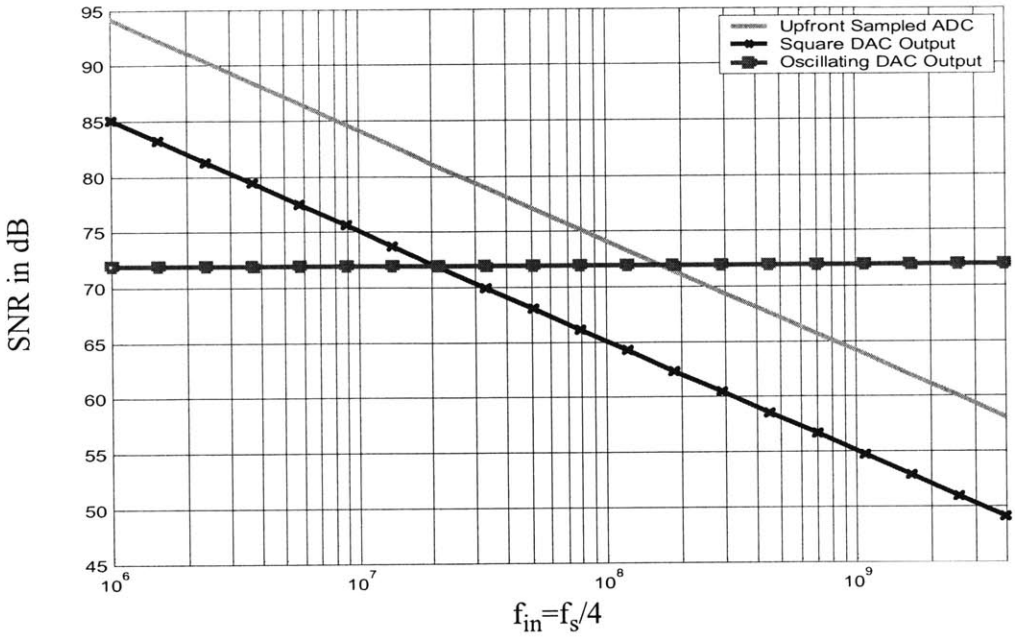

Figure 3-6: Comparison of maximum achievable SNR in an upfront sampled ADC with jitter σ_t =0.7ps$_{rms}$, a square waveform feedback CT ΣΔM with jitter σ_t =0.7ps$_{rms}$, and a DAC with an oscillatory output waveform where the oscillator has phase noise -150dBm. The bandwidth of the input signal is 40MHz for all three curves.

deviation of the jitter is σ_t=0.7ps$_{rms}$. These values were chosen as typical numbers from current state-of-the-art.

Note that, as f_{in} increases, the maximum achievable SNR degrades for the upfront sampled converter and the square-pulse feedback CT ΣΔM, but not for the CT ΣΔM with oscillating pulse. For these typical clock jitter and oscillator phase noise numbers, the oscillating pulse has better performance than the conventional CT ΣΔM above $f_{in} \sim 20MHz$ and better performance than an upfront sampled converter above $f_{in} \sim 200MHz$.

There are a few more potential advantages of the oscillatory feedback CT ΣΔM that are not depicted in Figure 3-6:

- If the DAC is built on a large single chip system, it is likely that the only clock or oscillator available will be noisy with σ_t >>0.7ps$_{rms}$ and large close-in phase noise. As long as the phase noise around DC and $2w_s$ stays at the thermal limit, the curve in Figure 3-6 for the oscillatory

waveform will be almost the same, outperforming the upfront sampled ADC and square waveform.

- If the phase noise around $2w_s$ is notched or nulled, the cosine feedback ΣΔM could also perform better than indicated in Figure 3-6.

- Building an accurate upfront sampled converter which operates at high f_s is very difficult without a large amounts of power [28] and/or an operational amplifier in the converter. Once the opamp is introduced, however, settling time limits the maximum conversion speed [6]. Thus building an upfront sampled converter to meet the SNR curve of Figure 3-6 in the high MHz and GHz regions is very difficult in practice.

3.3.1.3 Amplitude Noise

Amplitude noise in the oscillating waveform also causes variations in the fed-back charge. Expressing the amplitude noise in the mean as $A_m(t)$ and the amplitude noise in the oscillatory pulse as $A_c(t)$, the fed-back charge is

$$q_f = \int_0^T (A_I + A_m(t) - (A_I + A_c(t))\cos w_s t)dt \tag{3.35}$$

For comparison, the error in the fed-back charge due to amplitude noise in the square-wave pulse is given by

$$E_q = \int_0^T A_m(t)dt \tag{3.36}$$

The noise $A_m(t)$ depends on the noise of a voltage source in both DACs. On the other hand, $A_c(t)$ is dependent upon the oscillator. The oscillatory and square-wave pulses are compared in a system with the same voltage source reference quality. In this case, the oscillatory pulse has an additional amplitude noise sensitivity over the square-wave pulse

$$E_q = \int_0^T (A_c(t)\cos w_s t)dt \tag{3.37}$$

To obtain an intuitive analysis, consider the response to a tone at frequency f_τ, $A_c(t)=A\cos(w_\tau t+\theta)$. Substituting into Equation 3.36 and simplifying,

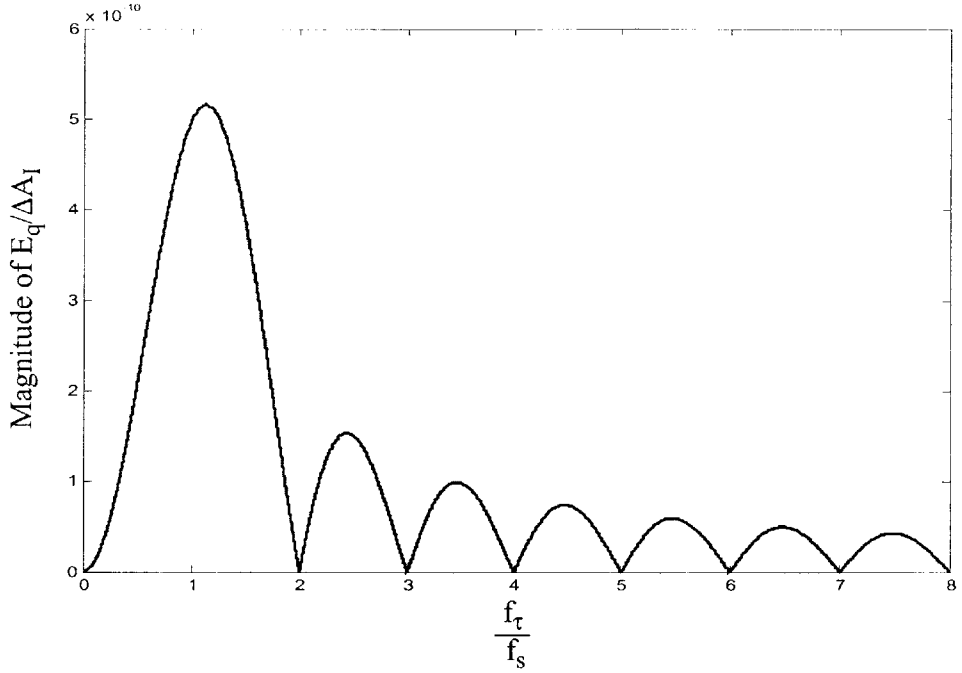

Figure 3-7: Envelope of additional amplitude noise (E_q/A) in the oscillating pulse versus

$$\frac{E_q}{A}(w_\tau) = \frac{w_\tau}{w_\tau^2 - w_s^2}(\sin(w_\tau T + \theta) - \sin(\theta)) \tag{3.38}$$

for $w_\tau \neq w_s$ and

$$\frac{E_q}{A} = \frac{T}{2}\cos(\theta) \tag{3.39}$$

for $w_\tau = w_s$.

This extra amplitude noise error in the cosine pulse is plotted in Figure 3-7. The error in the fed-back charge is again most sensitive to amplitude noise at a frequency of f_s away from the carrier. If the amplitude noise is small or nulled at these large offset frequencies, then the amplitude noise sensitivity will approach the same performance as the square-wave pulse.

Using Equation 3.37 to calculate the exact additional variance of the fed-back charge due to amplitude noise,

$$\sigma_e^2 = E\left[\int_0^T\int_0^T A_c(t)A_c(t')\cos(w_s t)\cos(w_s t')dtdt'\right] \tag{3.40}$$

$$\sigma_e^2 = E\left[\int_0^T\int_0^T R_{AA}(t-t')\cos(w_s t)\cos(w_s t')dtdt'\right] \tag{3.41}$$

$R_{AA}(t\text{-}t')$ can be found from Equation 3.28, given the power spectrum of the amplitude noise. This can be substituted into Equation 3.41 to find the exact value of σ_e^2. If the amplitude noise is assumed to be flat over the sensitive frequencies around DC and $2w_s$, the calculations fall out exactly as in the phase noise case and Equation 3.34 gives the additional SNR limit due to amplitude noise in the oscillator. The curve in Figure 3-6 is then also the maximum achievable SNR for an oscillatory pulse with -150dBm of amplitude noise near frequencies w_s away from the carrier, assuming no noise in the mean of the fed-back pulse. There will be additional degradation due to variations in the mean, but they are the same as in the square-wave pulse and are expected to be small in a system with a good bandgap reference. If the oscillatory pulse has phase and amplitude noise, the total noise variance can be found as the sum of the two variances in Equation 3.41 and Equation 3.33.

3.4 Multiple pulses per sampling period

Figure 3-3 assumes that the oscillator frequency is the same as the sampling clock frequency. Suppose instead that the cosine pulse frequency is n times the sampling frequency. An example feedback waveform is shown in Figure 3-8 for the case n=4 with four oscillator periods per sampling period.

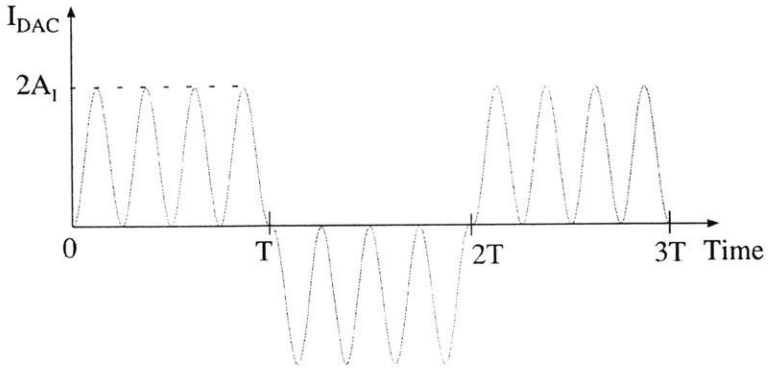

Figure 3-8: Four pulses per sampling period.

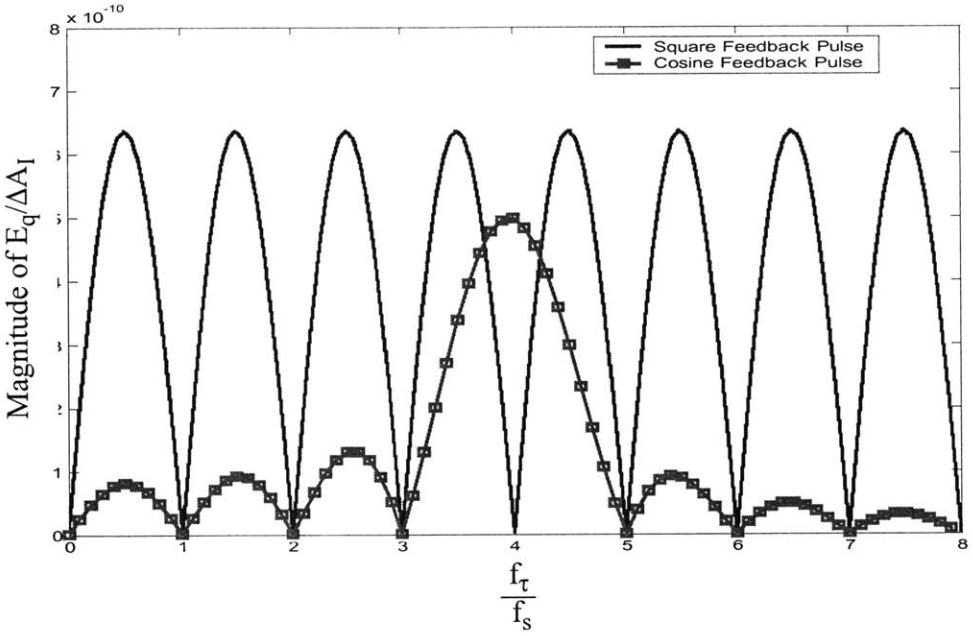

Figure 3-9: Envelope of $E_q/\Delta A_I(f_\tau)$ with four oscillatory pulses per sampling period.

This DAC is much more sensitive to locking errors than a DAC with only one pulse per sampling period, since smaller values of locking error t_o can cause the clock edges to land in the middle of the cosine pulse, giving the same or worse sensitivity to clock jitter than the square wave pulse. However, amplitude and phase noise sensitivity are expected to improve due to averaging. A new error envelope for the phase noise is plotted in Figure 3-9. The error in the delivered charge is now most sensitive to noise at offset frequencies $n*w_s$ away from the sampling frequency. Thus a DAC with oscillatory output $n>1$ offers a trade-off between locking error and phase and amplitude noise sensitivity. The chosen value of n will likely depend on the accuracy of the locking scheme that can be built.

4 Prototype Design

The RF DAC concept could be used in many applications, including a direct transmit or low-IF DAC for communications systems, a direct digital synthesis (DDS) DAC, or a feedback DAC in a CT ΣΔM. The prototype implemented to demonstrate the RF DAC concept needed to be flexible in order to demonstrate, compare and fully test the concept. Specifically, the prototype needed the ability to test different ratios of oscillating and sampling frequency, compare square waves to oscillatory waves, adjust the phase between the sampling clock and oscillatory wave, handle a wide range of communications input vectors, and demonstrate high speed operation for communications applications. This section begins by discussing the specifications and architectural trade-offs in implementing a prototype to meet all of these needs. The circuit design and layout is then discussed, focusing on the design trade-offs in implementing RF DAC that are different from those encountered when implementing a conventional DAC.

4.1 System specifications

Since wireless communications is pushing the development of high speed, high resolution converters, it seemed appropriate to pick a challenging wireless transmit specification to demonstrate the RF DAC concept. Table 4-1 lists a few of the current wireless transmission standards.

Table 4-1: State-of-the-art wireless standards

System Generation	Wireless System	Base-station TX Frequency (MHz)	Base-station RX Frequency (MHz)	Channel Bandwidth
2G	GSM 850 (MXM)	869-894	824-849	200kHz
2G	GSM 900	925-960	880-915	200kHz
2.5G	EDGE (Europe)	925-960	880-915	200kHz
2G	GSM 1800 (DCS)	1805-1880	1710-1785	200kHz

The GSM 900/EDGE system was chosen as the target design specification due to its modern day wide deployment in the industry. However, RF DAC could just as easily be applied to any of the systems in Table 4-1.

The target specifications for a TX DAC in the GSM 900 system are shown in Table 4-2. A 17.5MHz bandwidth target is chosen as half the 35MHz total GSM band. Often this band is split among one or more suppliers, making a converter that operates on only half the band potentially desirable to industry. The SNR specification for a 17.5MHz band is calculated from GSM transmit masks found in reference [29]. These masks indicate that a -80dBc noise level is needed at 6MHz away from the signal over a 100kHz band. This requires -130dBc/Hz, which over a 17.5MHz band gives 57.5 dB. Note that these are the levels needed at the transmit antenna. Extra noise will be added from the filter and power amplifier still needed in the transmit signal path before the antenna. SFDR should also be greater than 80dBc. Since the bandwidth is so narrow, the only spur expected to fall inband is the third order intermodulation product (IMD3). For lower frequency communications DACs which require mixing and filtering stages after the DAC, other spurs could mix inband through the nonlinearities of these later stages. However, since the RF DAC concept eliminates the need for the extra mixers, the SFDR requirements can be relaxed to be closer to those actually needed at the antenna. The full scale output current of the DAC should be maximized, since power amplifiers are only ~20-40% efficient [39]. A large output amplitude can also increase the SNR by ensuring that the output is above the other sources of noise in the system. Pouring extra output power into the DAC doesn't make much sense unless the DAC is more efficient than the power amplifier. For reference, state-of-the-art low-IF DACs typically used in transmit applications have 10-20mA full scale output currents.

Table 4-2: RF DAC Target Design Specifications

Parameter	**Value**
1/2 GSM 900 and EDGE System Band	933.75-951.25 MHz (17.5MHz Bandwidth)
SNR	> 60dB
Inband SFDR (IMD3)	> 80dBc
Full Scale Output	maximum, > 20 mA (13dBm with 50Ω, 10dBm with 25Ω, 10-30dBm output power typically required in transmit applications)

4.2 RF DAC Architecture

4.2.1 ΣΔ DACs and Mismatch Shaping

Nyquist rate DACs have an input and output bandwidth of half the clock rate. The number of bits in the DAC sets the output quantization noise floor. High resolution typically requires trimming in a Nyquist rate DAC [30]. In contrast, ΣΔ DACs rely on oversampling to reduce the quantization noise in a narrow band of interest, thereby reducing the number of elements needed in a ΣΔ DAC. Mismatch shaping offers the additional benefit of reducing the accuracy required in the DAC unit elements. A ΣΔ DAC trades digital complexity and oversampling for reduced sensitivity to analog accuracy.

Figure 4-1 shows the input data path for a ΣΔ DAC. The narrowband digital input data is shaped by a quantization noise shaper, typically a digital ΣΔ ADC. A wealth of details about ΣΔ ADCs, modulation, and quantization noise shaping can be found in [31]. Once the data is quantization noise shaped, mismatch shaping is employed to decide which elements of the DAC should be used to implement each input code. Mismatch shaping algorithms seek to mimic transfer functions that place zeros in the band of interest, thereby nulling the inband mismatch noise [32] [33]. Although theoretically any order mismatch transfer function centered around any band of interest is possible [32], there are trade-offs in complexity and cost of implementing different mismatch shaping transfer functions [33].

The N-Path filter approach to bandpass mismatch shaping is an efficient method that can be implemented in modern digital technology. An example is shown in Figure 4-2. The desired transfer function shown in Figure 4-2 (a) is $H(z)=1+z^{-2}$. This transfer function has a zero which will reduce the noise in a band near $f_s/4$. Figure 4-2 (b) shows an alternative implementation of H(z). This shows that two first order interleaved filters $H'(z)=1+z^{-1}$ can be used to implement H(z). Figure 4-2 (c) shows the algorithm used to mimic H(z) in selecting the unit elements of an 8-element DAC that are used to implement each input code. The dark arrows and light arrows rep-

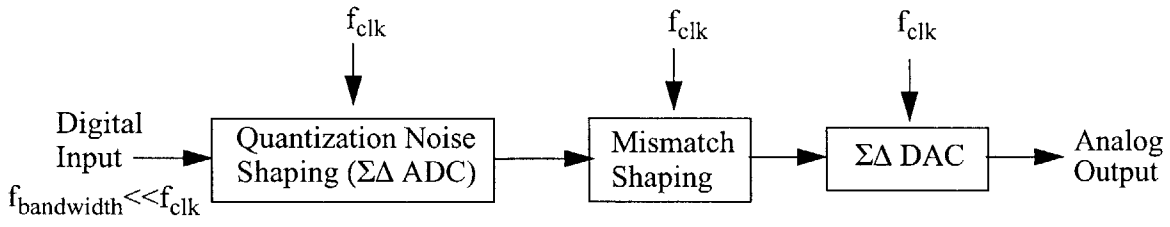

Figure 4-1: Data path for a ΣΔ DAC.

resent the two filters. The input data is alternated between the two filters. Each filter rotates back and forth through the most recently used elements. The reason for reusing the most recently used elements is that the impulse response of H(z) is {1,0,1}, indicating that the errors made selecting the elements in the previous step need to be repeated.

Reference [33] recognizes that mismatch shaping increases the data switching activity. Each element in the process of switching introduces noise and distortion. Modified mismatch shaping is introduced in an attempt to keep the number of elements switching constant. This reduces the switching distortion to a DC offset. The 'modified mismatch shaping' algorithm described in [33] offers a trade-off between mismatch shaping performance and switching noise performance.

An example MATLAB simulation of an 8-element ΣΔ DAC with a band centered around $f_s/4$ is shown in Figure 4-3. The MATLAB simulation was performed using the Sigma-Delta Toolbox [34] [35]. The ideal spectrum has an SNR of 79dB. If implemented with elements matched to 1%, the SNR degrades to 65dB. Mismatch shaping as described in Figure 4-2 in the $f_s/4$ band improves the SNR by 12dB to 77dB. Modified mismatch shaping improves the inband SNR by only 4.6dB to 69.6dB, but offers a near constant 3 elements switching per clock cycle. The simulation of Figure 4-2 only models 1% element mismatches, so no SNR improvements due to reduction in switching-induced noise can be seen.

Table 4-3 shows the mean and standard deviation of the number of elements switching for various input vectors. These values are simulated using Matlab and are the actual numbers for the test vectors. As expected, the modified mismatch shaping algorithm has the lowest standard deviation of the number of elements switching.

Table 4-3: Switching statistics for various input vectors.

Input vector	Meaning	Mean number of elements switching (out of 8)	Standard deviation of number of elements switching
'Normal' input vector	sigma-delta quantization noise shaping, but NO mismatch shaping	1.9827	1.1429
Mismatch shaping	quantization noise shaping, standard mismatch shaping	3.2658	1.3645
Modified mismatch shaping	quantization noise shaping, mismatch shaping with a 'modified' algorithm that attempts to keep the number of elements switching a constant	2.655	0.68

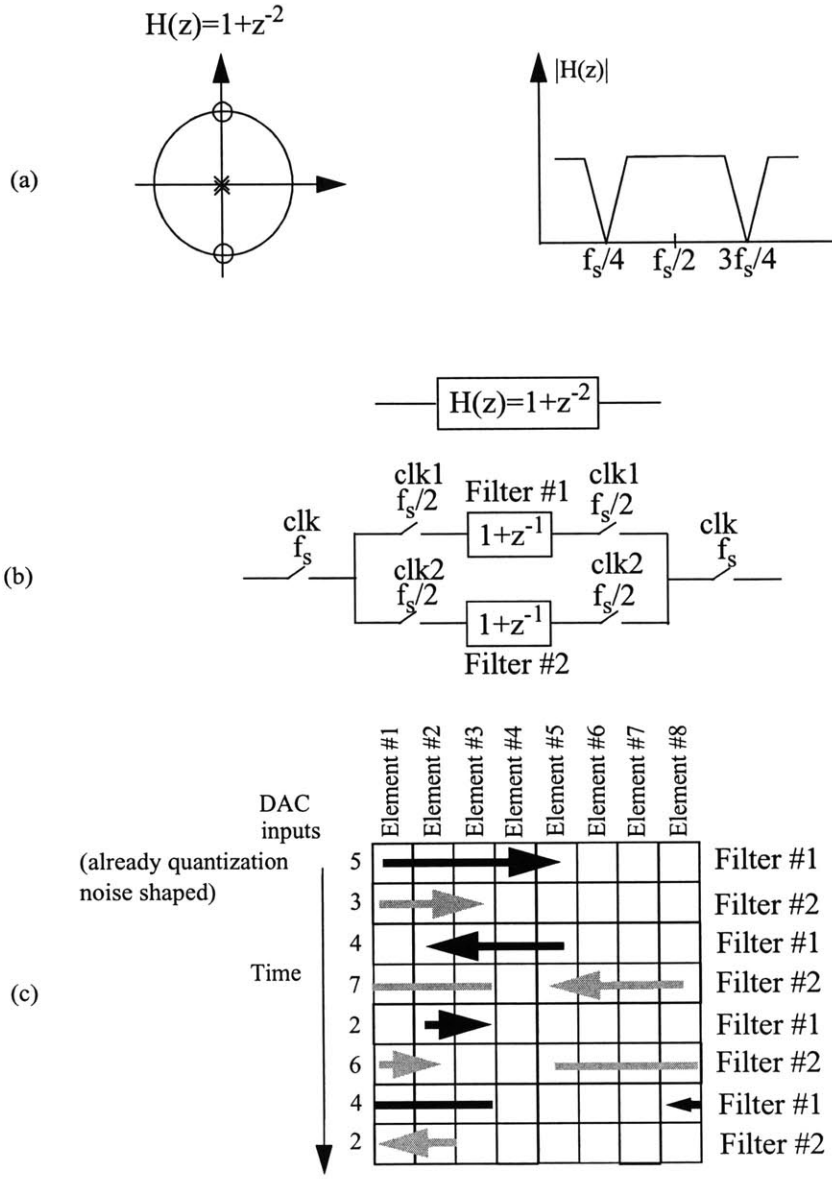

Figure 4-2: Mismatch shaping in ΣΔ DACs (a) Desired mismatch shaping transfer function with zeros at fs/4. (b) Two-path filter implementation of H(z). (c) Example of element rotation to implement H(z) as in (b).

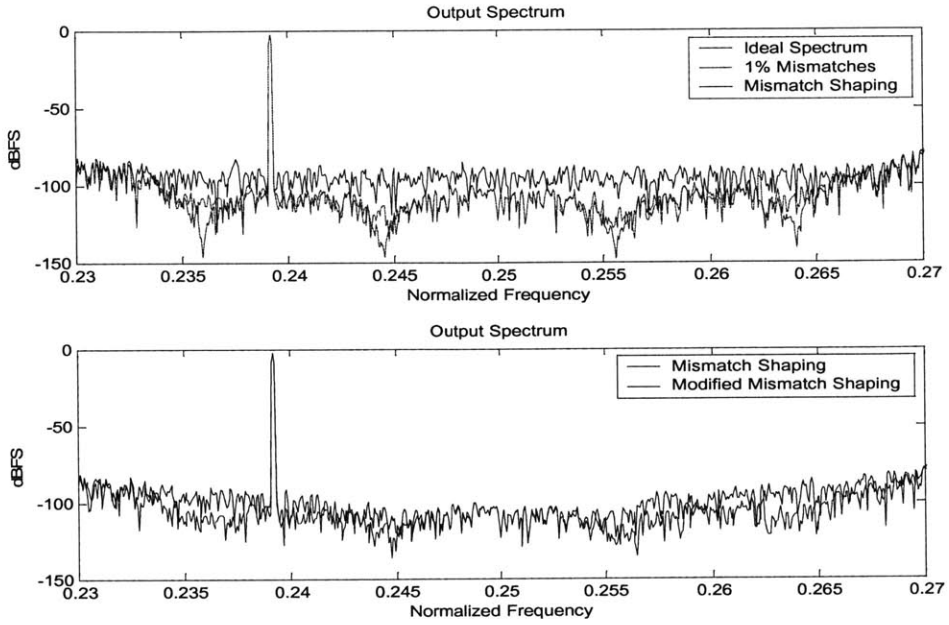

Figure 4-3: Example of mismatch shaping for a band centered at fs/4. The ideal spectrum has an inband SNR of 79dB. The spectrum with a 1% mismatch in the elements has an SNR 65.4dB. The spectrum with mismatch shaping has an SNR 77.5dB.

4.2.2 Nyquist vs. ΣΔ DAC

The RF DAC concept could be applied to both Nyquist rate and ΣΔ DACs. However, communication transmit applications require SNR and SFDR performance only in a narrow signal band. Out-of-band distortion is filtered by the BPF shown in Figure 1-1. Although ΣΔ DACs are currently not deployed or heavily researched for high speed applications, there are several good reasons why they are good candidates. This chapter is devoted to clarifying the advantages of ΣΔ DACs at high frequencies.

High frequency, high accuracy DACs are typically CMOS current steering architectures because they are fast and cost effective [36] [24] [37]. Unit current sources are used for the MSBs to achieve good static and dynamic performance. The static performance of these DACs is limited by the matching of the current source transistors in these unit elements. For instance, to achieve half of a least significant bit (LSB) accuracy at 10 bits requires a device with an area of about $300\mu m^2$. These large current source devices consume a lot of die area and require careful layout techniques to ensure good matching.

Using a ΣΔ DAC with mismatch shaping alleviates the matching constraint. If mismatch shaping is employed, inband resolution can exceed device matching. Thus smaller current source devices can be used to achieve the same inband resolution. Furthermore, there can be fewer elements in the DAC since quantization noise is also shaped out-of-band. This allows ΣΔ DACs to be built with reduced area.

Large current source devices needed in a Nyquist rate DAC also have a large gate to source capacitance C_{gs}. If the high frequency oscillating control waveform needed for the RF DAC controls these gates directly, their combined C_{gs}'s will require a lot of power to drive. Smaller, fewer current sources achievable in ΣΔ DACs have reduced input capacitance and require lower power to drive.

In addition to current source transistor matching, ΣΔ DACs also shape static timing offset mismatches between the elements of the DAC. Although previous work [36] [24] [37] solves this problem in Nyquist rate DACs by careful layout, this may become intractable as speeds increase. Mismatch shaping can ensure that this source of distortion does not dominate.

Since mismatch shaping allows smaller current sources, these current sources have a lower capacitance at their drains. This drain capacitance can dominate the output impedance of the current source at high frequencies. Reduced drain capacitance improves the output impedance of the current source. This improved output impedance allows the elimination of the impedance-boosting cascode transistor found in conventional Nyquist-rate DACs. This will be discussed further in Section 4.3. The elimination of this transistor allows increased headroom so the DAC can be implemented with a reduced supply voltage.

Since the use of ΣΔ DACs for high frequency transmit applications is a relatively new concept, the advantages over a Nyquist architecture are summarized below.

- The same inband noise can be achieved with lower area due to mismatch shaping.
- ΣΔ mismatch shaping also shapes static timing differences and offsets in the unit elements. This allows higher SNR and SFDR performance.
- Smaller devices mean smaller drain capacitance, giving larger output impedance at high frequencies. Elimination of the output impedance boosting cascode transistor allows DACs to be built with low supply voltages in aggressive technologies. It also gives associated power and area reduction since the cascode and its bias circuitry are eliminated.

- Smaller drive capacitance for the oscillating control waveform (advantage applies to RF DAC implementation only).

The primary disadvantage of using a ΣΔ architecture is that the out-of-band quantization noise needs to be filtered. Transmit communications applications require a filter before the power amplifier anyway. The filter may have to be narrower than previously required, or extra bits added to the DAC to widen the bandwidth and relax constraints on the filter. Thus there is a trade-off between the filter roll-off and bandwidth of the ΣΔ DAC.

4.2.3 Frequency Planning

There are some interesting trade-offs in choosing the input, sampling, and oscillating control waveform frequencies. The system is intended for the GSM 900/EDGE specification as given in Table 4-2. Setting the band center at 942.5MHz gives a constraint on the relation between the control waveform frequency f_{osc} and the input frequency f_{in}:

$$f_{osc} - f_{in} = 942.5MHz \tag{4.5}$$

The sampling frequency f_s is another design parameter. A large oversampling ratio (OSR=f_s/ $2f_b$=f_s/35MHz) increases the SNR that can be achieved in a ΣΔ implementation. Thus f_s=f_{osc}/2 was chosen to maximize the OSR. Mismatch shaping in a ΣΔ DAC is easier to practically implement and more effective if the additional following constraint is met [32] [33]:

$$f_{in} = \frac{af_s}{b} \tag{4.6}$$

where a and b are integers.

Figure 4-4 shows the RF DAC input and output frequency spectrums as a function of f_s, f_{in} and f_{osc} for m = 4, 8. Large f_{in} is desirable so that the signal band is far away from any control waveform feed through at frequency f_{osc}. However, the larger f_{in}, the faster the operating speed of the front end digital hardware operating speed.

Table 4-4 summarizes solutions to Equation 4.5 and Equation 4.6 with f_s=f_{osc}/2. The final target frequencies were chosen with f_{in}=f_s/4 to give an extra 3dB mismatch shaping over the f_s/8 case and a slightly larger OSR (15.4 versus 14.4). Since the input and oscillatory control waveforms are implemented off-chip, the f_{in}=f_s/8 case as well as many other cases can be easily implemented, tested and compared.

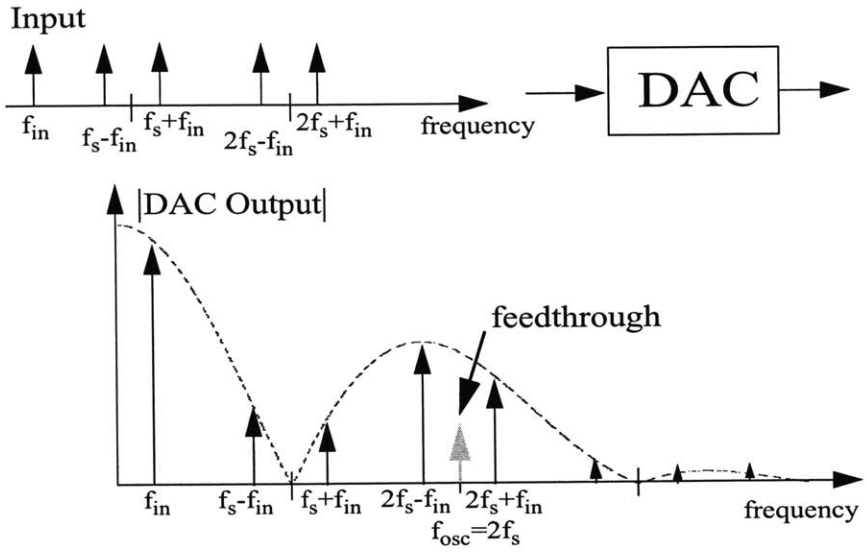

Figure 4-4: Output spectrum of DAC illustrating frequency planning issues.

Table 4-4: Possible DAC input, update, and control frequencies.

Parameter	**Possible values**
$f_{in}=f_s/4$ ($f_{in}=f_s/8$)	134 MHz (62.8 MHz)
f_s = DAC Update Rate	538.57 MHz (502.6 MHz)
f_{osc} = Oscillator Frequency = $f_s/2$	1.077 GHz (1.005 GHz)

4.2.4 ΣΔ Design Space

ΣΔ DAC achievable performance with the frequencies chosen above is shown in Table 4-5. These numbers were obtained by simulating a ΣΔ ADC with an *nlev*-level quantizer in Matlab. The *nlev*-output of the ADC is the input of the *nlev*-DAC, and the maximum SNR at the output of the ADC is the maximum SNR of the DAC. Worst case mismatches were implemented on the ADC output values to simulate mismatches in the DAC unit elements. The SNR numbers in Table 4-5 are shown with 1% and 5% mismatch. The numbers in parentheses are without mismatch shaping; the numbers with parentheses have mismatch shaping. Although mismatch shaping is implemented in Matlab, since $f_{in}=f_s/4$ it could easily be implemented on-chip in the future.

Table 4-5: ΣΔ DAC Design Space

Number of DAC levels nlev	Loop Order	Out of Band Gain	Max. stable input amplitude in dBFS	SNR with 1% mismatch (no shaping) in dB	SNR with 5%mismatch (no shaping) in dB
9	6	2	-1	(61) 64	(50) 58
9	6	4	-2	(61) 71	(46) 58
9	8	2	-3	(60) 69	(46) 59
9	8	4	-3	(60) 72	(46) 58
13	6	2	-1	(64) 66	(51) 59
13	8	2	-1	(65) 74	(52) 63

The maximum stable amplitude input amplitude (MSA) is a measure of the stability of the ΣΔ loop for a given loop order and out-of-band gain. The higher the loop order and out-of-band gain, the larger the in-band SNR, but the loop becomes less stable and the MSA is lowered. A low MSA means that the entire full scale of the DAC cannot be utilized. Table 4-5 shows the trade-off between SNR and the maximum stable input amplitude.

There is another trade-off not depicted in Table 4-5. The more levels or elements in the DAC, the larger the area and the more power required in the oscillator to drive the DAC. It is also desirable to have the number of DAC elements be a power of two so that the oscillatory control waveform can be delivered to the DAC in a tree to reduce timing offsets between the elements.

The number of DAC levels *nlev* is the critical design parameter, since it determines how many unit elements are put on the chip. In the final design, *nlev*=9 (i.e. 8 unit DAC elements) were chosen to give >60dB SNR with 1% device mismatch. Since the ΣΔ modulator and mismatch shaping will be off-chip, any of the 9-level systems shown in Table 4-5 can be studied.

4.2.5 System Block Diagram

Figure 4-5 shows the RF DAC testchip system design. The ΣΔ modulated data is generated on a computer by simulating a ΣΔ ADC in Matlab. Mismatch shaping and serial-to-parallel conversion are then performed in Matlab on the output of the ΣΔ ADC, and the results are fed to the DG2020 pattern generator. The DG2020 has 36 outputs that can operate at a maximum output rate of 200MHz. The eight data lines are parallelized to 32 signals at 134.6MHz. An on chip mux serial-

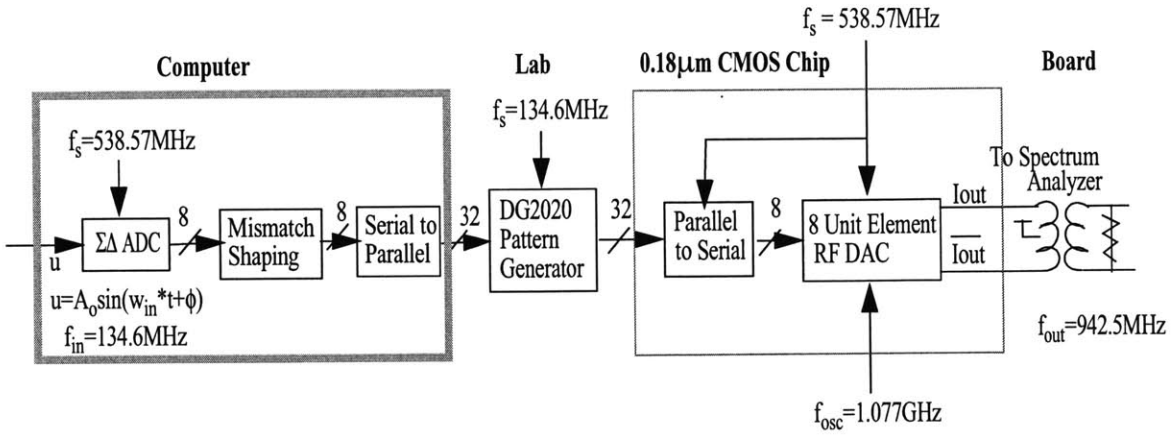

Figure 4-5: RF DAC system block diagram.

izes the data for the unit element DAC. The current output of the DAC is fed through resistors and a transformer on the test board to a spectrum analyzer.

The clocks for the system, f_s and f_o are generated from HP8644A and Rhode & Schwartz SML01 signal generators. This allows the frequencies and relative phases to be easily adjusted. Furthermore, the bias point of f_o can be adjusted to compare the noise performance when driving the current source transistors into accumulation. Thus the 1/f noise reduction theory described in Section 2.2 can be tested.

4.3 Output Impedance for DACs

Since communications applications are replacing static measures of performance such as INL and DNL with frequency-domain specifications like SNR and SFDR, it is important to re-evaluate DAC design constraints. One particular area for improvement is the specification of DAC output impedance. Previous work has shown that a minimum output impedance is required for given single-ended (SE) INL [38] and single-ended second harmonic distortion (HD2) [40] performance. SNDR and SFDR for single-ended binary DACs have been derived in [17]. This section extends that analysis to compare output impedance specifications for INL, DNL, second harmonic distortion, and IMD3 in both SE and fully-differential (FD) implementations. It is shown that the output impedance specifications are significantly reduced when a fully-differential implementation is used [41].

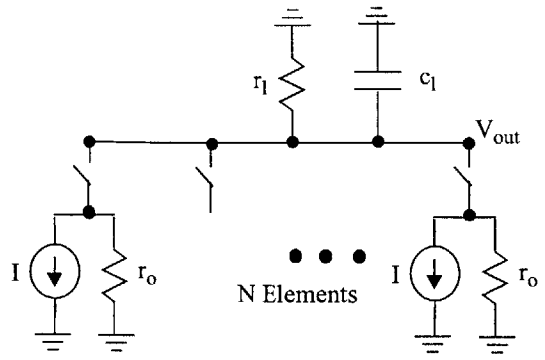

Figure 4-6: Single-ended DAC model with load resistor r_l and unit element output impedance r_o.

4.3.1 Static Performance Specifications

There is a minimum DAC output impedance that is required to meet static INL and DNL specifications. These limits can be derived by considering the simple DAC model in Figure 4-6. Each element of the N-element DAC has a current I and an output impedance r_o. Output impedance is modeled resistively since it is typically dominated by output resistance of the switch transistor, the current source transistor, or a cascode transistor. Ideally, the output current is terminated through r_l to produce a voltage V_{out}. The capacitance c_l models the output capacitance due to pads or large output traces. Although often significant, c_l does not effect static measures of performance or cause harmonic distortion. In the model of Figure 4-6, the output voltage is

$$V_{out}(k) = \frac{kI}{g_l + g_o k} \tag{4.7}$$

where k is the number of elements turned on. To find the single-ended DNL, the width of each code is:

$$V_{out}(k) - V_{out}(k-1) = \frac{kI}{g_l + g_o k} - \frac{(k-1)I}{g_l + g_o(k-1)} \tag{4.8}$$

The nominal code width or least significant bit (LSB) is $\frac{I}{g_l + Ng_o}$. The DNL expressed in LSBs is

$$DNL_{SE}(k) = \frac{V_{out}(k) - V_{out}(k-1)}{\frac{I}{g_l + Ng_o}} - 1 \tag{4.9}$$

Substituting and simplifying gives

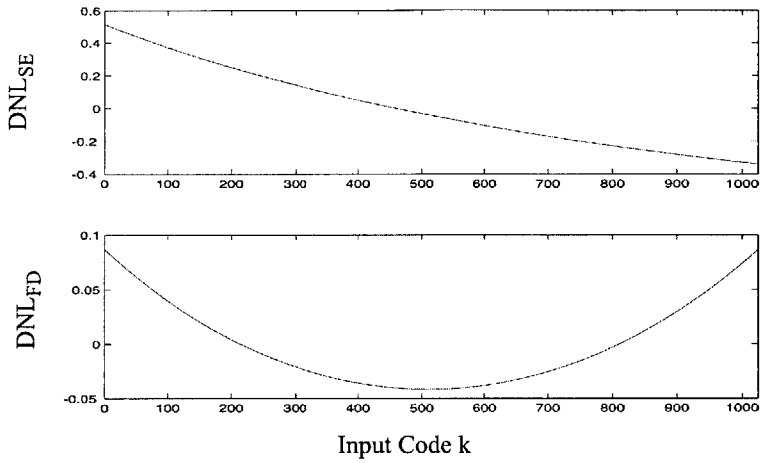

Figure 4-7: DNL caused by finite output impedance for single-ended and fully-differential DACs. In this example, r_o=100 kOhms, r_l=50 Ohms, and N=2^{10}=1024.

$$DNL_{SE}(k) = \frac{g_o g_l(N-2k+1) - g_o^2(k^2-k)}{g_l^2 + 2g_o g_l k - g_o g_l + (k^2-k)g_o^2} \tag{4.10}$$

$DNL_{SE}(k)$ is plotted at the top of Figure 4-7. The minimum unit element output impedance needed to achieve a maximum 1/2 LSB DNL can be found by solving for $r_o=1/g_o$ in Equation 4.10. The total output impedance $r_t=r_o/N$ is plotted in Figure 4-9. The load resistor $r_l=1/g_l$ is assumed to be 50 Ohms. The number of elements N is assumed to be 2^b, where b is plotted on the x-axis of Figure 4-9. As the number of elements grows, a higher output impedance per element is required.

The fully-differential DNL can be derived similarly to the above single-ended analysis. The fully-differential DNL is plotted in Figure 4-7 versus the input code k. Output impedance requirements for fully-differential DNL are also plotted in Figure 4-9. The output impedance is a factor of two lower than that required for single-ended DNL.

The single-ended INL requirement is derived in [38]

$$INL_{SE}(k) = \frac{Ir_l^2 k(k-N)}{r_o} \tag{4.11}$$

The single-ended INL of Equation 4.11 is plotted at the top of Figure 4-8 versus input code k. The INL is even with a maximum at k=N/2. The minimum total output impedance required to give a 1/2 LSB INL is plotted in Figure 4-9.

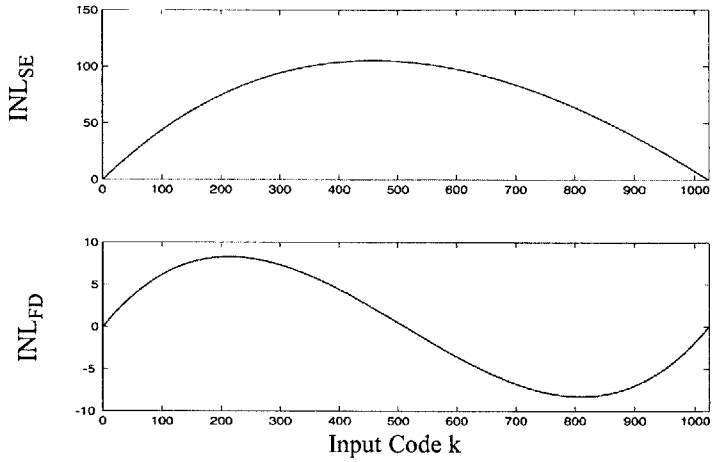

Figure 4-8: INL caused by finite output impedance for single-ended and fully-differential DACs. In this example, r_0=100 kOhms, r_l=50 Ohms, and N=2^{10}=1024.

The INL for a fully-differential DAC is found by considering a fully-differential output

$$V_{outdiff} = \frac{kI}{g_l + g_o k} - \frac{(N-k)I}{g_l + g_o(N-k)} \tag{4.12}$$

where N is the total number of unit elements in the DAC and k is the number of elements turned on. Finding the endpoints of Equation 4.12 and writing the equation for this straight line gives

$$V_{line} = \frac{I(2k-N)}{g_l + g_o k} \tag{4.13}$$

The INL can be found by

$$V_{INL} = V_{outdiff} - V_{line} \tag{4.14}$$

Expanding Equation 4.14 and normalizing to an LSB gives

$$INL_{FD}(k) = \frac{-g_l g_o^2 k(2k-N)(N-k)}{2(g_l^2 + g_l g_o N + g_o^2 kN - g_o^2 k)(g_l + Ng_o)} \tag{4.15}$$

The INL of Equation 4.15 is plotted in Figure 4-8. The INL is odd in the fully-differential case and has extrema at k=N/4 and k=3N/4.

Equation 4.15 can also be solved for the minimum impedance r_0 required to give 1/2 LSB INL performance. The minimum total output impedance r_t=r_0/N is plotted in Figure 4-9. Figure 4-9

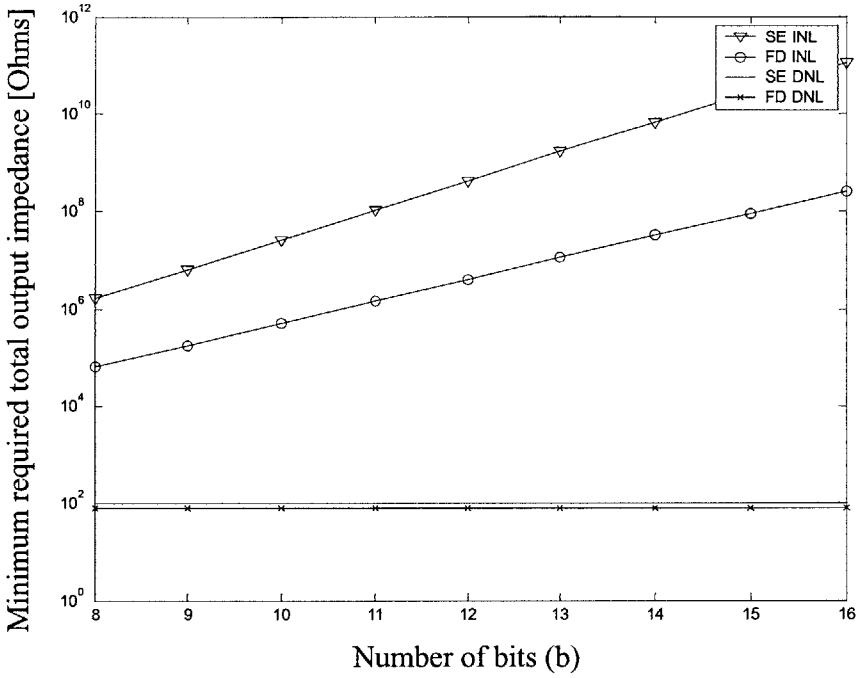

Figure 4-9: Minimum total output impedance required to meet static 1/2 LSB INL and DNL specifications for fully differential and single ended implementations. The load resistor r_l is 50 Ohms and the number of elements is 2^b where b is plotted on the horizontal axis.

shows that the INL output impedance requirements for a fully-differential DAC are reduced by over an order of magnitude relative to the INL requirements for a single-ended DAC.

4.3.2 Dynamic Performance Specifications

Communications applications are demanding good frequency domain performance in the form of low harmonic distortion. For a fully-differential DAC, the INL of Figure 4-8 is odd, causing IMD3 to dominate the distortion. In practice, however, any imbalance in the fully-differential output path will also cause some second order harmonic distortion (HD2). Since the single-ended INL curve of Figure 4-8 is even, the second harmonic will be the SFDR limiter in the single-ended case.

The output impedance required for a given IMD3 is derived by considering a DAC with a sinusoidal output. The number of switches "on" at time t for a DAC with a sin(wt) output is:

$$S(t)_{on} = N\frac{\sin(wt)+1}{2} \tag{4.16}$$

The number of switches "off" at time t is:

$$S(t)_{off} = N\frac{1-\sin(wt)}{2} \tag{4.17}$$

The impedance looking into the output terminal is

$$g_{outon} = g_l + g_o N\frac{\sin(wt)+1}{2} \tag{4.18}$$

The impedance looking into the complementary terminal is

$$g_{outoff} = g_l + g_o N\frac{1-\sin(wt)}{2} \tag{4.19}$$

The voltage at the output terminal is

$$V_{outon} = IN\frac{(\sin(wt)+1)}{2g_l + g_o N(\sin(wt)+1)} \tag{4.20}$$

The voltage on the complementary terminal can be similarly written, and the total fully-differential output voltage is

$$V_{outdiff} = \frac{IN4g_l\sin(wt)}{4g_l^2 + 4g_l g_o N + g_o^2(1-\sin^2(wt))} \tag{4.21}$$

Equation 4.21 can be expanded in a power series. As expected in a fully-differential topology, there are no even order harmonics.

$$V_{outdiff} \approx \frac{J}{1+K}\sin(wt) + \frac{JK}{1+K^2}\sin^3(wt) \tag{4.22}$$

$$V_{outdiff} \approx \alpha_1\sin(wt) + \alpha_3\sin^3(wt) \tag{4.23}$$

where J and K are as follows

$$J = \frac{IN4g_l}{4g_l^2 + 4g_l g_{imp} N} \tag{4.24}$$

$$K = \frac{g_{imp}^2 N^2}{4g_l^2 + 4g_l g_{imp} N} \tag{4.25}$$

The fundamental and third order (IM3) components have an amplitude [39]

$$Fundamental = \alpha_1 + \frac{9}{4}\alpha_3 \tag{4.26}$$

$$IM3 = \frac{3}{4}\alpha_3 \tag{4.27}$$

The ratio of the fundamental to the third harmonic is used to find the IMD3.

$$IMD3 = \frac{\frac{14}{3}K + \frac{4}{3}}{K} \tag{4.28}$$

Substituting and simplifying gives:

$$IMD3_{FD} = \frac{\frac{14}{3}g_o^2N^2 + \frac{16}{3}(g_l^2 + g_l g_o N)}{g_o^2 N^2} \tag{4.29}$$

The minimum required output impedance for a given IMD3 can be found by solving for g_o in Equation 4.29. To achieve a 70dBc IMD3, the minimum total required output impedance is plotted in Figure 4-10. R_l is assumed to be 50 Ohms and b is plotted on the horizontal axis, where $N=2^b$ is the number of elements in the DAC.

In narrowband communications systems, IMD3 is often the only significant harmonic that will fall inband in the presence of more than one carrier. However, the output impedance required for a given HD2 is included for completeness. Reference [40] derives the single-ended HD2 for a given output impedance in a similar way

$$HD2_{SE} = \frac{Ng_o}{4g_l + 2Ng_o} \tag{4.30}$$

The minimum total output impedance required for 70dBc HD2 performance is also plotted in Figure 4-10. Single-ended HD2 requires over an order of magnitude larger output impedance than fully-differential IMD3 for the same 70dBc spurious performance level.

Figure 4-10 summarizes the comparison in output impedance requirements for INL, DNL, HD2 and IMD3 DAC performance. If the DAC is fully-differential, the output impedance requirements drop by over an order of magnitude for both INL and spurious performance.

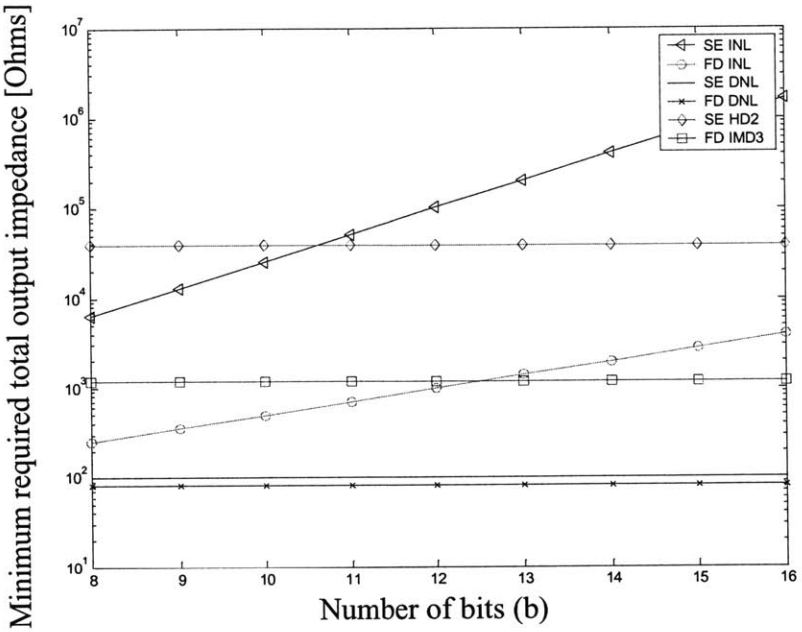

Figure 4-10: Comparison of total output impedance requirements for frequency domain and static performance requirements. All curves assume r_l=50 Ohms and the number of elements N is 2^b where b is plotted on the horizontal axis. HD2 and IMD3 requirements are plotted for -70dBc spurious performance.

4.3.3 Elimination of the Cascode Transistor

Figure 4-11 shows a DAC current steering element. M2 and M3 switch M1's current to I_{out} or $\bar{I}_{out}$ depending on the digital input, D_n. M1 is typically a large device for good matching. The high-frequency output impedance of the current source is dominated by capacitance C_d at the drain of M1 [40]. Since this capacitance degrades high frequency output impedance, an output-impedance-boosting cascode transistor M_{cas} is often added at the drain of M1.

As shown in the previous section, output impedance requirements can be reduced for the same INL and spurious performance by using a fully-differential topology. Communications applications often require good frequency-domain performance in a narrow bandwidth. If only inband SNR is relevant, device matching requirements are relaxed by oversampling compared to a Nyquist-rate DAC. Furthermore, if a ΣΔ DAC or any type of shuffling algorithm is used, matching requirements can become even more relaxed. This reduced matching requirement means a smaller device size for M1, so lower C_d and higher current source output impedance. Switches M2 and M3 can be operated in the saturation regime, further boosting output impedance. All of these design factors combined eliminate the need for the traditional impedance-boosting cascode

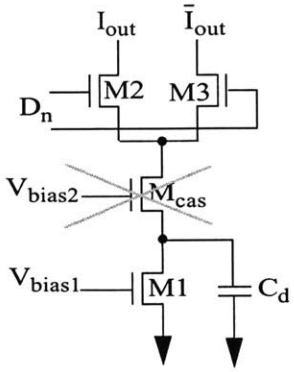

Figure 4-11: Traditional current steering DAC element.

transistor M_{cas} at the drain of M1. Elimination of M_{cas} offers a headroom savings that allows DACs to scale with technology to lower supply voltages.

4.4 Circuit Design

The TSMC 0.18μm, 1.8V CMOS technology was chosen to implement the RF DAC. It was chosen for the high transistor f_t, allowing fast switching edges and reduced gate delay. The low 1.8V supply voltage also demonstrates the ability of the DAC to be built with reduced supply voltages by elimination of the cascode transistor. TSMC's 0.18μm technology features 1 poly layer, 6 metal layers, deep N-Well for isolating NMOS transistors, metal-insulator-metal capacitors (MIMCAPs), and a thick inductor top level metal.

TSMC's 0.18μm CMOS technology also features a 3.3V option. Two versions of the RF DAC unit element core were implemented on the chip. One is built with a 1.8V supply designed for a peak current of 20mA. The signal power at the output is divided in half by the sinusoidal nature of the output and then in half again by the impulse response of the DAC at 942MHz, as indicated by Figure 3. Thus the output signal current is only 10mA at 942MHz while the peak output current is 20mA. The 3.3V DAC core has a nominal peak current of 80 mA, while the signal current at the output is 40mA. Depending on the stability of the ΣΔ, a full scale input may not be stable. Thus the output current is further reduced by the maximum stable input amplitude (MSA).

A block diagram of the 0.18μm RF DAC testchip is shown in Figure 4-12. A mux and timing circuitry serialize the data from 32 lines at 134 MHz to 8 lines at 538.5 MHz. Switch drivers drive the DAC switches at 538.5 MHz. A dummy switch driver path provides constant switching or constant injection of current in the switch driver supplies and substrate. This has shown potential for improving noise performance of high-speed DACs [37]. The gates of the RF DAC current

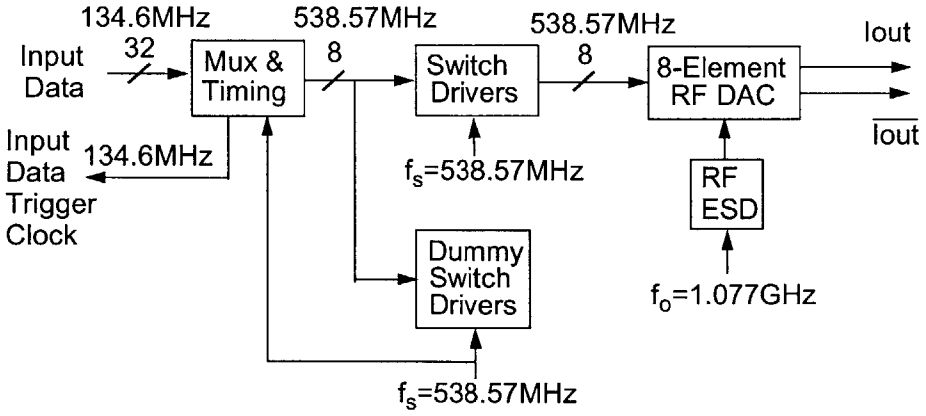

Figure 4-12: Simplified block diagram of 0.18μm RF DAC test chip.

sources are driven by an off chip oscillator at frequency f_o. The pin for this control waveform also has ESD protection. Finally the current output of the DAC is sent through an off-chip transformer to the spectrum analyzer.

There are three coefficients that can be loaded upon startup to configure the state of the DAC. Enable_dummy enables the dummy switch drivers. By allowing the dummy path to be enabled and disabled, measurement results can be obtained to verify if the dummy path affects the performance of the DAC. Disable_mux disables the mux so the 8 unit elements of the DAC can be driven directly from the first 8 inputs. This method only allows the DAC to be driven up to 220MHz, limited by the pattern generator in the lab. However, this option was included as a bail-out and a quick way to test functionality without any timing issues. The final coefficient switches the input lines between the 1.8V and 3.3V DAC. Thus when the 1.8V DAC is being tested, the 3.3V DAC should not be switching or injecting any noise, and vice versa.

4.4.1 Unit Elements

The DAC unit element core design is shown in Figure 4-13. An NMOS DAC was chosen over a PMOS DAC for increased switching speed. M1 is the current source with an oscillating gate driven by V_{osc}. Switches M2 and M3 steer M1's current to either I_{out} or $\bar{I}_{out}$ depending on the value of the data. Since the impedance boosting cascode transistor of Figure 4-11 has been eliminated, M1-M3 are designed in the high output impedance saturation region.

Design considerations for the size of MN1 include full scale current and matching requirements. A 1% target matching requirement gives a constraint on the total area of device M1. Predicted

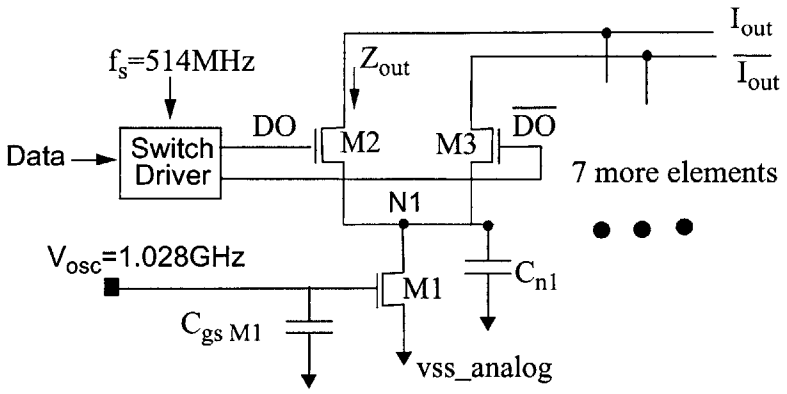

Figure 4-13: One of eight identical current steering DAC elements implemented in 1.8V, 0.18μm CMOS technology.

matching data was only available for devices with common centroid layout techniques, but RF DAC does not utilize these techniques (For additional comments, please see Chapter 4.5). Thus the device size was over-designed by a factor of about 5. The W/L ratio was chosen to give the desired peak output current at a peak gate drive of 1V. There is a trade-off in the maximum output power and the noise sensitivity when designing the gate drive Vosc. The zero region of the output could be longer to reduce noise sensitivity and ensure that all switching transients fit within this region, but this extended zero region reduces the available output power. Although a larger peak gate drive voltage could be used, this increases the V_{ds} needed for M1 to stay in the saturation regime, decreasing the maximum full scale output voltage. The final design values for M1 and the associated capacitances C_{gs} and C_n are shown in Table 4-6.

Table 4-6: RFDAC test chip design summary. All values taken at the peak gate voltage V_{osc} =1V.

Parameter	1.8V DAC	3.3V DAC
Peak Output Current at V_{osc}=1V, slow, nominal & fast process models	16, 23.2, 28.8 mA (2, 2.9, 3.6 mA/element)	58.4, 80, 101.6 mA (7.3, 10, 12.7 mA/element)
W/L of M1	88μm/1.1μm	200μm/0.7μm
Current Source Vgs-Vt at Vgs=1V, slow, nominal, fast process models	0.489V, 0.567V, 0.622V	0.473V, 0.552V, 0.605V
Matching Expected from TSMC Non-Relaxed Matching Data (1% needed)	0.23%, 0.2%, 0.19%	0.2%, 0.18%, 0.16%
W/L of M2,M3	30um/0.24um	150um/0.35um
Vdd of the switch driver	1.8V	2.2V

Table 4-6: RFDAC test chip design summary. All values taken at the peak gate voltage V_{osc} =1V.

Parameter	1.8V DAC	3.3V DAC
Maximum output voltage swing of each side so all transistors stay in saturation	1.8V-1.13V	3.3V-1.8V
C_{gsM1}	4.8pF (0.6 pF/element)	7.0 pF (0.89 pF/element)
C_{n1}	182 fF	730fF
C_{n1} due to wiring	45.6 fF	114fF
Z_{out} Simulated (Z_{out} needed)	26.4k (8.6k)	15.7k (8.6k)
Inband SNR Simulated with -2dB full scale (FS) input	79.4dB with 0.5% mismatches, no timing offsets 73dB with mismatches, 0.2ns timing offset	65dB with 0.5% mismatches, no timing offset 54dB with 0.5% mismatches, 0.4ns timing offset (middle of current peak)
Max SNR calculated due to simulated transistor noise (1/f, thermal)	87.6 dB	91.3 dB

The size of the switches M2 and M3 were chosen as a compromise between maximizing the output impedance and keeping V(N1) high enough for M1 to stay in saturation. To clarify, the output impedance looking into the I_{out} terminal when M2 is on is

$$z_{out} = r_{o2}\left(1 + g_{m2}\left(r_1 \parallel \frac{1}{j\omega C_n}\right)\right) + \left(r_1 \parallel \frac{1}{j\omega C_n}\right) \tag{4.31}$$

For high output frequencies present in RF DAC,

$$z_{out} \approx \frac{r_{o2} g_{m2}}{j\omega C_n} \tag{4.32}$$

As the size of M2 increases, r_{o2} ($r_{o2} \propto L$) and g_{m2} ($g_{m2} \propto \sqrt{\frac{W}{L}}$) increase, but the capacitance C_n ($C_n \propto$ W*L+ constant) at node N1 also increases. Therefore, there is an optimal size for M2 to maximize the total output impedance. The output impedance versus width W of M2 is plotted in Figure 4-14. For low values of W, Vgs of M2 is large and M1 goes out of saturation. Once M1 is

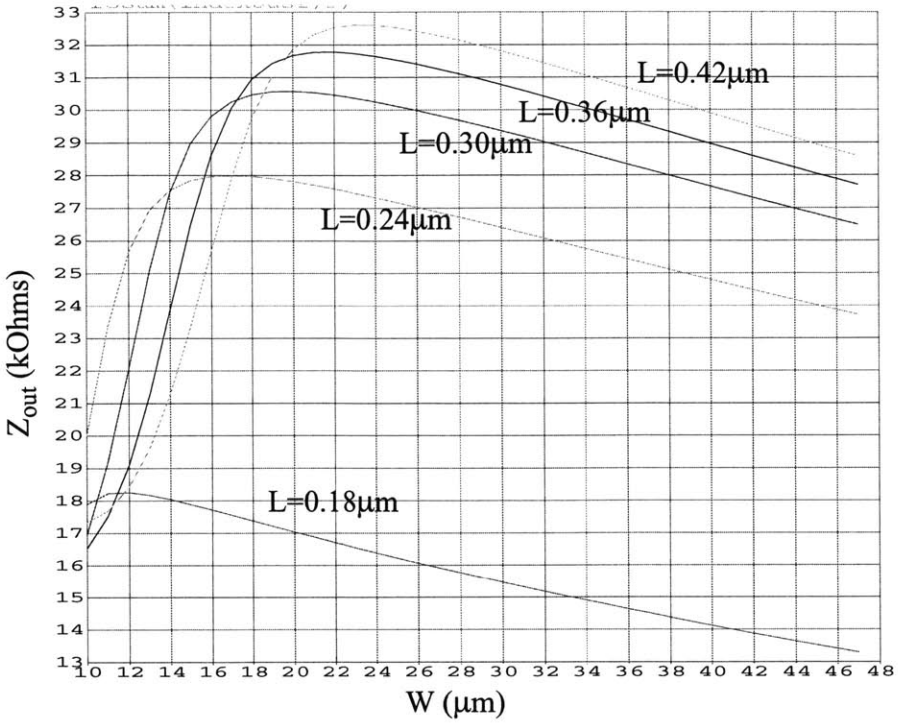

Figure 4-14: Output impedance versus width W of M2. Plots are for various lengths of M2 with an output frequency of 942MHz at the peak output current. The current source device size M1 of 88μm/1.1μm in the 1.8V DAC.

in saturation, the curves follow the expected $\sqrt{\frac{1}{W}}$ relationship. Figure 4-14 plots the output impedance for several values of L. A large L is desirable for slightly higher output impedance and better matching. However, a low L is desirable for ease of driving the switch and for lower V_{gs} of M2 so node N1 is kept high. Thus a compromise was reached for the device size by selecting a point close to the optimal output impedance but with slightly larger W to ensure M1 stays in the saturation regime.

The switch driver peak output voltage (Vdd_{swdr}) is another design parameter. Keeping M2/M3 in the saturation regime, the voltage at the output can swing from a maximum of the supply at the output (Vdd_{output}) to a minimum of Vdd_{swdr}-V_{t2} where V_{t2} is the threshold voltage of M2/M3. If the output voltage swings below this value, M2/M3 will go out of saturation and output impedance will be degraded. Thus it is desirable to have a low Vdd_{swdr} to maximize the output swing. However, large Vdd_{swdr} speeds up the switching time. If the edges are faster, more of the switching happens in the zero region of the control waveform. Large Vdd_{swdr} also ensures a high voltage for node N1 to keep M1 in saturation. A compromise was made so a full swing Vdd_{swdr}=1.8V

was designed for the 1.8V DAC and a slightly reduced Vdd_{swdr}=2.2V in the 3.3V DAC. In the final design, Vdd_{swdr} is connected to a pad and taken off chip so the value could be both changed and decoupled from other supplies.

There are a few things in this architecture that are unlike a conventional DAC design. Conventional DACs try to keep the current in the tail current source constant by minimizing variations in node N1 [24]. In this design, however, node N1 varies with V_{osc}. Any disturbance to N1 or the output nodes due to the switching of M2, M3 appears as a constant disturbance on each switching cycle. This is because the switches always switch when M1 has nominally zero current. This means that nodes N1, I_{out} and $\bar{I}_{out}$ always have the same voltage when M2 and M3 switch. Thus the output disturbance is proportional to the number of elements switching, which is also proportional to the input signal and does not cause any inband distortion.

Conventional DACs also seek to minimize coupling of the control signals to the outputs through C_{gd} of the switch transistors M2 and M3. This typically involves minimizing the sizes of M2, M3 and reducing the voltage swing at the input of the switches. However, since the output of RF DAC returns to the same voltage at every data switching instant, the coupling is proportional to the number of elements switching, causing no inband distortion.

Given these transistor sizes, the noise in the unit element must also be considered. The noise of the DAC will get mixed with the input and fall directly in band. Flicker and thermal noise of M1 dominate the noise performance of the DAC core, as shown in the top plot of Figure 4-15. The current noise is calculated from a simulation of the output voltage noise

$$\bar{i}_n = \frac{2\bar{v}_n}{r_l} = \frac{2\sqrt{\int n^2(f)df}}{r_l} \tag{4.33}$$

where $n^2(f)$ is the noise voltage at the output in $\frac{V}{\sqrt{Hz}}$, $\bar{v}_n$ is the integrated voltage noise, $\bar{i}_n$ is the integrated current noise, and r_l is the 25 Ohm output load resistor. The factor of 2 in Equation 4.33 indicates that the integrated noise is not single sided in frequency, although the simulations are single sided in frequency. So to get the total noise in a 17.5MHz bandwidth, the amplitude of the noise must be doubled. The total noise $\bar{i}_n$ is plotted in Figure 4-15. The maximum SNR is

$$SNR = 20\log\frac{nI_{rms}}{\sqrt{n}\bar{i}_n} = 20\log\frac{\sqrt{n}I_{rms}}{\bar{i}_n} \tag{4.34}$$

where n is the number of elements in the DAC and I_{rms} is the rms output current. Using the value of $\bar{i}_n$=0.237μA at 8.75MHz from the top plot of Figure 4-15, Equation 4.34 gives a maximum achievable SNR of 85dB for the 1.8V DAC and 91dB for the 3.3V DAC. If these noise models are accurate, noise in the DAC core transistors should not limit the SNR of the system, given the 64-72dB numbers in Table 4-5.

The bottom plot of Figure 4-15 shows the noise referred to the output expressed in dBm/$\sqrt{Hz}$. This plot shows that the 1/f noise corner of device M1 is around 10MHz, but that around 100kHz the output noise will be dominated by the output resistors. The output resistor for this simulation was modelled as 16.6Ohms, which is the actual 50Ohm resistor in parallel with 25Ohms reflected through the transformer. This resistance was used to get the noise of the transistors correct. However, the thermal noise of the actual output resistors themselves is off since they are modelled as the noise associated with 16.6Ohms instead of the noise associated with 50Ohms. Thus the corrected curve is also plotted on the bottom of Figure 4-15.

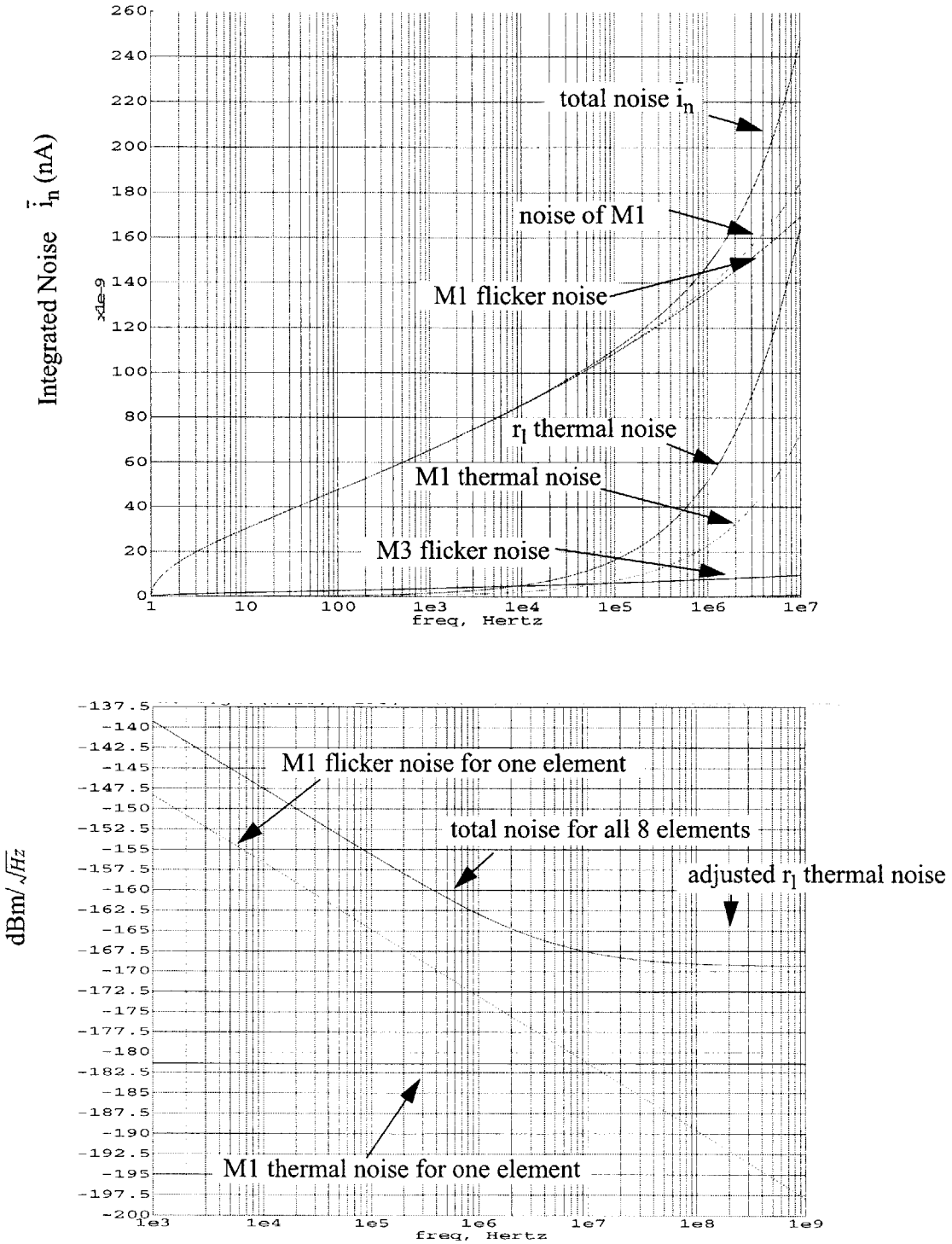

Figure 4-15: Integrated current noise at the output of a single 1.8V DAC element as a function of frequency. The output load resistor r_l is assumed to be 16.6 Ohms, composed of a 50 Ohm termination resistor and 25Ohms as the analyzer input reflected through the transformer. The bottom plot shows the total noise of all the elements referred to the output in dBm/$\sqrt{Hz}$

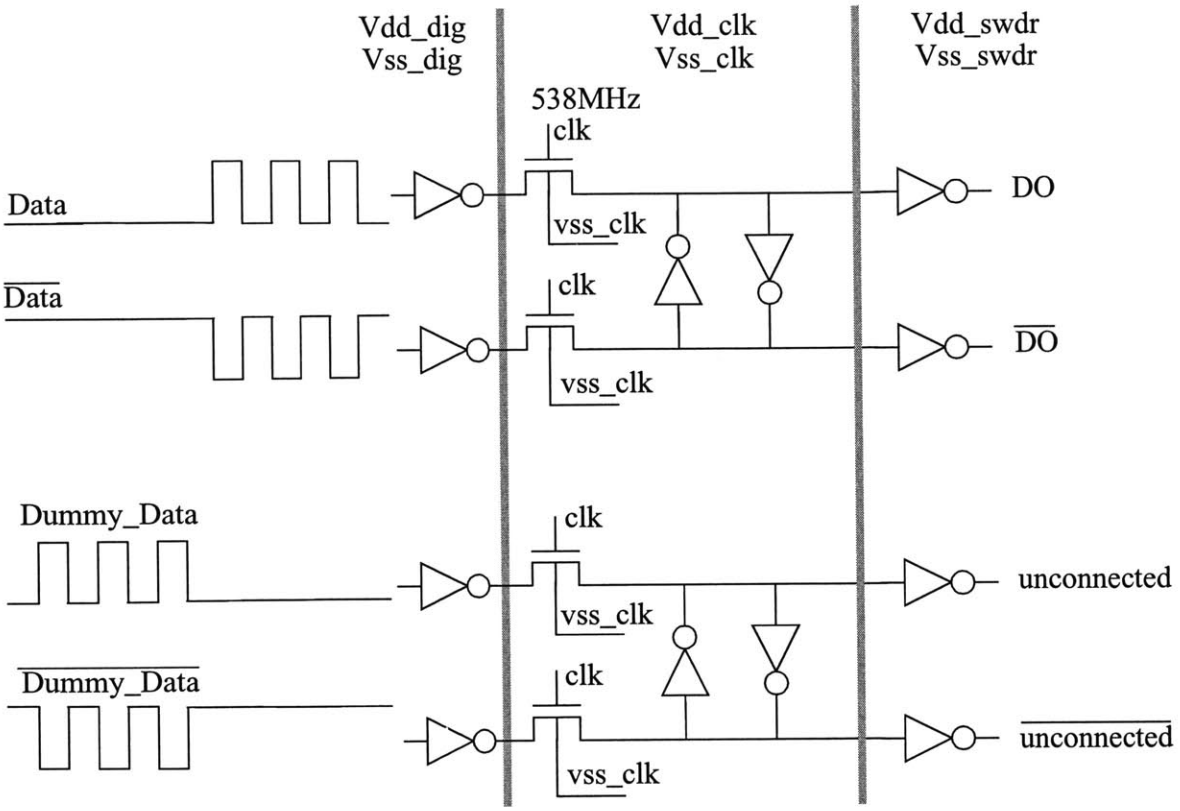

Figure 4-16: Switch drivers for each unit element of the DAC. A dummy switch driver switches whenever the data does not. Also shown are the power and ground plane divisions. Dummy_Data allows the Vdd_clk and Vdd_swdr supply domains to see constant switching.

4.4.2 Switch Drivers

The switch drivers receive the digital data and drive the current steering switches M2 and M3 of Figure 4-13. The switch driver schematic is based on the work of [42] and is shown in Figure 4-16. Examples of input Data and generated Dummy_Data show that the Dummy_Data path switches whenever the input Data does not switch. Also shown are the divisions of the power and ground supply planes. The final inverters that drive the switches M2 and M3 are on their own separate supply Vdd_swdr. This allows the switching voltage to be adjusted and also prevents coupling from the clock and digital domains. Vdd_dig is the supply that is used for all the digital timing and input data. The Vdd_clk domain is used for the inverters that buffer the clock on chip as well as for the middle section of the switch drivers. Since either the Data or Dummy_Data is switching on every cycle, glitches on the vdd_clk supply from the

switching inverters should be constant every clock cycle, reducing code-dependent timing errors. Similarly, since either the Data or Dummy switch driver switches every cycle, the supply injection in the Vdd_swdr domain should also be constant and data-independent to first order. To second order, there will be some inconsistencies Conventional switch driver design tries to achieve a high crossing point, so M2 and M3 of Figure 4-13 are never simultaneously in the off state and node N1 is held constant. If M2 and M3 are simultaneously off, node N1 will start to rise. This will cause the current through the element to change, causing distortion in the output [15] [19].

In this design, the current is oscillating, so node N1 oscillates with the current. Node N1 should nominally be at the same voltage for every switching point. The critical constraint in this design is that all the switching transients 'fit' into the zero region of the current waveform. This ensures that sampling clock jitter does not limit performance and that switching distortion is constant on every cycle. Although V_{osc} could be DC shifted to give a longer zero region, this reduces the output power that can be achieved. Thus the switch driver design in this work strives to minimize the total switching time, ensuring that all switching transients fit into the zero region of the output waveform.

Conventional high speed DAC designs also use a reduced swing at the output of the switch drivers [15] [19] to minimize charge injection of the digital control signals to the output. However, this technique reduces the switching speed of the waveform and was therefore not used in this design.

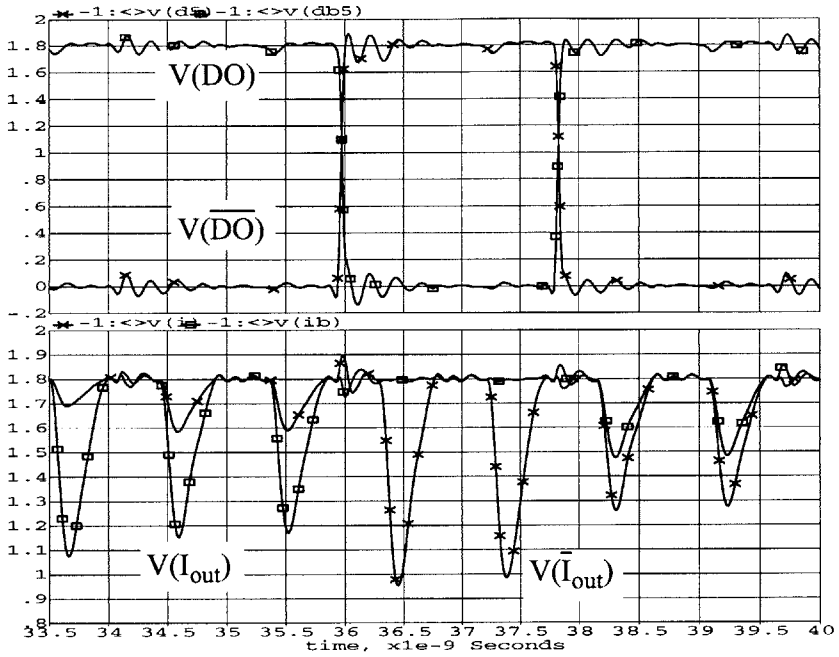

Figure 4-17: Time domain simulation of a single switch driver switching waveform and the corresponding output waveform change. Note that more than the single switching element D0 is switching at the output.

A sample RF DAC switching waveform is shown in Figure 4-17. The switching point was designed near midscale to reduce the total switching time. The swing of the switches is 1.8V for the 1.8V DAC and 2.2V for the 3.3V DAC. The total switching time versus process is 0.05ns to 0.1ns for the 1.8V DAC and 0.1ns to 0.2ns for the 3.3V DAC.

4.4.3 Analog DAC Core Summary and Simulations

A summary simulation of the total analog DAC core is shown in Figure 4-18. Simulated are the unit elements, switch drivers, and lead frame/bond wire models on the power supplies. Plotted first in Figure 4-18, v(d5) and v(db5) show a unit element switching. v(vosc) is the voltage at the gate node of the current source, oscillating at 1GHz. Shown beneath v(vosc) is <x4>i(mn1,d), the current in one of the unit elements of the DAC core. Note that this waveform is slightly out of phase with v(vosc), and the phase difference would be even worse if the R-C parasitics of the Vosc bond wires, traces, and on-chip wiring were included. Thus lining up the phase of the switching clock with the zero region of the current waveform can only be accomplished by looking at the SNR of the output, not the phase of the signals as they appear on the PC board. <x4>v(n1) is the voltage at node N1 of Figure 4-13. Switches M2 and M3 pull this node high as

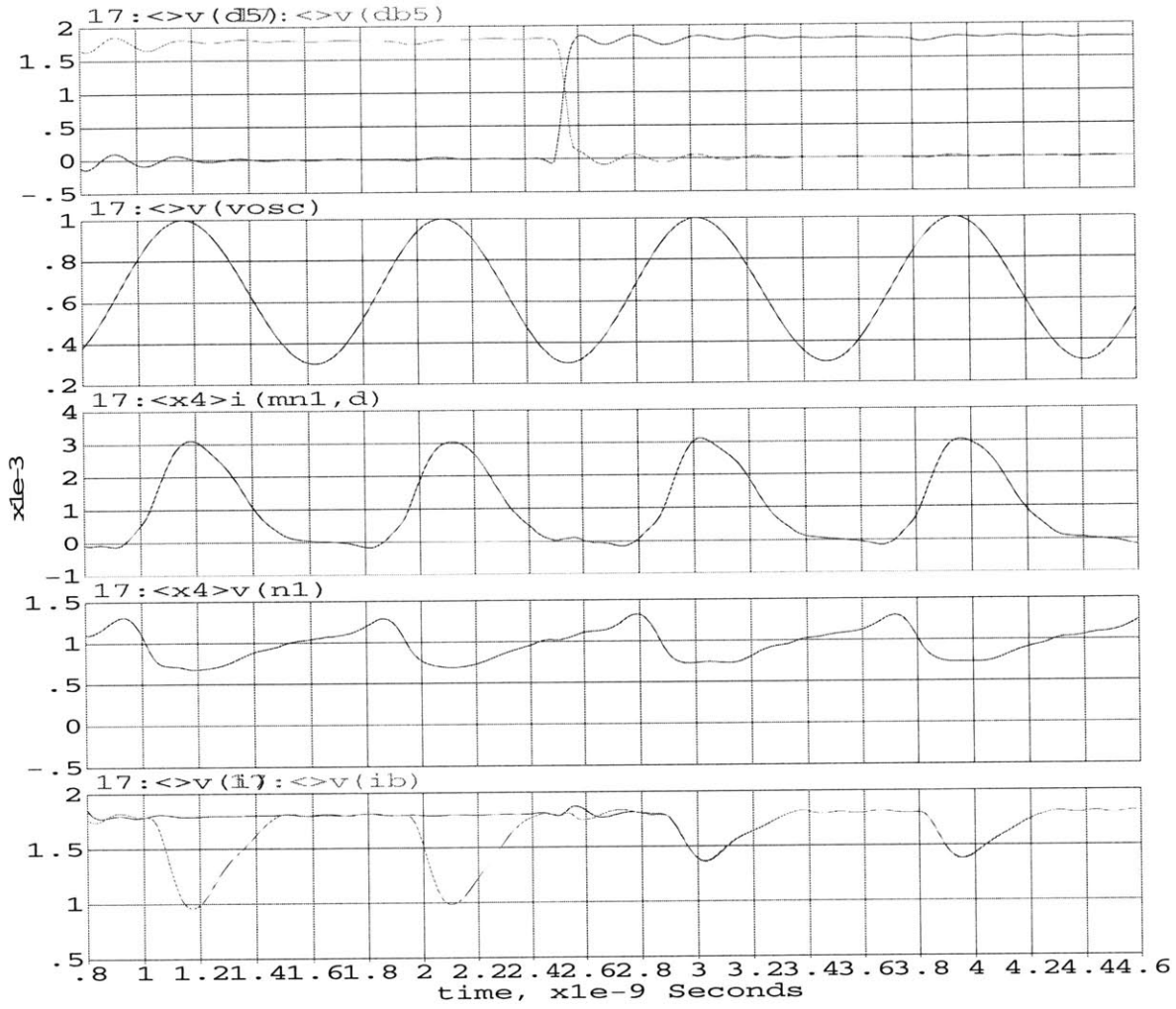

Figure 4-18: Time-domain simulation showing relevant DAC core node voltages and currents for the 1.8V DAC. At the top is a single unit element switching waveform. V(vosc) is the oscillating gate waveform, and <x4>i(mn1,d) is the drain current in one of the unit elements. <x4>v(n1) is node N1, and v(i), v(ib) are the two halves of the differential output voltage waveform.

the current decreases. The last plot shows the output voltages v(i) and v(ib) when the DAC is resistively terminated. Notice that there are some transients in the output voltage, i.e. the minimum voltage near 1.2ns does not quite equal that at 2.1ns. This indicates that the output current will not quite be the same on every switching cycle, causing some code-dependent distortion.

The total analog DAC core was simulated in the time domain and the SNR calculated. This includes the unit element current sources, switches, switch drivers, supplies with lead frame and bond wire models. The analog unit elements and switch drivers also have mismatches, the values

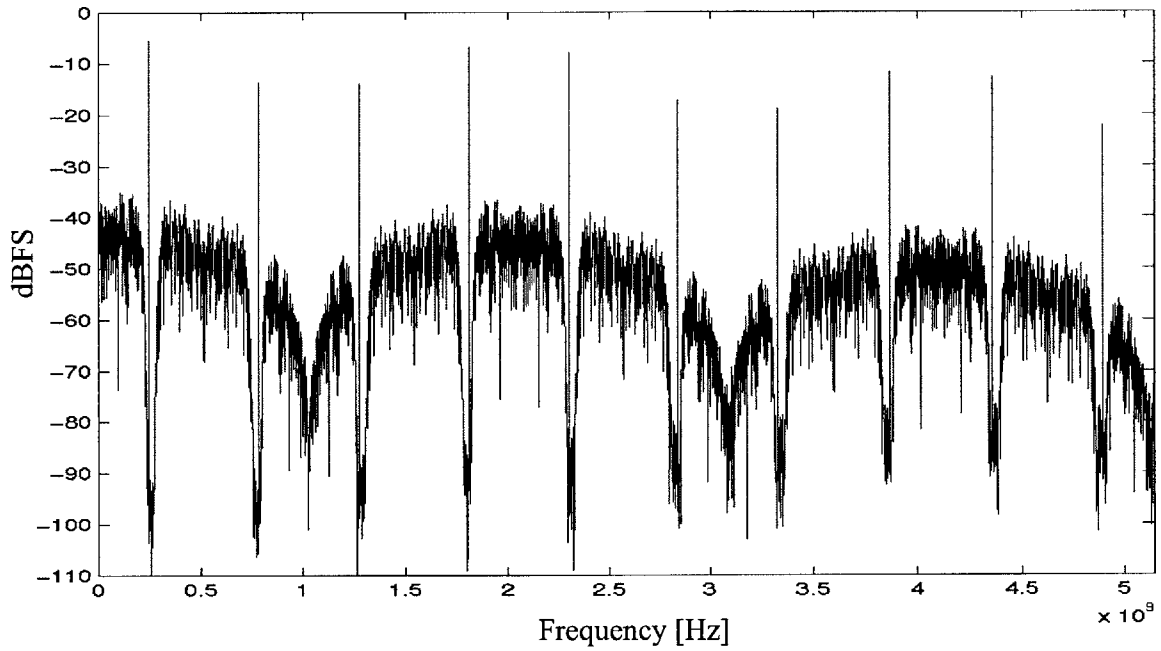

Figure 4-19: Total output spectrum of the analog DAC core simulation. The clock frequency is f_{clk}=514MHz and f_{osc}=1.028GHz.

of which are estimated. 1024 input codes were used, with 128 time domain points per input code. This large number of points ensures that time domain glitches or code dependencies are included in the SNR. The results are shown in Figure 4-19 for f_{clk}=514MHz and f_{osc}=1.028GHz. The inband region is centered around $f_{clk}/6$ and the images of the input show a scaling by the predicted sinc with a high-frequency, high-energy lobe. Note that the unwanted images of the input can be easily filtered, since the filter will need a roll-off dictated by attenuating out of band quantization noise.

The inband SNR is about 8 dB lower than the ideal Matlab simulation of 74dB. This is due to the distortion in the drain current of the unit elements, as shown in Figure 4-20. Figure 4-20 shows the simulated current through one unit element plotted in dB. Any distortion not at multiples of f_{osc}=1.028GHz will alias with the out of band quantization noise of the digital input and alias that noise back inband.

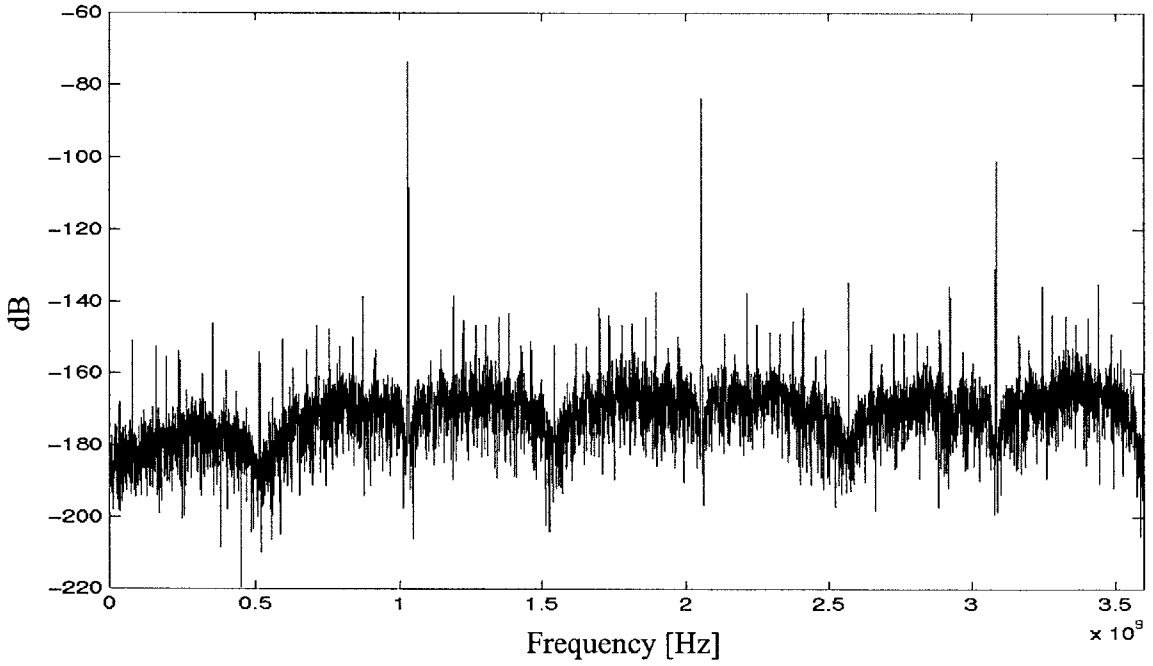

Figure 4-20: Simulation of the current through one unit element for f_{clk}=514MHz and f_{osc}=1.028GHz.

4.4.4 Timing Circuits and Multiplexer

Since the lab equipment available could only input a maximum of 36 channels at up to 220MHz, a mux and timing circuits were needed to serialize the data by a factor of 4 from 32 lines at 134.6MHz to 8 lines at 538.57MHz. The main timing circuit is shown in Figure 4-21. The 538.57 MHz clock is divided into 4 phases, c<1> through c<4>. These phases are used by the mux to switch the input data to a high speed latch running at 538.57 MHz. The flip-flops are reset on start-up if more than one of the phases c<1:4> are high. In this case, all the flip-flops are reset while the first flip flop (on the left) of Figure 4-21 is set (set presides over reset). Similarly, if the disable_mux coefficient is high, all of the flip flops are kept in the reset state while the first flip flop is kept in the set phase. This allows the first 8 inputs to drive the DAC directly through path c<1> in the mux.

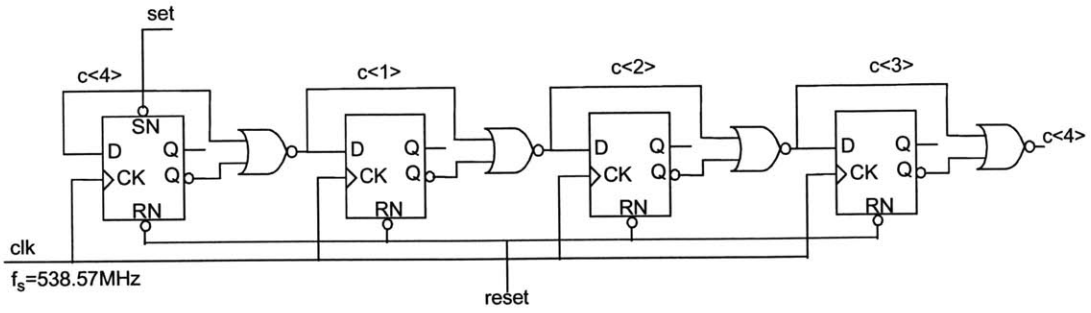

Figure 4-21: Timing circuitry, generating 4 clock phases at $f_{clk}/4$.

An example simulation of the circuit of Figure 4-21 is shown in Figure 4-22. The 538MHz clock in the bottom of Figure 4-22 clocks the latches in Figure 4-21 to create c<1:4>, effectively dividing the clock into four phases to multiplex the input data.

In addition to driving the mux, c<4> is buffered and drives the latches that latch the new input data. Then on the next c<1> phase, the new data is loaded into the DAC. Similarly, c<2> and c<3> are buffered and combined to get a 50% duty cycle at $f_s/4$. This clock is driven off chip to

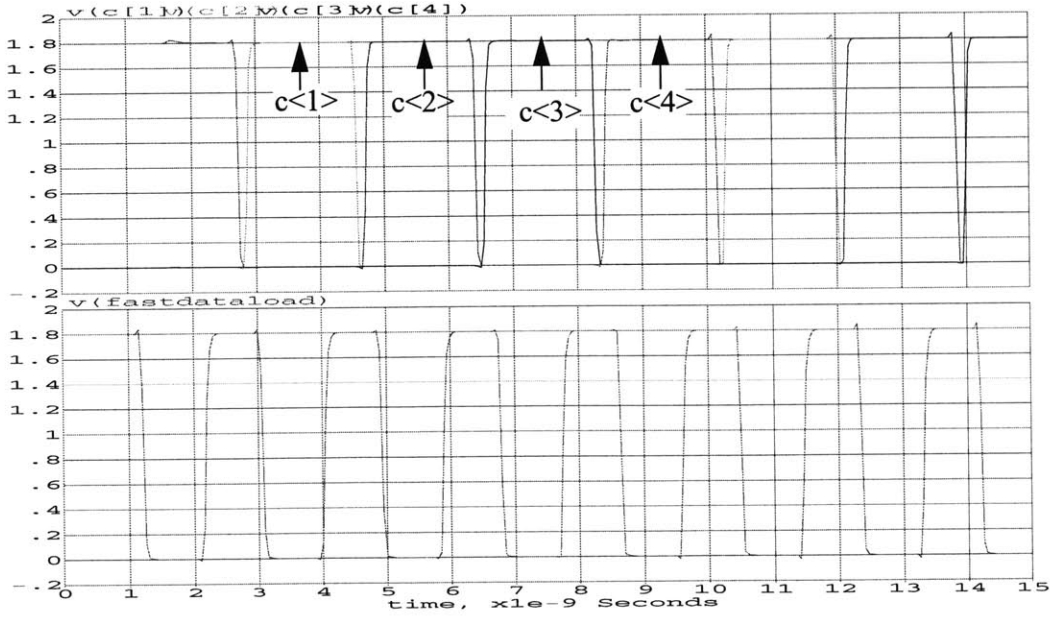

Figure 4-22: Simulation of the circuit of Figure 4-21, showing the division of the bottom clock into four phases that multiplex the data.

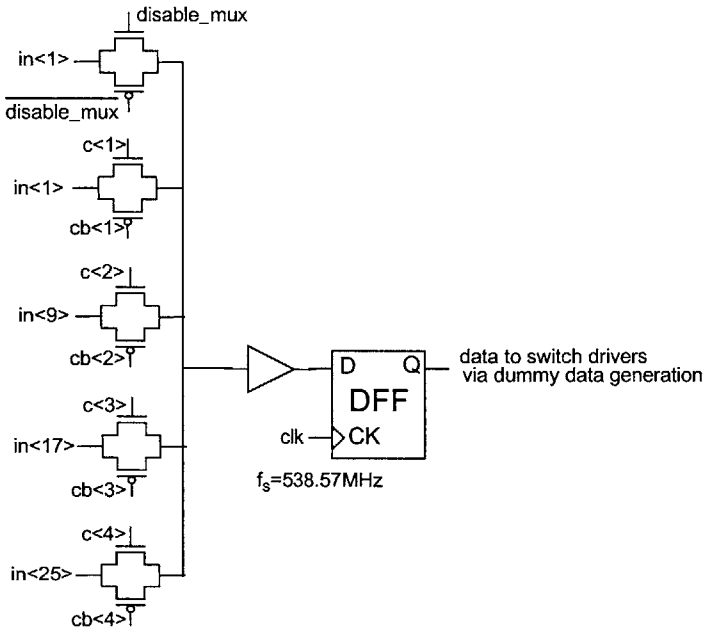

Figure 4-23: Single mux cell, repeated 8 times for each of the 8 DAC elements.

trigger the pattern generator to send more input data. Since c<2:4> are all buffered and used by both the mux and for other purposes, c<1> also had a dummy buffer so that c<1:4> all see the same load.

While it seemed like a good idea at the time to have the chip trigger the input data, it turns out that driving the pad capacitance and trigger input required large buffers with lots of current drive to be used. This created large current injection into the supplies and into the substrate at $f_s/4$. Since this was desired to be the input frequency band, these clock tones showed up inband in the output spectrum and mixed with the input to create unwanted spurs. Final testing had to be performed at a band other than $f_s/4$, but this problem may have been avoided in the first place if the input data trigger were built from a divider or PLL off chip.

The mux is shown in Figure 4-23. The clock phases c<1:4> determine which pass gate is turned on. The appropriate input is then connected to the buffer and latched with a high speed latch running at 538.57MHz. The top pass gate connects the first input directly to the latch when the disable_mux coefficient is high.

Constraints on the timing circuits and latches were simulated over process, temperature, and supply. The timing constraints in all cases were met by a margin of about a factor of four. Thus the inputs should be able to reach the 220MHz input data clocking limit of the pattern generator.

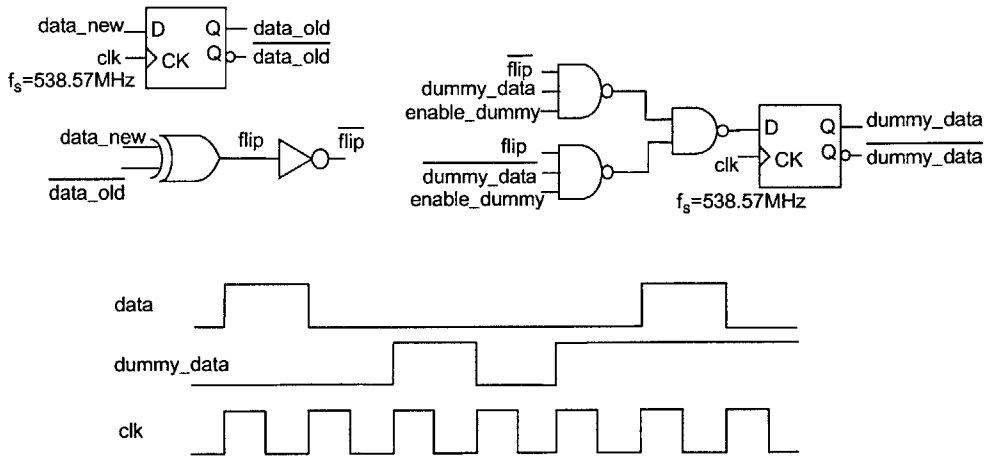

Figure 4-24: Dummy data generation logic.

4.4.5 Dummy Data Generation

The dummy data path ensures that the vdd_clk and vdd_swdr supply domains see almost constant switching. This is achieved by digital logic that senses if the input data has switched. If the input data has not switched, then the dummy data will switch. Thus either the input or dummy path is switching on each clock cycle. The logic to generate dummy data and an example waveform is shown in Figure 4-24. A latch stores the old value of the data so it can be "xor"ed with the new data. This creates the 'flip' signal, indicating whether or not the dummy data should flip. If 'flip' is low, 'dummy_data' should not switch since the 'data' path has switched. Similarly, if 'flip' is high, 'dummy_data' should switch since the 'data' path has not switched. Thus either the 'data' path or 'dummy_data' path is switching on every clock cycle. There is also an 'enable_dummy' coefficient so the converter performance can be compared with and without the dummy path switching.

4.4.6 High Frequency Electrostatic Discharge (ESD)

The low gate oxide breakdown voltage in aggressive CMOS processes necessitates the use of electrostatic discharge (ESD) protection for gates connected to pads. Conventional ESD clamps result in large series resistance and large junction capacitance on the input pad [43]. Low frequency digital inputs can tolerate this large R-C time constant. However, since node V_{osc} is designed to operate near 1GHz, alternative ESD structures were investigated.

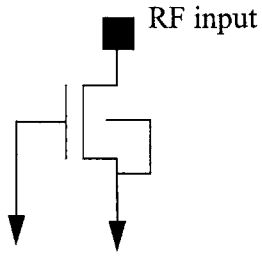

Figure 4-25: A gate-grounded NMOS ESD clamp.

A gate grounded NMOS transistor shown in Figure 4-25 has been shown to have an 8kV HBM (Human Body Model) ESD level when stressed with a negative voltage, but only a 500V HBM ESD level when stressed with a positive voltage [43]. This is because the NMOS ESD current is dominated by drain breakdown for positive voltages and a forward biased drain for negative voltages. A complimentary PMOS device can be added to the NMOS to increase the ESD tolerance to positive voltages. However, this increases capacitance and requires a positive supply. Since the supply of the analog portion of the DAC is on the board instead of on the chip, only an NMOS ESD clamp was used at the V_{osc} input. The drain contact to poly gate spacing was increased from the minimum 0.16μm spacing to 1.5μm and silicide blocking was used in this region. This increases the series resistance, thereby improving the ESD tolerance [43]. Furthermore, this NMOS ESD structure was built in a deep N-well to isolate the V_{osc} node from any substrate coupling.

Standard TSMC ESD structures were used on the low frequency digital inputs. No ESD protection was used on the analog output of the DAC since drain diffusions are much more ESD robust than thin oxide gates.

4.5 Layout

DAC layout is typically challenging in terms of minimizing mismatches in the current source transistors and timing mismatches between the elements of the DAC [15] [17] [30]. Adding a 1GHz oscillating control waveform creates additional constraints. Current source matching in this design was only needed at a level of 1%, since mismatch shaping reduces the effect of matching errors. However, the capacitance at node N1 needed to be minimized to reduce degradation of output impedance at high output frequencies. Furthermore, the 1GHz Vosc gate oscillating voltage needed to be delivered to all of the elements at the same time. The 500MHz switching waveforms should likewise be delivered to the unit elements at the same time.

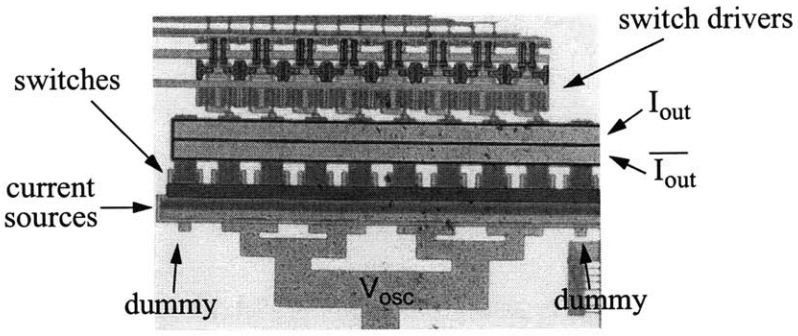

Figure 4-26: 1.8V RF DAC analog core die photo. Active area is $0.06mm^2$.

This set of constraints gave the final analog core layout of Figure 4-26. While conventional current source layout uses a common-centroid scheme, with only 1% matching needed, the current sources here are laid out in a row with dummies on the ends. This minimizes the routing on node N1 and allows V_{osc} to be delivered in a tree to all of the elements simultaneously. The bulks of the current sources are all isolated from the substrate together in one deep N-Well. The isolated P-Well of the current sources is connected to their common grounded sources (vss_analog) and deep N-well is star connected to a pad and pin where it is connected to Vdd. The switches are located directly above the unit elements in their own separate deep N-Wells. They are as close to the current sources as possible without violating deep N-Well spacing rules. The output lines I_{out} and $\bar{I}_{out}$ are located above the switches, and are wide for large current carrying capability. The switch drivers are above the output lines, and the digital circuits are located a few hundred microns away from the switch drivers.

The switch drivers are laid out symmetrically to minimize imperfect synchronization of the control signals at the switches. Furthermore, all the transistors in the Vdd_clk and Vdd_swdr domains are in separate deep N-wells to isolate their backgates from the digital substrate.

The total chip layout is shown in Figure 4-27. The 1.8V and 3.3V DAC cores are as close as possible to the output pads to reduce loss. They are also separated from the digital circuitry. The layout is pad limited by the 32 digital input lines. The DAC core are a relatively small portion of the

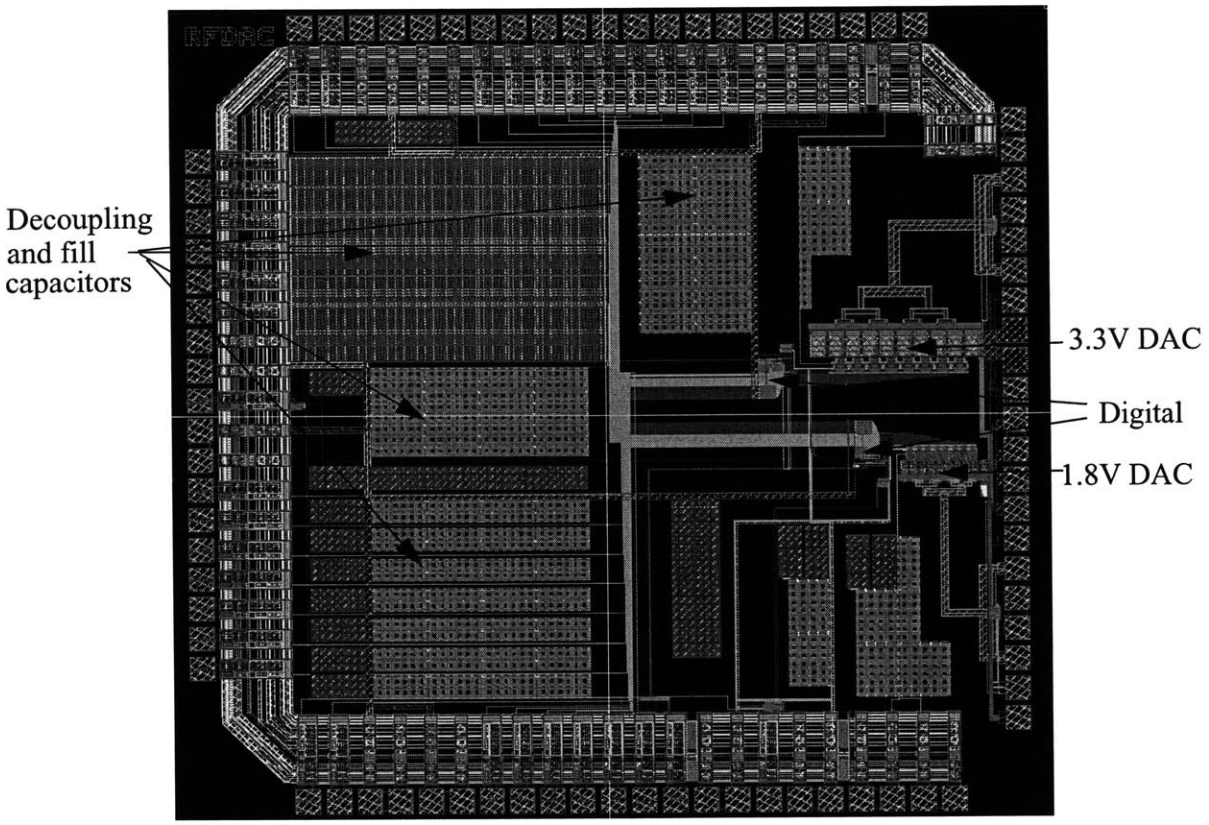

Figure 4-27: Total RF DAC test chip layout.

total chip area. The rest of the chip consists of MIM-capacitors and metal capacitors that satisfy the minimum processing fill requirement and also decouple the supplies.

The chip is packaged in a chip-scale-package (CSP) with 64 leads. The pin-out shown in Figure 4-28 was designed to minimize coupling from the digital inputs to the analog outputs. The left side of the chip contains the 32 digital inputs with digital power and ground. The right side of the pinout has the analog outputs: 'I', 'IB', 'I33' and 'IB33'. These outputs are surrounded on the chip, leadframe and board by metal lines named 'Isurround'. This 'Isurround' node can be connected on the board to the 1.8V supply, 3.3V supply or 'Vss_analog'. The oscillating signal that goes to the gates V_{osc} is also surrounded by 'Vss_analog', the source of the NMOS current source

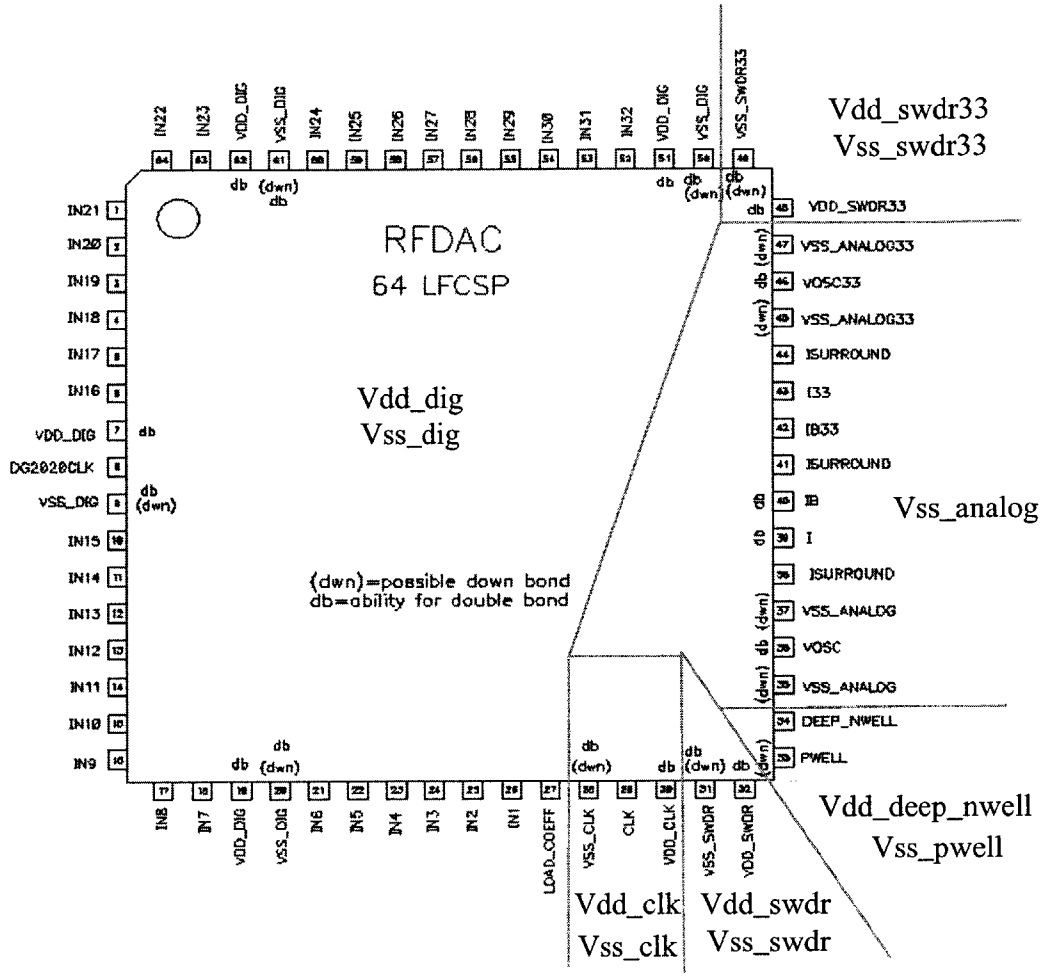

Figure 4-28: RF DAC testchip pinout, including separation of the power and ground planes.

transistors. This ensures that the current that charges the current sources is returned along 'vss_analog'.

The power and ground plane divisions are also shown graphically in Figure 4-28. The analog vss_analog, deep N-Well, switch drivers, and clock domains are separated on the chip, pinout, and board layout. The separation minimizes coupling between the digital and analog sections of the test chip. The grounds can be connected on the board through footprints that support either shorts, resistors or inductors.

Double bonds are indicated by 'db' next to the pins of Figure 4-28. The double bonds require two pads, which increase the area of the already pad-limited design. Double bonds are used to reduce the inductance and resistance of the connections only on supplies and critical analog nodes. Since the 1.8V DAC design is headroom limited, downbonds were used on I and $\bar{I}$ to minimize the volt-

age drop across the bond wire and leadframe. Since the 3.3V DAC has a larger output voltage swing before the unit elements go out of the saturation region, a larger resistive drop could be tolerated and no double bonds were used.

4.6 Board Design

The test board also includes the power and ground separations indicated in Figure 4-28. Furthermore, the digital inputs from the pattern generator also had their own ground, which is not depicted in Figure 4-28. The termination resistors for the digital inputs were as close as possible to the return ground connection. This ensures that the large digital switching return currents are routed directly back to the pattern generator.

The schematic for the gate bias and oscillator inputs is shown in Figure 4-29. The vb_vosc and vb_vosc33 DC input voltages are decoupled on the board before reaching the resistors R3 and R4. The AC signal from the oscillator is terminated with a 50 Ohm resistor and then AC coupled to the gate node. The jumpers offer test points where the voltages can be measured using a FET probe that attaches directly to the jumpers.

The main challenge in the board design was minimizing the parasitics on the critical current output nodes. The board schematic for the output nodes is shown in Figure 4-30. Resistor footprints are provided for DC testing, while the capacitor and inductor footprints provide the opportunity to filter the output. The first transformer converts the fully differential output to a single ended one. The center tap is connected to Vdd, and the 50Ohm input impedance of the spectrum analyzer is reflected through the transformer so the outputs see 25Ohms to V_{dd} at the center tap.

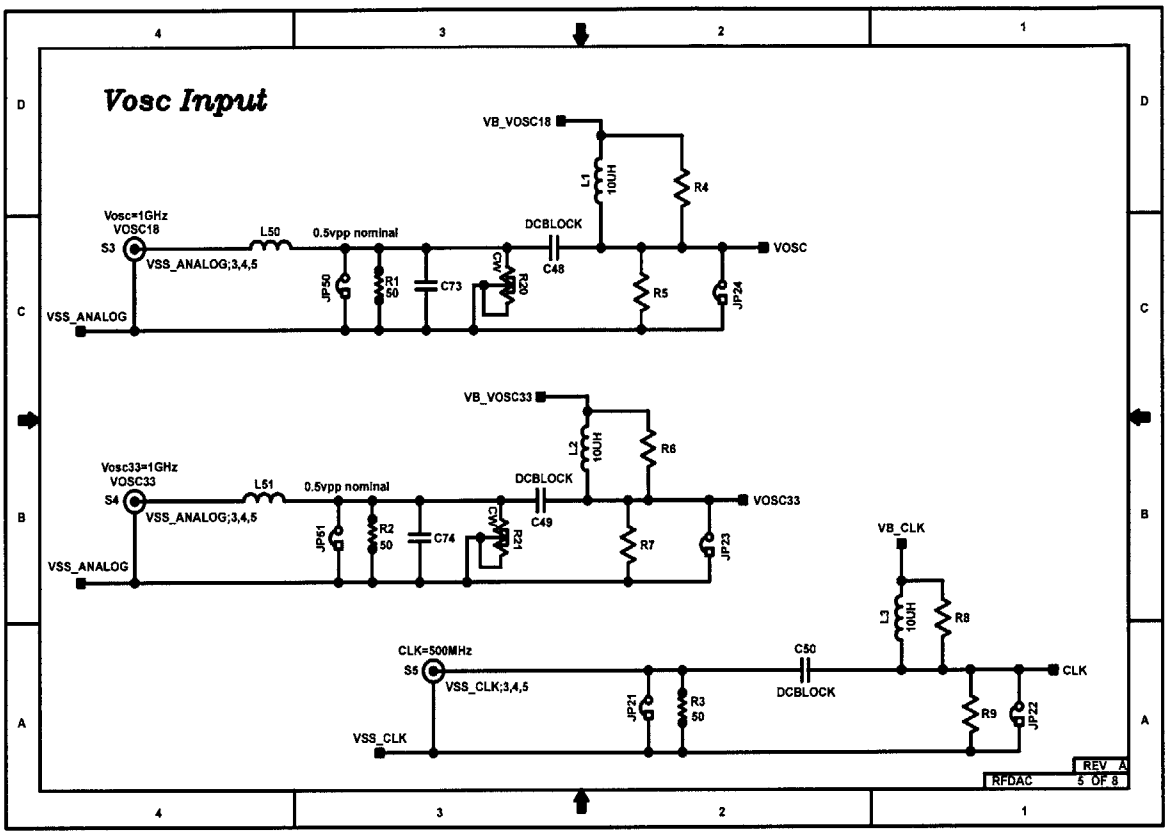

Figure 4-29: Schematic of the gate bias inputs for the 1.8V DAC and 3.3V DAC. The clock bias circuitry is also shown.

[1]Special thanks to Greg Proehl from Coilcraft for making these parts!!

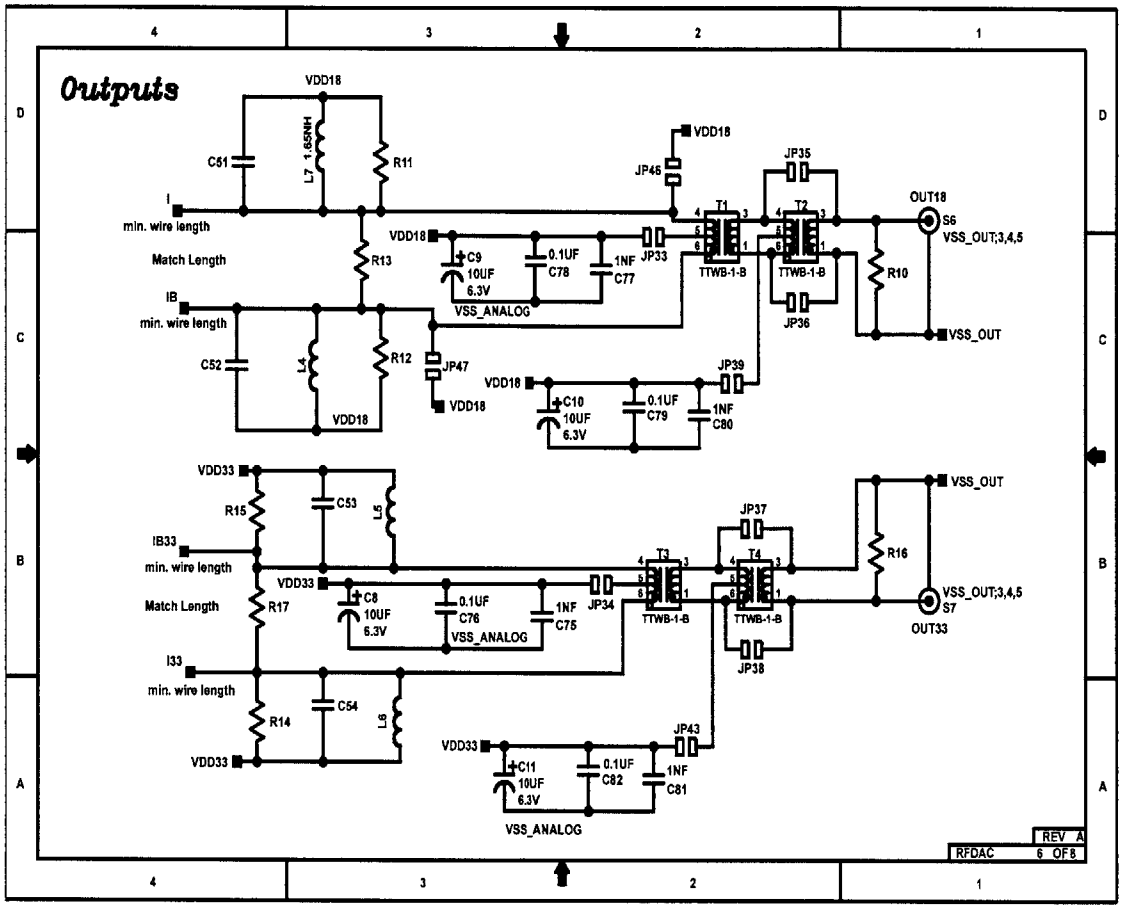

Figure 4-30: Schematic of the outputs on the board.

The transformers used were special Coilcraft 'TTWB' solder mount parts specially tuned to high frequencies[1]. The lower 3dB bandwidth was around 3 MHz and the upper 3dB bandwidth around 1GHz. Total insertion loss in the middle of the band was specified at around -1.8dB. The transformer has an unknown parasitic capacitance between the primary and secondary. This capacitance can couple the single-ended output signal unequally to one side of the fully differential output. A second transformer footprint was included to provide the option of reducing this unequal coupling. The routing on the current outputs was minimized and the transformers placed as close as possible to the test chip. The edges of the traces were rounded to prevent stray high frequency electric fields.

5 Measurement Results

The prototype RF DAC was measured for both DC and AC performance. Although only AC performance matters in communications systems, measuring the DC performance can help characterize the 0.18μm CMOS technology mismatch performance. Note, however, that the DC mismatch measurements are best case for RF DAC since they do not include the higher frequency capacitive mismatches that are present when RF DAC is operated at its full 1GHz speed.

All 26 chips returned were found to be functional at DC. The DC measurements were performed with the parts in connected to the PC board through an S-lead socket. High frequency measurements were performed with a part that had been soldered directly to the PC board.

5.1 DC Results

DC measurements of the DAC were taken using an HP 3458A digital volt meter (DVM). One side of the DAC was terminated to V_{dd} via a 200Ω resistor, while the other side of the DAC was connected directly to V_{dd}, as shown in Figure 5-1. Using this large resistor helped ensure a large enough voltage swing that the voltage measurements are larger than the noise of the DVM.

Two DC measurements were performed. First, one single bit in the middle of the array was turned on and its gate voltage was swept over a large range to determine the I-V characteristic of the current source device MN1. During the second test, the current in each element was measured for a shorter sweep of gate voltages to determine the matching across the array. Since RF DAC in normal operation has a varying V_{gs}, matching is measured versus V_{gs}. These measurements were taken for all 26 chips.

Note that RF DAC was laid out in a row, using no common-centroid or array techniques. It is expected that the matching will be worse than common centroid layout structures predict. How-

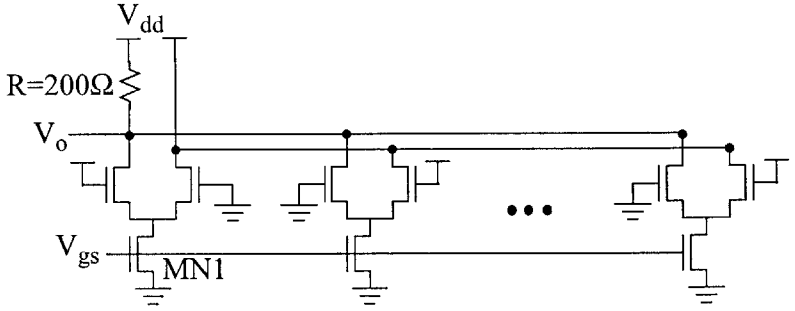

Figure 5-1: DC testing configuration

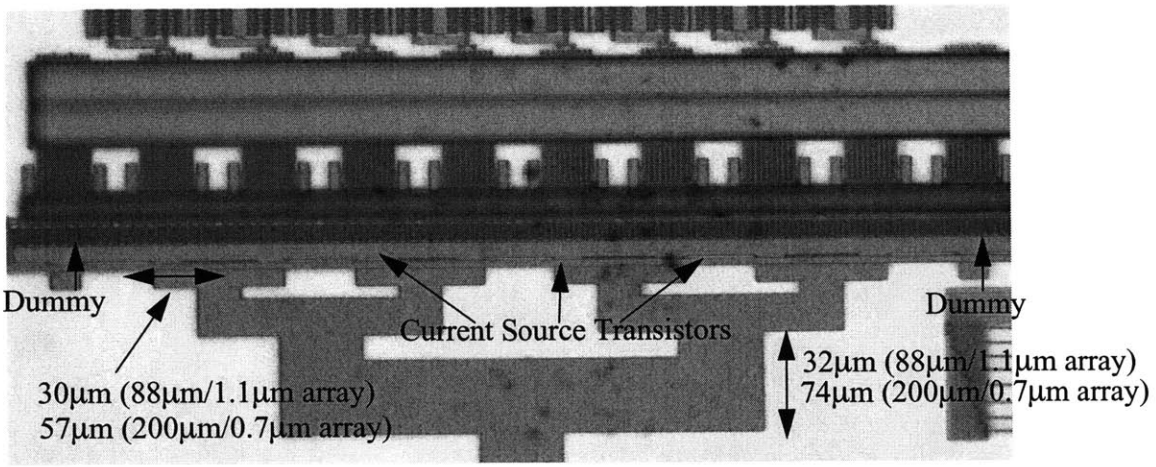

Figure 5-2: RF DAC unit element layout. Transistors are in a row with dummies on the end. No common centroid techniques were used.

ever there are dummies on each end of the RF DAC array, equal in size to the current sources in the array. The 1.8V version of RF DAC has current source transistor sizes of 88μm/1.1μm (18 stripes per transistor) and the 3.3V version has current source transistor sizes of 200μm/0.7μm (46 stripes per transistor). A die photo is shown in Figure 5-2.

5.1.1 Repeatability

The same element on the same DAC was measured 100 times. This data shows the repeatability of the measurement, which will also drift over time. The repeatability measurements were re-taken about every 7 chips throughout the course of these DC tests. The standard deviation of all the measurements is 0.28mV, which corresponds to a current of 1.43μA and a matching of 0.027%. This is significantly lower than the measured matching of 0.3-0.4%, and than the predicted matching of 0.2%. Note that if the termination resistor had been the designed 25Ω instead of 200Ω, the current repeatability would have been 11.3μA and 0.22%, close to the predicted matching.

5.1.2 Transistor Transfer Characteristics (I vs. V_{gs})

The DC value of output current I was measured by turning on one bit in the middle of the DAC array, sweeping the gate voltage V_{gs}, and measuring the output voltage. The results were averaged over all of the chips and are shown in Figure 5-3. Simulations using nominal and slow models are also shown. For comparison, an ideal square law was fit to the measurements at low voltages.

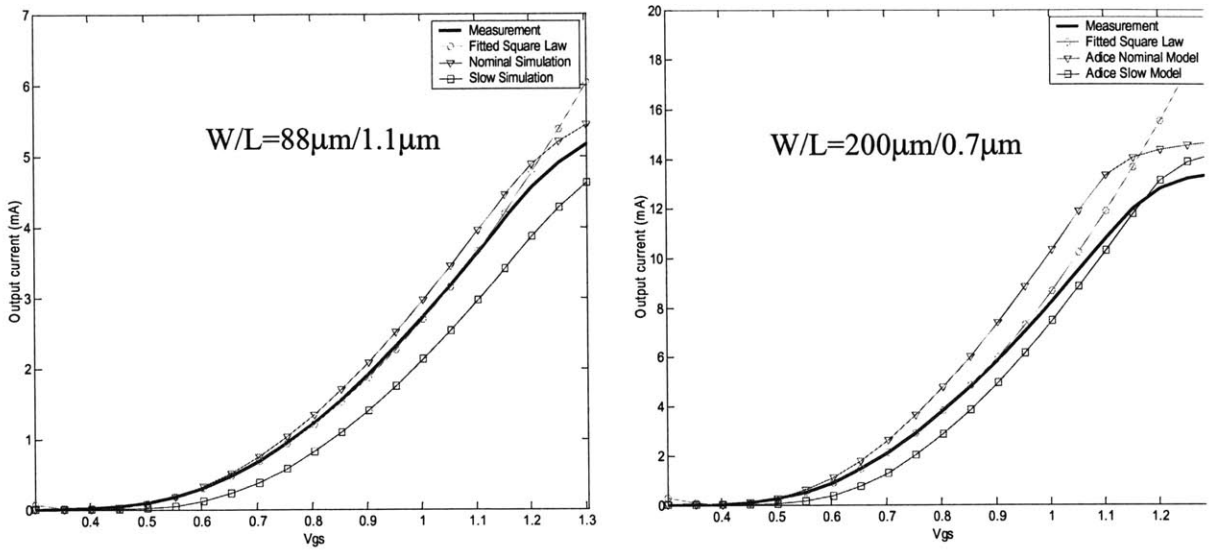

Figure 5-3: Output current as a function of gate to source voltage V_{gs}.

5.1.3 Threshold Voltage

The threshold voltage was measured by turning on each bit one at a time, sweeping the gate voltage by 0.1V increments, and measuring the output voltage. The threshold voltage can then be extracted from two adjacent data points. It is assumed that the I-V_{gs} characteristic follows a square law:

$$I = \beta(V_{gs} - V_t)^2 \tag{5.1}$$

Figure 5-3 shows that the square law is a good approximation up to about 1V for the 88μm/1.1μm device and up to about 0.9V for the 200μm/0.7μm device. The mean value of the threshold voltage is shown in Figure 5-4. The threshold voltage values are extracted from different values of the gate voltage, and are therefore plotted as a function of the gate voltage. Also shown in Figure 5-4 is a comparison to the expected threshold voltage over process variations.

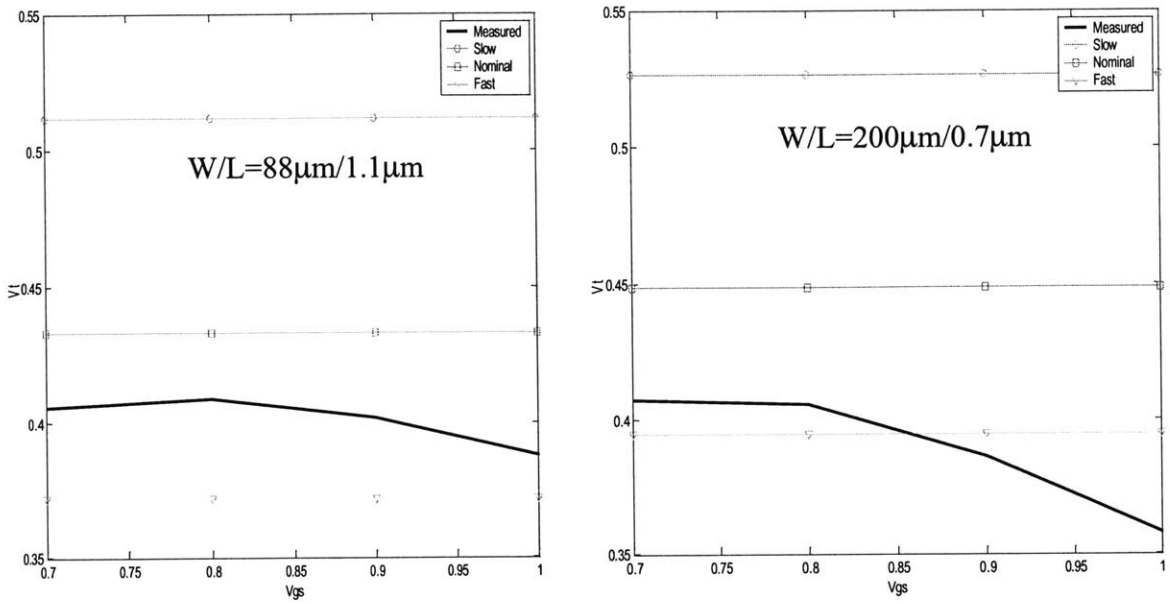

Figure 5-4: Threshold voltage extracted from I-V_{gs} measurements as a function V_{gs}. Alsc shown are the simulated values for slow, nominal and fast process variations.

5.1.4 Matching

The threshold voltage was extracted for every element of the array and for every V_{gs} value. The mean for each chip was subtracted to give the threshold voltage variation in each element. The variations were collected for all of the chips and the standard deviation was taken to give σ_{vt}. The results are shown in Figure 5-5.Note that the 200μm/0.7μm device deviates from a square law as V_{gs} goes above 0.9V and the extracted V_t becomes inaccurate.

Substituting variations in β and V_t in Equation 5.1 gives

$$\frac{\Delta I}{I} = -\frac{2\Delta V_t}{V_{gs} - V_t} + \Delta\beta \tag{5.2}$$

Variations in threshold voltage ΔV_t have already been calculated and nominal variations in current ΔI/I can also be calculated directly from measurements. These can be used to extract Δβ, as plotted in Figure 5-6. The value of Δβ is larger for the 88μm/1.1μm device. This may be due to the fact that the 200μm/0.7μm device has 46 stripes, whereas the 88μm/1.1μm device only has 18

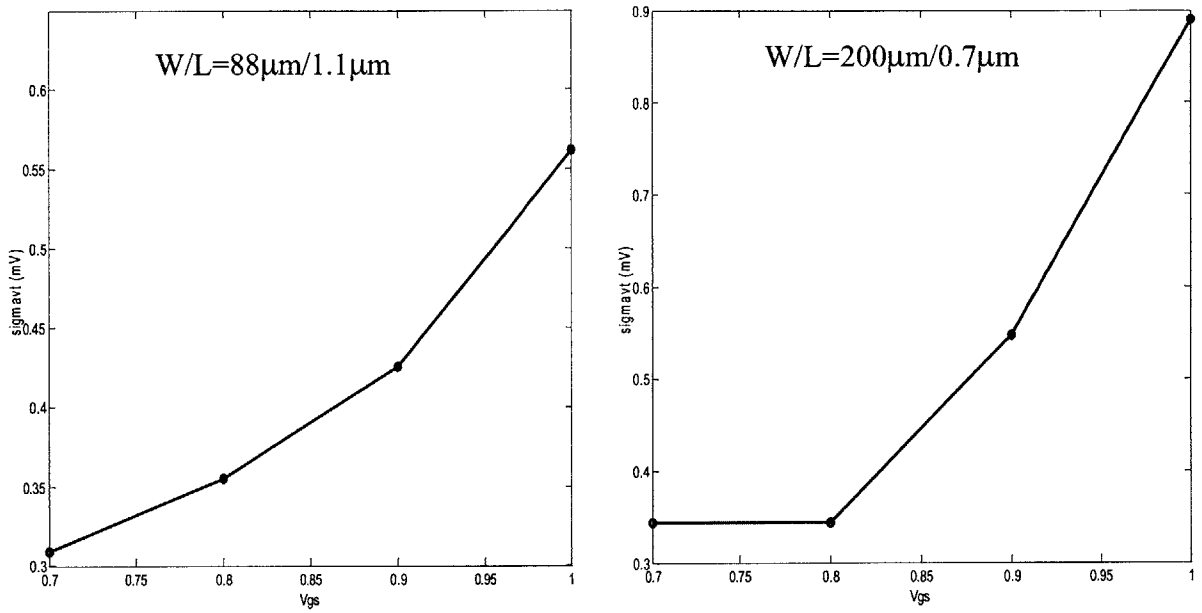

Figure 5-5: Standard deviation of threshold voltage variation, plotted as a function of V_{gs}.

stripes. Furthermore, the dummies on the ends of the arrays are the same size as one current source transistor. The relatively large values of $\Delta\beta$ could also be due to the lack of a common centroid layout scheme.

The measured total current matching is plotted in Figure 5-7 versus V_{gs}. The large β variation in the 88μm/1.1μm device causes the large deviation from the predicted current matching.

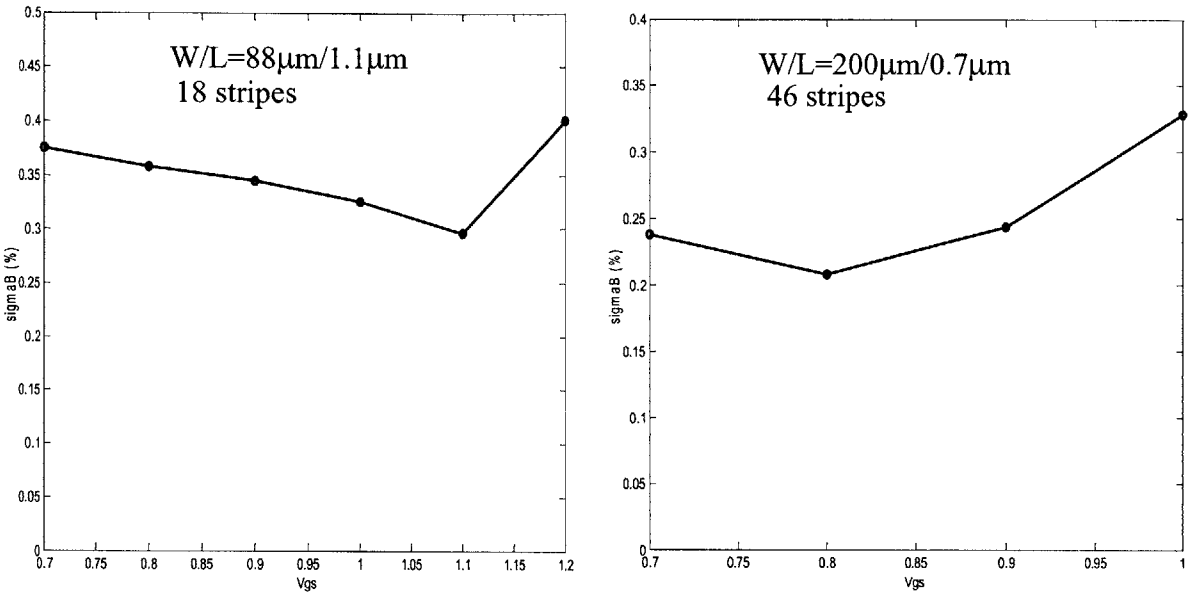

Figure 5-6: β variation versus V_{gs} (i.e. the point at which β is extracted).

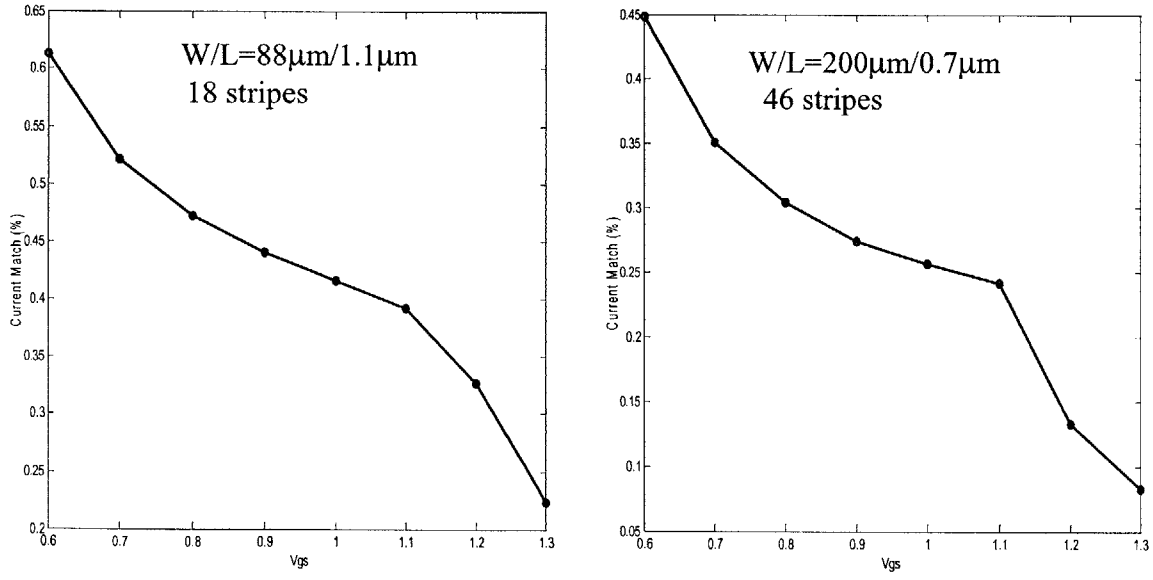

Figure 5-7: Total current matching as a function of V_{gs}.

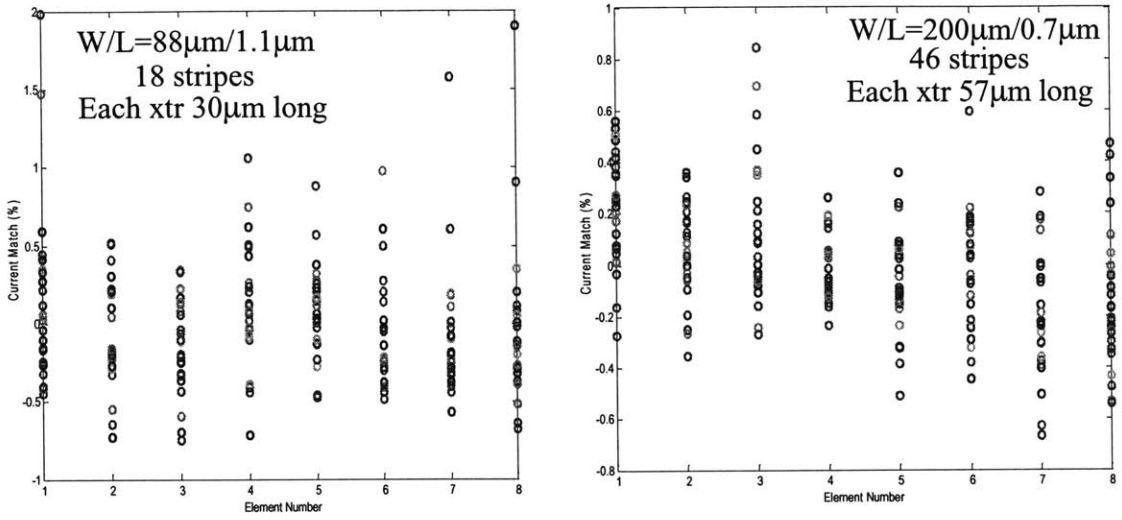

Figure 5-8: Current matching versus element number for 26 chips.

5.1.5 Edge Effects

In the course of processing the data, it was noticed that there were 'edge' effects for the smaller device. The transistors at the edges of the current source array were observed to have worse matching than those in the middle. The total current matching for all of the chips versus element number is shown in Figure 5-8. The 88μm/1.1μm device has a few chips that are matched very poorly at the end points. The 200μm/0.7μm device appears to have a gradient, since the current matching changes from one side of the array to the other.

The mean and standard deviation of Figure 5-8 are plotted in Figure 5-9 to show the 'edge' effect. The 200μm/0.7μm device does not have the edge effects, but it does appear to have a gradient, which is apparent in the mean of the current mismatch versus element number. The 200μm/0.7μm array is 570μm long, compared to 300μm in length for the 88μm/1.1μm array. Therefore gradient effects are expected to be more prominent in the larger 200μm/0.7μm array.

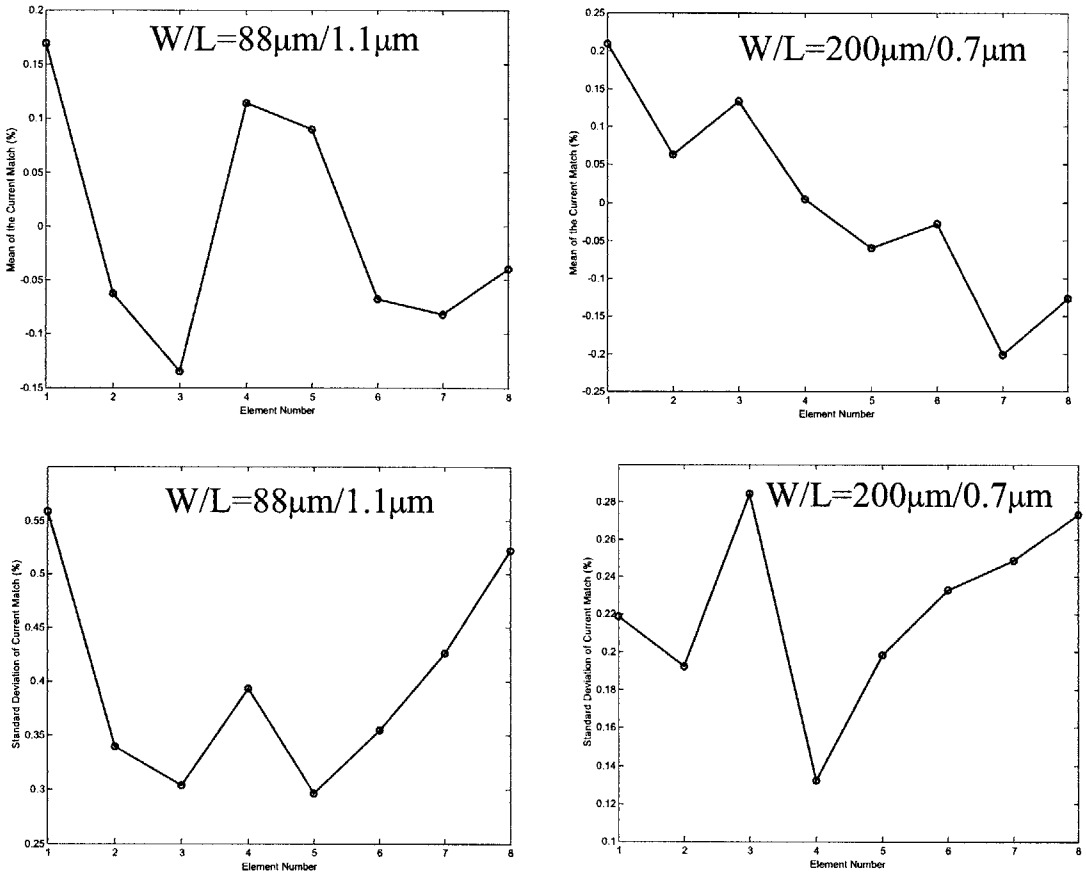

Figure 5-9: Mean and standard deviation of the current matching as a function of element number.

5.1.6 Summary of Matching Results

Matching results are summarized in Table 5-1. The matching values are extracted from the previous plots at V_{gs}=1V for the 88μm/1.1μm device and V_{gs}=0.9V for the 200μm/0.7μm device. The devices were designed to run at a peak V_{gs}=1V. However, above 0.9V the 200μm/0.7μm device characteristic starts to deviate from the square law approximation used for the matching calculations. Thus V_{gs}=0.9V was chosen to compare the matching data for the 200μm/0.7μm device.

Parameter	88μm/ 1.1μm 18 stripes	200μm/ 0.7μm 46 stripes
σ_{Vt}	0.56mV	0.55mV
σ_B	0.33%	0.24%
Current Error	0.42%	0.27%

Table 5-1: Summary of measured matching parameters. Values are extracted at V_{gs}=1V for the 88μm/1.1μm device and at V_{gs}=0.9V for the 200μm/0.7μm device.

5.2 AC Results

The AC measurements in this chapter are taken for one chip which was soldered to a board, although all chips were shown functional from the DC testing. Unfortunately, the soldered chip was not measured first for DC matching. Thus the exact DC matching characteristics of this chip are unknown. The board is configured initially with one transformer connected to the output to convert the differential DAC output to a single-ended signal.

5.2.1 Test Setup

The laboratory setup for measuring the AC performance of RF DAC is shown in Figure 5-10. The DG2020 pattern generator has the ability to output 36 bits at adjustable voltage levels up to a speed of 220MHz. The AWG420 has the same number of bits and speed, but the voltage levels are a constant 3.3V and cannot be changed. When testing with the AWG, extra termination resistors were added to the inputs of the board to reduce voltage levels, to a nominal 0-1.8V. The data switching clock f_{clk} is provided by a Rhode & Schwartz SML signal generator, while the oscillating control waveform is provided by the HP 8644B signal generator. The generators are phase locked by connecting a 10MHz reference in the back of the instruments. The phase between the waveforms can be adjusted manually on the Rhode & Schwartz SML. Although the exact phase between the oscillating DAC current and the data switching instants on the chip cannot be measured, the phase can be visually adjusted by observing the output waveform amplitude and the noise floor on the spectrum analyzer.

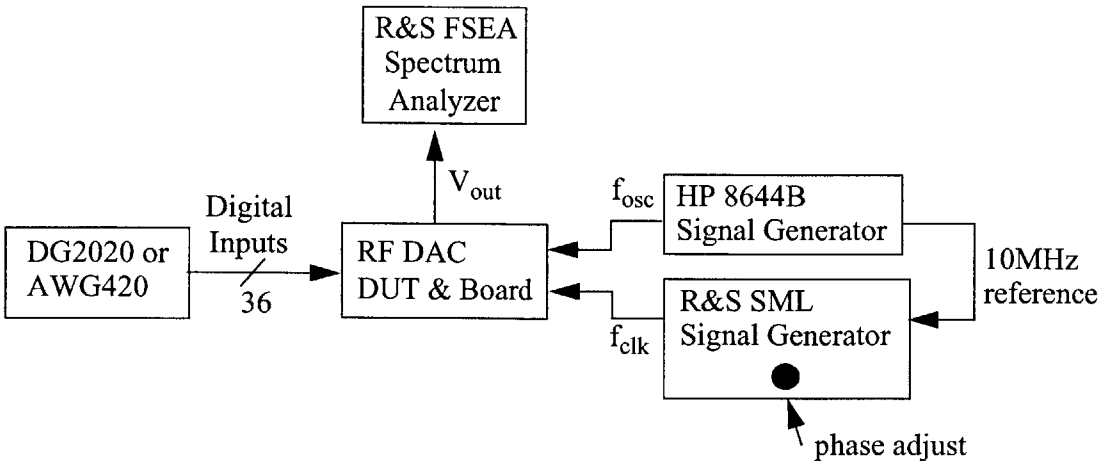

Figure 5-10: Lab test setup for AC measurements.

5.2.2 Spectrum and Overall Functionality

The RF DAC testchip is fully functional and can be tested up to speeds of f_{clk}=880MHz, limited by the $f_{clk}/4$=220MHz input pattern generator data rate. The only functionality that can not be directly tested is whether or not the dummy data is actually switching correctly. However, the switch driver supply current is measured and found to have the expected almost two-fold increase when the dummy data scheme described in Chapter 4.4.5 is operating. The current increase is expected to be slightly lower than a factor of two since the dummy data path switch drivers do not have any load.

One unexpected result is the appearance of the multiplexer clock in the output spectrum. The chip outputs the multiplexer's $f_{clk}/4$ signal to trigger the input data. This means that there is a large on-chip driver to drive the clock to the output pad, pin, and buffer. The strong $f_{clk}/4$ signal is likely coupled to the output either through the chip substrate or the PC board ground. Since the multiplexer needs a clock at $f_{clk}/4$, it appeared in the output spectrum and mixed with the input tone. Thus the $f_{clk}/4$ planned center frequency has to be abandoned for an $f_{clk}/6$ input center frequency.

The complete output spectrum for the DAC with a constant bias voltage in drive-direct mode (i.e. no multiplexer) is shown in Figure 5-11. The DAC is being clocked at f_{clk}=100MHz in the top spectrum, and at f_{clk}=514MHz in the bottom spectrum. Both plots compare the DAC with a constant gate bias and with the gate oscillating. The primary or low frequency tones are visually aligned to give the same amplitude with and without the gate oscillating. The amplitudes of the output images follow the predicted sin(x)/x behavior for the DAC without the gate oscillating, but

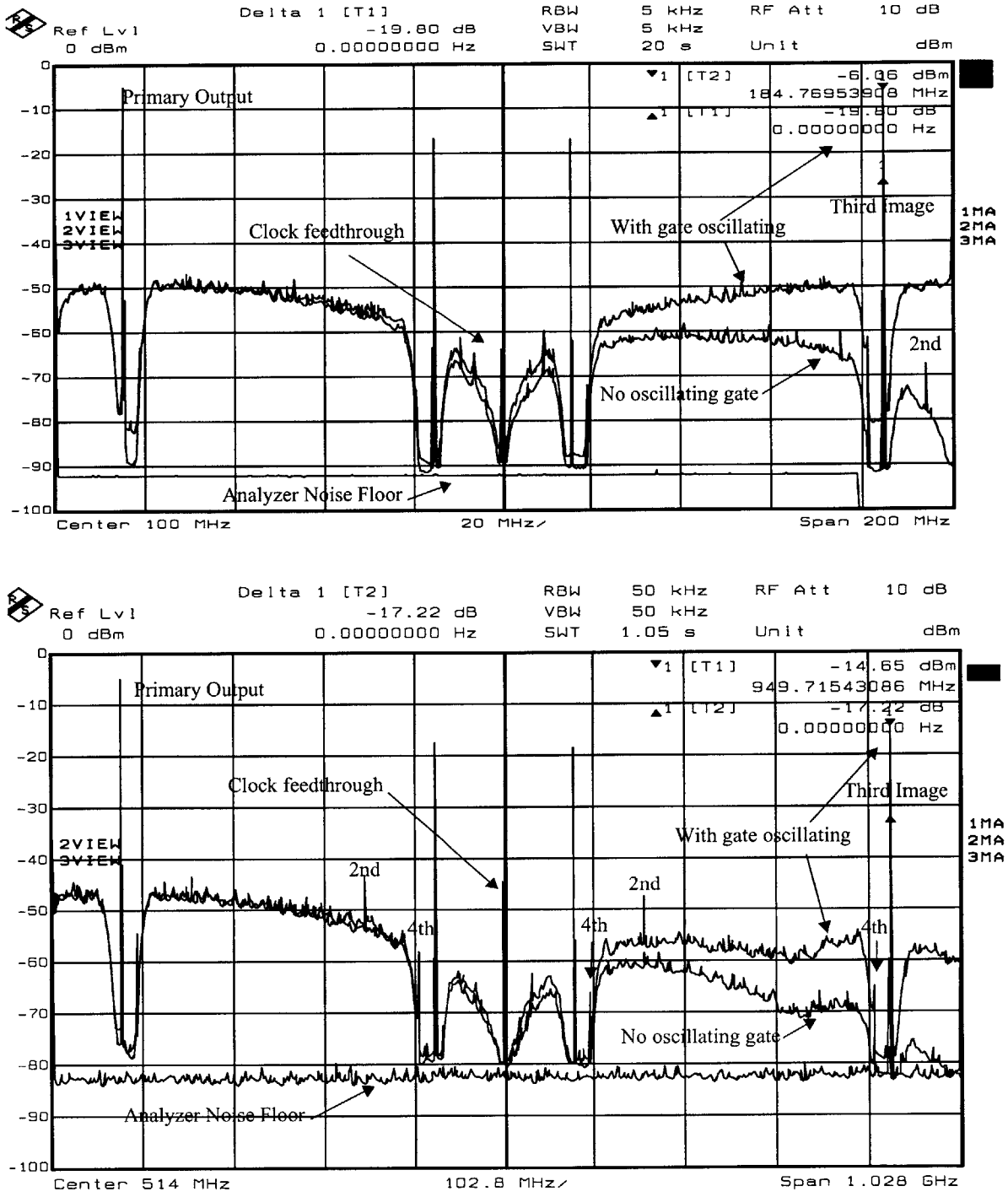

Figure 5-11: Total output spectras for the 8-element sigma-delta DAC. The clock speed is 100MHz for the top spectrum and 514MHz for the bottom spectrum. The input is centered around $f_{clk}/6$.

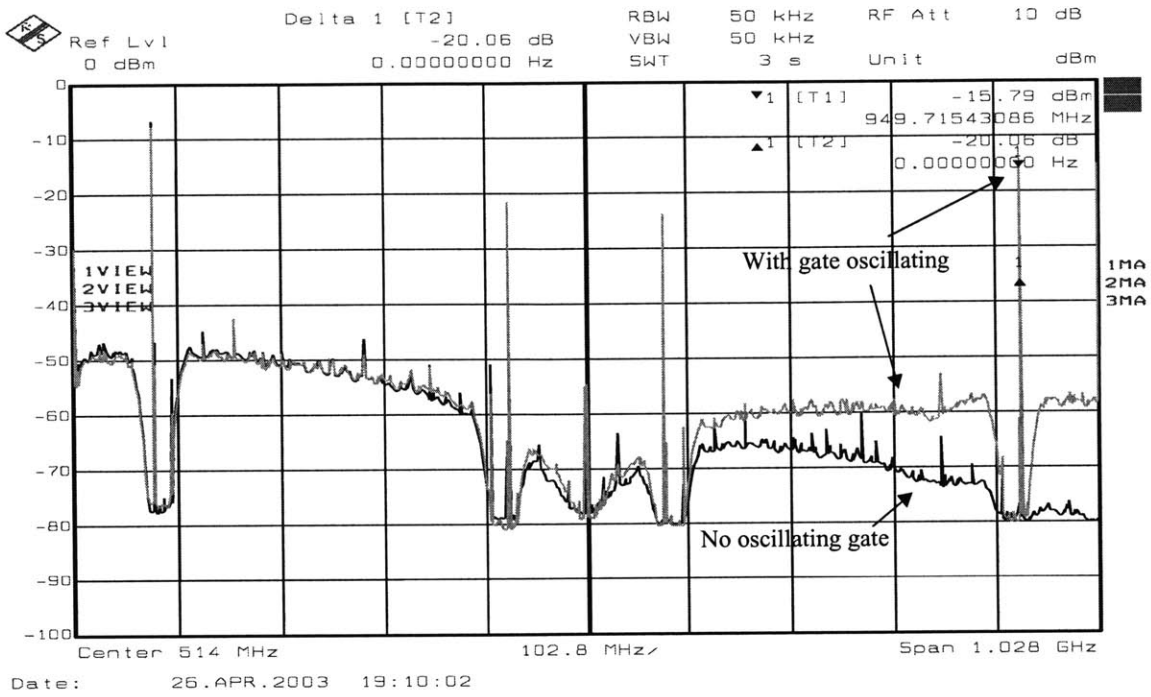

Figure 5-12: Output spectrum with extra transformer added in the output path.

the amplitude of the third image is boosted in the oscillating DAC case due to the high frequency, high energy impulse response lobe. The relative amplitudes of the primary and third image outputs are determined by the level of the DC bias and by the amplitude of the oscillating waveform. As frequency increases, more of the oscillating waveform amplitude is lost in the input circuit on the board. Thus, at high frequencies a larger drive amplitude must be used to obtain the same output power.

At increased clock frequencies, even-order harmonics and IM products of the input appear, as labelled in Figure 5-11. Since the DAC is differential, no even-order distortion is expected. The harmonics are believed to be due to mismatches in the differential paths. Since the harmonics appear at high frequencies, an unequal capacitive coupling is suspected. However, since special care was taken to ensure that the output paths are completely symmetrical, it is suspected that the second harmonic is due to unequal coupling of the single-ended output to one of the nodes through the transformer at the output. This is the reason for the inclusion of the footprint for the second transformer. When added, the second transformer should provide increased isolation between the single-ended and differential signals.

The second transformer is added and the resulting output spectrum is shown in Figure 5-12. Although the second harmonic is slightly improved, the fourth intermodulation product is worse. When the second transformer is added, jumpers JP35 and JP36 are opened. These jumpers extend under the transformer and are close together so they actually form a capacitance between the input and the output. However, even if this capacitance is large, the harmonics should still stay about the same. Thus it appears that the unequal coupling is not dominated by the transformers, but instead by some other asymmetry in the chip layout or board routing. The insertion loss increased slightly as expected, especially at high frequencies.

Clock feedthrough is also present in the output spectrum, and is boosted at high frequencies as demonstrated in Figure 5-11. In fact, at lower gate bias levels, or lower output levels, even more feedthrough can be seen. This is shown in Figure 5-13. The top spectrum is without the multiplexer at the maximum pattern generator speed of 220MHz. Clock feedthrough at f_{clk} and second harmonic distortion are seen. The bottom spectrum is clocked at the same 220MHz rate with the multiplexer running. Clock feedthrough at both f_{clk} and $f_{clk}/4$ can be seen, as well as the mixing of $f_{clk}/4$ with the inputs. Note that for such low output amplitudes the noise floor of the third image is limited by the noise floor of the spectrum analyzer in both cases. Figure 5-14 shows the output spectras with the clock running at 500MHz. The feedthrough and mixing effects become worse at higher frequencies.

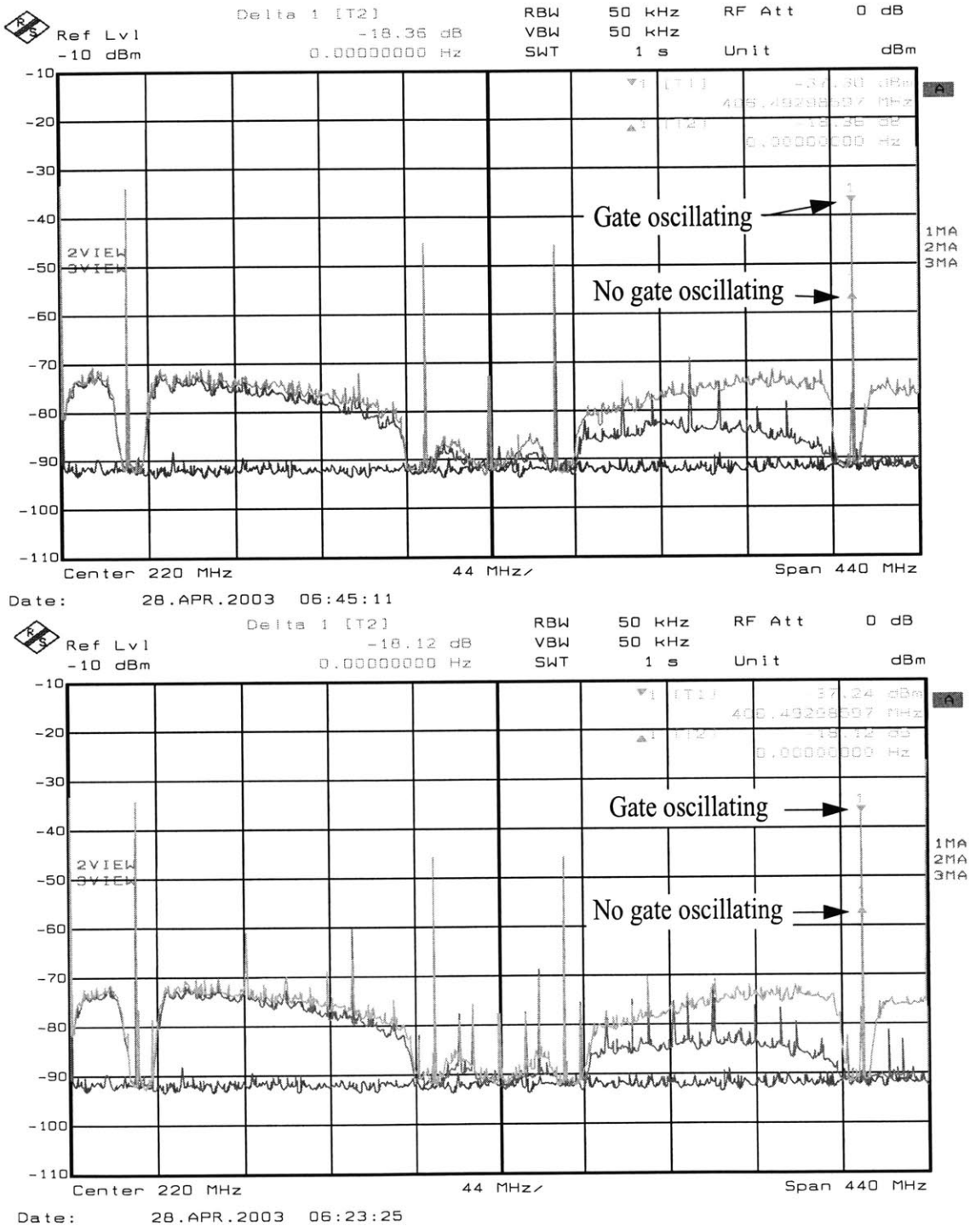

Figure 5-13: Output spectras without the multiplexer running (top) and with the multiplexer running (bottom) at low gate bias levels, i.e. low output power levels. Both spectrums are for f_{clk}=220MHz.

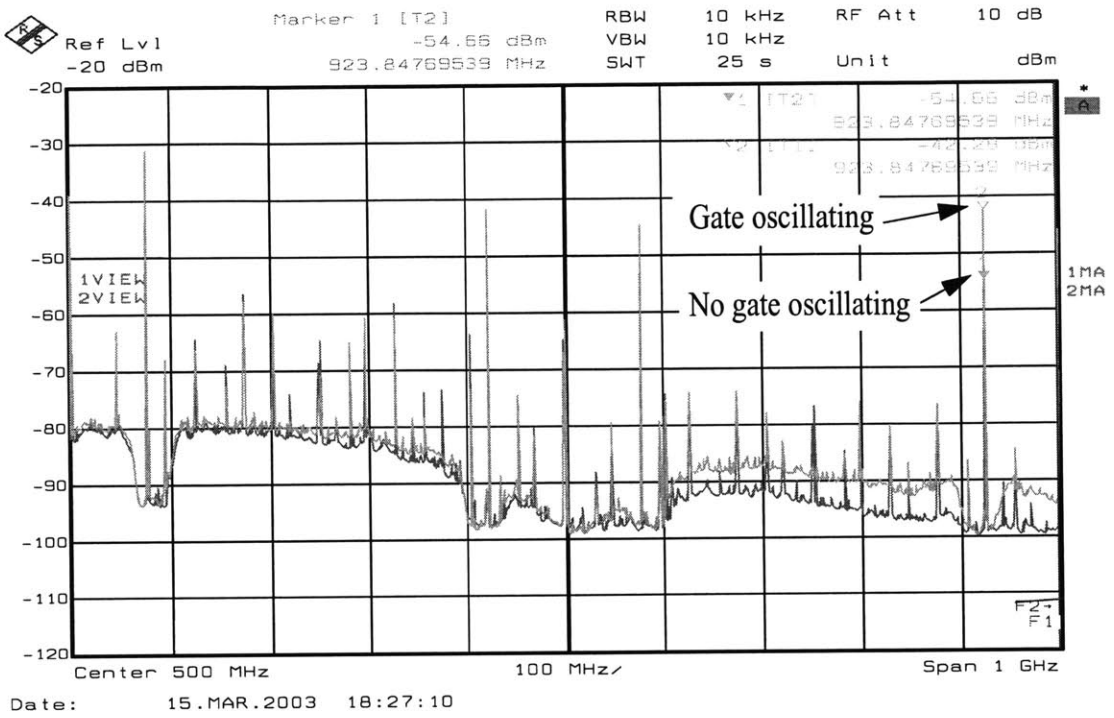

Figure 5-14: Output spectras with the multiplexer running. The clock frequency is 500MHz.

5.2.3 Single-Tone Performance

A single input tone centered around $f_{clk}/6$ is used to measure the SNR performance of RF DAC. As a first step, the SNR of the DAC running at f_{clk}=30MHz with a constant 0.9V gate bias voltage is measured. This places the output tone at around 5MHz, just above the 3dB bandwidth of the transformer. The best measurement results compared with MATLAB simulation are shown in Table 5-2. Since the DC matching of the chip is unknown, the SNR is compared to simulations with both 0.42% and 0.6% mismatching.

Table 5-2: DAC SNR with constant gate bias, f_{clk}=30MHz.

Output tone, Type of input vector	**Expected low frequency SNR with 0.42% mismatch**	**Expected low frequency SNR with 0.6% mismatch**	**SNR limit due to analyzer noise floor (also depends on output amplitude)**	**Measured SNR**
Primary Output, Normal	71.46dB	68.9dB	81.6dB	67.65dB
Primary Output, Mismatch Shaping	76.24dB	76.2dB	81.6dB	69.66dB
Primary Output, Modified Mismatch Shaping	75.08dB	73.43dB	81.6dB	70.26dB
Third Image (@ 55MHz), Normal	71.46dB	68.9dB	63.5dB	61dB

The slight improvement in the measurements with mismatch shaping indicates that a little of the SNR degradation is due to mismatch. The SNR improves slightly with modified mismatch shaping, so some of the degradation may also be due to noise injected during switching. However, there is still at least a few dB discrepancy in the SNR measurements. The sources of possible SNR degradation are described in the following section.

5.2.3.1 Sources of SNR Degradation

A few possible sources of SNR degradation are listed in Table 5-3. For large output amplitudes, all of the predicted noises of Table 5-3 are smaller than the measured noise.

Overloading the front end of the spectrum analyzer with large tones could also cause the front end to saturate and produce inband noise. These tones could be either the large inband signal or the image tones out of band. Bandpass and notch filters have been used to notch the tones, but the SNR remains the same, indicating that this is not the source of noise.

Table 5-3: A few possible sources of SNR degradation

Source	**Simulated/Estimated value**
Thermal noise of output resistors	-164dBm/$\sqrt{Hz}$
Thermal noise of resistor biasing the gate node	-164dBm/$\sqrt{Hz}$
Thermal & 1/f noise of the DAC core transistors	-172dBm/$\sqrt{Hz}$
Noise of the spectrum analyzer	-150dBm/$\sqrt{Hz}$ to -160dBm/$\sqrt{Hz}$, depending on the analyzer used

An experiment was conducted with the DAC chopping between all zeros and all ones. This is performed at half the clock rate, and the output tone is observed. The results are plotted for different gate bias voltages in Figure 5-15. As the gate bias (and therefore the current through the transistors) increases, flicker noise near the carrier increases, as does the wideband noise. Theoretically, the thermal noise should be below these levels, however the scaling of noise with the current does indicate flicker and thermal noise.

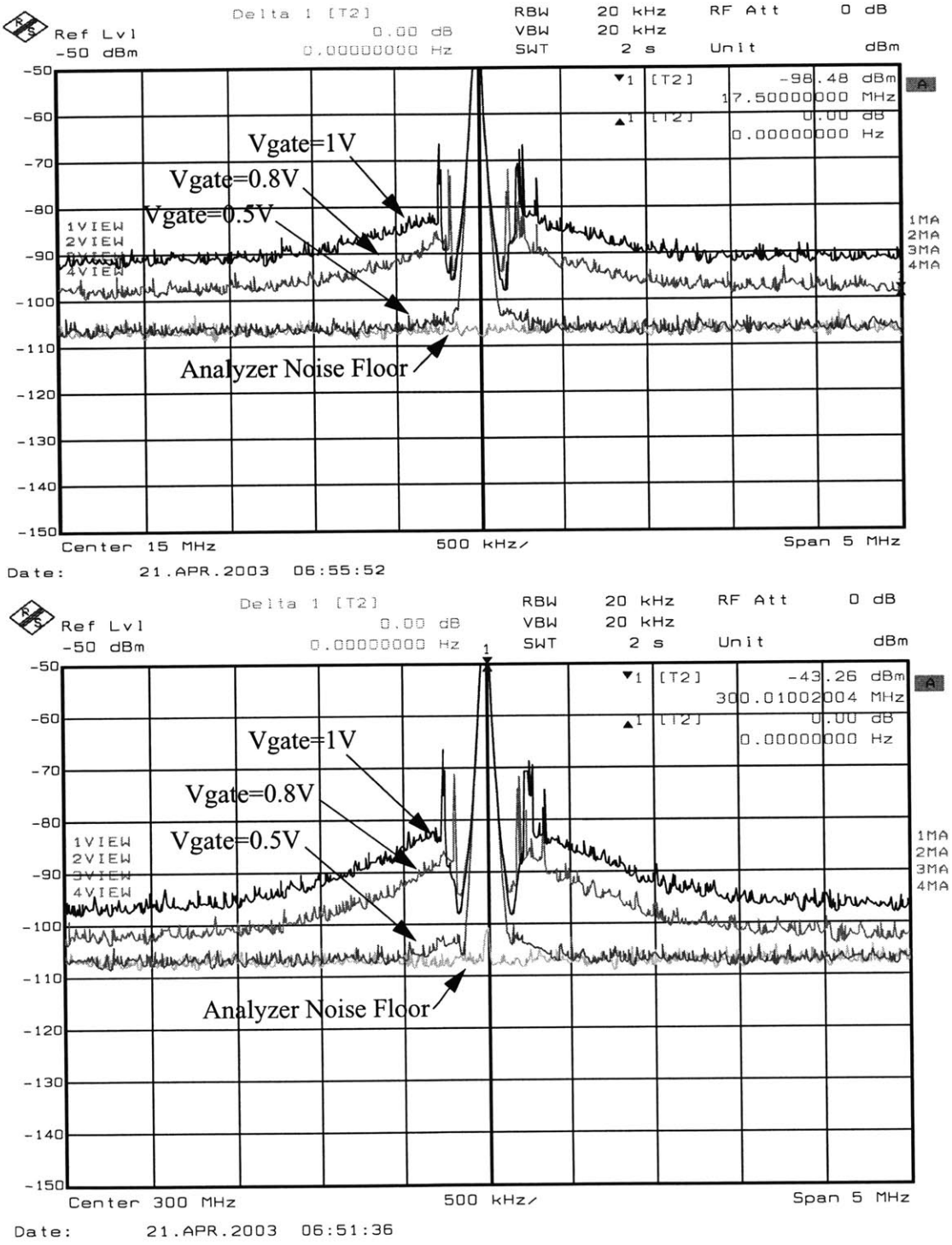

Figure 5-15: Output spectras for the DAC configured to chop between all zeros and all ones at half the clock rate. Shown are traces for different constant DC bias levels. The top plot is for f_{clk}=30MHz and the bottom plot is for f_{clk}=600MHz.

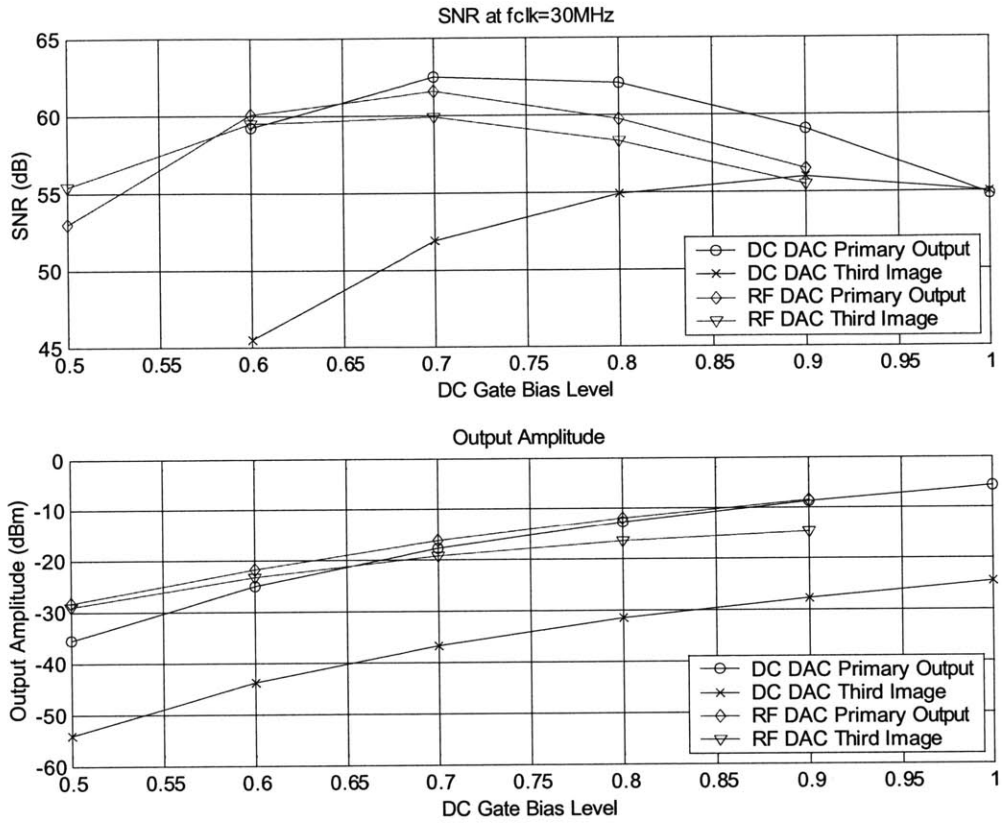

Figure 5-16: Plot of SNR as a function of DC gate bias voltage for the DAC running at f_{clk}=30MHz. The primary output is centered at 5.12MHz, and the third image is centered at 54.93MHz. The bandwidth is 1MHz for both measurements. The bottom plot shows the amplitude increase with gate bias voltage.

A plot of the SNR versus DC gate bias level is shown in Figure 5-16 for both the primary output at 5.12MHz and the third image at 54.93MHz. Shown on the bottom is the amplitude of the output tone at both frequencies. As expected, the amplitude of the output increases with DC gate bias, since the current through the transistors increases. However, the SNR ideally should be limited by quantization noise and should not vary with the bias voltage applied to the current sources. The SNR is also lower than that predicted by Matlab. The bandwidth is 1.02MHz, so the 1/2 bandwidth used for integration is 510kHz. According to Figure 5-15, this should still be in the region where the device is dominated by 1/f noise. Figure 5-16 indicates that the noise scales roughly with the signal amplitude, keeping the SNR constant.

At higher frequencies, the SNR scales with the output amplitude as shown in Figure 5-17, where the SNR as a function of DC bias level at a f_{clk}=514MHz is depicted. The primary output is now

at 88.46MHz and the third image is at 942.5MHz. The bandwidth is 17.5MHz, so the integration bandwidth is 8.75MHz, and is chosen to be centered away from the 1/f noise near the carrier. Results are plotted for various input vectors, with and without the dummy data switching enabled. No significant differences are seen between the curves.

It turns out that the slope of the SNR is consistent with a noise proportional to $\sqrt{Vgs-Vt}$. This curve is fitted and plotted in Figure 5-17 with the measurement results. The $\sqrt{Vgs-Vt}$ dependence and wideband noise characteristic points directly to transistor thermal noise, but it is curious that this level is about 12dBm/$\sqrt{Hz}$ higher than predicted.

The bias node of the gate V_{osc} is also sensitive to noise coupling. When a decoupling capacitor is added to the bias node on JP24 to create a low pass filter, the SNR improvement is only on the order of 0.1dB. This indicates that the gate bias node is fairly insensitive to coupling on the board, at least up to the point where JP24 is on the board (i.e. about half way between where the supply comes in and the pin of the chip). The decoupling capacitor had to be removed for AC testing because it would short the AC signal. However, since the SNR with and without the capacitor was about the same, coupling onto the gate bias node does not appear to be limiting the SNR performance of the DAC.

There is also a coupling mechanism on the PC board. This is illustrated in the measurements of Figure 5-18. When the clock is turned off, there should ideally be no signal at the output. However, there is clearly some coupling of the digital inputs to the output. When the resistors connecting the digital inputs to the chip are pulled out, the inband noise drops further. This indicates that there is a coupling path on the PC board. It is only when the digital inputs are completely disconnected that no coupling is seen. When the DAC is operating, any coupling of the digital inputs to the current source would cause the mixing of the input with itself. This means out-of-band quantization noise will be aliased back in band.

Other possible sources of noise could be substrate coupling or some other type of noise coupling to the gate bias node. Switching distortion is another possibility, but this should be minimal at low frequencies and should appear as tones, not as broadband noise which was observed inband on the spectrum analyzer. Noise on the output supply voltage is another possibility.

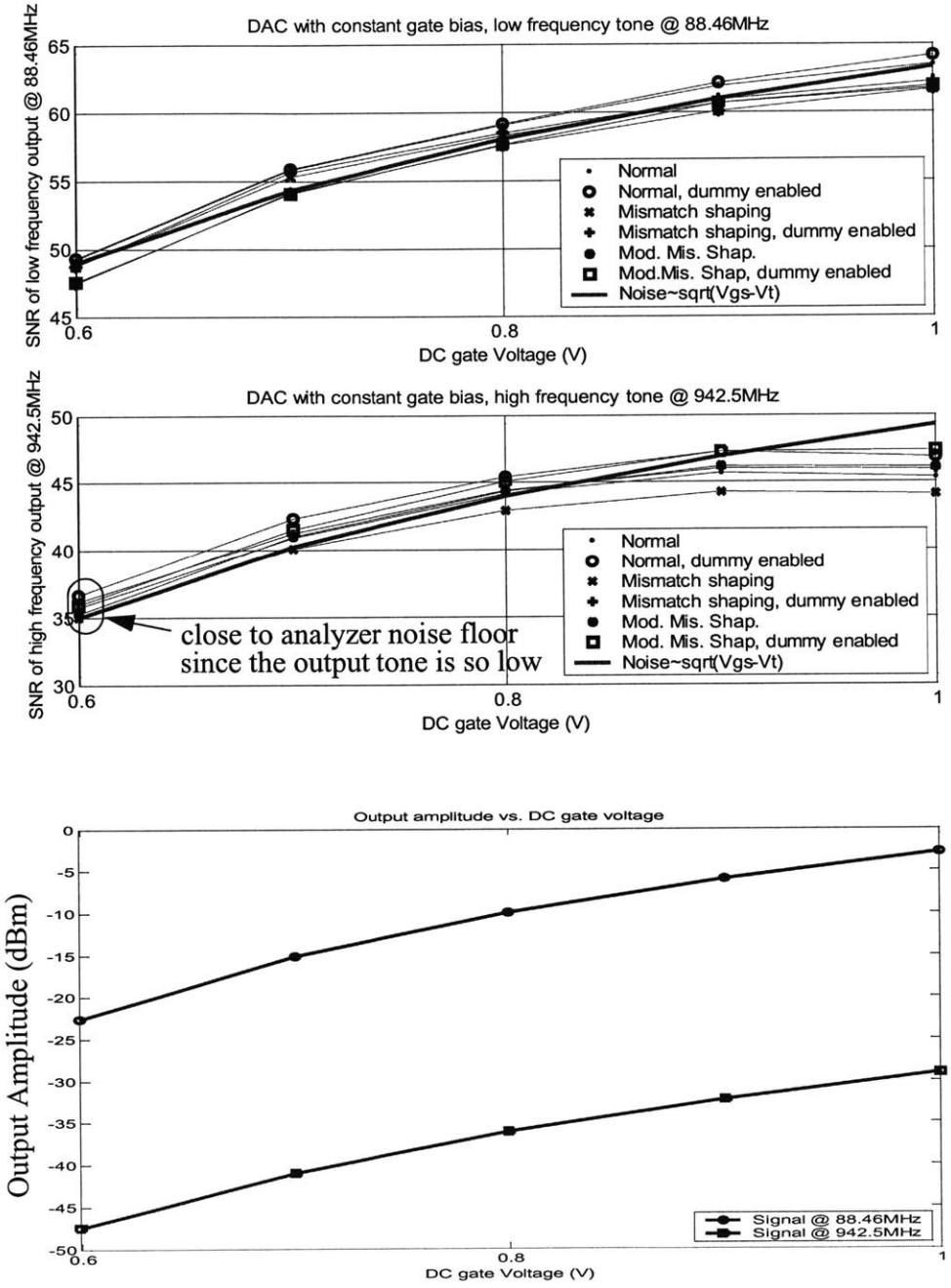

Figure 5-17: SNR versus DC bias level for the DAC with a constant gate bias. The first two plots show the primary output tone at 88.46MHz and the third image of the input at 942.5MHz. Shown in the bottom plot is the amplitude of the output tone for the two frequencies. The clock frequency f_{clk} is 514MHz.

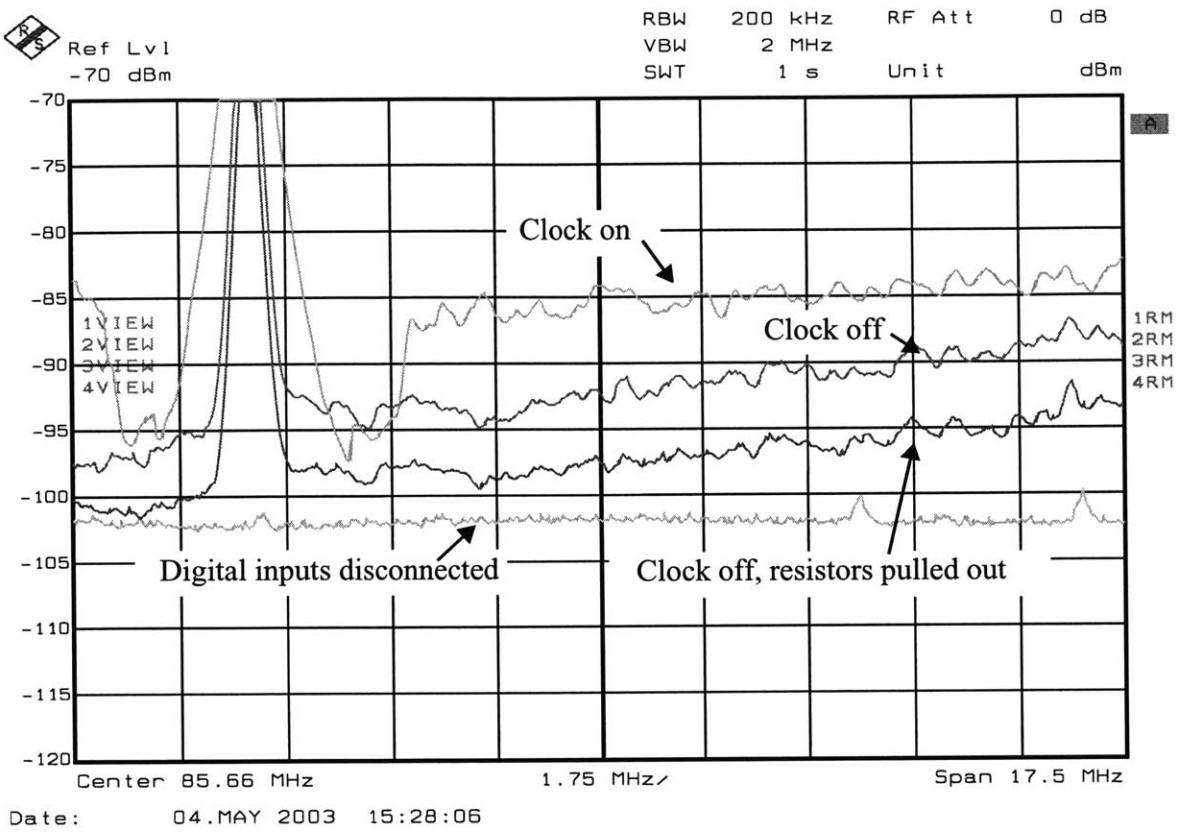

Figure 5-18: Inband primary output spectrum with the clock turned on, the clock turned off, the clock off with the resistors pulled out, and the clock off and the digital inputs disconnected.

5.2.3.2 SNR versus Frequency

The SNR of the DAC with a constant bias voltage is plotted as a function of output frequency in Figure 5-19. The SNR is compared between the DAC running with and without the multiplexer. Also plotted is the output amplitude as a function of frequency. The top two plots are for the primary output frequency, and the bottom two plots are for the third image of the output. Note the different output frequency scales in the primary and third image plots of Figure 5-19.

The amplitudes of the primary and third images are effected by the transformer lower and upper 3dB bandwidths, 5MHz and 1GHz respectively. Otherwise the amplitudes are relatively flat with frequency. The SNR is similar whether the DAC is running with or without the multiplexer. It was initially suspected that the extra digital switching when the multiplexer is running could

cause more inband noise, since Figure 5-13 indicates that it does cause more distortion tones. This is apparently not the case.

The SNR of the primary output stays relatively constant with frequency, while the SNR of the third image falls off rapidly with frequency. Ideally, the third image SNR should be the same as the primary output SNR. However, some other source of noise appears to be aliased inband and limiting the SNR of the third image.

SNR as a function of frequency for the RF DAC is shown in Figure 5-20. The SNR is practically independent of the type of vector used at the input. Although not shown in all the graphs in this chapter, many measurements were compared for different input vectors, and no significant difference was seen. As a general trend, the normal input vector had slightly ~1dB better SNR, but this was not always repeatable.

The gate bias voltage and amplitude of the oscillating waveform at the input are kept constant as a function of frequency in Figure 5-20. Due to a varying input impedance at the gate node on the board, the amount of amplitude that actually gets to the gate varies with frequency, so the output amplitudes vary with frequency. The output amplitudes are also plotted in Figure 5-20.

SNR as a function of frequency for RF DAC is also compared in Figure 5-21. In this case, either the DC bias or the amplitude of the oscillating waveform was varied to keep the third image output as constant as possible at about -21.5dBm over the entire frequency range. Although not as severe as in the DAC configured with constant gate bias, SNR still falls off with frequency.

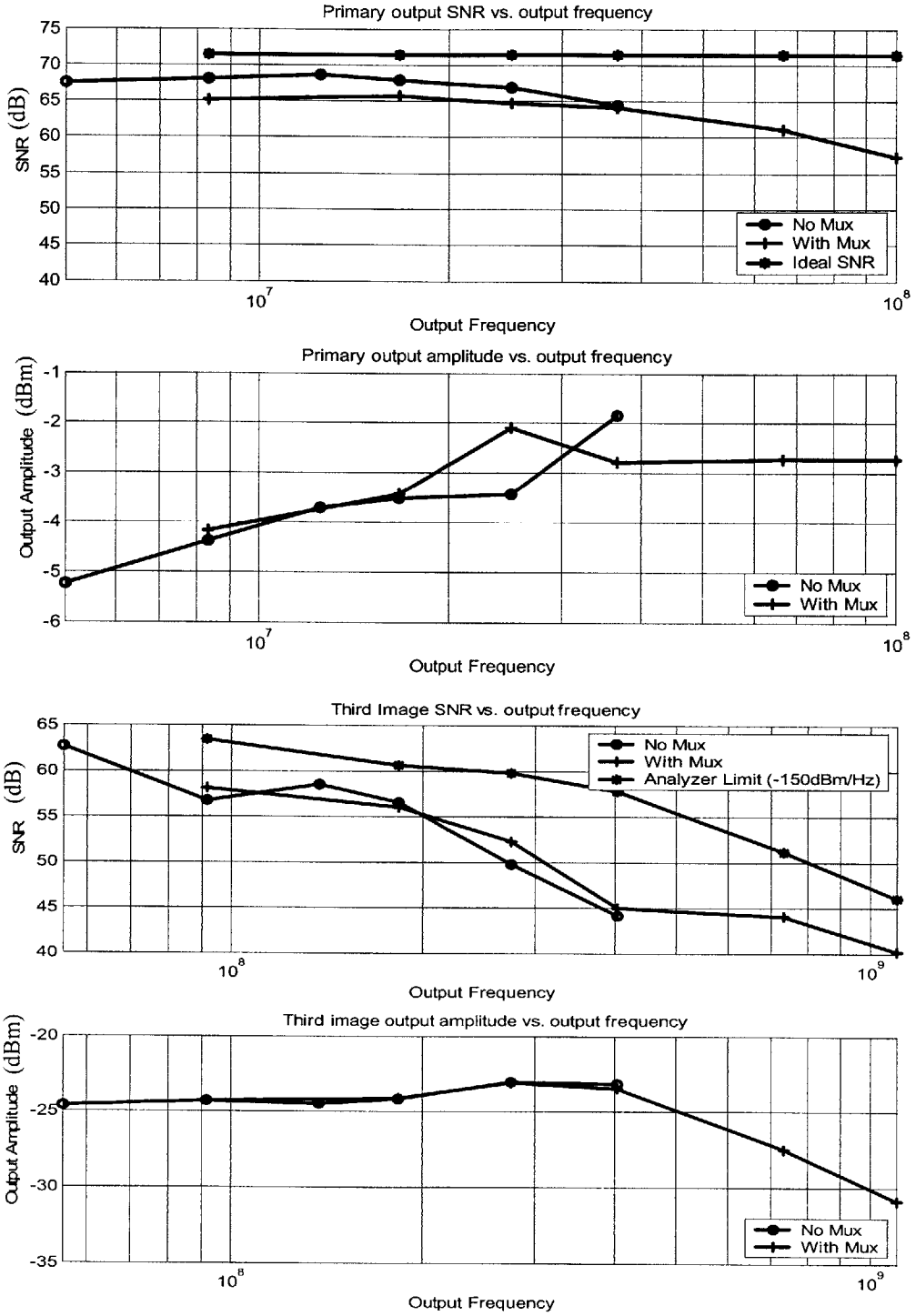

Figure 5-19: SNR as a function of output frequency for the DAC with a constant bias voltage. The SNR is compared with the DAC running with and without the mux. The SNR is shown for the primary output as well as the third image. Also shown is the output amplitude as a function of frequency.

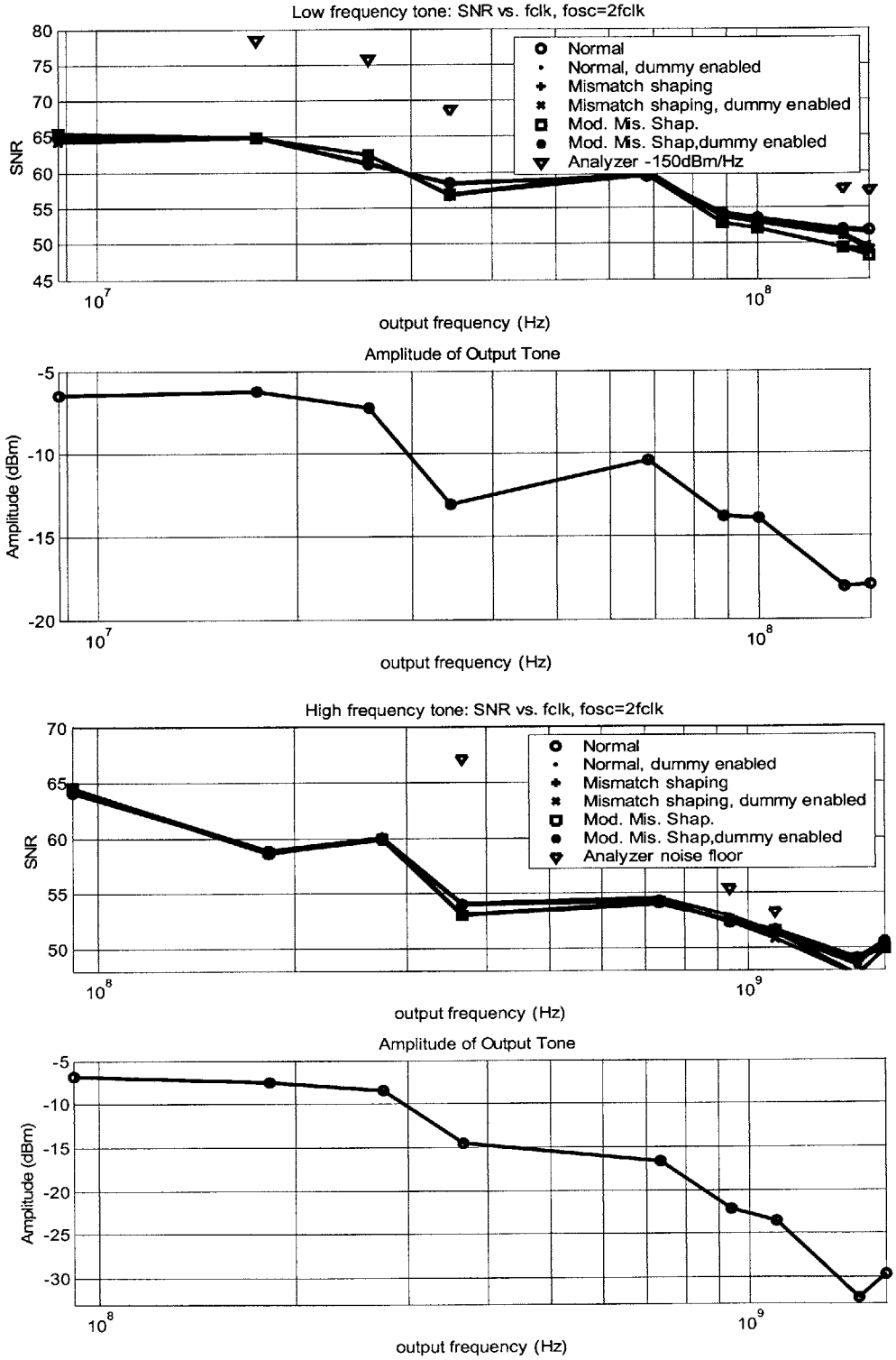

Figure 5-20: SNR as a function of output frequency for the DAC operating with an oscillating gate bias voltage.

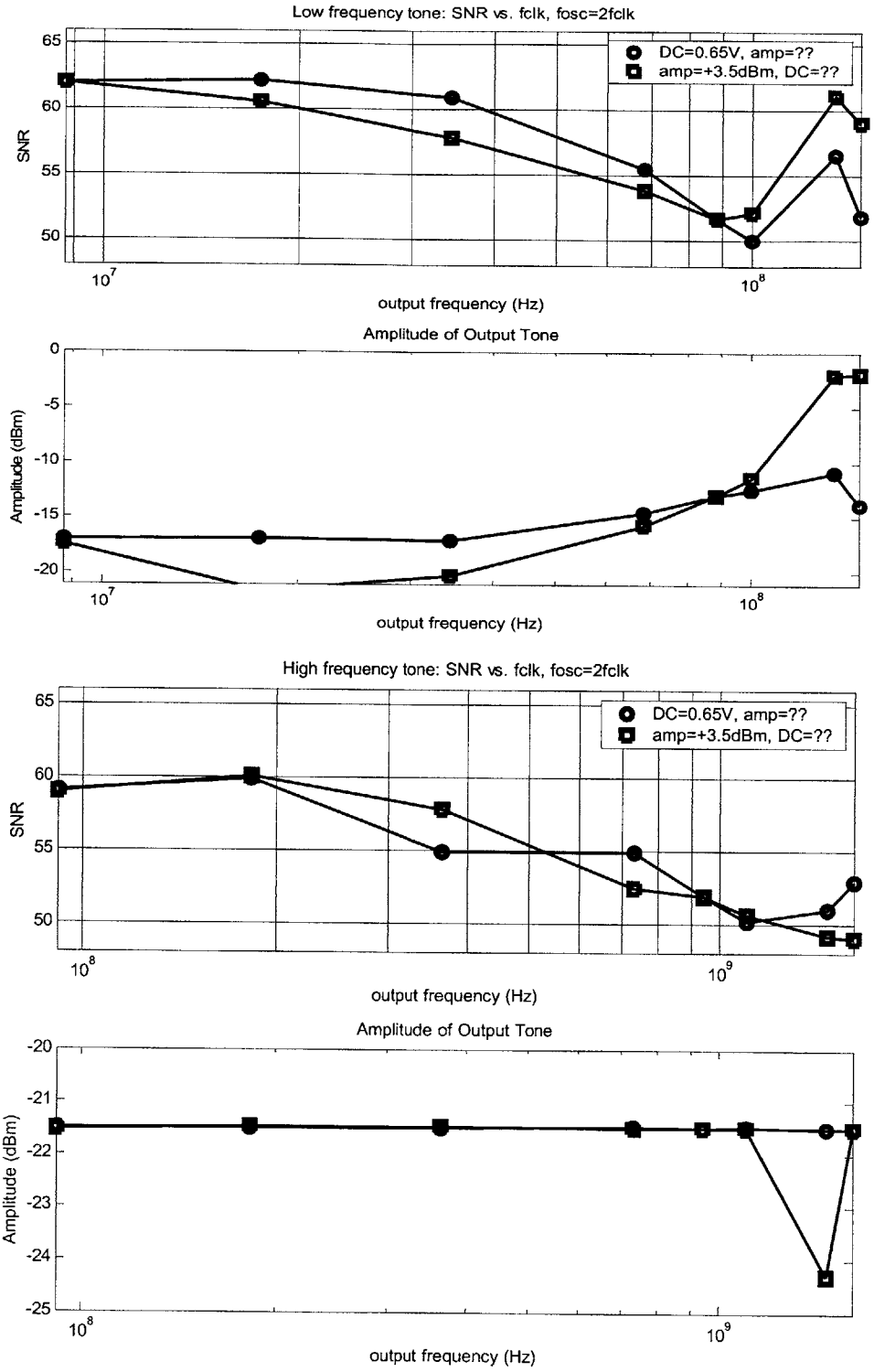

Figure 5-21: SNR as a function of output frequency for RF DAC with adjustments made in either the DC level or the amplitude of the gate bias to keep the third image output as constant as possible over the range of frequencies.

5.2.3.3 SNR versus Digital Input Amplitude

Figure 5-22 shows the ideal expected SNR as a function of the digital input amplitude, expressed in dB relative to full scale (dBFS). This graph was obtained by simulating in MATLAB. As the digital input is increased by approximately 10dB, the output amplitude also increases by about 10dB. Since the sigma-delta is only stable up to a maximum full scale of about -1dB relative to full scale (dBFS), vectors only up to -1.1dBFS are measured. The input digital amplitude used for most of the measurements in this chapter is at -1.8dBFS. Figure 5-23 shows the measured SNR and output amplitude as a function of digital input amplitude for the DC DAC with a constant gate bias voltage. Figure 5-24 shows the same plots for the RF DAC with an oscillating gate bias voltage. The output amplitude scales as expected, but the SNR improvement is lower than expected, showing some compression at large digital amplitudes.

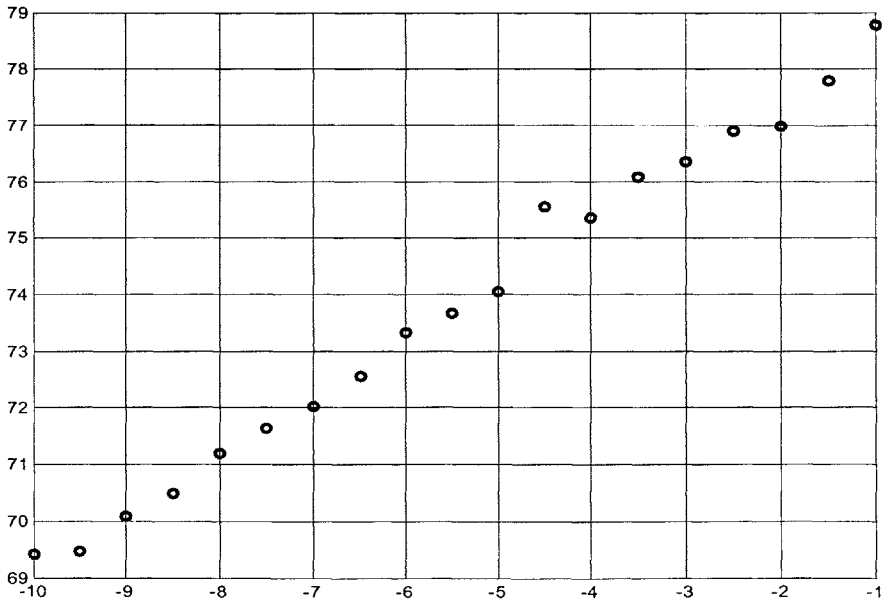

Figure 5-22: Simulated SNR as a function of the digital input amplitude in dB relative to full scale (dBFS).

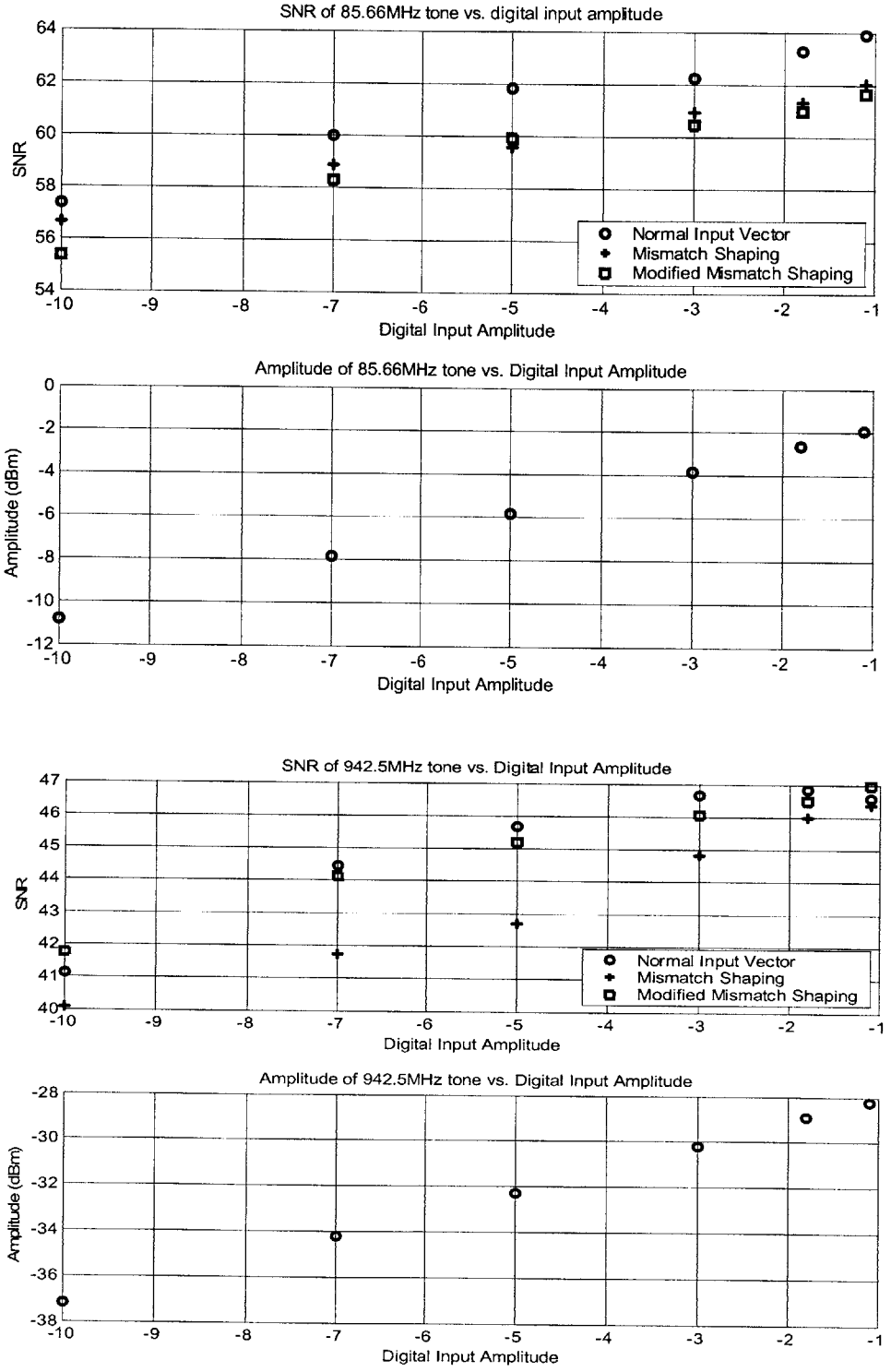

Figure 5-23: SNR as a function of digital input amplitude (in dBFS) for the DAC operating with a constant bias voltage. The measurements were taken at f_{clk}=514MHz and an output bandwidth of 17.5MHz.

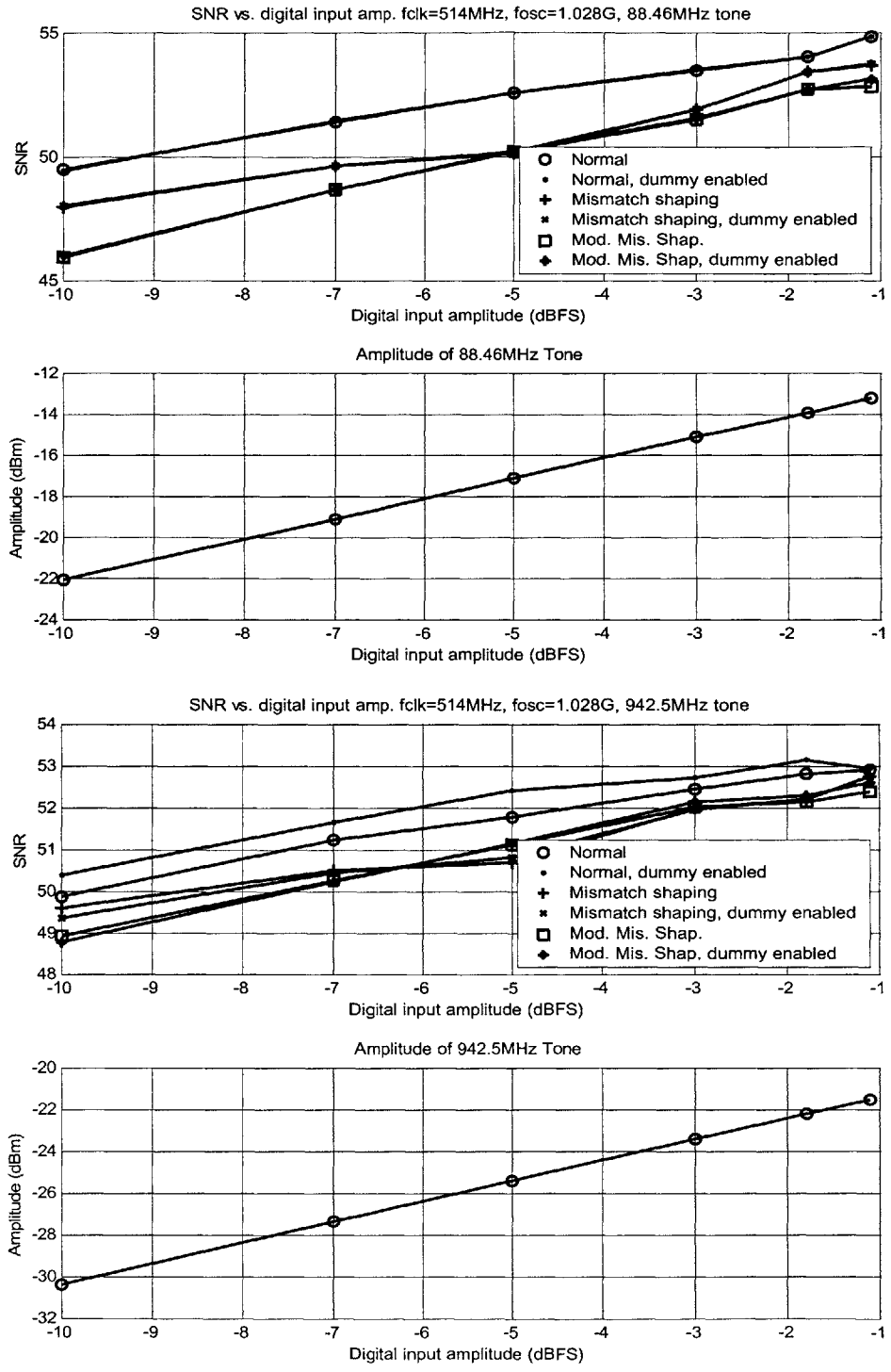

Figure 5-24: SNR as a function of digital input amplitude for the RF DAC with an oscillating gate bias voltage.

5.2.3.4 SNR versus Phase

The SNR of RF DAC was measured as the phase was varied between the data clock and the oscillator. This is depicted in the time domain pictures of Figure 5-25. The top plot shows the output when the phase between the oscillator and clock are well aligned. The bottom plot shows the output when the data switches in the middle of the oscillating waveform. The switching instants are marked with vertical lines on the horizontal axis. These plots are shown at a reduced frequency in order to capture the dynamics on the scope.

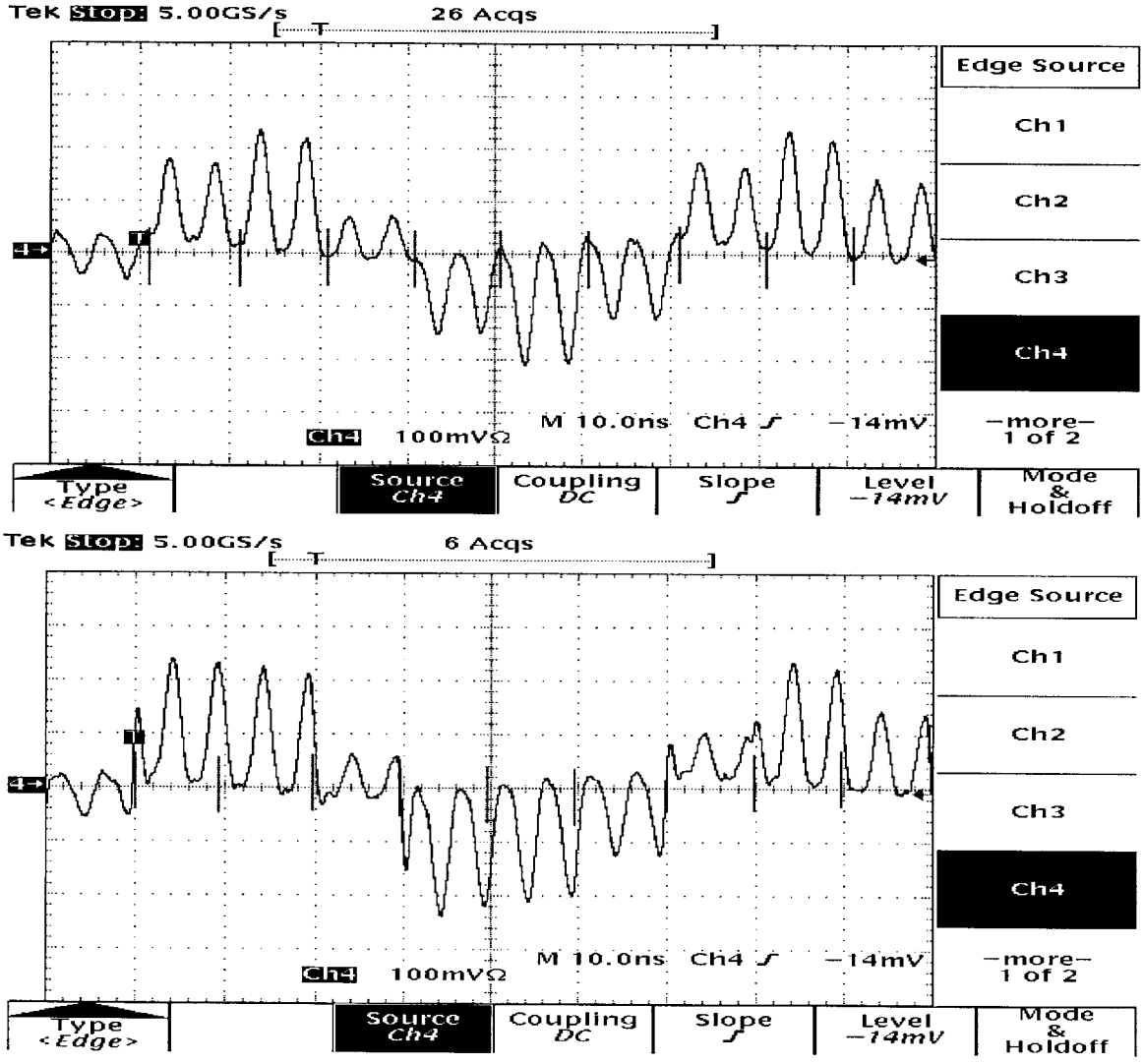

Figure 5-25: Time domain output waveforms of the DAC. The top plot shows the oscillator and clock waveforms aligned so the data switches in the zero regions of the oscillating waveform. The bottom shows the clock and oscillator misaligned so the data switches near the peak of the oscillating waveform.

The SNR is expected to degrade as the data goes from switching in the zero regions to switching at the peaks of the oscillating waveform. This is because of clock jitter, switching distortion, and ISI present when the DAC switches at the peak of the waveform. The amplitude is also expected to decrease slightly, since switching at the peaks of the oscillating waveform causes loss of some of the signal energy.

SNR is plotted as a function of the phase between the clock and the oscillator in Figure 5-26. The SNR and output signal amplitude of the third image for f_{clk}=514MHz are plotted. Three curves are shown for increasing values of the gate bias voltage, or for increasing bias levels of the current in each unit element. As the bias voltage is increased, the zero region of the output waveform decreases. Thus the region of SNR degradation widens and deepens. The triangle curve in Figure 5-26 shows that there is now no longer a zero region of the output waveform, there is always some DC current through each element. The whole SNR as a function of phase curve is shifted down. Notice that the SNR changes by more than the output amplitude, indicating that the noise floor is indeed increasing.

Figure 5-27 depicts the SNR and output amplitude as a function of phase at the maximum f_{clk}=880MHz and a very large +16dBm input amplitude. This shows that the SNR variation is larger at higher frequencies. Also compared in Figure 5-27 is the SNR of the primary and third image output tones.

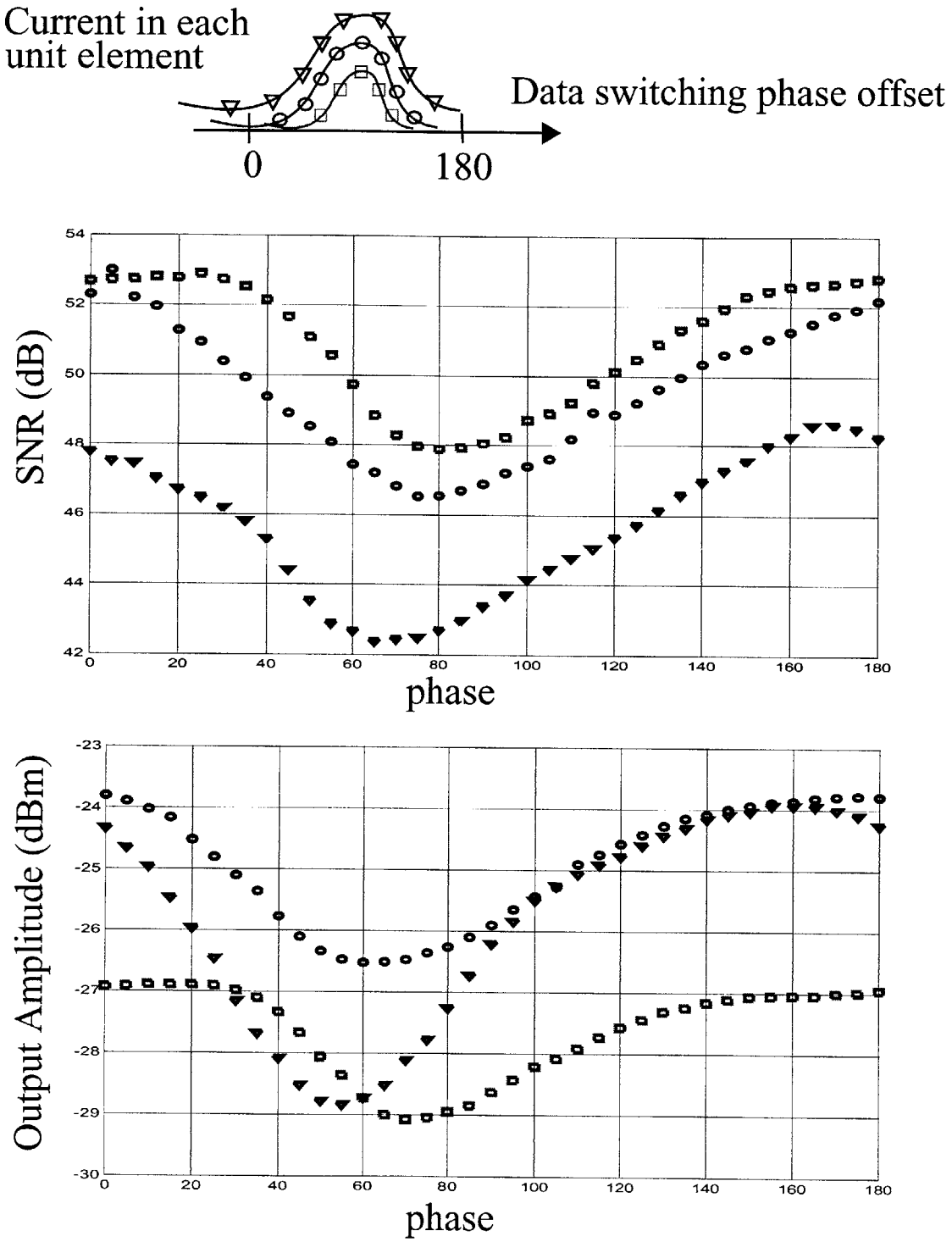

Figure 5-26: SNR and output amplitude versus phase for increasing values of the gate bias voltage. The measurements were taken at f_{clk}=514MHz.

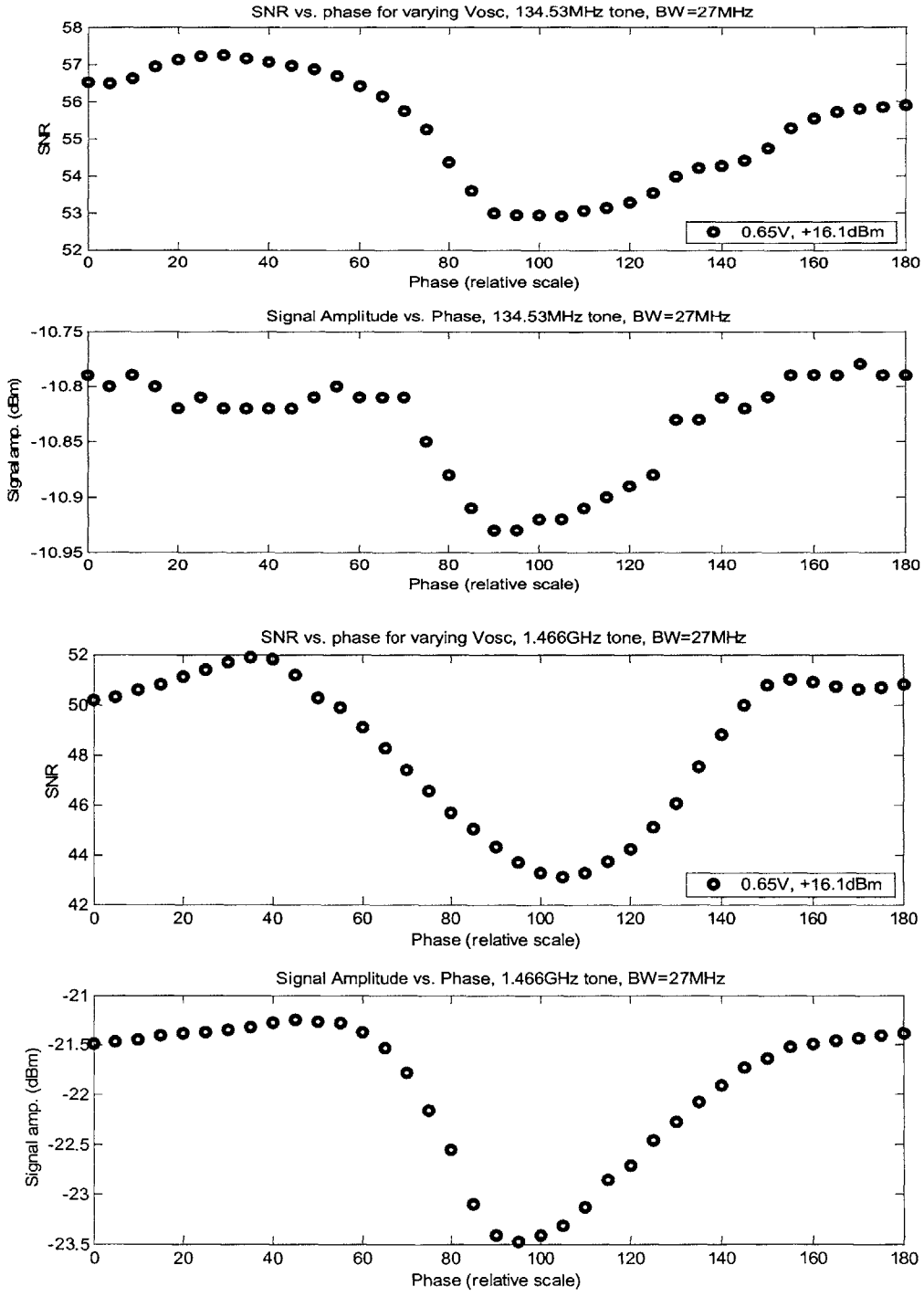

Figure 5-27: SNR as a function of the phase for f_{clk}=880MHz and a large oscillating gate amplitude. The top two plots are the primary output frequency and the bottom two are for the third image.

5.2.3.5 Sensitivity to Switch Driver Supply Voltage

The SNR and output amplitudes of the primary and third image are plotted versus the switch driver voltage (Vddswdr) in Figure 5-28. This supply controls the maximum gate voltage of the inverters that drive the switches. The output amplitude and SNR drop with Vddswdr since the current source transistors start to go out of saturation and into the linear region.

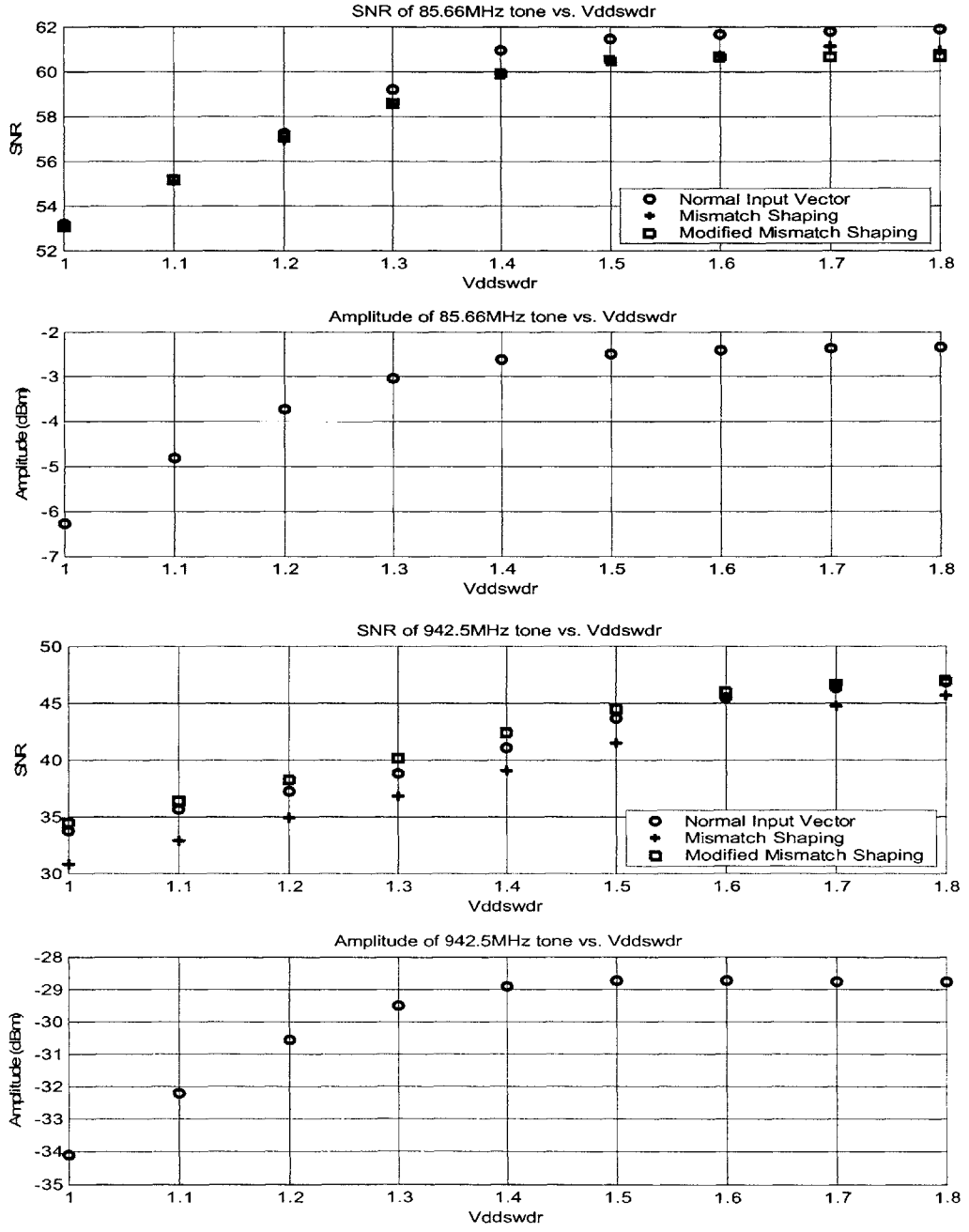

Figure 5-28: SNR and output amplitudes as a function of the supply voltage of the switch driver. These plots are for a constant gate bias voltage and f_{clk}=514MHz.

5.2.4 Two-tone IMD3 Performance

Two-tone IMD performance for RF DAC is shown in Figure 5-29. The clock frequency f_{clk} is 514 MHz and the oscillator frequency f_{osc} is 1.028GHz. The two tones are placed in the middle of the in-band region. The third order distortion component at marker 1 is in the noise floor, as designed. This proves that the traditional output impedance boosting cascode transistor is not necessary.

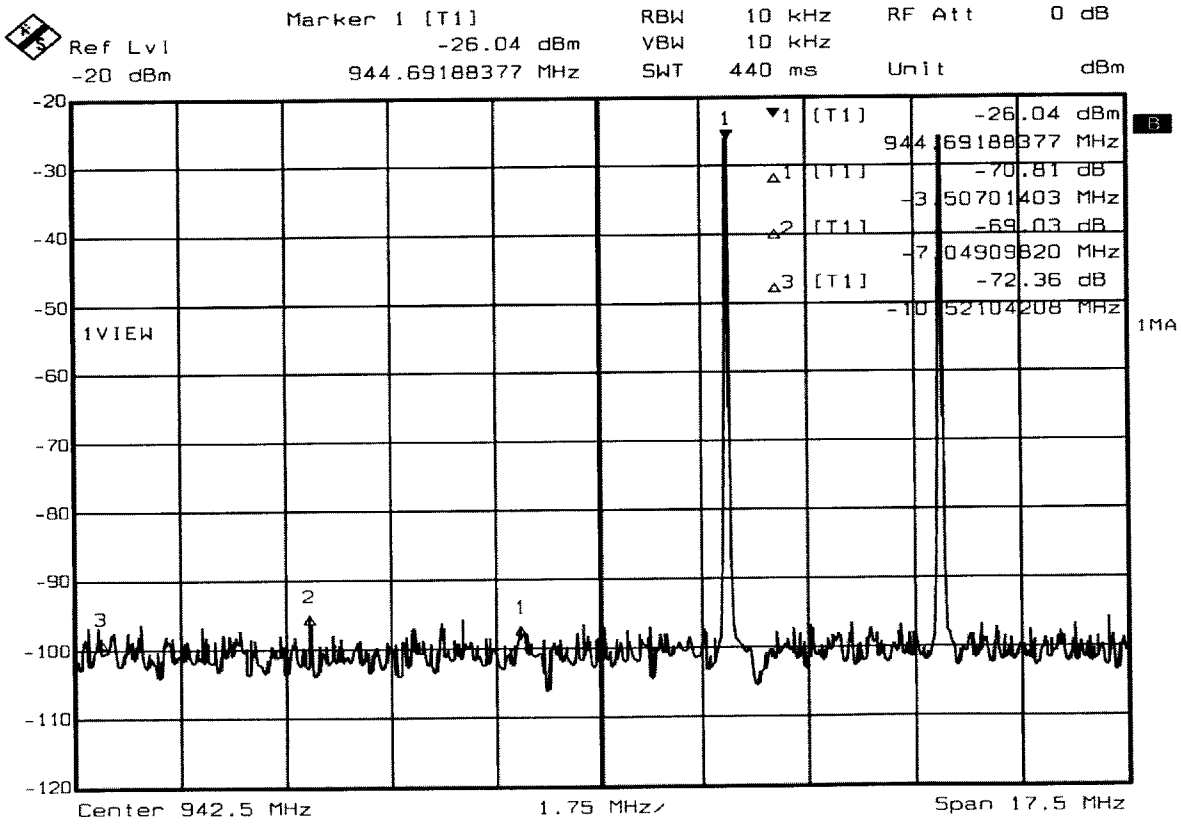

Figure 5-29: Two-tone IMD performance of the RF DAC third image for f_{clk}=514MHz.

5.3 Performance Comparison

A comparison of the RF DAC performance to other state-of-the-art DACs is shown in Table 5-4. RF DAC is the highest output frequency DAC reported to date. Both the noise floor and IMD3 performance are competitive with those of the lower output frequency DACs.

Table 5-4: Performance comparison

Work	IMD3	Noise Power Spectral Density	Maximum Output Frequency
Schofield, ISSCC 2003 [37] Nyquist Rate DAC	-80dBc at 310MHz	-162dBm/$\sqrt{Hz}$ at 6MHz offset from 385MHz carrier	385MHz, f_{clk}=400MS/s
Bosch, JSSC March 2001 [15] Nyquist Rate DAC	-65dBc at 100MHz	N/A	490MHz, f_{clk}=1GS/s
Falakshahi, JSSC May 1999 [19] ΣΔ DAC	N/A	-157dBm/$\sqrt{Hz}$ inband	5MHz band centered at DC, f_{clk}=120MS/s
Bugeja, ISSCC 2000 [20] Nyquist Rate DAC	-79dBc at 25MHz	-140dBm/$\sqrt{Hz}$ far away from carrier	50MHz, f_{clk}=100MS/s (poor performance up to f_{clk}=200MHz)
RF DAC ΣΔ DAC (concept could be extended to Nyquist rate DAC)	-70dBc at 942.5MHz	-142dBm/$\sqrt{Hz}$ at 5MHz away from 942.5MHz carrier	942.5MHz, f_{clk}=514MHz, bandwidth=17.5MHz (up to 1.6GHz, f_{clk}=880MHz, bandwidth= 30MHz)

6 Conclusions

6.1 Summary

A DAC output current controlled by an oscillating waveform is proposed to mitigate the effects of switching distortion and clock jitter. The oscillating waveform is a multiple ($k*f_s$) of the sampling frequency (f_s), where $k>1$. The waveforms are aligned so that the data switching occurs at the zero crossings of the oscillating current output. This makes the DAC insensitive to both switch dynamics and clock jitter. While this RF DAC is no longer sensitive to sampling clock jitter, it is sensitive to phase and amplitude noise of the oscillating waveform.

The architecture has the additional benefit of mixing the DAC impulse response energy to a higher frequency. An image of a low IF input signal can therefore be output directly at a high IF or RF frequency for transmit communications applications. This saves power and hardware by eliminating the need for mixers and intermediate frequencies present in traditional transmit communications systems.

The potential advantages of ΣΔ DAC architectures for narrowband communications applications are highlighted. An 8 unit element ΣΔ DAC is implemented in 0.18μm CMOS technology to demonstrate this concept. Performance specifications are targeted for GSM transmitters. Several circuit design techniques differ from those of a conventional DAC. Specifically, the output impedance required for a differential DAC is shown to be lower than that required for a single-ended DAC for communications applications. Sufficient output impedance was obtained by designing the current source and switches of the DAC in the saturation regime, and no extra cascode transistor is necessary. Another design difference is in the switch drivers. Conventionally designed for a high crossing point so neither switch is off, the switching waveforms in this work are designed for a fast switching time so that they 'fit' in the zero regions of the control waveform. Careful integrated circuit and board layout techniques are used to minimize the paths and coupling of high frequency signals.

DC matching measurement results show that the current mismatch is higher than expected due to β mismatches in the linear array layout of the current source transistors. Edge effects can be seen in the smaller current source transistors, while a gradient can be seen in the larger transistors.

AC measurements show full functionality up to the speed of the input digital pattern generator. Second harmonic distortion is seen at high frequencies, indicating an unequal coupling to one side of the differential outputs. The inband noise is higher than expected both for the primary and third

image outputs at high frequencies. Several experiments have been performed to confirm the source of this noise, and the best hypothesis is that coupling to the current source is mixing out-of-band quantization noise back inband. RF DAC has a 10dB improvement over the DC DAC at high frequencies, which is attributed to increasing the signal amplitude above the other sources of noise. The inband SNR degrades as the phase between the oscillating waveform and data switching instants is varied, as expected. Two tone results show IMD3 at the -70dBc level, limited by the inband noise floor, demonstrating that no impedance-boosting cascode is needed.

6.2 Contributions of Thesis

The contributions of this thesis are outlined below.

1. RF DAC Concept

   A. High output frequency saves power and hardware by eliminating the need for mixers and additional intermediate frequencies in communications systems.

   B. Potential for lower noise than a DAC + mixer solution by switching in the zero regions of the output waveform

2. Clock jitter and phase noise

   A. Intuitive and analytical analysis of why trading clock jitter for phase noise might be a good idea.

3. Recognizes use of ΣΔ DACs for high frequency narrowband communications applications

   A. Previous work focuses on development of ΣΔ DACs for low frequency audio applications.

   B. This work highlights the advantages of ΣΔ DACs over Nyquist-rate DACs for high-frequency applications.

4. DAC Circuit Design

   A. Comparison of DAC output impedance requirements for INL, DNL, HD2, IMD3 specs for single-ended and differential implementations.

   B. "Traditional" output impedance boosting cascode transistor can be eliminated in a differential implementation for narrowband communications applications, reducing headroom requirements.

6.3 Future Work

This work could be extended to a larger array size to achieve a wider output bandwidth. Extending all the way to a Nyquist rate DAC would pose new challenges in delivering the oscillating waveforms accurately to all the elements at the same time and driving a large capacitance at high frequencies.

The DAC could also be used as a feedback DAC in high-speed, CT ΣΔ ADC. This has the potential to reduce the jitter limit found in state-of-the-art CT ΣΔMs. The impulse response of the DAC in this case would be different than a traditional square pulse feedback DAC, so the loop transfer function would need to be adjusted accordingly.

It would also be interesting to study integration of the RF DAC with a filter and power amplifier to complete the transmit signal path. A study of the power efficiency of the DAC compared to the power efficiency of the power amplifier may give clues as to when it makes sense to spend more of the power budget in the power amplifier as opposed to boosting the power levels of the DAC.

A suggestion for continuing this research directly would be to use high-speed, low-voltage, fully-differential digital inputs to reduce both the pin count and coupling noise of the large-swing digital inputs.

Appendix A: Jitter Limits in DACs

Figure A-1 shows sample output waveforms for a pulse or return-to-zero (RZ) DAC and a non-return-to-zero (NRZ) DAC. The duration of the RZ pulse T' can be any fraction n<1 of the input data rate. The transition timing points are shown with clock jitter Δ_{tn}, which are assumed in this analysis to be independent Gaussian random variables with standard deviation σ_t.

SNR can be calculated by finding the signal and noise power of the waveforms in Figure A-1. The signal and noise powers can be found by calculating the area under the waveforms of Figure A-1. For a current-output DAC, the area under the curve is equivalent to the amount of charge delivered.

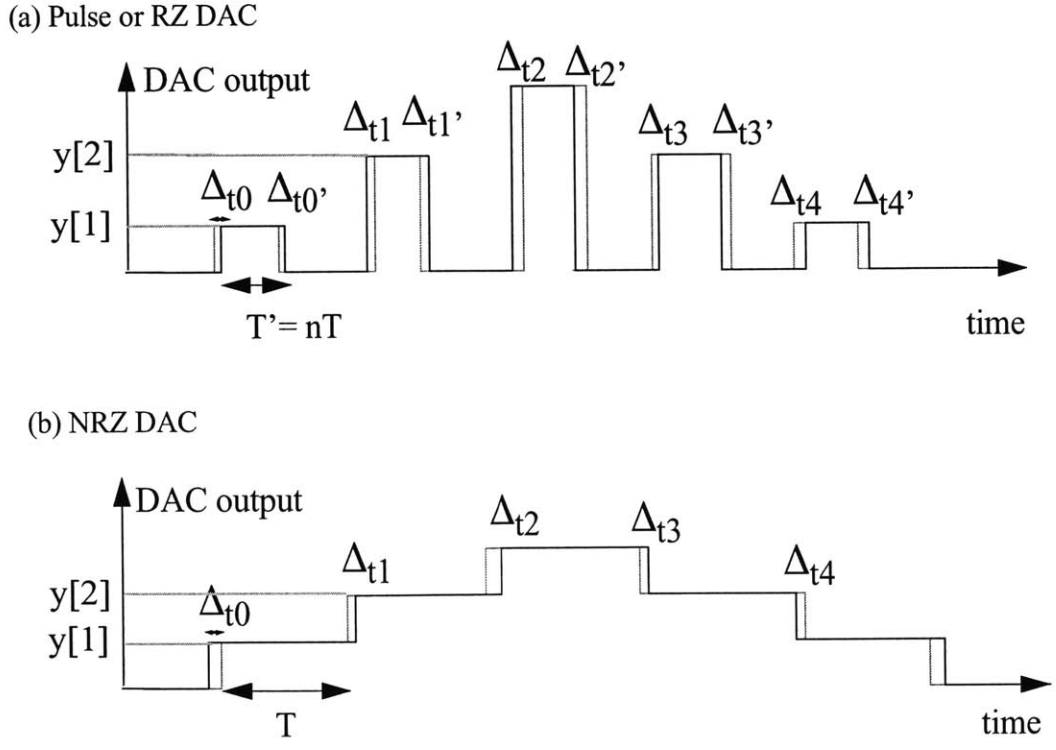

Figure A-1: Example RZ and NRZ DAC outputs with clock jitter.

A.1 RZ DAC Jitter Limit

In the RZ DAC waveform, the output signal is S=T'y[n] where y[n] is the quantized DAC output. The error is $E = \Delta_{tn}\, y[n] + \Delta_{tn'}\, y[n]$, which has a standard deviation of $\sqrt{2}\,\sigma_t\, y[n]$. The SNR is then

$$SNR = 20\log\frac{T}{\sqrt{2}\sigma_t} = 20\log\frac{n}{\sqrt{2}f_s\sigma_t} \tag{A.1}$$

For a narrowband signal, the inband noise is reduced by the OSR and Equation A.1 becomes

$$SNR = 20\log\frac{n\sqrt{OSR}}{\sqrt{2}f_s\sigma_t} = 20\log\frac{n}{2\sqrt{f_s f_b}\sigma_t} \tag{A.2}$$

Note that the jitter limited SNR in the RZ DAC case is independent of the number of bits in the DAC and the frequency of the input.

A.2 NRZ DAC Jitter Limit

In the NRZ DAC case, the signal is S=Ty[n] and the error is $E = D_{tn}$ (y[n]-y[n-1]). The standard deviation of the error is σ_t(y[n]-y[n-1])=$\sigma_t y_{diff}$[n]. The rms values of y[n] and y_{diff}[n] are

$$yrms = \sqrt{Average(y^2[n])} = \sqrt{\frac{1}{M}\sum_{n=1}^{M} y^2[n]} \tag{A.3}$$

$$ydiffrms = \sqrt{Average(ydiff^2[n])} = \sqrt{\frac{1}{M}\sum_{n=1}^{M} ydiff^2[n]} \tag{A.4}$$

where M is the number of samples taken per period of the input waveform, M=round($\frac{f_s}{f_{IF}}$).

Assuming y is a sinusoid quantized to b bits

$$y[n] = Quantized\left(A\sin\left(\frac{2\pi n}{M} + \phi\right)\right) \tag{A.5}$$

the rms values in Equation A.3 and Equation A.4 can be calculated. The SNR is

$$SNR = 20\log\left(\frac{y_{rms}}{f_s\sigma_t y_{diffrms}}\right) \tag{A.6}$$

For a narrow band signal, the inband SNR is

$$SNR = 20\log\left(\frac{y_{rms}\sqrt{OSR}}{f_s\sigma_t y_{diffrms}}\right) = 20\log\left(\frac{y_{rms}}{\sqrt{2f_s f_b}\sigma_t y_{diffrms}}\right) \quad \text{(A.7)}$$

References

[1] P. Kenington, "Emerging Technologies for Software Radio," Electronics and Communication Engineering Journal, pp. 69-83, April 1999.

[2] G. Ragavan, J. Jensen, et al. "Architecture, Design, and Test of Continuous-Time Tunable Intermediate-Frequency Bandpass Delta-Sigma Modulators," *IEEE Journal of Solid State Circuits*, pp. 5-13, January 2001.

[3] G. Geelen, "A 6b 1.1 GSample/s CMOS A/D Converter," *IEEE Solid State Circuits Conference*, pp. 128-129, February 2001.

[4] M. Choi, A. Abidi, "A 6b 1.3 GSample/s A/D Converter in 0.35um CMOS," *IEEE Solid State Circuits Conference*, pp. 126-127, February 2001.

[5] K. Nagaraj, D. Martin et al. "A Dual-Mode 700-Msample/s 6-bit 200-Msample/s 7-bit A/D Converter in a 0.25μm Digital CMOS Process," *IEEE Journal of Solid State Circuits*, pp. 1760-1769, December 2000.

[6] Y. Park, S. Karthikeyan, F. Tsay, E. Bartolome, "A 10b 100MSample/s CMOS Pipelined ADC with 1.8V Power Supply," *IEEE Solid State Circuits Conference*, pp. 130-131, February 2001.

[7] A. Karanicolas, "Digital Self-Calibration techniques for high-accuracy, high speed analog to digital converters" Ph.D Thesis, Massachusetts Insitute of Technology, 1994.

[8] S. Jantzi, R. Schreier, M. Snelgrove, "Bandpass sigma-delta analog-to-digital conversion," *IEEE Trans. on Circuits and Systems*, Vol. 38, No. 11, pp. 1406-1409, Nov. 1991.

[9] L. J. Breems, E. van der Zwan, et al. "A 1.8mW CMOS ΣΔ modulator with integrated mixer for A/D conversion of IF signals," in ISSCC Dig. Tech. Papers, pp. 52-53, Feb. 1999.

[10] J. Cherry, W. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion*. Boston, MA: Kluwer Academic Publishers, 2000.

[11] K. Vleugels, "A 2.5V Broadband Multi-Bit ΣΔ Modulator with 95dB Dynamic Range" *IEEE Solid State Circuits Conference*, pp. 50-51, February 2001.

[12] A. Jayaraman, P. Asbeck, et al. "Bandpass delta-sigma modulator with 800-MHz center frequency," in *GaAs Int. Circuit Symp.*, pp. 95-98, 1997.

[13] L. Kushner, M. Ainsworth, "A spurious reduction technique for high-speed direct digital synthesizers," *Proceedings of the IEEE International Frequency Control Symposium*, pp. 920-927, June 1996.

[14] P. Hendriks, "Specifying communication DACs," *IEEE Spectrum*, vol. 34, pp.58-69, July 1997.

[15] A. Bosch, M. Borremans, M. Steyaert, W. Sansen, "A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," *IEEE Journal of Solid State Circuits*, pp. 315-324, March 2001.

[16] R. Adams, "A 113dB SNR oversampling DAC with segmented noise-shaped scrambling," *IEEE Journal of Solid-State Circuits*, pp.1871-1878, December 1998.

[17] J. Wikner, N. Tan, "Modeling of CMOS Digital-to-Analog Converters for Telecommunication," *IEEE Transactions on Circuits and Systems*, vol. 46, No. 5 May 1999.

[18] I. Fujimori, A. Nogi, T. Sugimoto, "A Multi-Bit ΣΔ Audio DAC with 120dB Dynamic Range," *IEEE Solid State Circuits Conference*, pp. 152-153, February 1999.

[19] K. Falakshahi, C. Yang, B. Wooley "A 14-bit 10-MSample/s D/A Converter Using Multibit ΣΔ Modulation," *IEEE Journal of Solid State Circuits*, pp. 1841-1852, December 2000.

[20] A. Bugeja, B. Song, "A Self-Trimming 14-b 100-MS/s CMOS DAC," *IEEE Journal of Solid State Circuits*, pp. 1841-1852, December 2000.

[21] H. Tao, L. Toth, J. Khoury, "Analysis of Timing Jitter in Bandpass Sigma-Delta Modulators," *IEEE Trans. on Circuits Syst. II*, Vol. 46, pp. 991-1001, August 1999.

[22] .Dr. Bob Walden's ADC and OEIC Survey, http://www.hrl.com/TECHLABS/micro/ADC/adc.html

[23] B. Zhang, "Delta-Sigma Modulators Employing Continuous-Time Circuits and Mismatch-Shaped DACs" Ph.D Thesis, Oregon State University, 1996.

[24] A.Van den Bosch, M. Steyaert, W. Sansen, "SFDR-bandwidth limitations for high-speed high-resolution current-steering CMOS D/A converters," in *Proc. IEEE Int. Conf. Electronics, Circuits and Systems (ICECS)*, pp.1193-1196, Sept. 1999.

[25] I. Bloom, Y. Nemirovsky, "1/f noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation," *Appl. Phys. Lett.*, vol. 58, no. 15, pp. 1664-1666, Apr. 15, 1991.

[26] E. Klumperink, S. Gierking, A. Wel, B. Nauta, "Reducing MOSFET 1/f Noise and Power Consumption by Switched Biasing," *IEEE Journal of Solid State Circuits*, vol. 35, no. 7, pp. 994-1001, July 2000.

[27] S. Luschas, H.-S. Lee, "High Speed Sigma Delta Modulators with Reduced Timing Jitter Sensitivity," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, issue: 11, November 2002, pp. 712-720.

[28] K. Poulton, R. Neff, A. Muto, W. Liu, A. Burstein, and M. Heshami, "A 4 GSample/s 8b ADC in 0.35um CMOS," in *Proc. IEEE Solid-State Circuits Conf.*, pp. 166-485, Feb. 2002.

[29] European Telecommunication Standard No. ETS 300577, *Digital Cellular Telecommunications System (Phase 2); Radio transmission and reception*, GSM 05.05 version 4.23.1, December 1999.

[30] D. Mercer, "A 16-b D/A converter with increased spurious free dynamic range," *IEEE Journal of Solid State Circuits*, pp. 1180-1185, October 1994.

[31] S. Norsworthy, R. Schreier, G. Temes, *Delta-Sigma Data Converters*, IEEE Press, New York, 1997.

[32] R. Schreier, "Mismatch-Shaping Digital-to-Analog Conversion," *103rd Convention of the Audio Engineering Society*, preprint no. 4529, September 26-29, 1997.

[33] T. Shui, R. Schreier, F. Hudson, "Mismatch-shaping for a current-mode multi-bit delta-sigma DAC," *IEEE Journal of Solid-State Circuits*, vol. SC-34, no. 3, pp. 331-338, March 1999.

[34] The MathWorks, Inc., *Matlab*, Version 3.5, The MathWorks, Inc., Natick, MA, 1992.

[35] R. Schreier, The Delta-Sigma Toolbox available from the MathWorks website: http://www.mathworks.ch/matlabcentral/fileexchange/loadFile.do?objectId=19&objectType=file

[36] K. Nyguen, R. Adams, K. Sweetland, "A 113dB SNR oversampling sigma-delta ADC for CD/DVD application," *IEEE Transactions on Consumer Electronics*, vol. 44, no. 3, pp. 1019-1023, August 1998.

[37] W. Schofield, D. Mercer, L. St. Onge "A 16b 400MS/s DAC with < -80dBc IMD to 300MHz and <-160dBm/Hz Noise Power Spectral Density," *IEEE International Solid State Circuits Conference*, pp. 126-127, February 2003.

[38] B. Razavi, *Principles of Data Conversion System Design*, Prentice Hall, 1998, ISBN 0-7803-1093-4.

[39] B. Razavi, *RF Microelectronics*, IEEE Press, 1995, Prentice Hall, 1998, ISBN 0-13-887571-5.

[40] A. Van den Bosch, M. Steyaert, W. Sansen "SFDR-Bandwidth Limitations for High Speed High Resolution Current Steering CMOS D/A Converters," in Proc. IEEE Int. Conf. Electronics, Circuits, and Systems (ICECS), Sept. 1999, pp. 1193-1196.

[41] S. Luschas, H.-S. Lee, "Output Impedance Specifications for High-Frequency, Narrowband Communications Digital-to-Analog Converters," *International Symposium on Circuits and Systems*, May 2003.

[42] D. Mercer, L. Singer, "A 12-b 125 MSPS CMOS D/A designed for spectral performance," IEEE International Symposium on Low Power Electronics and Design, pp. 243-246, August 12-14 1996.

[43] M. Ker, T. Chen, C. Wu, H. Chang, "ESD Protection Design on Analog Pin with Very Low input Capacitance for RF or Current-Mode Applications," Twelfth Annual IEEE International ASIC/SOC Conference, pp. 262-266, 1999.

[44] H. Lin, R. Schreier, "A Bandpass Mismatch-Shaped Multi-Bit ΣΔ Switched-Capacitor DAC using Butterfly Shuffler," *IEEE International Solid State Circuits Conference*, pp. 58-59, February 1999.