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Rail-to-Rail Timing Signals Generation Using InGaZnO TFTs For Flexible X-Ray Detector

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ABSTRACT This paper reports on-chip rail-to-rail timing signals generation thin-film circuits for the first time. These circuits, based on a-IGZO thin-film transistors (TFTs) with a simple staggered bottom gate structure, allow row and column selection of a sensor matrix embedded in a flexible radiation sensing system. They include on-chip clock generator (ring oscillator), column selector (shift register) and row-selector (a frequency divider and a shift register). They are realised with rail-to-rail logic gates with level-shifting ability that can perform inversion and NAND logic operations. These logic gates are capable of providing full output swing between supply rails, V_{DD} and V_{SS}, by introducing a single additional switch for each input in bootstrapping logic gates. These circuits were characterised under normal ambient atmosphere and show an improved performance compared to the conventional logic gates with diode connected load and pseudo CMOS counterparts. By using these high-performance logic gates, a complete rail-to-rail frequency divider is presented from measurements using D-Flip Flop. In order to realize a complete compact system, an on-chip ring oscillator (output clock frequency around 1 kHz) and a shift register are also presented from simulations, where these circuits show a power consumption of 1.5 mW and 0.82 mW at a supply voltage of 8 V, respectively. While the circuit concepts described here were designed for an X-ray sensing system, they can be readily expanded to other domains where flexible on-chip timing signal generation is required, such as, smart packaging, biomedical wearable devices and RFIDs.

INDEX TERMS Rail-to-rail logic gates, IGZO TFT, timing signals, flexible radiation sensing system.

I. INTRODUCTION

Design of flexible electronic systems with emerging hybrid technologies is gaining significant interest [1]–[3]. One good example is organic p-type and oxide n-type semiconductors to create complementary metal-oxide semiconductor (CMOS) thin-film circuits at low temperature [2], [3]. Another case of an hybrid system is an X-ray sensor based on oxide thin-film transistor (TFT) readout circuitry and organic photoconductors [4]. The flexible X-ray radiation detectors can find potential applications in different domains including health, radioactive plants and security systems. State-of-the-art work is limited to rigid systems, where mostly readout circuits are being developed with standard crystalline silicon CMOS technologies [5], limiting the applicability of the sensing systems.

Leveraging on the benefits of hybrid technologies in developing flexible systems, circuits are being designed with either a-Si:H or indium-gallium-zinc-oxide thin-film-transistors

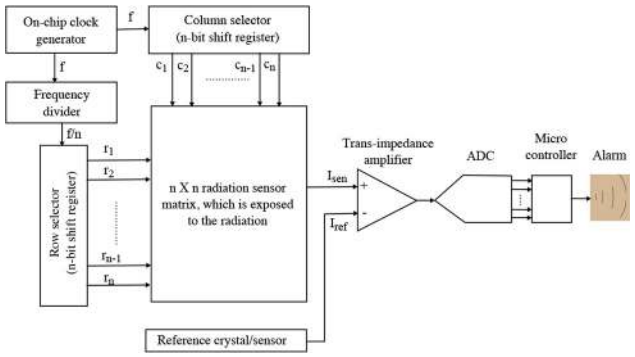

FIGURE 1. **Radiation sensing system with on-chip timing signals and signal conditioning blocks to measure dose level.**

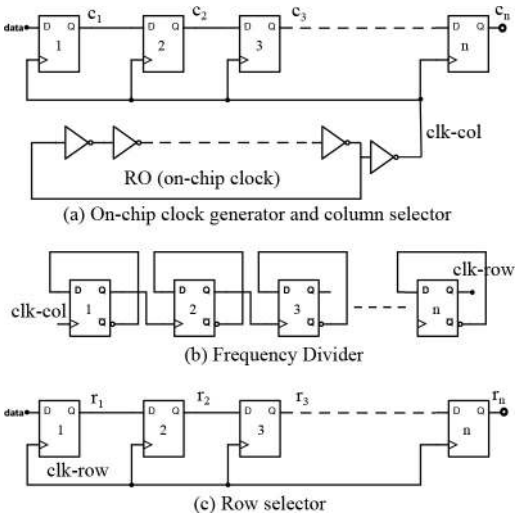

FIGURE 2. **Proposed on-chip rail-to-rail n X n matrix row and column selector for a flexible radiation sensing system: (a) Ring oscillator for generation of on-chip clock and column selector (b) n-stage frequency divider for generation of row selector clock from on-chip clock. (c) Row selector.**

(IGZO TFTs), whereas organic crystals are being considered to be radiation sensors [6], [7]. In order to implement a self-contained flexible electronic system, all the required signals should be generated on-chip, which eliminates complex interfacing and results in a compact system with high reliability. With the invention of printed batteries [8], it is possible to have on-chip power supply (consisting of DC-DC converters, clock generators and printed batteries). Operating circuits at low supply voltages will relax constraints on the supply voltage generation block. Literature [9]–[12] reports driving and other analog circuits using a-Si:H TFT technology. However, the intrinsic mobility of a-Si:H TFT device is almost one order of magnitude lower than the oxide TFT devices. Therefore, a-Si:H TFT based circuits need high operating voltage. As a result, oxide TFT circuits are the preferred choice for the application under consideration. In addition, the large-area flexible devices with IGZO TFT technology are immune to permanent damages due to high doses of radiation [13], [14]. Therefore, IGZO TFT based circuits are believed to exhibit robust performance even if they are close to the X-ray radiation sensor matrix. IGZO TFTs are inherently n-type transistors, as the channel is formed by accumulation of electrons in the active layer. When circuits need to be designed using unipolar devices, new circuit design techniques must be developed [15], as CMOS design techniques cannot be adapted directly.

To conceive an X-ray detector testbed as shown in Fig. 1, it is required to develop circuits enabling timing signals generation. This is fundamental to select rows and columns of a n×n sensor matrix. Moreover, the transimpedance amplifier depicted in Fig. 1, was also reported using IGZO TFTs [4], which together with the circuit reported here, completes the full system integration of readout and signal conditioning. For row and column selector implementation, it is required to have clock signals of different frequencies to achieve sequential row and column scanning, similar to displays. The complete system demands two rail-to-rail clock signals with different frequencies and shift register(s). To date, most of the work has been limited to individual building blocks demonstration. Ring oscillators (RO) or clock generators have been reported with IGZO TFTs [16], [17]. However, the former is limited by output swing and is not suitable for clock generation, while the latter uses dual gates, demanding higher mask count and processing steps. Both these designs are employing high supply voltages (> 20 V) and the performance is being degraded at low voltages. Similar challenges exist with shift registers [18]. Then, in order to implement the flexible radiation sensing system, this paper proposes on-chip row and column selectors with rail-to-rail functionality (see Fig. 2), where these blocks use full swing logic gates as described below.

The absence of stable p-type oxide TFTs imposes limitations on circuit performance, particularly in achieving rail-to-rail output of logic gates. Conventional 'NMOS' based loads are formed with diode connected transistors, where the driver is made wider than the load to favour some gain. However, this configuration cannot ensure full output voltage swing. The dynamic logic gates reported in [19], while improving power consumption and circuit area compared to static logic circuits, have limited voltage swing. The maximum voltage reached by the gates is one threshold voltage less than the supply voltage. In addition, it requires two explicit signals for controlling the operation in pre-charge and evaluation phase. On the other hand, the gates reported in [20] employ a large number of transistors for implementation of simple gates. For a single inverter, 7 TFTs were used to obtain the desired performance. Pseudo-CMOS NOT gate reported in [21] requires two different supply voltages to get the complete swing at the output. On the other hand, only bootstrapped pseudo-CMOS NOT gate with dual gate IGZO TFT is reported in [22]. The dual gate structure adds to fabrication cost. It can be noticed from the literature that the previously reported gates are not suitable for the targeted application, which requires low voltage operation for self-contained electronics. In addition, the gates should operate

without any external excitation and with standard device structures to minimize the effective cost and complexity of the system. Then, this work demonstrates high performance logic gates by introducing a switching TFT for each input in capacitive bootstrapping based logic gates. They can ensure complete rail-to-rail operation with standard device structure for lower values of V_{DD} without using any external control signal and hence, they have the level shifting ability, as the output logic '1' level can be made equal to V_{DD}, independent of the input signal logic '1' level. Furthermore, this work compares the performance of these gates (NOT and NAND) with diode connected load and pseudo CMOS configurations from measured characteristics. Then, rail-to-rail swing on-chip row and column selectors for a 2 x 2 sensor matrix are also demonstrated as a proof of concept, from measurements and simulations, respectively.

II. CIRCUIT FABRICATION

Circuits were fabricated on PEN substrates based on oxide TFTs with a staggered bottom-gate, top contact structure. For gate, source, and drain electrodes a 60 nm-thick Mo layer was deposited by RF magnetron sputtering. The oxide semiconductor was a 30 nm-thick IGZO layer, and the dielectric layer was a 175 nm-thick multicomponent/multilayer stack based on Ta_2O_5 and SiO_2. Both the semiconductor and dielectric layers were deposited by RF magnetron sputtering. On the top of the TFT stack a 1 μm–thick parylene-C film was produced by chemical vapour deposition (CVD), acting as a passivation layer. All layers were patterned by optical lithography and wet etching (IGZO) or reactive ion etching (Mo, Ta_2O_5-SiO_2 and parylene-C). The samples were annealed on a hot-plate for one hour at 180°C.

III. CIRCUIT DESIGN

A. LOGIC GATES

Inverter and NAND gates circuit schematics and micrographs with diode connected load and pseudo CMOS configurations are presented in Fig. 3. The newly proposed gates, where a switch is added for each input to the bootstrapping capacitive load are depicted in Fig. 4. For the inverter, output rails are given by: diode load (1), pseudo cmos (2), capacitive bootstrapping load (3) and high performance gates (4).

$$V_{OHd} \approx V_{DD} - V_{TH};\ V_{OLd} \approx V_{DD} - \left(\frac{1}{g_{mT2}} \cdot I_{DS}\right) \quad (1)$$

$$V_{OHcm} \approx V_{DD} - 2V_{TH};\ V_{OLcm} \approx V_{DD} - \left(r_{offT4} \cdot I_{DS}\right) \quad (2)$$

$$V_{OHbs} \approx V_{DD};\ V_{OLbs} \approx V_{DD} - \left(r_{dsT2} \cdot I_{DS}\right) \quad (3)$$

$$V_{OHprop} \approx V_{DD};\ V_{OLprop} \approx V_{DD} - \left(r_{offT2} \cdot I_{DS}\right) \quad (4)$$

where V_{OH} and V_{OL} are output logic high and low levels, respectively, whereas, r_{ds} and r_{off} are output/drain to source resistance and effective off resistances of the TFT, while g_m represents transconductance of the transistor. The subscripts *d*, *cm*, *bs* and *prop* represent different logic gate configurations, namely, diode load based, pseudo cmos, bootstrapping load based and proposed gates.

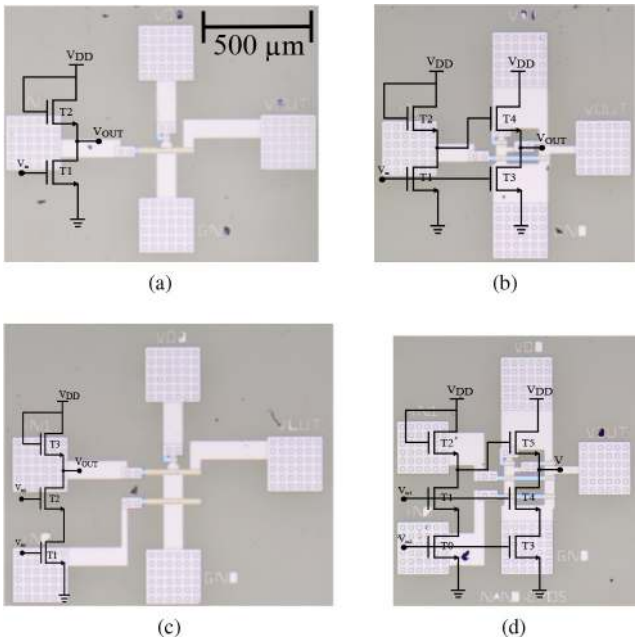

FIGURE 3. Conventional logic gates circuit schematics and micrographs using IGZO TFTs: (a) Inverter with diode load (b) Inverter in pseudo CMOS configuration (c) NAND with diode load (d) NAND in pseudo CMOS configuration.

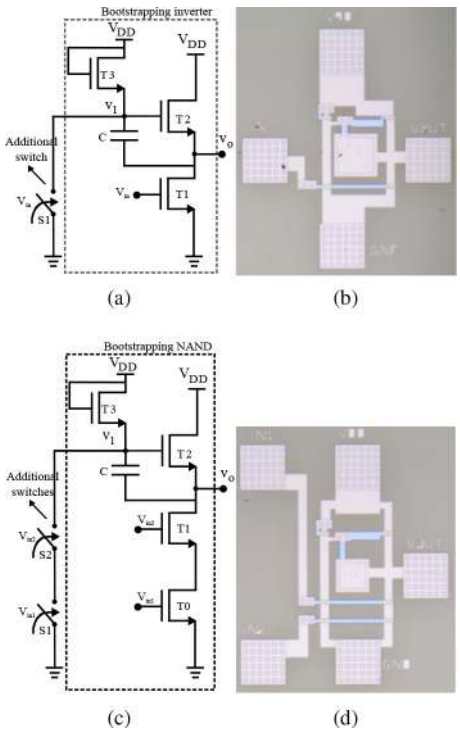

FIGURE 4. High performance logic gates formed by adding a switch for each input to the bootstrapping capacitive load (a) Inverter circuit schematic (b) Inverter micrograph (c) NAND circuit schematic (d) NAND micrograph.

As per (1), an inverter based on diode load (Fig. 3(a)) limits the swing and demands higher driver size compared to the load to favour some gain. On the other hand, the pseudo

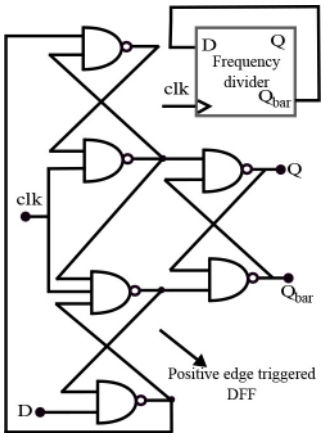

FIGURE 5. Frequency division from a positive edge triggered DFF and DFF circuit schematic with NAND gates.

CMOS configuration limits the V_{OH} value as per (2). The bootstrapped inverter (Fig. 4) can ensure V_{OH} very close to V_{DD} value due to capacitive bootstrapping operation as the voltage at node v_1 is almost $2V_{DD} - V_{TH} - V_{OL}$, where V_{TH} refers to the threshold voltage of the biasing transistor T3. However, V_{OL} is limited as per (3). In the bootstrapping inverter, by introducing a switch (S_1) between node v_1 and ground, which is controlled by the same input as the inverter, the logic low level can be made almost zero, when the input is logic '1'. For this condition, the switch closes and v_1 is pulled down to ground potential. Therefore, T2 will be turned off, turning the effective load resistance (r_{off}) very high. This leads to complete rail-to-rail operation ($V_{OH} = V_{DD}$ and $V_{OL} = V_{SS}$/Gnd). Here the switch is implemented with a n-type oxide TFT.

B. RING OSCILLATOR

In order to obtain on-chip rail-to-rail clock, a ring oscillator is being used, as it is simple in architecture. In this work, a 31-stage RO is used, where each inverter is implemented with the high performance configuration as shown in Fig. 4(a). The output of the RO is directly used as a clock for the column selector block, named as col-clk. The RO schematic is presented in Fig. 2(a).

C. FREQUENCY DIVIDER

In the radiation sensor scanning process, each row is scanned sequentially and while scanning each row, all the columns should be scanned in a sequential manner. In the proposed system a single clock generator is used and by using a frequency divider, it is possible to generate the clock for row selection (clk-row). When the radiation sensor matrix size is 2 × 2, clk-row = (clk-col)/2. This needs a frequency divider by a factor of 2, which is implemented with 1 positive edge triggered data flip flop (D-FF) as shown in Fig. 2. The D-FF circuit schematic is depicted in Fig. 5, and all NAND gates there represented are designed according to the high performance configuration in Fig. 4(c).

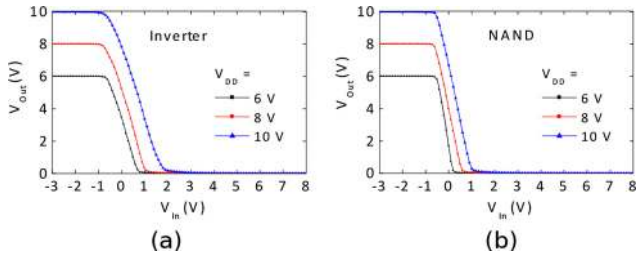

FIGURE 6. Measured VTCs of (a) inverter and (b) NAND by using the high performance logic gates, demonstrating rail-to-rail operation and level shifting ability.

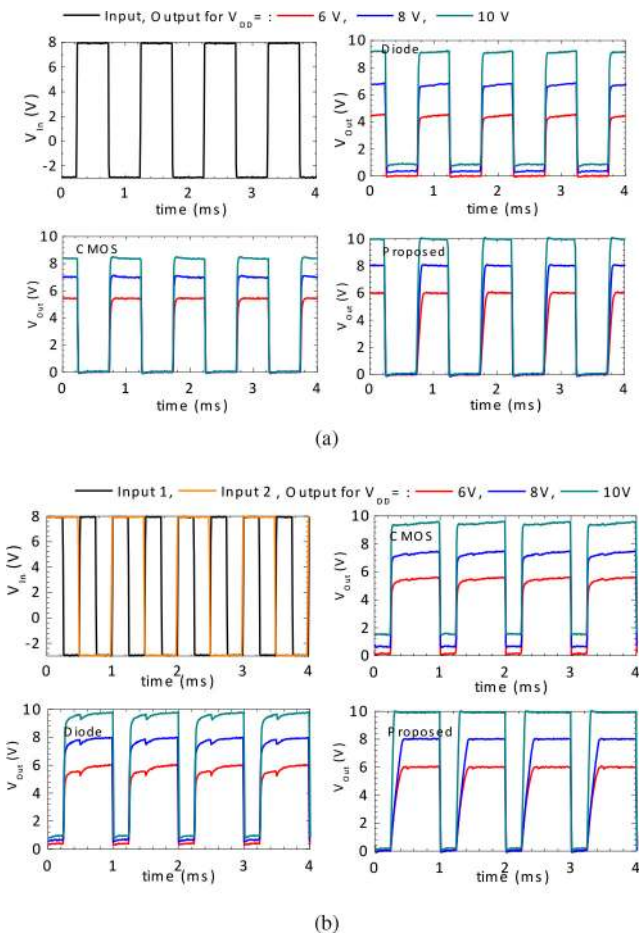

FIGURE 7. Measured dynamic characteristics under normal ambient, for the different gate designs, namely based on diode connected loads (diode graph), pseudo-CMOS (CMOS graph) and rail-to-rail (proposed graph) demonstrating level shifting ability with different supply voltages: (a) Inverter (b) NAND.

D. SHIFT REGISTER

The n-bit shift register using positive edge triggered D-FFs is presented in Fig. 2. This circuit can be used for row/column selection by providing proper clock signal (either clk-row or clk-col). Since the basic logic gates are ensuring high performance, the shift register is also able to show complete rail-to-rail operation. Whenever the circuit encounter a positive edge of the clock, the input is shifted to the right by 1-bit so that the corresponding row/column can be selected.

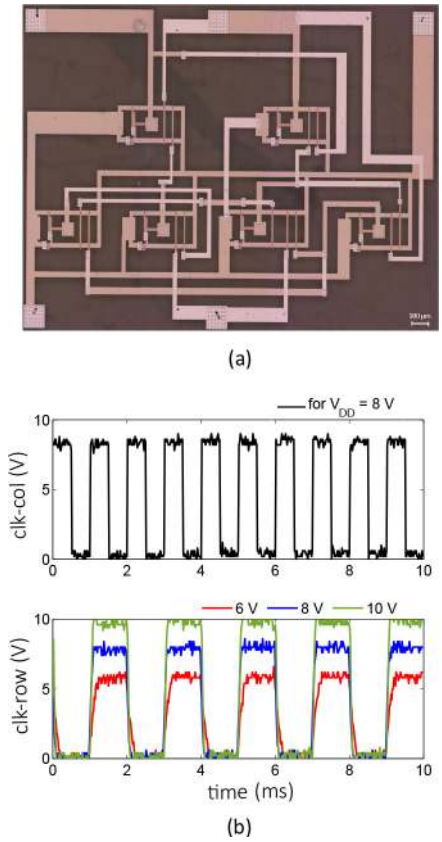

FIGURE 8. **(a) Micro-graph of the frequency divider (b) Measured response of frequency divider at 1 kHz.**

It should be noted that for the proof of concept, a 2-bit shift register is considered.

IV. RESULTS AND DISCUSSION

All logic gates were characterised from measurements under typical room environment. As expected a complete rail-to-rail operation together with level shifting ability is being noticed from the voltage transfer characteristics (VTCs) of inverter and NAND gates (one input is set to logic '1') from Fig. 6. Expected trend is also being noticed from the measured dynamic characteristics from Fig. 7, validating the output rails described in equations (1), (2) and (4). In case of diode load based gates, $(W)_{driver} = 240\ \mu m$ and $(W)_{load} = 20\ \mu m$. In pseudo-CMOS and in the proposed high-performance configurations all TFTs have $W = 40\ \mu m$. In addition, the device channel length (L) for all the circuits is 10 μm.

If a single clock is used for the entire system, then frequency dividers are used to address rows and columns selection. Therefore, by using high performance NAND gates, frequency divider is reported (for a 2 x 2 matrix) whose micropgraph and measured response at 1 kHz frequency are shown in Fig. 8. The frequency divider has shown a power consumption of 380 μW. Finally, to have entire timing signal generation circuitry, a 31-stage RO and 2-bit shift registers are needed (for a 2 x 2 matrix). Given the higher transistor count of these blocks, the fabrication process is still being optimized to turn their effective fabrication possible. Still, simulation results using IGZO TFT model with a supply voltage of 8 V [23] show rail-to-rail operation (Fig. 9). The RO is generating almost 1 kHz and showing a power consumption of 1.5 mW. The power consumption of a 2-bit shift register was observed to be 820 μW. From this characterization, it can be concluded that the proposed selector is able to provide complete rail-to-rail operation using high performance logic gates.

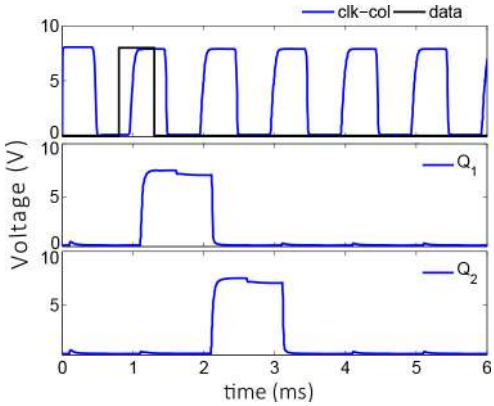

FIGURE 9. **Proposed rail-to-rail row/column selector response from simulations with a power supply voltage of 8 V. 31-stage ring oscillator response (clk-col at 1 kHz) for column selector clock and shift register response (Q_1 and Q_2) for either row/column selection.**

V. CONCLUSION

For the first time on-chip rail-to-rail timing signal generation blocks to address a sensor matrix in a radiation sensing system are demonstrated. All these circuits used novel high-performance logic gates that can ensure complete rail-to-rail operation with IGZO TFTs. Their performance is compared with other well known techniques, such as, diode load and pseudo CMOS gates from measurements. Proposed gates have shown superior performance in terms of voltage swing (between V_{DD} and V_{SS}). Using high performance gates, row and column selectors for a 2 x 2 sensor matrix have been demonstrated. The simulation and measurement results of the selectors have shown a complete rail-to-rail operation even with a supply voltage of only 6 V. Moreover, the circuits reported here only require a simple staggered bottom gate TFT structure and a lower transistor count compared to literature to achieved such level of performance. Proposed on-chip row/column selector with high performance gates find direct application in the flexible hybrid radiation sensing system, which is useful in health and security domains.

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