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Readout architectures for superconducting nanowire single photon detectors

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Advances in the development of superconducting nanowire single photon detectors (SNSPDs) have guaranteed that they remain a leading photon detection technology in applications such as quantum information [1–3], low power optical communications [4], and the life sciences [5, 6]. Recent demonstrations have shown significant improvements in key metrics such as high count-rates [7], jitter (<15 ps) [8], wide wavelength-sensitivity (315 nm–10.6 μm) [9–11], and high efficiencies (>90%) with low dark counts (<1 Hz) [12, 13]. Additionally, these devices have seen rapid commercialization in the last 5 years, with several companies now offering plug-and-play systems, making them more accessible than ever. However, to date, the largest arrays have integrated a maximum of $N = 64$ SNSPD pixels. This limitation has prevented the development of a highefficiency single-photon-sensitive camera in the infrared and mid-infrared, as well as limited the scale of readout of on-chip integrated devices such as those used in quantum information [14]. It remains an open challenge to develop and implement a readout architecture that can scalably interface hundreds or thousands of SNSPDs.

What makes designing a SNSPD readout particularly difficult is that the output pulses they generate are both broadband and small in amplitude. After absorbing a photon, a typical SNSPD will produce a ~10 μA output current with a ~100 ps rising edge. When carried into a 50 Ω load, this amounts to less than a millivolt of signal. Although there is strong evidence that the local impedance environment of these nanowires is higher than that of most superconducting systems (>1 kΩ) [15, 16], trying to integrate a device with large output impedances can produce latching effects [17]. These properties make on-chip integration with semiconductor logic difficult, preventing the use of existing silicon-based array readout architectures like those already developed for single-photon avalanche diodes. There has been some progress in amplifying small superconducting signals into semiconductor-compatible signals [18–21], but the amount of power required to amplify and digitize a bitstream from thousands of detectors makes it unlikely to be a solution for a large-scale readout. For small numbers of detectors, the most common method of readout is to connect each detector to its own 50 Ω coax line and microwave amplifier [22]. The amplified signals are then digitized at room temperature with conventional electronics, such as an oscilloscope or time-tagger. However, beyond a few hundred elements this solution becomes both cost-prohibitive and thermally impractical.

The challenge then is to create a readout architecture which maintains the desired performance characteristics while scaling to hundreds or thousands of detectors. For

SNSPDs, their primary advantage over competitor technologies is their ability to count at high rates with low jitter, while maintaining a high detection efficiency and low rate of dark counts. Efficiency and dark count rate are related to the optical and material properties of the SNSPD and its surroundings, and thus those metrics are less likely to be affected by an electronic readout system. As a result, any candidate architecture should optimize for the metrics of count rate and jitter. Which of these metrics is more important varies by application; for instance, building an SNSPD camera for the detection of fast-moving exoplanets may require high total count-rates but be insensitive to poor jitter performance, while a quantum key distribution system may benefit from cutting-edge performance in both jitter and count rate.

Generally speaking, we can divide existing SNSPD readout architectures into two categories: those which attempt to provide on-chip digitization using superconducting electronics, and those which use analog multiplexing on-chip and then pass the multiplexed signal to conventional room temperature electronics for processing. There exists a tradeoff between the two approaches: digitization simplifies the processing required at room temperature at the cost of on-chip complexity, while analog multiplexing typically increases off-chip hardware requirements but reduces on-chip complexity.

At present, most of the larger SNSPD array demonstrations have been of the analog multiplexing variety. The implementations of this multiplexing vary widely and have various tradeoffs. For instance, the 64-pixel row-column readout demonstration [23] used only $2\sqrt{N}$ readout lines, but the architecture has a reduced signal-to-noise as N grows. One alternate approach frequency-multi plexed 16 pixels onto a single feed line while preserving a low jitter, but required nontrivial readout hardware to parse the mixed signal [24]. Another analog scheme utilized the slow propagation velocity in the superconducting nanowire as a delay line, creating a time-of-flight imager. This imager had a large number of distinguishable pixels ($N = 590$) and low jitter, but its large inductance limited its count rate [25]. In addition to these architectures, there are also a number of other approaches which have been demonstrated at smaller scales [26–29].

The prevalence of these analog implementations, however, in no way discounts the utility and potential of on-chip digitization. Rather, it is more likely an indication of the overhead cost and complexity of integrating a sensitive nanoscale sensor into superconducting digital system. Future systems, especially those with thousands of pixels, would likely benefit from on-chip digitization as a means of reducing off-chip hardware requirements. After all, photon detection in an SNSPD can be thought of as an approximately digital signal: since a typical SNSPD is not energy-resolving, the only analog information contained in a detection event is that of the time-of-arrival. Additionally, superconducting logic families excel at operating at high clock frequencies with low power dissipation [30–32], and they also operate in a low-impedance environment, allowing their logic elements to be directly connected to SNSPDs.

There have already been a handful of demonstrations of SNSPD integration with single-flux quantum (SFQ) electronics. These Josephson junction-based electronics were used to digitize SNSPD signals on chip, and then pass that processed information directly to a system at room temperature. In one example, SFQ logic was used to merge the signals together from a four-pixel SNSPD array, and the circuit complexity scaled linearly, with each added pixel potentially requiring only 11 additional Josephson junctions [33]. However, this circuit was not able to read out the pixels independently—simultaneous detection events were lost. In another case, an SFQ circuit was realized which read out each element of a four-pixel array independently [34], although it required a slightly more complex design. The work by Miyajima *et al* is another step on the path towards on-chip digitization of SNSPD signals. The researchers were able to demonstrate an SFQ circuit capable of time-resolving input signals on the order of 10 ps, approaching the lowest jitters recorded for a single SNSPD. Still, there is much remaining research to be done in order to integrate SNSPDs with superconducting electronics. Future work will benefit from advances in Josephson junction fabrication development [35] as well as improved SFQ circuit design.

The advancement of several scientific fields and commercial endeavors will benefit from the development of future SNSPD readout architectures which can integrate hundreds or thousands of pixels. Development of these architectures is difficult, but there are a wide variety of approaches which have already been demonstrated for small numbers of pixels ($N \leq 64$). Most of the present architectures rely on either on-chip analog multiplexing or on-chip digitization, with analog implementations currently dominating the field. Notably, one approach that has not yet been demonstrated is to combine analog multiplexing techniques with on-chip digitization. This type of analog–digital blending has been successful in semiconductor-based cameras such as the charge-coupled device and may allow SNSPD array sizes to be scaled while keeping the digitization circuit complexity low. The readout architectures shown so far have been promising, but breaching the thousand-pixel barrier while maintaining high efficiency, high count rate, low jitter, and low dark counts will still require additional innovation as well as disciplined engineering.

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