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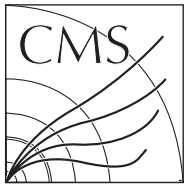

The Compact Muon Solenoid Experiment

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Readout electronics for the CMS Phase II Endcap Calorimeter system overview and prototyping experience

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Abstract

The frontend readout system for the silicon section of the CMS Phase II Endcap Calorimeter faces unique challenges due to the high channel count and associated bandwidth, limited physical space, as well as radiation tolerance requirements. I will give an overview of the frontend electronics design and will discuss the recent experience obtained from the first test system that integrates the HGCROC2 readout ASIC, lpGBT, and VTRX+ in a realistic manner, linking together prototypes of the hexaboard, engine, and wagon boards.

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Readout electronics for the CMS Phase II Endcap Calorimeter: system overview and prototyping experience

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Abstract: The frontend readout system for the silicon section of the CMS Phase II Endcap Calorimeter faces unique challenges due to the high channel count and associated bandwidth, limited physical space, as well as radiation tolerance requirements. I will give an overview of the frontend electronics design and will discuss the recent experience obtained from the first test system that integrates the HGCROC2 readout ASIC, lpGBT, and VTRX+ in a realistic manner, linking together prototypes of the hexaboard, engine, and wagon boards.

Keywords: Front-end electronics for detector readout; Calorimeters; Radiation-hard electronics

Contents

1 Introduction

The CMS Phase II Endcap Calorimeter [1] will fully replace the existing CMS endcap electromagnetic and hadronic calorimeters [2]. The upgraded detector will be an integrated 47-layer sampling calorimeter, which uses Pb, CuW, and Cu as absorber in the electromagnetic part (CE-E) and uses steel and Cu in the hadronic part (CE-H). The active detector material consists of 8-inch hexagonal silicon sensors in the high radiation areas and of scintillator tiles with on-tile silicon photomultipliers in the lower radiation areas. The upgraded calorimeter will provide information in 5 dimensions: highly granular 3D spatial information (0.5–1 cm^2 Si cell size, $23\times23mm^2$–$55\times55mm^2$ scintillator tile sizes), a large dynamic range of up to 10 pC for energy measurements, and timing information to tens of picoseconds. In the following, the frontend electronics for the silicon-based region will be described in more detail, including the results from the first prototypes.

2 Frontend architecture

The purpose of the frontend electronics is to digitize, concentrate, and transmit detector data to the off-detector trigger and data acquisition electronics. The electronics must also distribute clock and control signals (both "fast" and "slow"), and provide monitoring of temperature, currents, and voltages. The requirements include sufficient radiation tolerance (up to 1.5×10^{16} n_{eq}/cm^2 in the inner detector region), ability to fit in the limited physical space between absorber plates, low power consumption, and support the transfer of the required data volume for good physics performance.

The frontend electronics system is designed around a set of ASICs. The HGCROC [3] is the frontend readout chip, which receives signals from the Si sensors and digitizes them, providing ADC, TOT (time over threshold), and TOA (time of arrival) information. There are also two frontend concentrator chips: the ECON-T for the trigger path, which concentrates trigger channel

data via one of 4 trigger algorithms, and the ECON-D for the data acquisition (DAQ) path, which performs channel alignment and zero suppression after the accept signal is received from the Level-1 trigger. The system also makes use of the Rafael chip for clock and fast control fanout, and uses the CERN lpGBT [5] for sending and receiving data, clock, and control signals via optical link through the VTRX+ [4]. The HGCROC and ECON ASICs are custom for this project, but all other chips and components are common developments.

The frontend electronics for the silicon region are designed using a modular approach, which ensures that the geometrical constraints of fitting hexagonal sensors into a circular layer can be met in a cost effective manner. The basic detector unit is the silicon module, which is composed of the silicon sensor and hexaboard printed circuit board (PCB). There are two main types of module, denoted by "low" and "high" density. Low density (LD) modules have 192 channels and use a Si sensor of 200 or 300 μm thickness. High density (HD) modules have an active sensor thickness of 120 μm with 432 channels in order to maximize the signal-to-noise ratio in regions of the detector with higher levels of radiation. Figure 1 shows a schematic view of the frontend architecture for the LD region, along with the 3D model of a section of the detector. In this region, the LD engine board connects to two passive LD wagon boards, which are each connected to 1–4 modules. To ensure that all modules get connected while preserving sufficient space for services such as low voltage wires and optical fibers, the wagon boards will come in many shapes and sizes. This also ensures that the engine, which is a far more complex object, can remain the same regardless of its location in the detector, thereby reducing cost and development time.

3 Frontend boards and prototyping experience

3.1 Hexaboard

The main function of the hexaboard is to gather the analog signals from the silicon sensor and digitize them. The LD (HD) hexaboard contains 3 (6) HGCROCs, which receive the signals from the silicon sensor cells via wirebonds through stepped holes in the PCB. The hexaboard is a complex board with dense routing, made more challenging by the presence of the many stepped holes (one per 2-3 sensor cells). This also constrains the available space for placing other components. For this reason, two mezzanines plug into the LD hexaboard, one containing the ECONs and one containing two bpol12V DC/DC converters [7] along with their shielded coils for powering the module. These mezzanines provide the additional benefit of decoupling the development and testing of these components. The LD hexaboard also contains the Rafael chip, which is used for clock and fast control fanout to each of the HGCROCs. In the HD region, the Rafael chip and the ECONs will instead be placed on the HD wagon. The power for the HD region will come from "deported" bpol12V converters that are mechanically mounted to a LD module, where the radiation levels are below the tolerance of the converter. The output of the bpol12V is regulated via a low-dropout regulator down to 1.2V. The bias voltage for the sensor is brought in via wires.

The "V2" hexaboard prototype, shown in Figure 2 (left), was tested extensively in the lab. Higher than expected noise levels were observed, likely caused by digital switching noise affecting the HGCROC preamplifier ground node due to a large coupling between the analog and digital power planes. A second version of this board was produced ("V2b") with a revised PCB stackup,

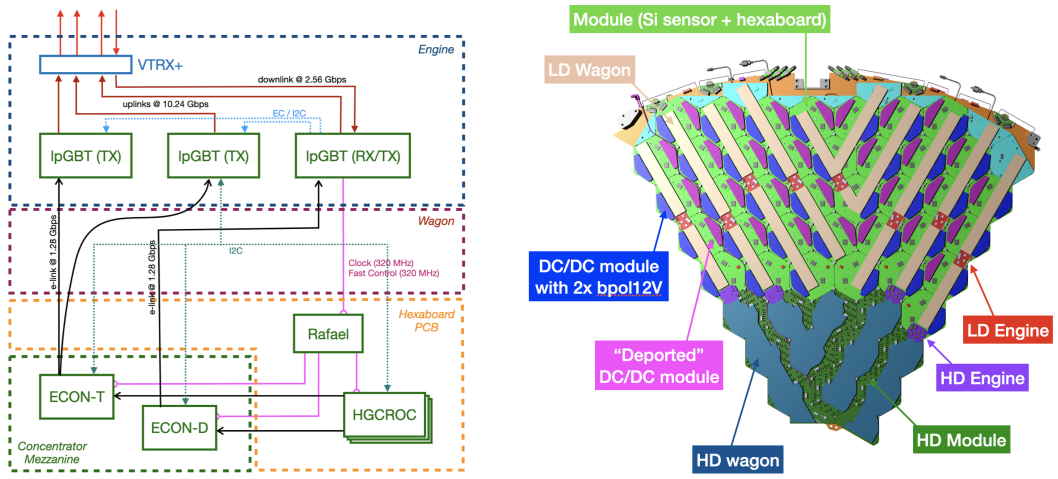

Figure 1. (left) Schematic view of the frontend architecture for the LD region. The *engine* board controls the frontend ASICs and collects trigger and DAQ data. The *wagon* boards connect the engine to up to 4 modules, which each consists of a silicon sensor and a *hexaboard* PCB. (right) 3D drawing for a 60° segment of one layer in CE-E, showing the different components in the frontend readout chain.

where ground planes around and between power and input layers were introduced. Coherent noise levels were much improved with this version. Recently, a new prototype version ("V3") of the LD hexaboard prototype was produced. This prototype design is close to the final design, and includes the final components and connector positions. The initial checkout of the bare PCB looks good, and assembly is ongoing. The design of the HD hexaboard is progressing as well.

3.2 Engine

The engine is a small, highly complex board with fine-pitch (down to 0.4 mm) components and dense routing. The board is designed with a minimum trace width of 0.0035 in and a minimum clearance between copper features of 0.003 in. An LD (HD) engine can support up to 7 LD (3 HD) modules, and contains 1 (2) VTRX+ and 3 (6) lpGBTs to accomplish that. One lpGBT (two for HD) acts as the controller and is operated in transceiver mode, whereas the other lpGBTs act as clients and are operated in transmitter mode. The downlink operates at 2.56 Gb/s, and includes fast control data at 320 Mb/s and slow control data at 80 Mb/s. The uplinks from all lpGBTs on the board are operated at 10.24 Gb/s using FEC5 encoding. They send either DAQ or trigger data serialized from up to 7 elinks (per lpGBT) running at 1.28 Gb/s.

The V2 engine prototype was the first prototype to include both the VTRX+ and the lpGBT, as seen in Figure 2 (middle). It has been extensively tested using a ZCU102 test bench (with Zynq system-on-chip). Tests included measuring bit-error rates on both optical and electrical links, sampling single-ended lines such as resets, and characterizing the behavior of the lpGBT ADC. A working "efuse" configuration that allows for correct startup of the control lpGBT's optical link was also established. The V2 engine did encounter difficulties during manufacturing, in particular, shorts were observed in the PCB after assembly. This issue was resolved by changing the BGA footprint strategy for a second version of the board ("V2b"), making use of solder-mask-defined

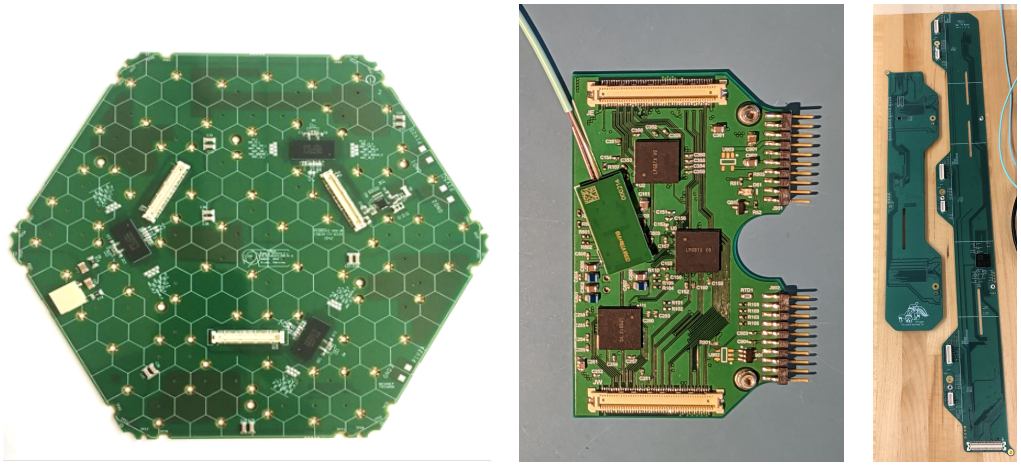

Figure 2. (left) V2 hexaboard prototype with 3 HGCROC2 ASICs; (middle) V2 engine prototype, with 3 lpGBT ASICs and 1 VTRX+; (right) V2 wagon prototypes in two lengths.

pads instead of copper-defined pads. This strategy will be used going forward. The design of the next ("V3") engine prototype is currently being finalized. It includes the final choice for the powering solution as well as all modifications needed to reflect the evolution of the system design.

3.3 Wagon

The wagon boards form the connection between the modules and the engine, and span across up to 4 modules. These are large boards, up to 45 cm long, and will come in different varieties in terms of length, shape (straight or more irregular), and elink allocation to each module. The LD region in particular will require a large number of varieties to accommodate the geometrical and bandwidth constraints. Originally, the system design envisioned using the GBT-SCA [6] slow control ASIC for experiment control and placed this component on the wagon. However, this chip has now been eliminated from the design, and its role taken over by the lpGBTs already present in the system. For the production system, the LD wagon will therefore be a fully passive board. The wagon prototyping has focused mainly on the LD wagon. Two wagon types, spanning 2 and 3 modules respectively, were produced and are shown in Figure 2 (right). Detailed studies were made of the transmission quality and cross talk via bit-error rate measurements using a pseudo-random bitstream. Only a small reduction of the error-free window was found when increasing the traffic on the board.

4 System test experience

The commissioning of a full system test bench including all available prototype components started at Fermilab and CERN in the summer of 2021. Figure 3 shows the setup at Fermilab. Communication with the HGCROC was established and the successful capture of HGCROC data over elinks and optical link was accomplished. To achieve this result, the slow-control EC/IC path of the lpGBT was used to relay I2C messages through the GBT-SCA to properly configure the HGCROCs. It also confirmed the successful transmission of and response to the fast command stream. Along with this effort, the testing software and firmware framework is actively being expanded and streamlined, in order to facilitate more thorough testing.

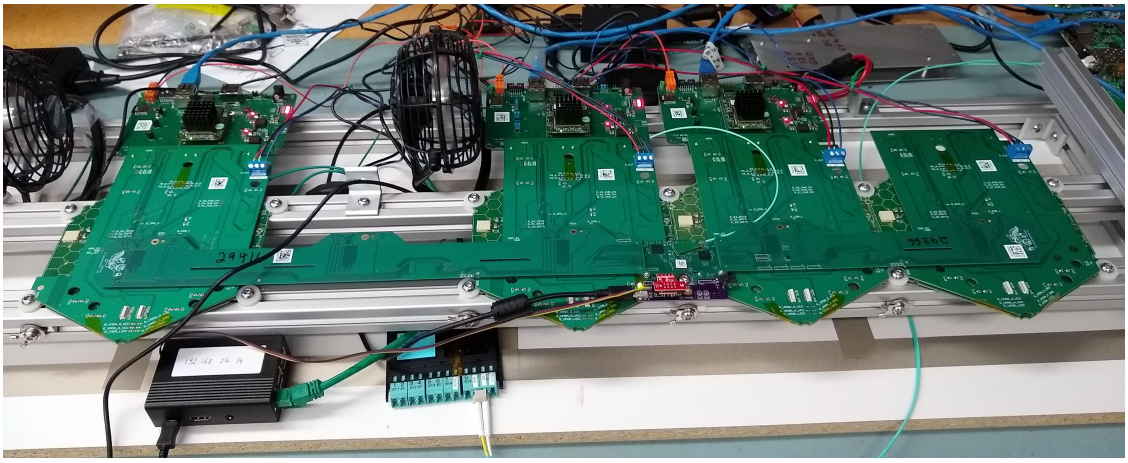

Figure 3. V2 test system at Fermilab, including the V2 engine and two V2 wagons, which are connected to 4 hexaboards via an interposer. This interposer connects to an FPGA that emulates the ECON chips, which are not yet available.

5 Summary and outlook

The frontend electronics for the CMS Phase-II Endcap Calorimeter are advancing well. Prototypes have been produced for all major boards in the system and the full chain of data capture and frontend configuration has been exercised, including the lpGBT, GBT-SCA, and HGCROC ASICs. Additionally, a beam test at the H2 beamline at CERN in September and October of 2021 further advanced the understanding of the full system. This test allowed for the measurement of noise in a realistic environment, the study of the effect of injecting large signals in many channels using an electron beam, and provided a measurement of the signal-to-noise ratio for minimum ionizing particles. In parallel, the overall system design is continuing, with a ramp up in activities related to the integration and detailed design of the partial sensors and the high density region.

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