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Real-time FPGA realization of an UWB transceiver physical layer

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REAL-TIME FPGA REALIZATION OF AN UWB TRANSCEIVER PHYSICAL LAYER

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I, Darryn W. Lowe, declare that this thesis, submitted in partial fulfilment of the requirements for the award of Master of Engineering – Research, in the School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, is wholly my own work unless otherwise referenced or acknowledged. The document has not been submitted for qualifications at any other academic institution.

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Darryn W. Lowe

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List of Abbreviations

ADC	Analog to Digital Convertor
AGC	Automatic Gain Control
ASR	Addressable Shift Register
BER	Bit Error Rate
CCDM	Complementary Code Division Multiplexing
DAC	Digital to Analog Convertor
DSSS	Direct Sequence Spread Spectrum
FCC	Federal Communications Commission
FCS	Frame Check Sequence
FIFO	First-In First-Out
FPGA	Field Programmable Gate Array
HCS	Header Check Sequence
I	In-Phase
ISI	Inter-Symbol Interference
LNA	Low Noise Amplifier
LOS	Line Of Sight
LSB	Least Significant Bit
LUT	Look Up Table
MAC	Medium Access Control
MCIDS	Multicode Interleaved Direct Sequence
MPDU	MAC Protocol Data Unit
MRC	Maximal Ratio Combining

MSB	Most Significant Bit
NLOS	Non-Line Of Sight
OPB	On-chip Peripheral Bus
PAR	Place and Route
PER	Packet Error Rate
PHY	Physical Layer
PRBS	Pseudo-Random Binary Sequence
PSD	Power Spectral Density
Q	Quadrature
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read Only Memory
RTL	Register Transfer Level
S-V	Saleh-Valenzuela
SFD	Start Frame Delimiter
SIFS	Short Inter-Frame Spacing
TDM	Time Division Multiplex
UWB	Ultra-WideBand

Abstract

An original ultra-wideband (UWB) physical layer (PHY) specification is developed and implemented in digital logic. The novelty of this UWB PHY is based on a combination of complementary code division multiplexing (CCDM), which yields a low-interference signal with a variable process gain, and multicode interleaved direct sequence (MCIDS) spreading, which provides an additional fixed process gain as well as multipath robustness. To operate at the high sample rates needed for UWB, the digital logic, realized in a Virtex-II field programmable gate array (FPGA), has a highly-pipelined architecture for real-time signal processing. In addition, the gate count is minimized by avoiding the use of explicit buffer memory wherever possible. The performance of the transceiver is analyzed under a variety of UWB channels and impairments. It is concluded that the proposed UWB PHY offers robust performance in real-world environments and that it is viable for use in future communication systems.

Acknowledgements

Cry havoc! And let slip the dogs of war.

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