Real-Time Power Quality Waveform Recognition with a Programmable Digital Signal Processor

M. Wang, *Student Member, IEEE*, G. I. Rowe, *Student Member, IEEE, and* A. V. Mamishev, *Member, IEEE*

***Abstract*--Power quality (PQ) monitoring is an important issue to electric utilities and many industrial power customers. This paper presents a DSP-based hardware monitoring system based on a recently proposed PQ classification algorithm. The algorithm is implemented with a Texas Instruments (TI) TMS320VC5416 digital signal processor (DSP) with the TI THS1206 12-bit 6 MSPS analog to digital converter. A TI TMS320VC5416 DSP Starter Kit (DSK) is used as the host board with the THS1206 mounted on a daughter card. The implemented PQ classification algorithm is composed of two processes: feature extraction and classification. The feature exaction projects a PQ signal onto a time-frequency representation (TFR), which is designed for maximizing the separability between classes. The classifiers include a Heaviside-function linear classifier and neural networks with feedforward structures. The algorithm is optimized according to the architecture of the DSP to meet the hard real-time constraints of classifying a 5-cycle segment of the 60 Hz sinusoidal voltage/current signals in power systems. The classification output can be transmitted serially to an operator interface or control mechanism for logging and issue resolution.**

***Index Terms*—Digital Signal Processor (DSP), Power Quality (PQ) Monitoring, Event Classification, Classification-Optimal TFR, Artificial Neural Networks.**

I. Introduction

The increasing popularity of power electronics has led to recent focus on power quality (PQ) related disturbances in power systems by electric utilities and industrial power customers. Software and hardware for automatic classification of voltage and current disturbances are highly desired. Existing recognition methods need much improvement in terms of their capability, reliability, and accuracy. Today, power quality has become a very interesting cross-disciplinary topic, coupling power engineering and power electronics with other research areas, such as digital signal processing, software engineering, networking, and VLSI.

Voltage related PQ disturbances are the major causes of disruption in industrial and commercial power supply systems, significantly affecting e-commerce and many manufacturing industries, such as semiconductors, automobiles, and paper. A report by CEIDS (Consortium for Electric Infrastructure to Support a Digital Society) shows that the U.S. economy is losing between $104 billion and $164 billion each year due to outages and another $15 billion to $24 billion due to PQ phenomena [1].

Traditional monitoring methods are based on RMS measurements and constrained by their accuracies. Recently proposed approaches for automated detection and classification of PQ disturbances are based on wavelet analysis, artificial neural networks, hidden Markov models, and bispectra [2-6]. Real-time PQ monitoring hardware should be capable of acquiring voltage or current waveforms, identifying the event type based on the waveform pattern, understanding the cause of the disturbance, and making system protection and prevention decisions.

Digital signal processors (DSP) are distinct from general-purpose microprocessor, mainly due to their capacity for real-time computing. With more optimized architectures towards faster multiplications and accumulations than general-purpose microprocessors, DSPs have wide applications in speech, digital audio, image, and video processing, and telecommunications.

This paper presents a digital signal processor-based hardware system for PQ classification based on a recently proposed PQ classification algorithm by the authors [7]. The algorithm is implemented with a Texas Instruments (TI) TMS320VC5416 digital signal processor (DSP) with the TI THS1206 12-bit 6 MSPS analog to digital converter. A TI TMS320VC5416 DSP Starter Kit is used as the host board with the THS1206 mounted on a daughter card.

This paper demonstrates the feasibility of implementing the proposed PQ classification algorithm in real-time with a DSP-based system and is one of the first case studies of using DSP technologies in the area of power quality monitoring [8,9].

II. The PQ Classification Algorithm

PQ disturbances cover a broad frequency range and significantly different magnitude variations. In this paper, a new PQ classification algorithm is presented with an example application of discriminating five major power system waveform events: harmonics, voltage sags, capacitor high frequency switching, capacitor low frequency switching, and normal voltage variations, as shown in Fig. 1. The complete

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All authors are with the SEAL (Sensors, Energy, and Automation Laboratory), Department of Electrical Engineering, Box 352500, University of Washington, Seattle, WA 98195. (E-mails: mwang@ee.washington.edu; gaber@ee.washington.edu; mamishev@ee.washington.edu)

implementation algorithm presented in this paper is shown in Fig. 2. The two sequential processes: feature extraction and classification are explained in details in the following two subsections.

A. Feature extraction

A.1. Theoretical background

There is an infinite number of possible time-frequency representations (TFRs) corresponding to a signal [10]. For waveform recognition problems, features need to be selected from a TFR that maximizes the separability of signals in different classes and minimizes the similarity of signals in the same class. Therefore, it is desirable to design a classification-optimal representation TFR_c that specifically emphasizes the differences between classes, but not necessarily describes the time-frequency information accurately [11,12].

Time-frequency ambiguity plane has been an important tool in the radar field, in analyzing and constructing radar signals, formulating the performance characteristics of a waveform, and relating range and velocity resolution [13]. It has also been used extensively in the fields of sonar, radio astronomy, communications, and optics [14]. Gillespie and Atlas have recently proposed feature extraction methods based on designing class-dependant TFRs from time-frequency ambiguity plane. This class of new techniques has been successfully applied for tool-wear monitoring and radar transmitter identification [12,15,16].

The connection between the ambiguity plane and time-frequency representations has been recognized for a long time. Any bilinear (Cohen class) TFR $P(t,f)$ can be expressed as the two-dimensional Fourier transform of the product of the ambiguity plane $A(\eta,\tau)$ of the signal and a kernel function $\varphi(\eta,\tau)$ [10]:

$$P(t,f)=\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}A(\eta,\tau)\,\varphi(\eta,\tau)\,e^{j2\pi\eta t}\,e^{j-2\pi f\tau}d\eta d\tau \quad (1)$$

where t represents time, f represents frequency, η represents continuous frequency shift, and τ represents continuous time lag.

Equation (1) shows that the kernel functions determine the TFRs and their properties. A kernel function is a generating function that operates upon the signal to produce the TFR. The characteristic function for each TFR $P(t,f)$ is $A(\eta,\tau)\,\varphi(\eta,\tau)$.

The classification-optimal representation TFR_c can be obtained through smoothing the ambiguity plane with an appropriate kernel φ_i, which is a classification-optimal kernel. The problem of designing the TFR_c becomes equivalent to designing the classification-optimal kernel $\varphi_i(\eta,\tau)$. Features can also extracted directly from the $A(\eta,\tau)\,\varphi_i(\eta,\tau)$, instead of the classification-optimal TFR_c.

Fisher's discriminant function (FDF), which was developed by R. A. Fisher in 1930s, is a method that projects high-dimensional data onto low-dimensional space for classification.

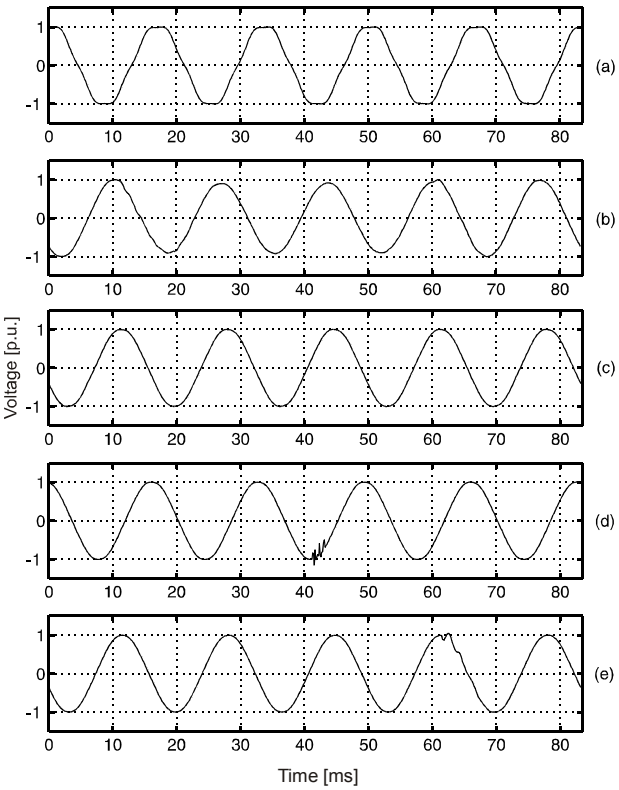

Fig. 1. Five classes of PQ signals for classification: (a) harmonics; (b) voltage sag; (c) normal voltage variations; (d) capacitor high frequency switching; (e) capacitor low frequency switching.

With the Fisher's criteria, locations on the ambiguity plane are ranked according to their importance for this classification task. For example, when designing kernel i, a Fisher's discriminant score is calculated for each location (η,τ) on the ambiguity plane,

$$J_{Fi}(\eta,\tau)=\frac{(m_i[\eta,\tau]-m_{i-remain}[\eta,\tau])^2}{D_i^2[\eta,\tau]+D_{i-remain}^2[\eta,\tau]} \quad (2)$$

where $m_i[\eta,\tau]$ and $m_{i-remain}[\eta,\tau]$ represent mean values corresponding to class i and the remaining classes at location (η,τ), and $D_i^2[\eta,\tau]$ and $D_{i-remain}^2[\eta,\tau]$ represent variance values.

A.2. Detailed training and implementation methods

According to the Fisher's discriminant function, four classification-optimal kernels are designed for four classes/class-groups: harmonics, voltage sags, capacitor switching class-group, and capacitor high-frequency switching, respectively. The discrete version of equations (1) is [12],

$$\begin{aligned}TFR[n,k]&=\mathcal{F}_{\eta\to n}^{-1}\{\mathcal{F}_{\tau\to k}\{A[\eta,\tau]\varphi[\eta,\tau]\}\}\\&=\frac{1}{N}\sum_{\eta=0}^{N-1}\sum_{\tau=0}^{N-1}A[\eta,\tau]\varphi[\eta,\tau]\,e^{-j(2\pi/N)\tau k}\cdot e^{j(2\pi/N)\eta n}\end{aligned} \quad (3)$$

with

$$A[\eta,\tau] = \mathcal{F}_{n\to\eta}\{R[n,\tau]\} = \sum_{n=0}^{N-1} R[n,\tau]\, e^{-j(2\pi/N)\eta n} \quad (4)$$

where n represents sample, k represents discrete frequency, η represents discrete frequency shift, and τ represents discrete time lag. The instantaneous autocorrelation function $R[n,\tau]$ is defined as

$$R[n,\tau] = x^*[n]\, x[\mathrm{mod}(n+\tau, N)] \quad (5)$$

where the function $\mathrm{mod}(p_1, p_2)$ represents modulus after dividing the first parameter p_1 by the second parameter p_2. In this application, the kernel $\varphi_i[\eta,\tau]$ is defined as a binary matrix (each matrix element is either *0* or *1*), therefore,

$$A[\eta,\tau]\varphi_i[\eta,\tau] = \begin{cases} A[\eta,\tau], & if\ \varphi_i[\eta,\tau]=1 \\ 0, & if\ \varphi_i[\eta,\tau]=0 \end{cases} \quad (6)$$

Feature points are ambiguity plane points of locations (η,τ) where $\varphi_i[\eta,\tau]=1$. Therefore, the process of feature extraction is to select points that are optimal for the classification task from the ambiguity plane. The feature ranking mechanism is shown in Equation (2). Locations that receive higher discriminant scores are selected as feature locations.

B. Classification

Multiple classifiers are adopted in the presented method. Each classification node consists of a kernel function and a classifier. Depending on the nature of the kernel, classification node *i* is to either discriminate signals that belong to class *i* from signals that belong to class *{i+1, ..., n}*, or discriminate signals in class *{i, ..., i+m}* from signals in class *{i+m+1, ..., n}*.

Four classifiers are employed in this classification application for five types of PQ events. They are a Heaviside linear classifier (for the class of harmonics) and three feedforward neural network classifiers (for the other three classes) with simple structures.

For a two-class classification problem and an input *f*, the Heaviside linear classifier is defined as

$$H(f-t) = \begin{cases} 1\ (f\ belongs\ to\ class\ 1), & if\ f-t\ge 0 \\ 0\ (f\ belongs\ to\ class\ 2), & if\ f-t<0 \end{cases} \quad (7)$$

where *t* is a real threshold value. Training this classifier is to determine the threshold parameter *t*.

Three feedforward neural network (FNN) classifiers adopted in this algorithm all have three layers. The structure of the FNN for discriminating sags is 2-12-2 (input layer node number-hidden layer node number-output layer node number); the one for capacitor switching is 3-10-2; the one for capacitor high-frequency switching is 3-10-2. The transfer and training functions adopted for the FNN include: the hyperbolic tangent sigmoid transfer function as the transfer function for the hidden layer, the linear transfer function as the transfer function for the output layer, the Levenberg-Marquardt backpropagation as the network training function, the gradient descent learning function as the weight learning function, and the mean squared error function as the performance evaluation function.

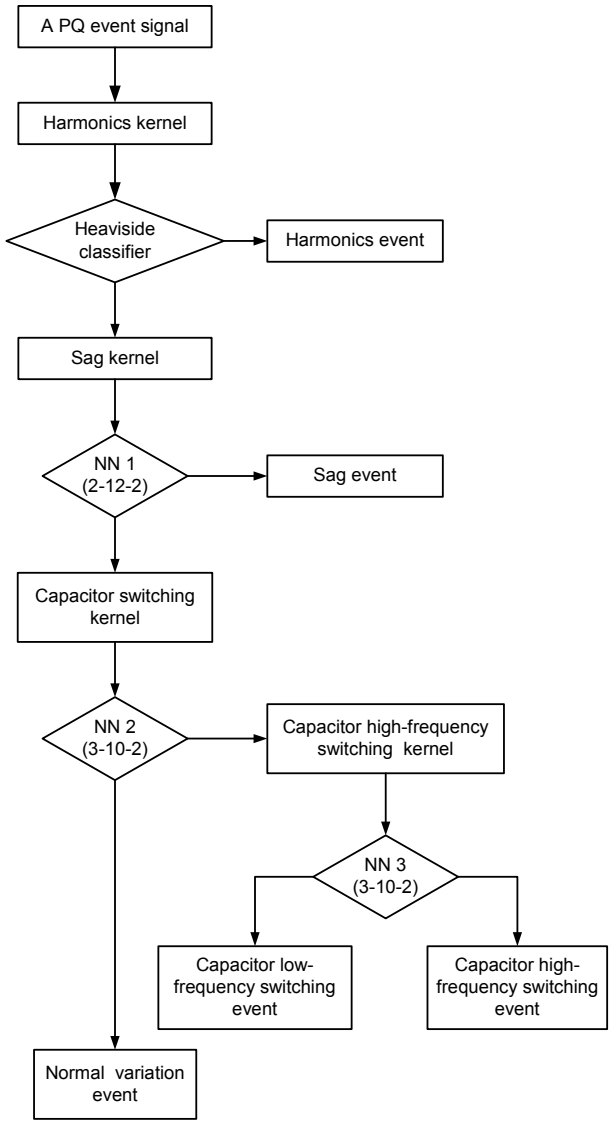

Fig. 2. The proposed PQ classification algorithm (implementation phase).

III. Data Flow and DSP Features

A global block diagram for the monitoring system is shown in Fig. 3. The input signal is first passed through a potential transformer and sampled using a 12-bit analog to digital converter (ADC) daughter card. The 12-bit ADC collects signed integer values with a range from -2047 to 2047. This data is then placed into a 32-word FIFO buffer. Upon filling the buffer, a "data available" signal activates an external interrupt on the C5416 processor External Peripheral Interface bus. Within the interrupt service routine, the FIFO is read

through an input/output (IO) port via the External Memory Interface bus on the C5416 processor. This data is moved into a 640-element array for input to the feature extraction and classification algorithm. While in file mode, text files are sent from a host computer via the USB port to the C5416 using the C standard IO functions conveniently modified for bi-directional transmission along the USB port. While in standalone mode, the resulting classification of a sampled signal would be relayed to a control device via the general purpose IO port on the Host Port Interface as a binary number from 1 to 5 (001…101).

The TMS302VC5416 is a fixed-point DSP processor with 128 KB of on-chip memory and a 160 MHz clock speed, which can perform 160 MIPS. This processor has a 17x17 parallel multiply accumulator unit which allows single cycle multiply accumulate operations. This allows for fast execution of integer multiplications. While floating point multipliers on other processors may allow direct multiplication of floating point values, this DSP processor executes single clock cycle integer multiplications. Optimization to use all integers is therefore necessary. However, if a loss of precision is allowable, this processor will actually execute an integer multiplication faster than a floating-point processor of a similar clock speed due to the parallel multiplier and accumulation units in the place of a pipelined multiplier. The pipelined multiplier on the TMS320VC6711, a 32-bit DSP, requires 4 cycles to complete a 32-bit multiplication. While the pipeline may theoretically allow for faster sequential multiplications, in practice a single multiplication is carried out and stalls the pipeline while it finishes and stores the result to the accumulator or a memory location.

IV. Optimization For Real-time Computing

Because the major task of the presented PQ monitor is to classify disturbances in real-time, significant optimization efforts have been taken when programming the DSP, in order to reduce the algorithm computation time.

A. Reduce the quantities to be calculated

The results of kernel and classifier training show that only nine kernel points from seven columns of ambiguity plane are needed for implementing the classification process. According to equations (5) and (4), it is enough to just calculate seven kernel-related columns from the matrix $R[n,\tau]$ and nine kernel points from the matrix $A[\eta,\tau]$.

If the process window size is *N*, the computation cost for calculating the entire autocorrelation matrix $R[n,\tau]$ is $O(N^2)$ multiplications, and the cost for calculating the entire ambiguity plane matrix $A[\eta,\tau]$ is $O(N^3)$ multiplications and $O(N^3)$ additions. After reducing the number of quantities to be calculated as stated in the previous paragraph, the worst-case computation cost for the autocorrelation step is reduced to $O(N)$ multiplications, and the worst-case cost for the ambiguity plane step is reduced to $O(N)$ multiplications and $O(N)$ additions. Since *N* is equal to 640 in this application, the optimization approximately reduces the computation time *640* times in the autocorrelation step and 640×640=409,600 times in the ambiguity plane step.

B. Use fixed-point integer multiplication as much as possible

Due to the 16-bit fixed-point nature of the processor used in this paper, optimization was required to ensure floating-point values were avoided. The analog to digital converter conveniently produces integer values ranging from -2047 to 2047 to allow a smooth transition into the algorithm execution without conversion. While these values could be stored as 16-bit integers, the subsequent steps required the use of long (32-bit) integers. The discrete Fourier transform (DFT) requires multiply accumulations which would easily exceed 32-bits quite quickly. The long integer values were broken into seven bit integers to allow for use of the single cycle multiply-accumulate (MAC) function. Each accumulation represents a portion of the final summation after being multiplied by 2^7 and is then normalized for storage into a floating-point value. For each DFT operation, this normalization and addition step would occur once for the real part and once for the imaginary part. This all-integer optimization cut the algorithm execution time in half.

C. Use hard-coded sin table and cos table

The discrete Fourier transform (DFT) is implemented with *cos* and *sin* functions instead of the exponential function, according to the Euler's Equation.

Due to the focus on accuracy in the standard C math header file, the *sin* and *cos* are quite costly in processor time. Because the on-chip memory had not been completely consumed by other operations of the algorithm, the use of a lookup table for these functions was chosen. The values were stored as signed integers ranging from -32767 to 32767. Due to the 12-bit ADC resolution, this range was adequate.

V. Results and Discussions

A. Real-time monitoring capability

The classification process of an 83.33 ms window takes 10.9 ms when the ADC is not running on the same board, which satisfies the real-time constraints in most power quality monitoring tasks. Within the 10.9 ms, 1.7 ms are used for the autocorrelation step, 8.5 ms for the DFT step, and 0.70 ms for classifier step. In Fig. 4, the classification process of the same five-cycle window takes 11.2 ms, which is measured when the ADC is running on the same board and interrupting 960 times per second. This requires a real-time constraint of moving the data from the FIFO buffer into program memory within a 1/960 sec window.

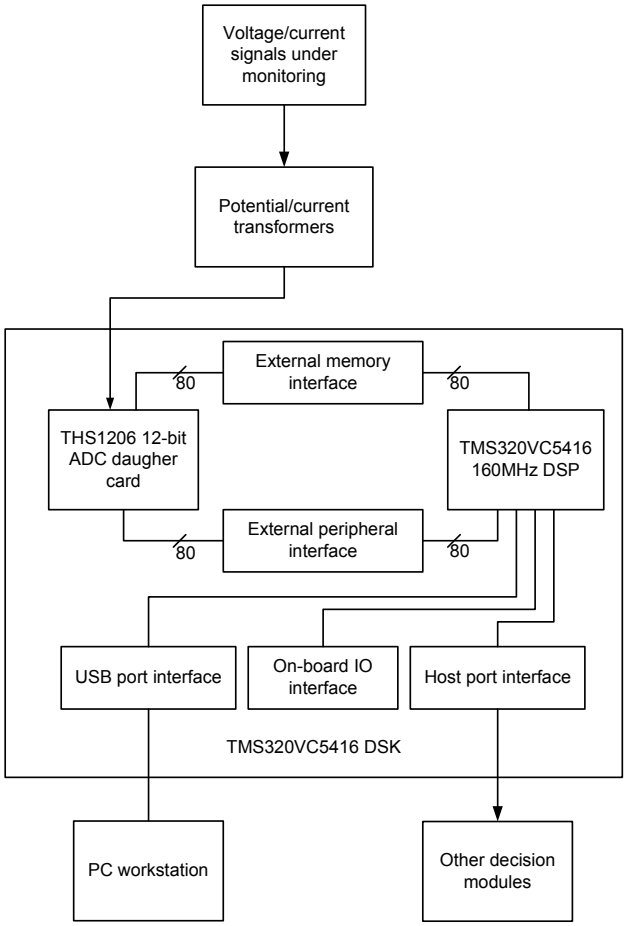

Fig. 3. Block diagram of the hardware PQ monitoring system.

B. Classification performance

In this study, the classification experiment is conducted with five-class examples, as shown in Fig. 1, under file mode via USB port. A total of 860 real world voltage signals were collected from industrial databases for system testing. A single text file represents a voltage signal to be identified. It consists of five cycles of voltage waveform sampled 128 times per cycle, and has a length of 640 sampling points. A window size of 83.3 ms (five sinusoidal waveform cycles in a 60 Hz system) was adopted due to the following two reasons. First, a five-cycle window is long enough to capture the characteristics of all types of PQ events under our study. Second, a five-cycle window is short enough for generating real-time monitoring outputs for many PQ-related applications. The 83.3 ms window size used in this paper for demonstration of the algorithm, can be adjusted appropriately for specific applications. For example, when this method is applied for the discrimination of different types of high frequency power system transients, the window size can be reduced to one or two cycles.

The classification results from Matlab simulations and from the DSP system (both 12-bit and 14-bit) are presented in Table 1. Matlab uses 64-bit for the double calculations, but the presented system uses 12-bit precision.

C. Discussions

The ADC daughter card allows for rapid evaluation of different ADCs with a host DSK. However, limitations due to processor context changes for interrupt service routines occur and typically limit these ADCs to 1MSPS (without Direct Memory Access ports). For the purposes of this paper, this was not an issue. However, this DSK may not be adequate for the high sampling rates associated with power protection applications. A custom printed circuit board would be required for this application and the use of non-interrupt based techniques, such as polling, would most likely be required to manage context switching delays.

TABLE 1. RESULTS OF A CLASSIFICATION EXPERIMENT WITH REAL WORLD POWER QUALITY DATA

Classes	Testing events	Matlab	DSP with 12-bit ADC	DSP with 14-bit ADC
Harmonics	200	100%	100%	100%
Sags	144	100%	100%	100%
Cap. slow switching	180	96.1%	92.2%	93.3%
Cap. fast switching	138	96.4%	92.8%	92.8%
Normal variations	198	98.0%	90.4%	96.5%
Total	860	98.0%	95.0%	96.5%

Programmatically, the optimizations enacted to yield faster algorithm performance could be carried further with the use of all assembly language routines and intrinsic functions. Average calculation times could also be decreased by performing only the portion of the algorithm required for each classification step and checking the neural network output immediately. While this would yield faster average computation times, this would increase the execution time length for the worst case as the function calls to perform these short queries would slow the DFT step even further. The assumption that only one power quality class will occur within a five-cycle window introduces the possibility of inaccurate classification.

VI. CONCLUSIONS

A DSP-based hardware monitoring system for power quality event identification is presented in this paper. The algorithm is implemented with a Texas Instruments (TI) TMS320VC5416 digital signal processor (DSP) with the TI THS1206 12-bit 6 MSPS analog to digital converter. In the algorithm, by designing classification-optimal TFRs, features are selected from the time-frequency ambiguity plane based on the Fisher's principle. Four linear and neural network classifiers are used as classifiers. The algorithm is optimized according to the architecture of the DSP to meet the real-time constraints of classifying a five-cycle segment of the 60 Hz sinusoidal voltage/current signals in power systems.

The proposed system is successfully tested with a five-class PQ classification experiment. A waveform window of 83 ms (640 sample points) can be classified in 10.9 ms. Recognition rate of 96.5% with 14-bit ADC and 95.0% with

12-bit ADC are achieved on 860 testing PQ waveforms. The real-time power quality monitoring system has potential applications of enhancing power system protections and accumulating PQ event statistics for power quality assessment.

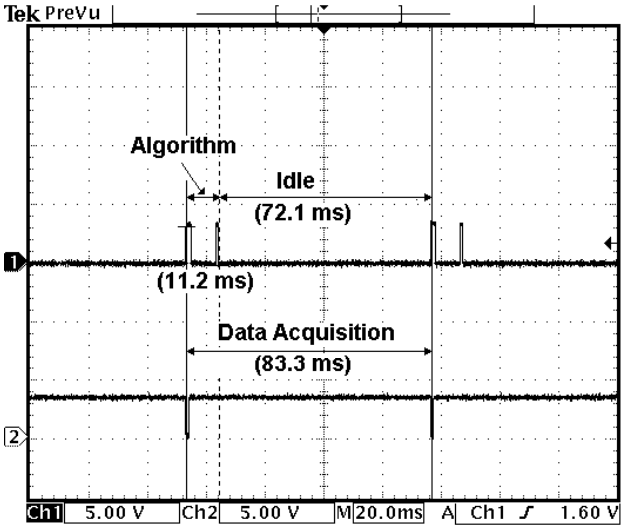

Fig. 4. Real-time monitoring duty cycle.

VII. Acknowledgments

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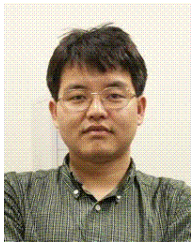
IX. Biographies



Min Wang received a Bachelor's degree from Tsinghua University, Beijing, China, in 1999, and a M.S.E.E. degree from the University of Washington, Seattle, in 2001. Currently he is a Ph.D. student and research assistant at the Department of Electrical Engineering, University of Washington. His research interests include pattern recognition, time-frequency analysis, digital signal processing, and power quality monitoring. He is a recipient of the First Prize Award in the Student Paper-Poster Competition in the 2002 IEEE Power Engineering Society Summer Meeting in Chicago.

Gabriel I. Rowe is an undergraduate student in the Department of Electrical Engineering at the University of Washington, Seattle. He will receive his BSEE in June 2003. His research interests include sensors and DSP for applications in power quality monitoring and the biomedical field. He is a recipient of the EEIC Scholarship in 2002.

Alexander V. Mamishev received an equivalent of B.S. degree from the Kiev Polytechnic Institute, Ukraine, in 1992, M.S. degree from Texas A&M University in 1994, and a Ph.D. degree from MIT in 1999, all in electrical engineering. Currently he is an assistant professor and director of SEAL (Sensors, Energy, and Automation Laboratory) in the Department of Electrical Engineering, University of Washington, Seattle. Prof. Mamishev is an author of about 50 journal and conference papers, and one book chapter. His research interests include PQ monitoring, sensor design and integration, dielectrometry, and electrical insulation diagnostics. He serves as an Associate Editor for the IEEE

Transactions on Dielectrics and Electrical Insulation and a reviewer for the IEEE Transactions on Power Delivery. He is a recent recipient of the NSF CAREER Award and the IEEE Outstanding Branch Advisor Award.