5-2012

Real-Time Selective Harmonic Minimization for Multilevel Inverters Using Genetic Algorithm and Artificial Neural Network Angle Generation

Faete Jacques Teixeira Filho
ffilho@utk.edu

To the Graduate Council:

I am submitting herewith a dissertation written by Faete Jacques Teixeira Filho entitled "Real-Time Selective Harmonic Minimization for Multilevel Inverters Using Genetic Algorithm and Artificial Neural Network Angle Generation." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Leon M. Tolbert, Major Professor

We have read this dissertation and recommend its acceptance:

Burak Ozpineci, Bin Hu, Fred Wang

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

Real-Time Selective Harmonic Minimization for Multilevel Inverters Using Genetic Algorithm and Artificial Neural Network Angle Generation

A Dissertation Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Faete Jacques Teixeira Filho

May 2012

Acknowledgements

This thesis would not possible without the support, guidance and feedback of the professors, staff, colleagues and friends. First and foremost I am very thankful to Dr. Tolbert for the opportunities offered and the assistance given during the course of my studies. I owe my deepest gratitude to Dr. Burak, Dr. Wang and Dr. Hu for their valuable advice. I was very grateful to have a dedicated staff in the department that was always ready to assist the students. I am indebted to many of the people who worked with me in the laboratory, my coworkers and friends that in some way help me or assisted me.

Last but not least, I would like to thank my family in Brazil and also the very encouraging friends in US for giving me the support and the strength to accomplish my goals.

Abstract

This work approximates the selective harmonic elimination problem using Artificial Neural Networks (ANN) to generate the switching angles in an 11-level full bridge cascade inverter powered by five varying DC input sources. Each of the five full bridges of the cascade inverter was connected to a separate 195 W solar panel. The angles were chosen such that the fundamental was kept constant and the low order harmonics were minimized or eliminated. A non-deterministic method is used to solve the system for the angles and to obtain the data set for the ANN training. The method also provides a set of acceptable solutions in the space where solutions do not exist by analytical methods. The trained ANN is a suitable tool that brings a small generalization effect on the angles' precision and is able to perform in real time (50/60 Hz time window).

Table of Contents

List of Tables

List of Figures

Chapter 1

Solar power, multilevel inverters and harmonic control: An introduction

This chapter will discuss current solar power development level, key features of multilevel inverters and introduce the cascade H-bridge converter. Next, the Fourier decomposition of the output waveform will be derived for an 11-level inverter for selective harmonic elimination of its higher order components. Unequal and equal DC source cases will be covered and compared with standard sinusoidal pulse width modulation. As a final point, the need and significance of real time angle calculation will be covered.

1.1 Solar-electric power market

Solar power is the process in which sunlight is converted into electricity, either directly using photovoltaic (PV) cells, or indirectly, for example, using concentrating solar power (CSP).

Solar panel research and development was documented in the 18th century by Charles Fritts. Almost a century later, a silver-selenide version was constructed by Bruno Lange at 1% efficiency. Later, in the 1940s with more research invested in solar technology, efficiencies of 4.5-6% were achieved at 286 USD/watt [58]. Further investments into research and development of solar electric cells brought this technology to a commercial level with prices of 2.49 USD/watt as shown in Figure 1. According to [59], 245 solar modules in the market today are priced below

$2.00 per watt. The price drop, which is shown in this figure, according to recent surveys [59] shows that there is little evidence that it will slow down.

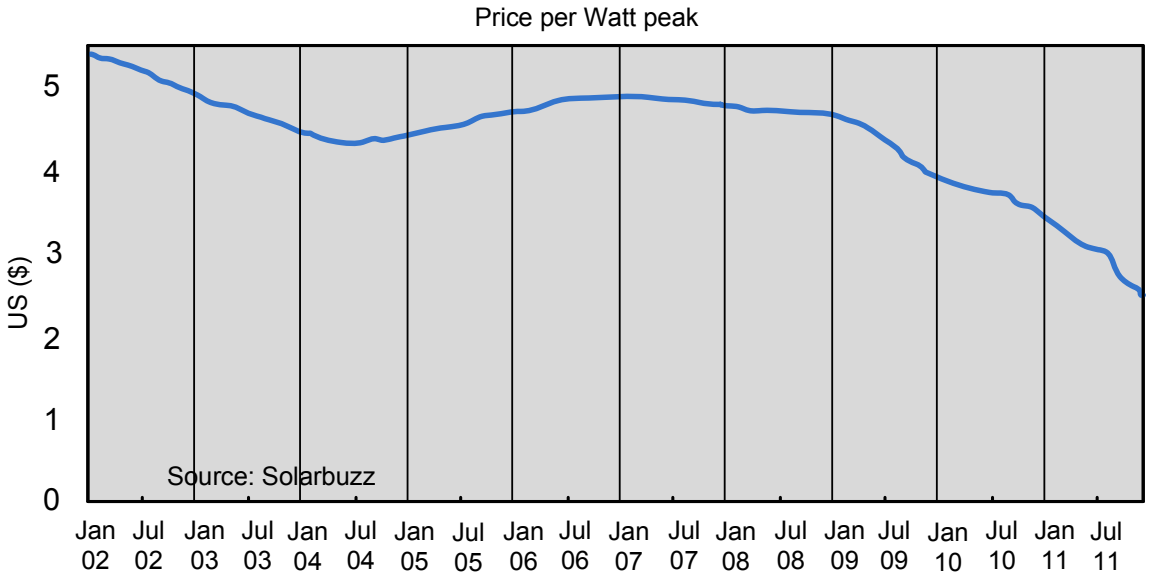


Figure 1 – Solarbuzz retail module price index [59].

A total of 15.9 GW in solar installations were accomplished in 2010 according to PVinsights, which reported a growth of 117% in solar PV installation on an annual basis. The 2010 Solar Electric Power Association (SEPA) report on solar power energy installed by utilities compiled all the solar power plant investments done by utilities in 2010 [58]. It shows that the solar electric market continues to expand across the country and is being seen as an important factor in the supply of energy, planning and customer management utilities. This report also points to two trends that are shifting the profile of solar electric energy in US: centralized projects and utility ownership. Centralized projects are gaining momentum as more utility companies invest in PV power plants such as the one shown in Figure 2 and Figure

3. Although the cost of the power electronics in those systems is not the dominant part, it has the shortest lifetime. While solar panels are warranted 25-35 years, the converters usually come with a 10-15 year warranty. A modular design for power converters would allow an increased reliability while reducing maintenance costs. Multilevel converters are one of the alternatives available that can achieve a low cost at a modular level.

Figure 2 – 48 MW Copper Mountain solar electric power plant project in Nevada [71].

Figure 3 – 30 MW Cimarron solar electric power plant project in New Mexico [72].

A cost breakdown for a typical PV installation is shown in Table 1. The module cost contributes to almost half of the price leaving the other half to installation costs and balance-of-system (BOS). All the components with the exception of the solar modules and power electronics are considered BOS. It is worth to note that the power electronics have a lifetime of almost half of the solar modules. This reliability issue could be addressed by modularity in design of power converters such as the one proposed in this work.

Table 1. Installed system price ($/W)[60].

	2010
Module	$1.70
BOS/Installation	$1.48
Power Electronics	$0.22
Total	**$3.40**

1.2 Photovoltaic inverters for high power

Research has been conducted in photovoltaic (PV) inverters to address key points such as cost, robustness, and efficiency. The modularity and low cost of multilevel converters positions them as a candidate for the next generation of efficient, robust, and reliable grid-connected solar power converters. The multilevel inverter architecture has the potential provide active, reactive support and smart grid capabilities that enhance grid stability. By deploying this architecture, system reliability is enhanced and production costs are lowered. This system architecture can reduce the cost and improve the performance of medium and large PV systems. In addition to regulating real power flow, it is also possible to achieve voltage regulation, frequency regulation, harmonic compensation, and damping of transients.

Many new multilevel topologies have been introduced as variations of the three popular multilevel converter architectures (cascaded, diode clamped and capacitor clamped). These architectures have been commercialized for applications

such as STATCOMs (static synchronous compensators) and large variable speed drives [2-3]. Journals and conference papers have discussed various configurations of inverters for solar applications that focus on efficiency and better utilization of individual panel power. Most attention has been given to a centralized DC bus with modularized DC-DC converters as a more efficient and cost effective way to connect solar panels. In this proposal, the use of DC-AC cascade multilevel inverters is proposed as an attractive option to a centralized DC bus. The same or better performance can be realized with one modularized and easily maintained inverter.

A centralized DC bus approach requires individual control boards for each device connected to the bus, and a centralized DC-AC inverter. Although the DC-DC converters can be modularized, the DC-AC inverter is often overrated in case more photovoltaic panels are added later. For this reason, cost may be higher with the standard architecture.

1.3 Multilevel converters

Multilevel converters make it possible to achieve medium voltage generation using low to medium voltage switches, preventing high *dv/dt* stress and the need for series connection of switches while allowing higher converter power rating. Multilevel converters have less filter requirements, generate a staircase waveform, have better harmonic profile (lower total harmonic distortion), and have less switching losses. However, they need more components, driver isolation becomes complex since additional levels need isolated power supplies, and the cost is higher compared to conventional single-cell topologies.

Cascade H-bridge (CHB), diode-clamped and capacitor-clamped are among the most common topologies and are well documented in the literature [44]. More emphasis will be given here to the features related to the CHB, since it is the topology to be used here for harmonic control.

The cascade multilevel topology and its universal module have several advantages over the traditional customized converter architecture including:

• Increased reliability: if one module fails, the system can reconfigure itself and continue operation until the faulty module is replaced.

• Reduced cost: the modular topology eliminates the need for a custom design for each installation, resulting in higher unit volumes with lower manufacturing costs.

• Serviceability: modules can be easily replaced thus reducing system downtime, increasing the availability of power, and reducing the cost of maintenance.

• Increased system lifetime: a standardized design will enable incremental continuous improvements in module hardware as experienced with standard utility equipment.

• Modularity and scalability: more PV capacity can be added in parallel to increase current carrying capacity or in series for higher voltage applications.

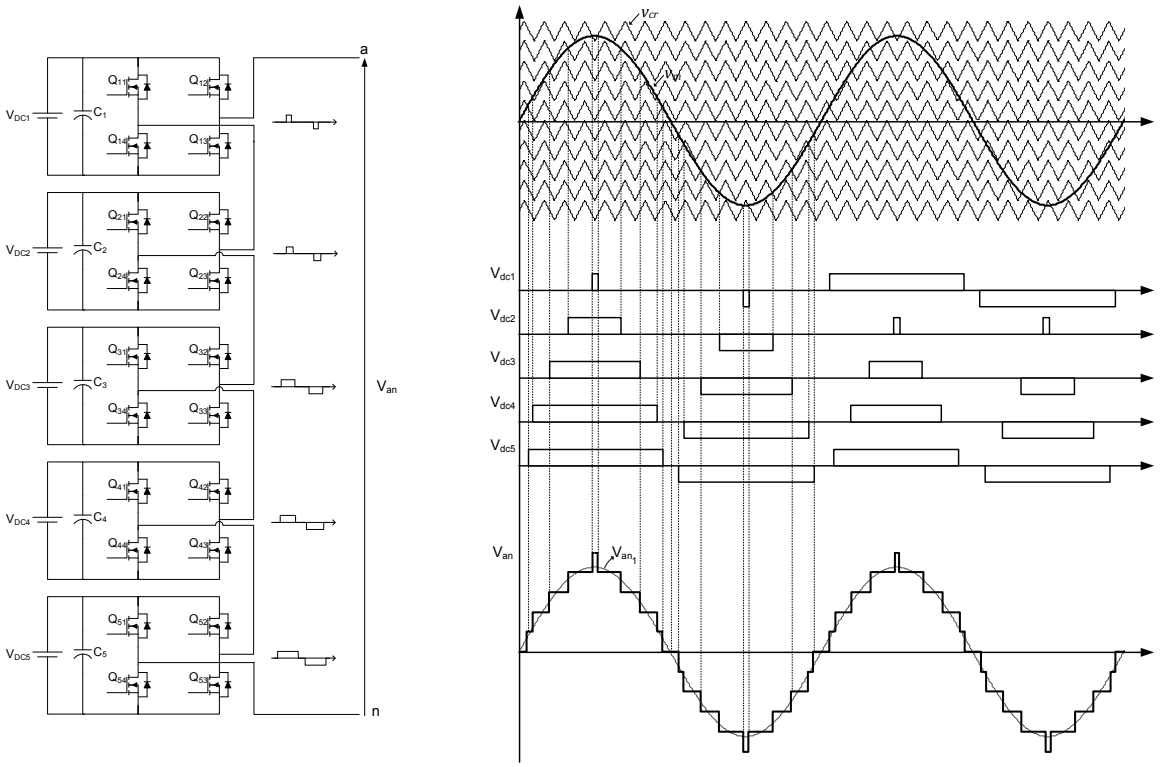
• Energy storage and backup power interface: adding energy storage (capacitors or batteries) is as convenient as adding another PV module.

1.3.1 Cascade multilevel inverter motivation in solar applications

The cascaded H-bridge multilevel inverter topology requires a separate DC source for each H-bridge so high power and/or high voltage can result from the combination of the multiple modules in a multilevel inverter. To maximize the energy harvested from each string, a maximum power point tracking (MPPT) control algorithm can be utilized for solar applications. The cascaded topology allows independent MPPT control for each separate PV array, which can increase the efficiency of the PV system in case of mismatches due to variability and shading. Development of modular H-bridge units will help yield standard power electronic converters that will have lower installation and operating costs for the overall system. Incorporating autonomous fault current limiting and reconfiguration capabilities into the modules and having redundant modules will lead to a durable and robust converter that can withstand the rigors of utility operation for more than 30 years and meet the lifetime requirements of the utility industry [61].

1.4 Cascade multilevel inverter topology

The 11-level cascade inverter topology is presented in Figure 4 (a). It has five full bridge series connected configuration with five isolated input DC supplies that may have different voltage levels. Each switch is subject to the *dv/dt* caused by its own power supply adding up in series to generate the staircase waveform. Level-shifted carriers v_{cr} are compared with the modulating signal v_m to generate the gate signals to the H-bridges, as shown in Figure 4 (b).



(a) (b)

Figure 4 - Eleven level cascade H-bridge inverter (a) and level shifted modulation (b).

An *m*-level topology requires *2*(m-1)* switches and *(m-1)/2* isolated power supplies. The eleven-level inverter shown above requires twenty switches and five DC sources. The number of levels of the output voltage can be increased without the addition of extra isolated supplies by using lower voltage level multiples. For example, with two H-bridges with voltages E and 2E, it is possible to generate seven levels instead of five. Two additional levels are introduced by the voltage difference. In this case, the inverter loses its modularity and the redundant states are reduced. Although unequal voltage sources will be covered in this work, modulation will still

be done using staircase modulation, without considering the additional steps produced by the voltage difference due to constant variation of voltage over time.

Modulation can be accomplished using phase shifting or level shifting. Figure 4 (b) shows the level-shifted in-phase disposition modulation. Each level has its own set of carriers v_{cr} to produce both positive and negative pulses. Additionally, duty cycle swapping can be employed to allow equal average power drawn from each cell module, as shown in the second cycle of Figure 4 (b). Modulation can also be accomplished by determining the angles so as to generate the staircase waveform with predefined harmonic contents, as will be shown in the following sections.

1.4.1 Innovation on system architecture for solar electric conversion

Cascade multilevel converters feature several DC links, making possible the independent voltage control and the tracking of the MPP in each PV string, which can maximize the efficiency of the whole PV system. In addition, the output waveform will consist of voltage steps for each of the levels or H-bridges as well as multilevel PWM to achieve a higher fidelity waveform or eliminate harmonics in the output even if the DC link voltages are unequal. Multilevel PWM and harmonic elimination are techniques that can be used in cascade multilevel inverters in order to achieve voltage waveforms with low total harmonic distortion (THD) with minimum switching losses and low filtering requirements [5-12].

Using a multilevel layout, an effective high switching frequency can be achieved in the output voltage waveform with each of the H-bridge modules having a relatively low switching frequency as shown in Figure 5. This approach will enable

increased converter efficiency. Reducing the filtering requirements would help to reduce the cost and improve the reliability and dynamic performance of the whole system.

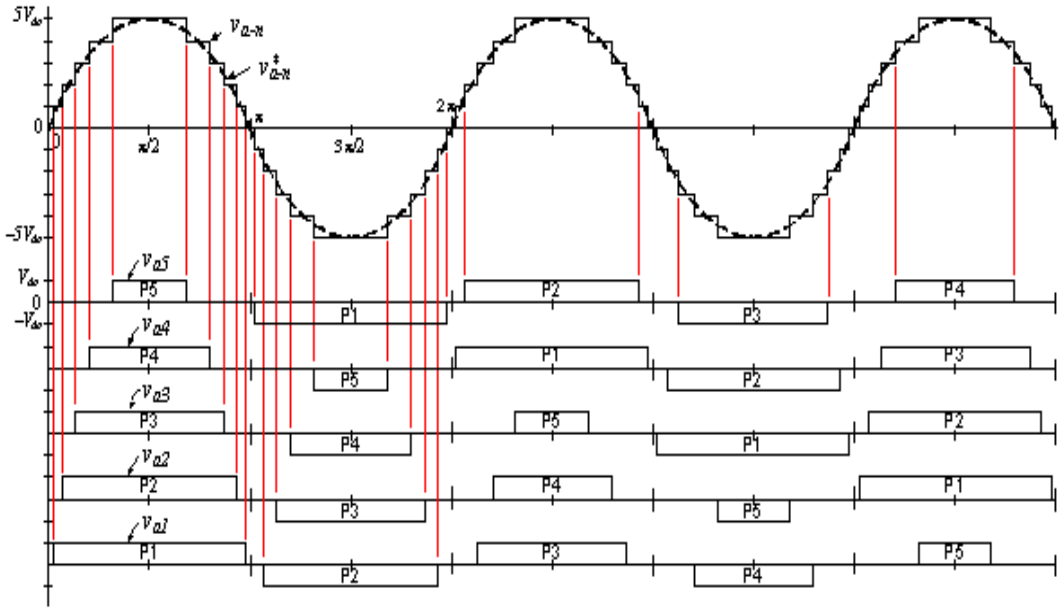


Figure 5 - Low loss low switching frequency multilevel inverter waveforms.

1.5 Performance and reliability

The cascaded H-bridge multilevel inverter has the potential to increase the reliability of the grid-connected PV system by bypassing a faulty H-bridge or failed PV array [62]. Output phase voltages of the multilevel inverter can be used as diagnostic signals to detect faults and their locations. Previous work has shown that all fault features in both open and short circuit cases can be detected using Fast Fourier Transform and a neural network. After failure identification and isolation of

a single module, the remaining modules in a converter installation can continue to operate.

Generally, passive protection devices in a utility installation will disconnect the power sources whenever a fault occurs. Cascaded multilevel inverter architecture has the ability to tolerate a fault for several cycles but if the fault type and location can be detected and identified, switching patterns and the modulation index of other active cells can be adjusted to maintain the operation under a balanced load condition. The remaining switches can be controlled such that the faulty switch is bypassed. Additionally, the control signal can be adapted such that for lower modulation indices, there is no noticeable difference in the output voltage after fault reconfiguration. For higher modulation indices the converter can continue to operate in an over modulation mode which may result in some moderate increased distortion in the output voltage of the converter. With faster control hardware presently available, it is anticipated that fault detection and the reconfiguration described could be done in less than 50 ms and possibly as fast as 30 ms. This enables the system to continue to operate even with hardware failures. This is a unique feature of multilevel converters that can help ensure higher reliability for utility applications even though the converter has more switches than conventional converters.

Another innovation enabled by this topology is the use of energy storage such as batteries or capacitors. With a capacitive small energy source connected in parallel with the renewable energy source, a multilevel converter can provide static

VAR compensation even when there is no power from the photovoltaic source. With banks of batteries or large capacitors on the DC bus, the multilevel converter can provide significant ride-through capability for voltage sags or load swings experienced at the utility interface connection [63-64].

The proposed architecture would also potentially improve power quality on the grid since both the line voltage and current are almost sinusoidal with the use of small output filters on the experimental converter. Electromagnetic interference (EMI) and common-mode voltage are also inherently less because of the low switching frequency, low dv/dt, and near sinusoidal voltage output. The switching angles that generate the staircase waveform of the cascade inverter can be controlled to eliminate low order harmonics as shown in the next sections.

1.6 Symmetry considerations in a 60Hz sinusoidal grid system

Before starting the mathematical treatment to characterize harmonic content in multilevel converters, some assumptions must be taken in order to formulate the problem as a practical application.

The output voltage waveform for many applications, such as motors and most loads, has a periodic, polarity-changing nature. In a full bridge topology, it is reasonable to assume that during one cycle of the fundamental frequency no voltage variation occurs, so the waveform with quarter wave symmetry can be obtained. Those assumptions are illustrated in Figure 6 (b).

(a) *(b)*

Figure 6 – Generic waveform (a) and H-bridge inverter waveform with quarter wave symmetry (b).

Figure 6 (b) shows the basic assumptions of constant DC voltage over a full cycle and quarter wave symmetry that will be assumed in the work proposed here. Thus, the DC voltage level and the switching angle are the parameters needed to fully characterize the waveform shape and the harmonic profile that will be analyzed.

1.7 The Fourier series

This mathematical tool was first introduced by Joseph Fourier (1768-1830) to solve a heat equation in a metal plate. It decomposes any periodic function into a sum of periodic sine and cosine functions [35]. For any periodic integrable function *f(x)* in the interval [0,2π], *f(wt)* can be written as a sum of sine and cosine functions such that *f(wt)* approximates *f(x)* as the number of coefficients *N* tend to infinity:

$$f(wt) = \frac{a_0}{2} + \sum_{n=1}^{N} \left[a_n \cos(nwt) + b_n \sin(nwt) \right] \quad (1)$$

The sine and cosine coefficients a_n and b_n are the Fourier coefficients and are defined as follows:

$$a_n = \frac{1}{\pi}\int_0^{2\pi} f(wt)\cos(nwt)dwt \quad (n \geq 0) \tag{2}$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} f(wt)\sin(nwt)dwt \quad (n \geq 1) \tag{3}$$

Equation (1) shows that a periodic function can be broken into an infinite number of trigonometric components at different frequencies or multiples of *w* (*nw* or $n2\pi f$). The waveform *f(x)* can be understood as composed of a fundamental frequency component (n=1), a DC component (a_0), and harmonic components (n≥2).

For the square wave shown in Figure 2 (b), operating under a constant DC input source, the output voltage in terms of the harmonic contents can be derived from Equation (1) as:

$$f(wt) = \sum_{n=1,3,5,\ldots}^{\infty}\left[\left(\frac{4V_{dc}}{n\pi}\cos(n\alpha_1)\right)\sin(nwt)\right] \tag{4}$$

Only odd harmonics are present as a consequence of the constant DC power supply considered; also a_0 is zero as a result of the wave form symmetry. The peak value of the sinusoidal is determined by b_n alone.

1.8 Harmonic decomposition general formulation

Equation (4) shows the harmonic content for the waveform shown in Figure 6 (b). Quarter wave symmetry was assumed as it is the case in a full bridge with constant DC source. In a cascade inverter, there may be more than one level with different DC voltages for each level. In addition, there may be more than one switching angle for each level.

In [16], a general formulation is derived for a single- and three-phase system for an *m* switching cells with α_n switching angles case as in Equation (5):

$$b_n = \frac{4}{n\pi}\left(V_1 \sum_{i=1}^{p_1} (-1)^{i+1} \cos(n\alpha_i) \pm V_2 \sum_{i=p_1+1}^{p_2} (-1)^{i} \cos(n\alpha_i) \pm \ldots \pm V_m \sum_{i=p_{m-1}+1}^{p_m} (-1)^{i} \cos(n\alpha_i) \right) \quad (5)$$

where,

b_n: peak value of the *n*-th harmonic component

n: harmonic component

V_m: voltage level of the *m*-th converter cell

p_m: number of switching angles on the *m*-th converter cell

α_i: *i*-th switching angle

The ± polarity symbol is positive if P_{m-1} is an odd number. As long as the waveform has quarter wave symmetry, Equation (5) can be used for any number of switching angles per cell for any number of cells under any voltage level. Voltage variation under the same period is not taken into account in this equation.

1.9 Eleven level cascade inverter equations

This topology has, as mentioned previously, five cells and they can have five DC inputs varying in a practical scenario. First, it will be considered that the inputs have the same value and if variation occurs it happens equally between them, and then a second set of equations will be derived to consider variation as indicated in Figure 7.

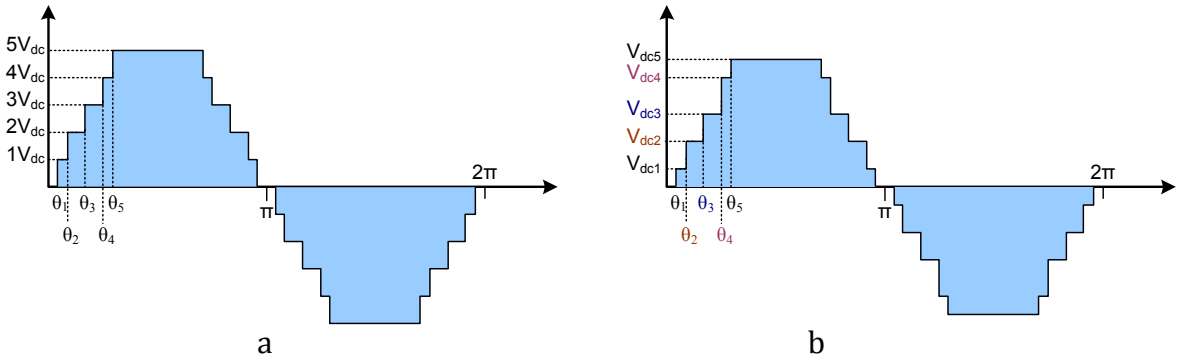


Figure 7 – Output waveform generation for (a) equal and (b) unequal input DC sources.

By manipulating Equation (5) for an eleven-level CHB with five switching angles, case *a* in Figure 7 becomes:

$$V(wt)=\sum_{n=1,3,5,\ldots}^{\infty}\left[\frac{4V_{dc}}{n\pi}\left(\cos(n\theta_1)+\cos(n\theta_2)+\cos(n\theta_3)+\cos(n\theta_4)+\cos(n\theta_5)\right)\sin(nwt)\right] \quad (6)$$

And for case *b*:

$$V(wt)=\sum_{n=1,3,5,\ldots}^{\infty}\left[\frac{4}{n\pi}\left(V_{dc1}\cos(n\theta_1)+V_{dc2}\cos(n\theta_2)+V_{dc3}\cos(n\theta_3)+V_{dc4}\cos(n\theta_4)+V_{dc5}\cos(n\theta_5)\right)\sin(nwt)\right] \quad (7)$$

The modulation index m_i can be defined for Equation (7) as the peak value of the fundamental voltage (b_1) divided by the peak value of the maximum fundamental voltage achievable for each cell. If each cell is switching a square wave with amplitude V_{dc}, then the peak value of the fundamental component will be $4V_{dc}/\pi$. The modulation index defined in Equation (8) will be then in the range $0 \leq m_i \leq 1$. A modulation index equals to one means that all converter cells are switching with a zero degree switching angle (square wave) [16]. That differs from the definition for sinusoidal pulse-width modulation (SPWM) where $m_i=1$ is the linear region limit where over-modulation starts.

$$m_i = \frac{b_1}{\frac{4}{\pi}\sum V_{dc_n}} \tag{8}$$

1.10 Selective harmonic elimination for equal and unequal DC sources

As shown in Equation (7), the output voltage is composed of a fundamental component (*n=1*) and harmonic components (*n>1*). Each component of the output voltage can be expressed by:

$$V_{n-th}(wt) = \left[\frac{4}{n\pi}(V_{dc1}\cos(n\theta_1) + V_{dc2}\cos(n\theta_2) + V_{dc3}\cos(n\theta_3) + V_{dc4}\cos(n\theta_4) + V_{dc5}\cos(n\theta_5))\right]\sin(nwt) \tag{9}$$

where $V_{n\text{-}th}$ is the *n-th* harmonic component, V_{dc1} is the voltage level of cell one, θ_1 is the switching angle of cell one (V_{dc1}), θ_2 is the switching angle for voltage V_{dc2}, and so on.

The five free variables θ_1 through θ_5 in Equation (9) can be used to form a system of five equations so that the zeros can be arbitrarily chosen to keep the fundamental value at its nominal value while four harmonics can be brought down to zero. The fundamental voltage can be set to 110 V or 120 V as shown in Equation (10) [15].

$$V_{fund}^{RMS} = \frac{4}{\pi\sqrt{2}}[V_{dc1}\cos(\theta_1) + V_{dc2}\cos(\theta_2) + V_{dc3}\cos(\theta_3) + V_{dc4}\cos(\theta_4) + V_{dc5}\cos(\theta_5)] = 120V \tag{10}$$

The target harmonics to be canceled can be arbitrarily set. For example, the 5th, 7th, 11th and 13th can be set as the target harmonics since the 3rd and 9th are canceled in the line-to-line voltage in three-phase applications. For single-phase applications the 3rd and 9th have to be included in the system of equations to be

solved. Consequently, the five equations to be solved are Equation (10) plus any four out of the six Equations (11) through (16).

$$V_{3^{rd}}^{RMS} = \frac{4}{3\pi\sqrt{2}}\left[V_{dc1}\cos(3\theta_1) + V_{dc2}\cos(3\theta_2) + V_{dc3}\cos(3\theta_3) + V_{dc4}\cos(3\theta_4) + V_{dc5}\cos(3\theta_5)\right] = 0 \quad (11)$$

$$V_{5^{th}}^{RMS} = \frac{4}{5\pi\sqrt{2}}\left[V_{dc1}\cos(5\theta_1) + V_{dc2}\cos(5\theta_2) + V_{dc3}\cos(5\theta_3) + V_{dc4}\cos(5\theta_4) + V_{dc5}\cos(5\theta_5)\right] = 0 \quad (12)$$

$$V_{7^{rd}}^{RMS} = \frac{4}{7\pi\sqrt{2}}\left[V_{dc1}\cos(7\theta_1) + V_{dc2}\cos(7\theta_2) + V_{dc3}\cos(7\theta_3) + V_{dc4}\cos(7\theta_4) + V_{dc5}\cos(7\theta_5)\right] = 0 \quad (13)$$

$$V_{9^{rd}}^{RMS} = \frac{4}{9\pi\sqrt{2}}\left[V_{dc1}\cos(9\theta_1) + V_{dc2}\cos(9\theta_2) + V_{dc3}\cos(9\theta_3) + V_{dc4}\cos(9\theta_4) + V_{dc5}\cos(9\theta_5)\right] = 0 \quad (14)$$

$$V_{11^{rd}}^{RMS} = \frac{4}{11\pi\sqrt{2}}\left[V_{dc1}\cos(11\theta_1) + V_{dc2}\cos(11\theta_2) + V_{dc3}\cos(11\theta_3) + V_{dc4}\cos(11\theta_4) + V_{dc5}\cos(11\theta_5)\right] = 0 \quad (15)$$

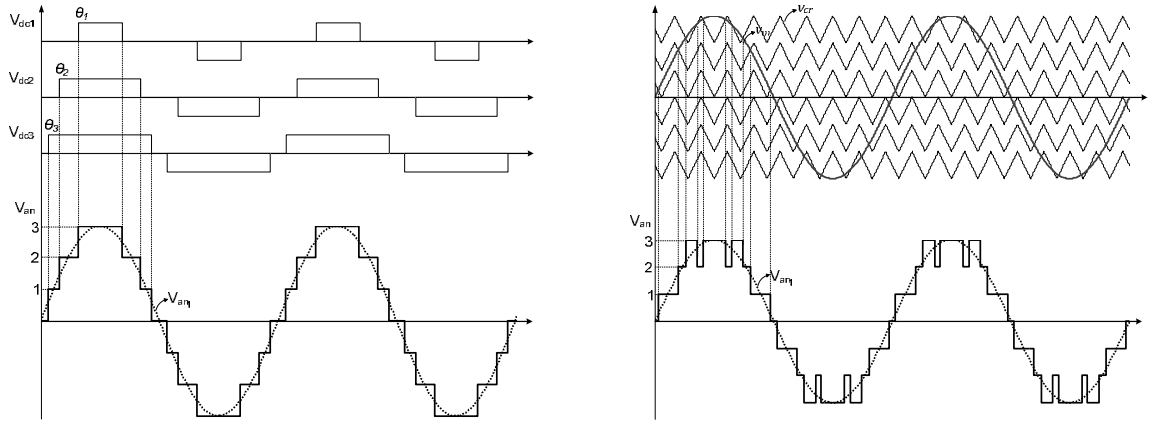
$$V_{13^{rd}}^{RMS} = \frac{4}{13\pi\sqrt{2}}\left[V_{dc1}\cos(13\theta_1) + V_{dc2}\cos(13\theta_2) + V_{dc3}\cos(13\theta_3) + V_{dc4}\cos(13\theta_4) + V_{dc5}\cos(13\theta_5)\right] = 0 \quad (16)$$

All those equations are nonlinear and transcendental, therefore, multiple solutions may be possible. In addition, many local minima may be possible which make it difficult to solve using some numerical methods. A non-deterministic method will be adopted here to solve for switching angles that will give exact solutions and approximate solutions even for cases where no solution exists. The algorithm developed in this proposal will show advantages in finding approximate solutions compared to algorithms that solve the equations exactly.

1.11 Selective harmonic elimination vs. sinusoidal pulse-width modulation

A seven-level CHB was modulated to produce a fundamental voltage V_{an1}=3 p.u. in Figure 8. The selective harmonic elimination (SHE) method uses the switching angles θ_1=57.106°, θ_2=28.717° and θ_3=11.504° to produce the 3 p.u. peak

fundamental at 12.5% total harmonic distortion (THD) and switching at the fundamental frequency as shown in Figure 8 (a). The SPWM method employs the carrier (f_{cr}=540Hz) comparison with the modulating wave (f_m=60Hz) to switch the bridges as shown in Figure 8 (b). In this case, a 20% THD is obtained with an average switching frequency of 90 Hz *($f_{cr}/(m-1)$)* since duty cycle swapping is considered [45].



(a) (b)

Figure 8 – Actual output voltage waveform using SHE (a) and SPWM (b) for a seven-level CHB with equal DC sources (V_{dc}=1 p.u.; V_{an1}=3 p.u. peak; f_m=60Hz; f_{cr}=540Hz) .

Although attractive, due to its performance, the SHE approach has some limitations. The angles must first be calculated within the required precision and then stored in the CPU's memory. Memory size requirements will vary according to the precision for interpolation and number of angles. The modulation index can be used to control the voltage if equal steady DC sources are used. The problem becomes complex when the voltage level variations are considered as the memory

requirements grow exponentially proportional to the number of levels. An alternate methodology is required for this last case.

1.12 Proposed ANN-based selective harmonic minimization

In this context, the work developed here proposes a methodology for providing switching angles for varying DC sources so that the required fundamental is achieved, the lower harmonics are minimized, and the system can be implemented in real time with low memory requirements. Genetic algorithm (GA) will be the stochastic search method to find the solution for the set of equations where the input voltages are the known variables and the switching angles are the unknown variables. With the dataset generated by GA, an artificial neural network (ANN) will be trained as one possibility to store the solutions without excessive memory storage requirements. This trained ANN will then sense the voltage of each cell and output the switching angles as shown in Figure 9. ANN and GA will be explored in the following chapters and their role in this work clarified.

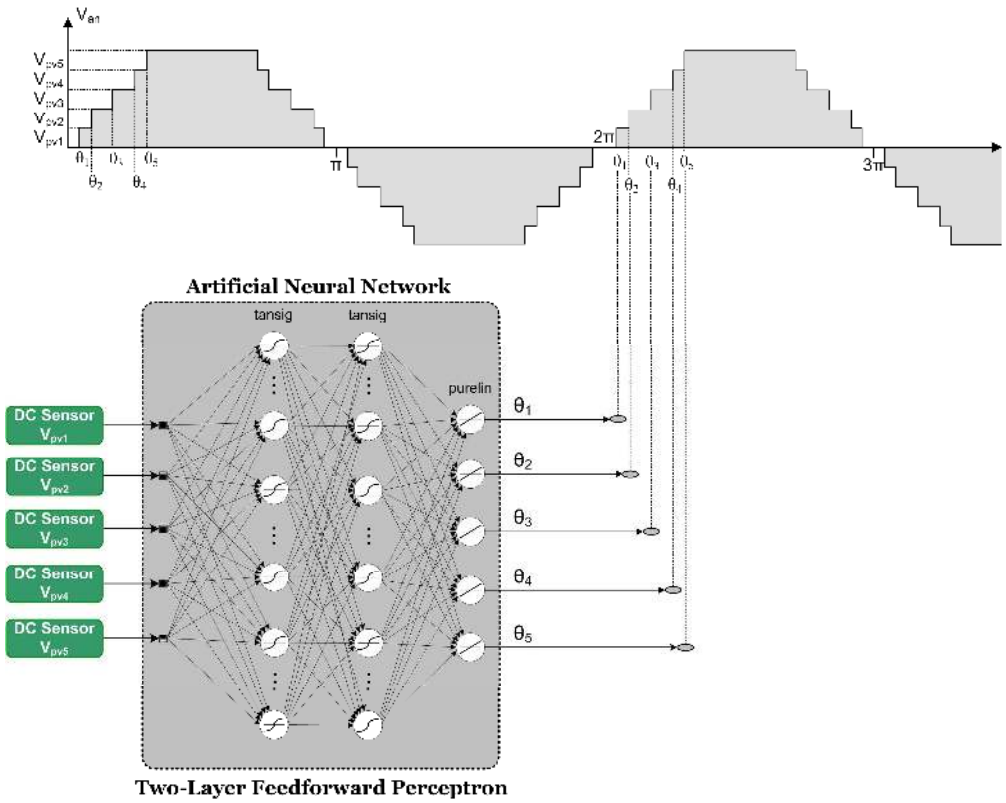


Figure 9 – Proposed artificial neural network based selective harmonic minimization.

1.13 Chapter summary

In this chapter an introduction to solar and power converters was done. The advantages and drawback of multilevel converters were presented and the potential of this topology in solar application and harmonic control was covered. The next section of this dissertation is organized as follows. In chapter 2 a literature review of real-time harmonic control, genetic algorithm, neural networks and multilevel converters will be done. Those techniques will be applied to generate the dataset for real-time angle generation in chapter 3. A technique to estimate the individual cell voltages of a multilevel converter will be presented in chapter 4. Experimental results will be shown in chapter 5 and conclusion and future work in chapter 6.

Chapter 2

Real-time harmonic control literature review

In this chapter, a literature review of the current state of art on selective harmonic elimination, genetic algorithm and artificial neural network will be presented. Their role in this work will be justified and explained and their contribution to the application here will be explored.

2.1 Selective harmonic elimination

A number of technical papers using selective harmonic elimination (SHE) or minimization have been reported for fundamental frequency operation using the most common multilevel (ML) inverter topologies [1-4]. In [1] multilevel topologies such as cascade, diode-clamped, capacitor-clamped, and hybrid topologies are presented. The advantages and disadvantages, control schemes and main applications for each topology are covered in [3].

High-frequency staircase switching modulation will result in a high switching frequency for the switches in each cell at the cost of a low THD. Switching at low frequency can be achieved using multilevel topologies at near fundamental frequency by properly choosing the switching angle. A classification of converters for high power drives is presented in Figure 6. Cascade H-bridge (CHB) is among the most popular topologies used in industrial applications [3]. Its structure makes it a suitable candidate for selective harmonic control as each cell switches both the positive and negative cycle in single-phase applications.

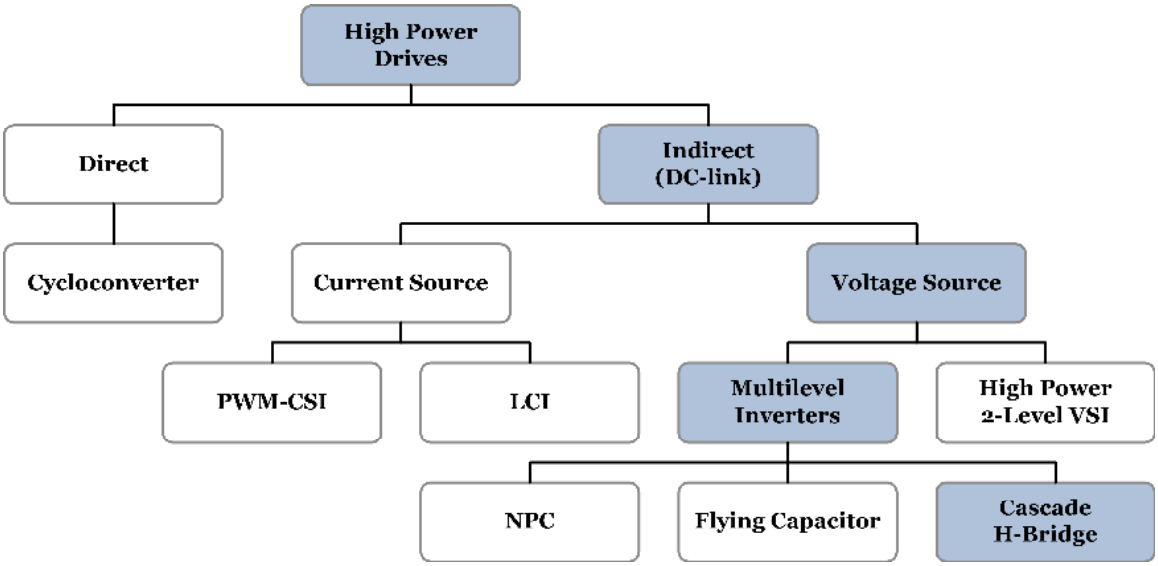
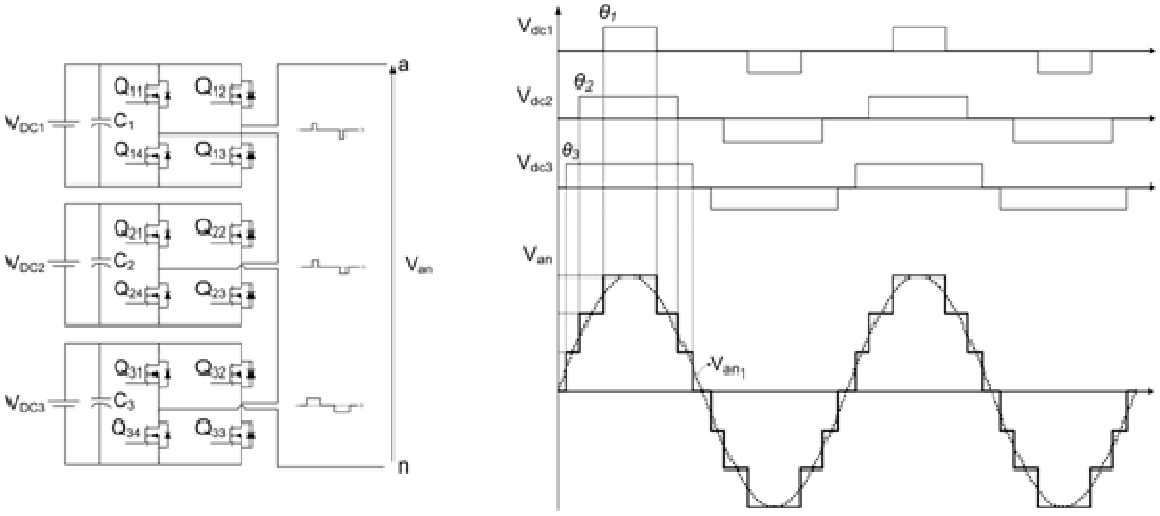


Figure 10 – Power converter drives classification [3].

The cascade H-bridge multilevel configuration has independent DC sources for each level that may have different voltages. Figure 11 shows a seven-level CHB and its modulation at fundamental frequency. As discussed before, SHE can provide better harmonic profile and lower switching frequency. However, SPWM is easy to implement. If SHE is chosen, then a methodology for finding and storing the switching angles is required.

For different voltage levels that are steady in terms of voltage variation, SHE can be applied to the inverter at the fundamental frequency with a look-up table of stored switching angles as shown in [5]. In this way, an *m*-level staircase can be synthesized using *(m-1)/2* separate DC sources. If the DC source voltages have a steady value, then a relation between voltage and modulation index can be found that is simple enough to be stored in a look-up table. If one of those DC voltages vary than a new relation has to be found and stored in the memory. This becomes

increasingly complex as the number of DC supplies allowed to vary increases. For example, if 32-bit floating point numbers (4 bytes per number) are considered then a set of five DC voltages and their respective switching angles will require 40 bytes (10x4) per row. This is approximately 1 KB per 26 lines.



(a) *(b)*

Figure 11 – Seven-level cascade H-bridge inverter (a) and inverter modulation (b).

The converter DC sources might be capacitors, fuel cells, or solar panels, and they will consequently bring a voltage unbalance, depending on the system dynamics. Thus, the assumption of steady voltage sources for each level is not practical for some applications. Table 2 illustrates both cases of equal and unequal DC sources. The voltage can have equal values and vary as in the first column or it can be not balanced as shown in the second column.

Table 2. Five-level CHB under equal and unequal voltage supply.

Balanced voltage [Vdc1 Vdc2]	**Unbalanced voltage [Vdc1 Vdc2]**
[20V 20V]	[20V 20V]
[25V 25V]	[20V 25V]
[30V 30V]	[20V 30V]
	[25V 20V]
	[25V 25V]
	[25V 30V]
	[30V 20V]
	[30V 25V]
	[30V 30V]

Numerous papers have used selective harmonic elimination or minimization for controlling the switches in cascade multilevel inverters. In [6], genetic algorithms were used to determine the optimal switching angles for DC sources of equal values. A seven-level cascade inverter with three equal DC source had its fundamental kept at 120 V and the fifth and seventh harmonics eliminated. A binary-coded GA was implemented and provided.

Analytical solutions for this problem using the theory of symmetric polynomials were also reported for unipolar and bipolar schemes [7-8]. In [7] the set of equations for a three-phase seven-level case is solved using the method of

resultants from elimination theory for the polynomial form of the equations. This approach considers different voltage sources with steady values. Thus, a look-up table is needed to store the switching angles. Solutions were found for a modulation index up to 2.5 ($m_{imax}=3$), where the modulation index was defined as:

$$m_i = \frac{b_1}{\frac{4}{\pi}V_{dc}} \tag{17}$$

The voltage sources are said to be steady if they do not vary significantly with time. That means that a 50 V power supply will stay at 50 V with some transient voltage depending upon the load characteristics. With a steady-state voltage, the solution set for the SHE equations can be easily found and stored to be used offline. This is illustrated in [50] where a three-level flying capacitor multilevel inverter is controlled using SHE for HVDC transmission.

If the voltage sources are unequal and varying with time, the solution set increases exponentially and also the number of switching angles increase. As a consequence, the degree of the polynomials increase and more time is required to solve it. To deal with these high order polynomials, the theory of symmetric polynomials is applied to reduce the dimension of the problem [8] and find the solutions for an eleven-level inverter.

In [9] analytical solutions are found for a five- and seven-level cascade H-bridge (CHB) in which each level has five switching angles. A five-level CHB has two full bridges and with five switching angles for each cell a total of 10 switching angles are obtained. This gives a system of 10 equations to keep the fundamental voltage at

the desired level and eliminate 9 harmonic components. The five-level CHB can eliminate up to the 31st harmonic and the seven-level can eliminate up to the 43rd component. Since those papers target a three-phase application, they do not eliminate the triplen harmonics. In a three-phase application, the triplen harmonics are canceled out in the line-to-line voltage. The methodology in [8-9] cannot find solutions analytically for all the modulation index range; even subsets inside the modulation index might not have solutions. All possible solutions were found when they existed.

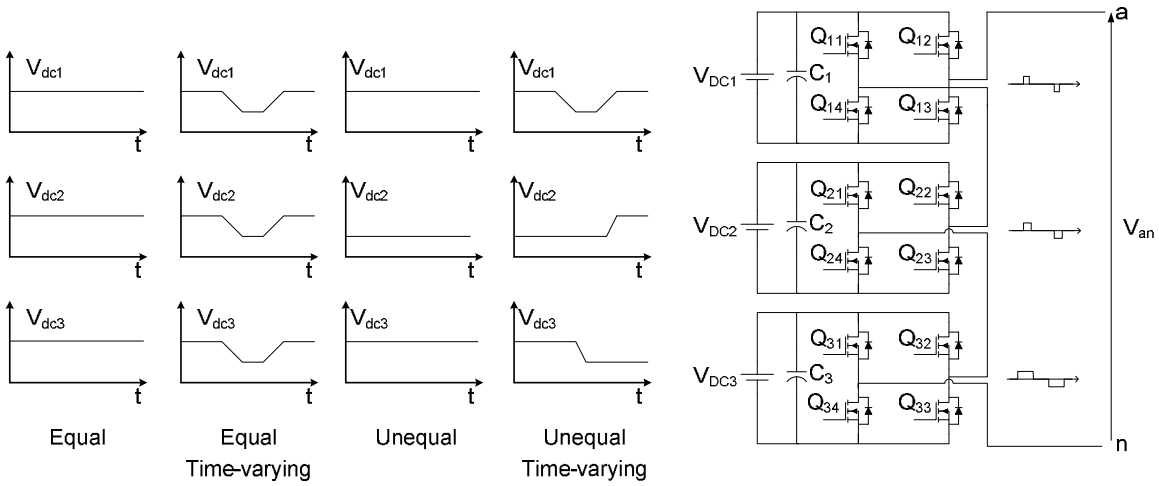


Figure 12 – Seven-level cascade H-bridge inverter and possible voltage profiles.

The four possibilities for the cell's voltage profile are illustrated in Figure 12. In addition to equal and unequal voltages they can also vary with time. All of the previous papers assumed that the DC sources are equal or unequal but with steady state voltages that do not vary with time. Thus, not all points in the second column of Table 2 were considered. If the voltage level changes, a new set of solutions needs to be found to keep the high-order harmonics eliminated. In addition, the number of

levels will add complexity to the problem as the equations will have higher order and take longer to solve.

One solution would be to use look-up tables as proposed in [10] that require exponentially proportional look-up tables as the number of angles and levels increases. Equal area criteria was used in [11] for a wide range of modulation indexes. The system of equations in this case is obtained by comparing the sinusoidal reference with the staircase waveform so that in the intersection they share the same area between levels. The whole set of solutions can be found by the analytical approach proposed. In [12-14], algorithms to solve for the angles have been proposed for seven- and nine-level topologies. In [13] a homotopy algorithm is proposed for finding the solutions of simplified high-order nonlinear transcendental equations. This algorithm solves for the switching angles with a simpler formulation for unequal DC sources.

In [15-16], a more general approach is formulated for the *m*-level *n*-harmonic case. Simplification of the basic SHE equations could allow the system to find solutions online for certain cases. A generalized formulation for quarter-wave symmetry is proposed in [51] for equal DC sources with a simple formulation. In this paper the solutions are still found off-line mainly to prove the methodology but they can be stored for real time operation. The bipolar and unipolar case is covered in a general approach that does not take into account waveform symmetry [15]. In this technique, angles can be arbitrarily distributed over the cycle to create the

waveform. Although a formulation is given for *m*-level *n*-switching angles, only two and three levels are discussed in detail.

In [16], a general formulation is derived for an *m*-level *n*-angles case considering quarter wave symmetry. Different voltage levels are taken in account, as well as the number of phases. Phase and line-to-line voltages and harmonics are included in the coefficients. The number of angles, number of levels, voltage levels, and target harmonics can be chosen according to the topology to be implemented. Results are shown for some selected cases. All of these papers use computationally intensive time consuming equations to solve for the angles. Those equations can easily increase in complexity as the number of levels or angles increases. The switching angles are calculated off-line in all the previous cases, as the computational burden does not allow real-time SHE.

The authors of [17-18] have developed methods to calculate the switching angles in real-time; however, their approach was not extended for unequal DC sources. In [17], the switching angles were generated comparing a reference sine wave with the voltage levels so as to calculate the volt-sec area of the waveform. This volt-sec area is matched with the volt-sec area of the staircase waveform of the inverter to obtain the switching angles. This approach performs better than the conventional one at low modulation indexes.

In [18] a method to solve for the angles was proposed with a simple set of equations that can be solved online using the Newton-Raphson method. That methodology was implemented for a seven-level CHB where a DSP board was used

to implement real-time calculation of the angles. In this case, the voltage sources are varying, but have the same value as in the first column of Table 2. Thus, all the voltage sources have the same value at any time, and they vary keeping the same relative value. In addition, THD was the target of the minimization instead of specific harmonic components. A mathematical proof was presented to show that the minimum THD obtained is the minimum achievable.

As shown before, an alternate approach to determining the optimum switching angles in real-time for varying DC sources is to calculate the switching angle solutions off-line and store the solutions in a look-up table as shown in Figure 13. Accurate representation of solutions for every different DC source case would require a huge look-up table. Such a lookup table would require an amount of memory and speed processing that can easily go beyond the processor capacity. Even then, for some operating points, the solutions might be missing and some type of interpolation would be required. For a three DC sources case [19], it is possible to avoid overhead and solution issues by using the generalization and parallelism of artificial neural networks (ANN) to quickly generate the switching angles for any number of levels and switching angles.

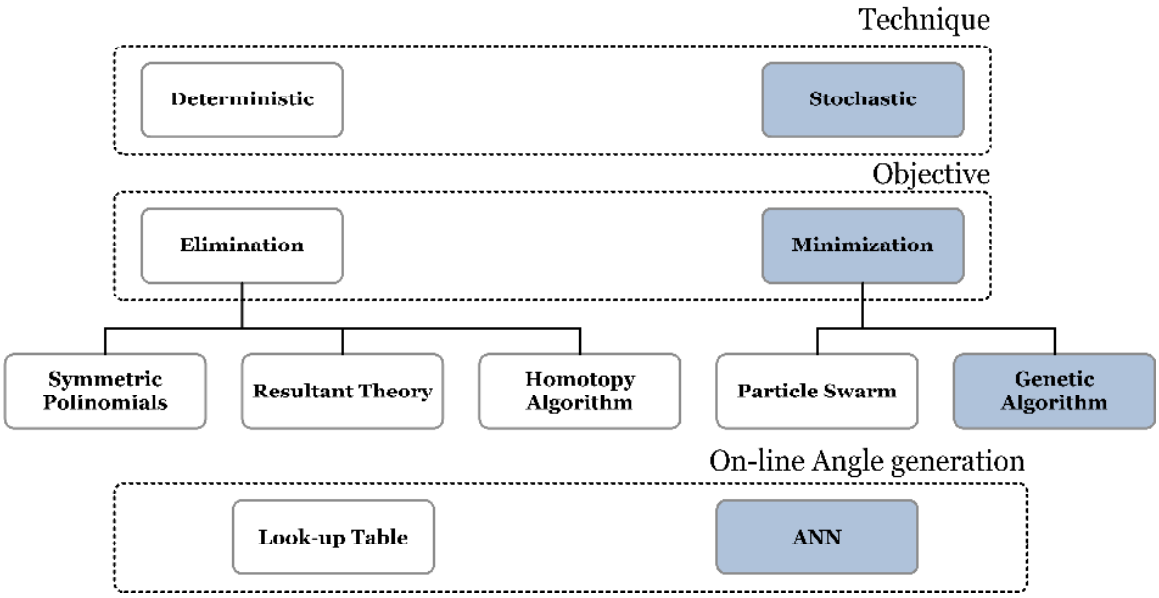


Figure 13 – Techniques employed in selective harmonic elimination and minimization.

In this work instead of using a look-up table, an ANN is employed, which, if well trained, has the inherent capability of generalizing solutions [19]. The missing points in the solution set are handled using genetic algorithms. If the correct range of data is used for training, and if the ANN is not over-trained, the network will extrapolate properly. Since ANN runs quickly, switching angles can be quickly determined to establish real-time control.

2.2 Solar cell model

A suitable model was derived to simulate the PV module behavior that reflects the experimental curves of the solar panel with relative accuracy. The single diode model was adopted, as shown in Figure 10, to simulate the PV module under different irradiance and temperature levels. A number of approaches and models

can be found in the literature to analyze the behavior of PVs that can grow in complexity in case better accuracy is needed [20-22].

The suitable model then becomes application dependent. In [21] a more complex model is derived that takes into account temperature, irradiance, and wind speed for long term and transient analysis. A model was developed in [22] to consider and study the shading effect on solar panels connected in series. Wind speed and other features add in complexity for the model, reflecting a more realistic behavior. Those features are not the main focus in this work. The main parameters desired are the influence of temperature and irradiance on the panel's voltage and current.

The PV cell model used in this work is a more intuitive model based on the single diode cell in Figure 14 and derived in [23]. The inputs used are those obtained directly from the PV module datasheet parameters, which are readily available from a panel's manufacturer. This model greatly simplifies the modeling task, once the iterations and nonlinear equations are solved. Equation (18) is the basic formula and the solar panel's datasheet provides the parameters to solve for the unknowns.

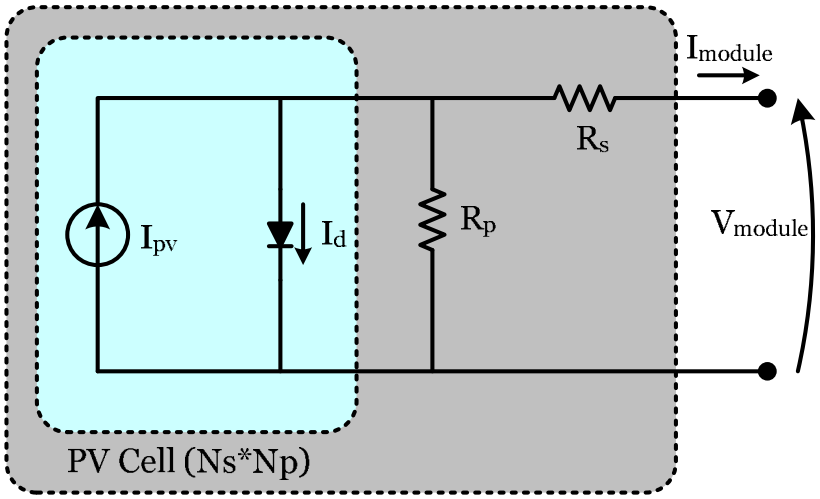


Figure 14 – Photovoltaic cell single diode model representation.

$$I = I_{pv} - I_0\left[e^{\left(\frac{V+R_S I}{V_t a}\right)} - 1\right] - \frac{V+R_S I}{R_p} \tag{18}$$

where,

I: photovoltaic module output current

V: photovoltaic module output voltage

I_{pv}: photovoltaic current

I_0: saturation current

V_t: thermal voltage

R_s: equivalent series resistance

R_p: equivalent parallel resistance

a: diode ideality constant

The results using this approach will be presented in the next chapter. The fill factor is another important parameter for solar panel modeling. It is defined as the percentage of area covered by voltage (V_{mpp}) and current (I_{mpp}) at the maximum power point and the area covered by open circuit voltage (V_{oc}) and short circuit current (I_{sc}). It is defined as shown in Equation (19) [52].

$$fill\ \ factor = \frac{P_{\max}}{I_{sc}V_{oc}} = \frac{I_{mpp}V_{mpp}}{I_{sc}V_{oc}} \tag{19}$$

Since this methodology takes into account all of the parameters in Equation 19, the fill factor will naturally match in all conditions.

2.3 Artificial neural networks

Artificial neural networks have found a number of applications in engineering, such as pattern recognition, control and classification, and others [24-27]. One of the main factors for choosing this technique is its generalization ability in nonlinear problems that are complex in nature and/or calculation intensive [28].

Artificial neural networks are computational models that were inspired by biological neurons [24]. They use a series of nodes with interconnections where mathematical functions are applied to do an input/output mapping. That means, for example, the information contained in a lookup table can be stored in an ANN. The challenge is to know how many neurons will be needed to train an ANN for a specific application. This will be dependent on complexity of the input/output relation,

number of inputs and number of outputs. This requires some trial and error in the first stage until a suitable ANN is found [25-26].

An important feature of the ANN that makes it suitable for this problem is its flexibility to generalize (interpolate) its output inside its domain, as well as work with the nonlinear nature of the problem [29-32]. The fundamentals are presented in [30-31], while application is the focus in [29], where many inverter control examples are covered, as well as training and types of ANNs.

The size of the ANN has to be determined in such a way to have maximum performance with minimum number of neurons. That becomes more challenging as the data set size increases and how complex is the function to be mapped. Methodologies to determine ANN topology has been proposed in [53]. One approach is to grow an ANN by increasing the number of neurons, training, and evaluating the performance. This is done until the required performance is obtained to determine the minimum ANN. That strategy will be employed here for a two layer ANN.

The data set presented to the ANN is not complete in terms of resolution, and not all combinations or solutions were obtained by the GA. For that reason ANN is employed here since it has enough flexibility to interpolate and extrapolate the results. Chapter 3 will cover ANN performance and results in more detail. The main reason to use ANN is the possibility of real-time angle generation. The ANN features, for example, make it suitable for common problems encountered in power electronics such as fault detection [33] and harmonic diagnostics [34].

ANNs are generally time consuming to train but fast to run and can be easily parallelized once accordingly trained. Its weights can be stored in a flash memory of a CPU, DSP, or FPGA for real-time processing of the outputs. It has the potential to replace lookup tables since an increase in the number of DC sources in the problem will exponentially increase the size of the look-up table. Look-up tables require extrapolation and comparisons, leading to time consuming algorithms. In addition, analytical approaches must deal with the computational time required for the task. In both cases, a methodology has to be found to handle the no-solution range. One promising candidate is genetic algorithms.

2.4 Genetic algorithms

Different approaches can be used to solve for the angles and the choice is application dependent. As the number of dimensions increases, the complexity and time to solve the equations increase. Analytical or numerical approaches may need computational power beyond current mathematical software. That is the case illustrated in [54] where the harmonic minimization problem is solved using Particle Swarm Optimization (PSO) to find 15 switching angles. Another stochastic technique is Genetic Algorithm which will be adopted in this work mainly because it is well known and documented technique with a matured Matlab toolbox.

Genetic algorithm (GA) is a technique based on the evolutionary process, where individuals are constantly adapting to a changing environment in order to survive [36]. It mimics the behavior of populations during generations, based on the idea that the best-suited individuals have greater probability to survive and pass on

their genetic codes to their descendants. Through generations, the quality of the population tends to improve. The obtained best individual is an end product containing the best elements of previous generations, where the attributes of a stronger individual are carried forward into the following generation [37-42].

In the SHE problem environment, many analytical solutions have been reported, as presented previously. If it is desired to keep the fundamental and eliminate the lower-order harmonics, the analytical formulation will solve the problem faster, and a more complete solution can be achieved. This technique (GA) is used for its ability to deal with complicated problems where analytical formulation is not yet possible or practical [37-38]. In the multiobjective SHE problem, if there is no set of angles that will satisfy the SHE equation, the analytical approach will not return an answer. The GA, on the other hand, will always return an answer that will not solve exactly for all variables but instead will give answers that are very close. Thus, instead of eliminating the harmonics it minimizes them [39].

2.5 Final remarks

The proposed approach in this work will be done in two steps: First a genetic algorithm (GA) will be implemented to find the switching angles (off-line) for a set of pre-determined input voltages for an 11-level cascade inverter; Then, with the previous data set, the ANN will be trained to give the set of angles for each voltage situation in real-time.

An important feature of the GA for this approach is that for the range space where there is no analytical solution the GA will find the nearest solution providing a smooth data set that is desired for the neural network training. In addition, such a complex technique can find a solution that might not be found by the analytical solution that is acceptable in terms of the current standards. For example, GA might find a solution that produces an output fundamental voltage of 110 V within ±5% while other analytical approaches find no solution or states that there is no solution.

2.6 Chapter summary

In this chapter, a thorough literature review was conducted in the area of harmonic elimination, genetic algorithms, and artificial neural networks. The technique proposed in this work was based on an extensive research of previous work. Solar cell models were revised and a model fit for the work requirement was proposed. GA and ANN were reviewed and its application to selective harmonic minimization has shown to be of great potential for real time angle generation. This is one of the main challenges that have not yet been proposed.

The techniques previously presented will be applied to generate the dataset for real-time angle generation in chapter 3.

Chapter 3

Dataset and real-time angle generation

This chapter will cover the theory behind genetic algorithms and neural networks. This will include their main features and drawbacks, as well as an illustrative example to prove their efficacy.

3.1 Genetic algorithms

A genetic algorithm (GA) is a stochastic search method shown to be well suited for problems where many global minimum and/or highly dimensional search spaces are possible. Each individual of a set has an associated cost value, referred to as “fitness function” that is a measure of how well this individual performs in the population. In previous works, analytical solutions were found partially in the range space of input voltage variation; however, this approach still uses GA first, because this range is used to calibrate it to perform in the range where there is no analytical solution. Therefore, the correct GA parameters are found to bias the algorithm through the desired solution. Also, it is possible to adjust the algorithm to arrive at its solutions looking at the previous results giving a future solution, or switching angles, in this case, which are smooth so that the ANN can be easily trained. The basic continuous GA execution flow is shown in Figure 15.

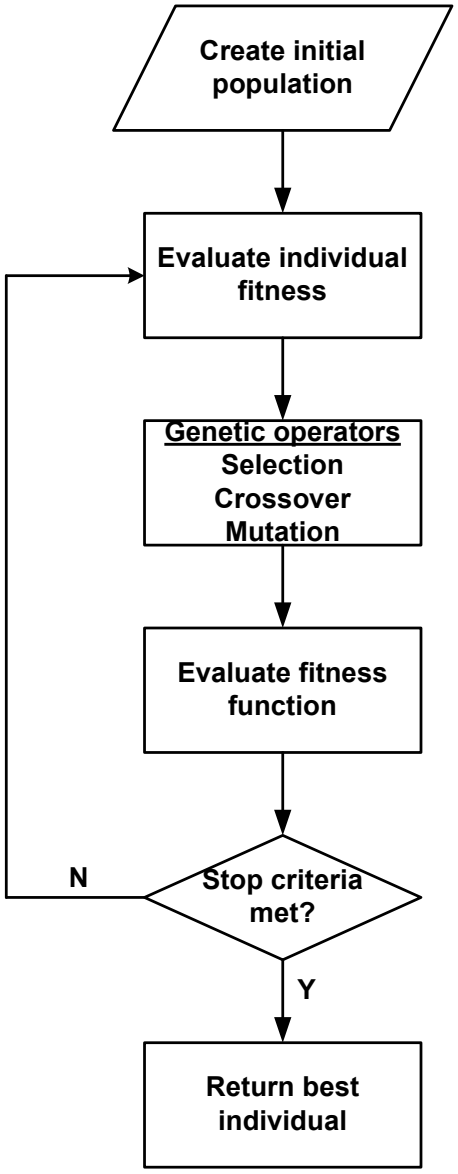


Figure 15 – Flow chart of a continuous GA.

The algorithm starts with a population of individuals that represent a set of possible solutions to the problem. The fitness function will return a value that gets closer to zero as the five set of SHE equations (out of Equations (11) to (16)) gets closer to zero. A fitness equal to zero means that an exact solution was found. Next, the genetic operators will act in the current population to generate the next

population using decision rules, so that on average, the solutions (individuals) will be improved. The new population is again evaluated (fitness), and if a satisfactory solution is found, the algorithm stops. In case the stop criteria are not satisfied, the algorithm keeps evolving its population until this occurs.

Deterministic methods use information extracted from the problem such as the gradient or the hessian matrix to determine the next point. Stochastic methods, such as GA, base searches in a set of stochastic decision rules to determine the next point [39]. Those decision rules and GA steps are explained in the following sections. The algorithm was written using Matlab toolbox for GA implementation. This toolbox has the main GA functions and routines implemented with a number of visualization options to help fine tune the GA for a specific problem. A code was written for the fitness function and the different settings for the SHE challenge were investigated. The following sections will show the main GA settings followed by a GA run to prove the settings chosen can find the solutions.

3.1.1 Individual representation

Many options exist for representing a single individual. In the original work by Goldberg [36], binary representation was used to introduce and explain the concept. Integer numbers, vectors, matrices or floating point numbers could represent a single individual inside the population. This work employed real-valued representation, as continuous or real-valued GA better relates the problem to its representation, and higher precision can be achieved compared to binary representation.

3.1.2 Selection operator

The next step requires choosing from the pool of individuals those who will reproduce based on their fitness. The fitness function describes how well the actual solution will perform. If a minimization problem is being analyzed, the fittest individuals are those nearest a global minimum, or that best satisfy the set of equations.

Many methods have been used as the selection operator, such as roulette, scaling techniques, tournament selection, elitist models and rank methods. In the roulette method adopted here, each individual is assigned a probability P_i of being chosen as presented below:

$$P_i = \frac{F_i}{\sum_{j=1}^{PopSize} F_j} \tag{20}$$

The fittest individuals will have a better chance to be chosen, as their fitness F_i will give them a bigger slot (P_i) in the roulette .

One disadvantage of this method arises when an individual with a very high fitness appears in the population and is more likely to have a comparatively higher probability. The population is then steered toward that individual, causing the algorithm to stop exploiting and exploring the search space, ultimately leading to premature convergence. Such behavior was observed in this work as premature convergence to local minima, so an alternative roulette with normalized ranking was used instead.

Using normalized geometric ranking rather than the roulette will minimize convergence problems. In this approach, the fitness function is used to sort individuals in the population and the probability of each individual P_i is chosen according to Equation (21).

$$P_i = \frac{q}{1-(1-q)^P}(1-q)^{r-1} \tag{21}$$

where,

q: probability of the best individual

r: rank of the individual (1 is the fittest)

P: population size

P_i: fitness of the *i-th* individual

3.1.3 Crossover operator

Once the individuals were selected, a crossover operator will act on the parents x and y to produce an offspring x' and y' according to Equations (22) and (23).

$$\vec{x}' = r\vec{x} + (1-r)\vec{y} \tag{22}$$

$$\vec{y}' = (1-r)\vec{x} + r\vec{y} \tag{23}$$

This is called "arithmetic crossover" and extrapolation is obtained by properly choosing r outside the boundaries *U(0,1)*.

3.1.4 Mutation operator

Uniform mutation can be achieved by choosing one individual and setting to a new value inside its boundaries, using a random number between the lower and upper limits for that entry.

$$\vec{x}'(j) = R(a_i, b_i) \tag{24}$$

where,

$R(a_i,b_i)$: random number between a_i and b_i for row j of vector $\boldsymbol{x}$

Mutation can also act in a non-uniform way using a non-uniform random number or using the boundaries as the new mutated individual. The settings are problem-dependent, and trial and error might be required to find the best parameters for a problem.

3.1.5 Algorithm initialization and termination criteria

At the very beginning, the algorithm should be provided a starting population. This population should then be spread over the search space in case of a bounded problem. If the variables are unbounded, knowledge of the application can be used to define the boundaries.

Number of generations can be used as the stop criteria. Often the GA will converge to a solution, so convergence combined with number of generations can become the stop criteria. Convergence is defined as no improvement in the solution over a certain number of generations (stagnation). Since the best solutions will have an increased survival chance, they often dominate the next generations faster than mutation and crossover, and premature convergence can occur. In that case, the

initial population and the genetic operator's settings must be adjusted to tune the algorithm behavior for that specific problem. In this work, number of generations, fitness function value, and population improvement is used as the criteria to stop the simulation. Fitness function value is the main criteria since the problem is defined so that the best individual achievable will have zero fitness and all others will have greater than zero fitness.

3.2 A single GA run for SHE minimization

In a practical situation in a multilevel converter, all the DC sources vary to some degree. This variation can be proportional to the state of charge in a battery or fuel cell system, or it can be a function of solar irradiation as is the case for solar panels. In such cases, switching angles must be controlled to retain the desired output voltage characteristics. A single GA run to find the solution for the parameters set in Table 3 was implemented to confirm GA performance.

Table 3. Problem definition for the GA.

Input Parameters	**Value**
V_{dc1}	40 V
V_{dc2}	42 V
V_{dc3}	38 V
V_{dc4}	36 V
V_{dc5}	42 V
Output Parameters	**Objective Function**
Fundamental voltage (V_{fund})	Keep at 120 V
Harmonics (V_{3rd}, V_{5th}, V_{7th}, V_{9th})	Eliminate or minimize

The set of equations to be used in the objective function in order to satisfy the requirements of Table 3 are:

$$V_{fund}^{RMS} = \frac{4}{\pi\sqrt{2}}\left[V_{dc1}\cos(\theta_1) + V_{dc2}\cos(\theta_2) + V_{dc3}\cos(\theta_3) + V_{dc4}\cos(\theta_4) + V_{dc5}\cos(\theta_5)\right] = 120V \quad (25)$$

$$V_{3^{rd}}^{RMS} = \frac{4}{3\pi\sqrt{2}}\left[V_{dc1}\cos(3\theta_1) + V_{dc2}\cos(3\theta_2) + V_{dc3}\cos(3\theta_3) + V_{dc4}\cos(3\theta_4) + V_{dc5}\cos(3\theta_5)\right] = 0 \quad (26)$$

$$V_{5^{th}}^{RMS} = \frac{4}{5\pi\sqrt{2}}\left[V_{dc1}\cos(5\theta_1) + V_{dc2}\cos(5\theta_2) + V_{dc3}\cos(5\theta_3) + V_{dc4}\cos(5\theta_4) + V_{dc5}\cos(5\theta_5)\right] = 0 \quad (27)$$

$$V_{7^{rd}}^{RMS} = \frac{4}{7\pi\sqrt{2}}\left[V_{dc1}\cos(7\theta_1) + V_{dc2}\cos(7\theta_2) + V_{dc3}\cos(7\theta_3) + V_{dc4}\cos(7\theta_4) + V_{dc5}\cos(7\theta_5)\right] = 0 \quad (28)$$

$$V_{9^{rd}}^{RMS} = \frac{4}{9\pi\sqrt{2}}\left[V_{dc1}\cos(9\theta_1) + V_{dc2}\cos(9\theta_2) + V_{dc3}\cos(9\theta_3) + V_{dc4}\cos(9\theta_4) + V_{dc5}\cos(9\theta_5)\right] = 0 \quad (29)$$

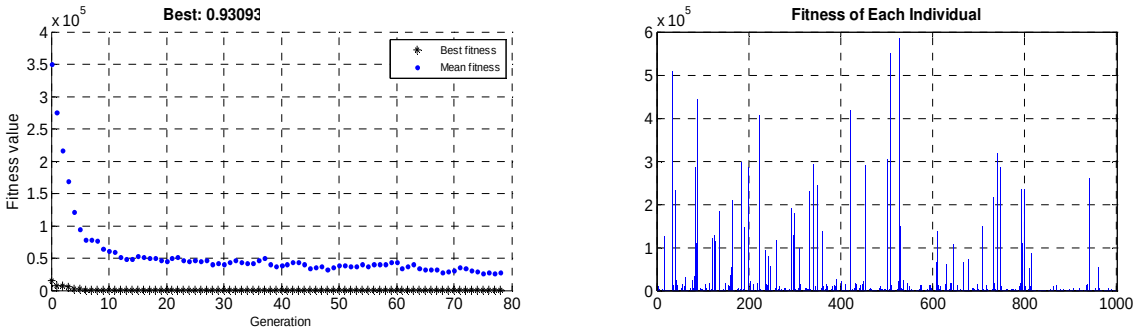
The GA was programmed to obtain the set of angles to control the multilevel inverter for each value of the DC sources defined in Table 3 using (25) to (29).

An objective function for the GA that represents the fitness, evaluates and classifies each individual in the population is defined as follows:

$$f(V_{fund}^{RMS}, V_{3rd}^{RMS}, V_{5th}^{RMS}, V_{7th}^{RMS}, V_{9th}^{RMS}) = k_1\left|V_{fund}^{RMS} - 120\right| + k_2\left|V_{3rd}^{RMS}\right| + k_3\left|V_{5th}^{RMS}\right| + k_4\left|V_{7th}^{RMS}\right| + k_5\left|V_{9th}^{RMS}\right| \quad (30)$$

The coefficients k_1 to k_5 are used to tune the algorithm to ensure the entire cost function is minimized uniformly. Otherwise, the fundamental voltage would bias the search towards its own value, because its error is usually greater than the harmonics at the very beginning of the search process.

Figure 16 (a) shows the results after 79 generations of the algorithm. Best and mean population values are shown. At the final generation, a fitness function of 0.93 is achieved, and the algorithm stops and returns its best solution. In this case, the stop criterion was the fitness function value less than 1.0 that caused the algorithm to stop. After 15 generations, a good solution is achieved so the GA works next generations on improving it until fitness function stop criterion was reached at generation 79. Figure 16 (b) shows the high diversity of individuals with each individual's fitness for a population size of one thousand.



(a) *(b)*

Figure 16 – GA average and best individual per generation (a) and final population fitness (b).

The coefficients used in Equation (30) are shown in Table 4. Those values were found through trial and error runs of the algorithm. They allow the fundamental to be kept very close to 120 V while keeping harmonics close to zero.

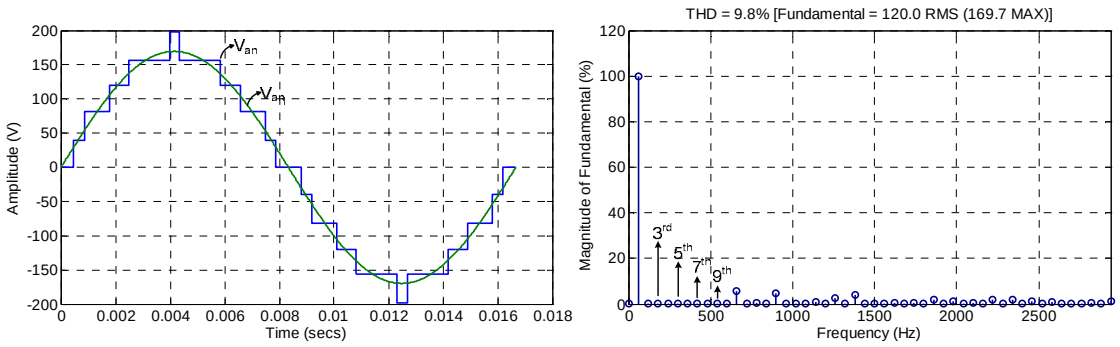
Table 4. Objective function coefficients of equation (30).

Variable	**Value**
k_1	10
k_2	100
k_3	100
k_4	100
k_5	100

The final result of the GA run after the 79th generation is shown in Table 5 for the voltages defined previously.

Table 5. GA results for best individual after 80 generations.

Voltage	Switching angles
V_{dc1}=40V	θ_1=9.98°
V_{dc2}=42V	θ_2=18.51°
V_{dc3}=38V	θ_3=38.13°
V_{dc4}=36V	θ_4=53.76°
V_{dc5}=42V	θ_5=86.04°



(a) *(b)*

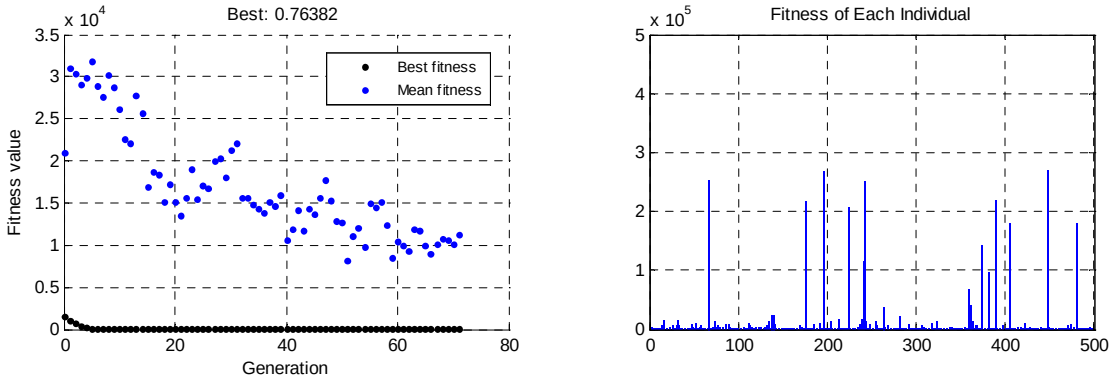
Figure 17 – Eleven-level waveform (m_i=0.67) and fundamental voltage (a) and frequency spectrum (b).

Figure 17 (a) shows the multilevel waveform and its fundamental component and (b) shows its frequency spectrum until the 49th harmonic component. All the lower harmonics were practically eliminated once the GA best individual reached a good fitness value (less than one for this case). The fitness value of 0.93 obtained was enough to guarantee harmonic elimination. The waveform THD calculated until the 49th harmonic (V_{49}) as shown in Equation (31) was 9.8% for this single-phase multilevel inverter configuration. The target harmonics (3rd, 5th, 7th and 9th) were in

the magnitude of 10^{-5} which can be considered as practically zero low order harmonic values.

$$THD = \frac{\sqrt{V_2 + V_3 + ... + V_{49}}}{V_{fund}} \tag{31}$$

Figure 18 (a) shows the results after 71 generations of the algorithm for a 9-level case. The value for the best individual in the population is shown in the top. At the final generation, a fitness function of 0.76 is achieved, and the algorithm stops and returns its best solution. In this case, the stop criterion was the fitness function value less than 1.0 that caused the algorithm to stop. Figure 18 (b) shows the diversity of individuals with each individual's fitness for a population size of 500. A population size between 500-1000 is usually enough for the algorithm to perform the search. For less number of levels a smaller population can be used as in the figure below where 500 is chosen as the population size.



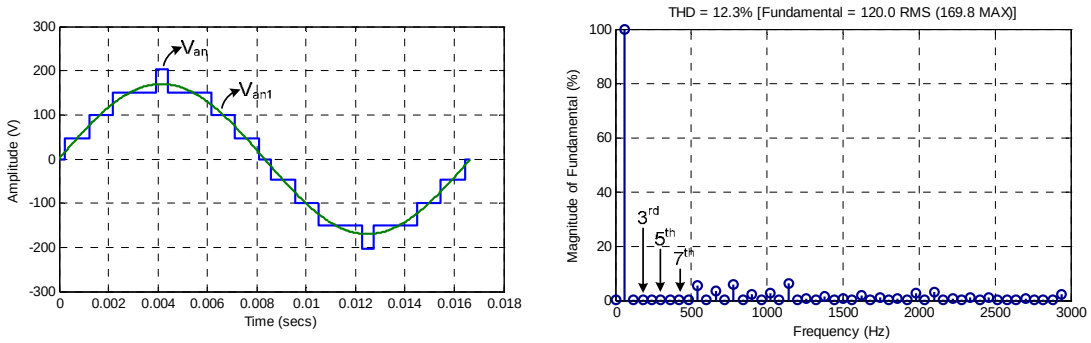
(a) *(b)*

Figure 18 – GA average and best individual per generation (a) and final population fitness (b).

The final result of the GA run after the 71st generation is shown in Table 6 for the voltages defined in this table. The coefficients of the fitness function are the same as shown in Table 4.

Table 6. GA results for best individual after 71 generations.

Voltage	**Switching angles**
V_{dc1}=47V	θ_1=9.77°
V_{dc2}=52V	θ_2=26.47°
V_{dc3}=52V	θ_3=51.07°
V_{dc4}=52V	θ_4=86.88°



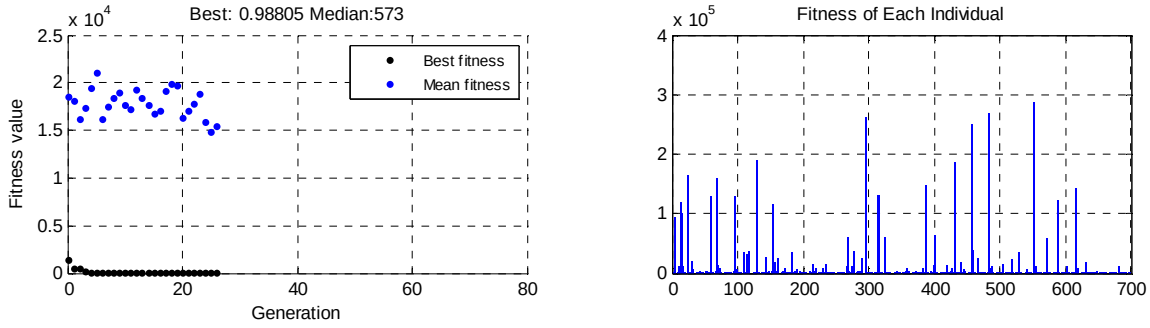
(a) *(b)*

Figure 19 – Nine-level waveform (m_i=0.65), fundamental voltage (a) and frequency spectrum (b).

Figure 19 (a) shows the multilevel waveform and its fundamental component, and (b) shows its frequency spectrum until the 49th harmonic component. All the lower harmonics were practically eliminated once the GA best individual reached a good fitness value (less than one for this case). The fitness

value of 0.76 obtained was enough to guarantee harmonic elimination. The waveform THD calculated until the 49th harmonic (V_{49}) as shown in Equation (31) was 12.3% for this single-phase multilevel inverter configuration. The target harmonics (3rd, 5th and 7th) were in the magnitude of 10^{-4} which can be considered as practically zero low order harmonic values.

Figure 20 (a) shows the results after 26 generations of the algorithm. At the final generation, a fitness function of 0.98 is achieved, and the algorithm stops and returns its best solution. In this case, the stop criterion was the fitness function value less than 1.0 that caused the algorithm to stop. Figure 20 (b) shows the diversity of individuals with each individual's fitness for a population size of 700.



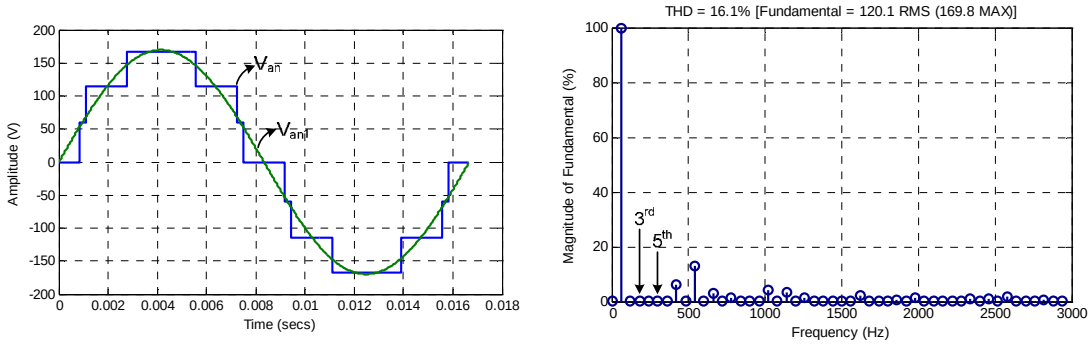
(a) *(b)*

Figure 20 – GA average and best individual per generation (a) and final population fitness (b).

The final result of the GA run after the 26th generation is shown in Table 7 for the voltages defined in this table. The coefficients of the fitness function are the same as shown in Table 4 (the first three coefficients).

Table 7. GA results for best individual after 26 generations.

Voltage	Switching angles
$V_{dc1}=60V$	$\Theta_1=17.87°$
$V_{dc2}=54V$	$\Theta_2=23.72°$
$V_{dc3}=53V$	$\Theta_3=59.68°$



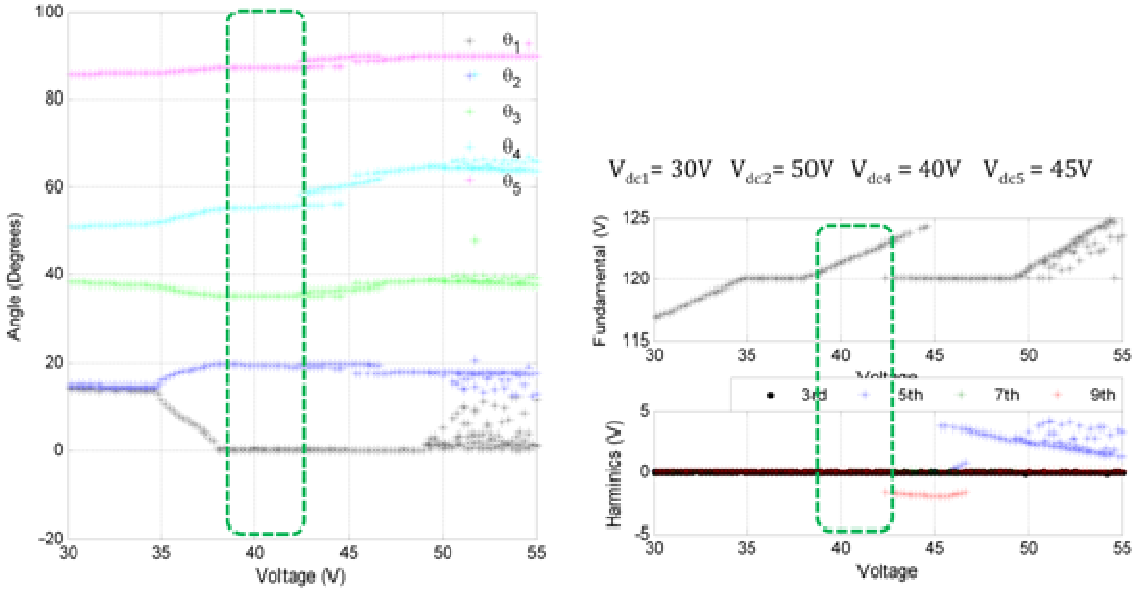
(a) *(b)*

Figure 21 – Seven-level waveform (m_i=0.80) and fundamental voltage (a) and frequency spectrum (b).

Figure 21 (a) shows the multilevel waveform and its fundamental component and (b) shows its frequency spectrum until the 49th harmonic component. All the lower harmonics were practically eliminated once the GA best individual reached a good fitness value (less than one for this case). The fitness value of 0.98 obtained was enough to guarantee harmonic elimination. The waveform THD calculated until the 49th harmonic (V_{49}) as shown in Equation (31) was 16.1% for this single-phase multilevel inverter configuration. The target harmonics (3rd and 5th) were in the

magnitude of 10^{-5} which can be considered as practically zero low order harmonic values.

There are some voltage conditions for which a solution cannot be found as illustrated in Figure 22. In this figure only one of the voltage sources is varying while the others are kept at a constant value as indicated. The GA does not know there is no solution so the algorithm keeps running until the stop criteria are met. As it can be noticed in the figure, although there is no solution, an acceptable result is obtained where the voltage is still close to the fundamental at a low level of harmonics. This is highlighted in the dashed square showing what happens to the angles in Figure 22 (a) and the fundamental voltage in Figure 22 (b). In (b) it can be noticed that the voltage starts to increase in value while the harmonics are kept at low levels. This ability to provide acceptable solutions is one of the key features of GA to explore the search space and return reasonable solutions. This feature will be explored in the further sections.



(a) *(b)*

Figure 22 – Eleven-level inverter switching angles (a) and output voltage and harmonics (b).

3.3 Artificial Neural Networks

The basic network chosen is shown in Figure 23. It is a multilayer network with one input stage, two hidden layers and one output layer. Variations of this basic topology might be adopted if it proves to have better performance. Neurons or layers may be added to the basic configuration, but the signal flow will be kept in the forward direction.

Vapnik and Chervonenkis [55-56] defined a parameter called the *Vapnik-Chervonenkis dimension* (VCDim) which is a measure of the generalization capability of an ANN. It is possible to bound the error during the testing stage if the number of samples is greater the VCDim number. The VCDim number is defined as:

$$VDCim = 2 \times N_w \times \log_e N_N \tag{32}$$

The number of nodes is defined as N_N and the number of weights is N_w. This equation will be used in this work as an additional tool to analyze generalization and performance.

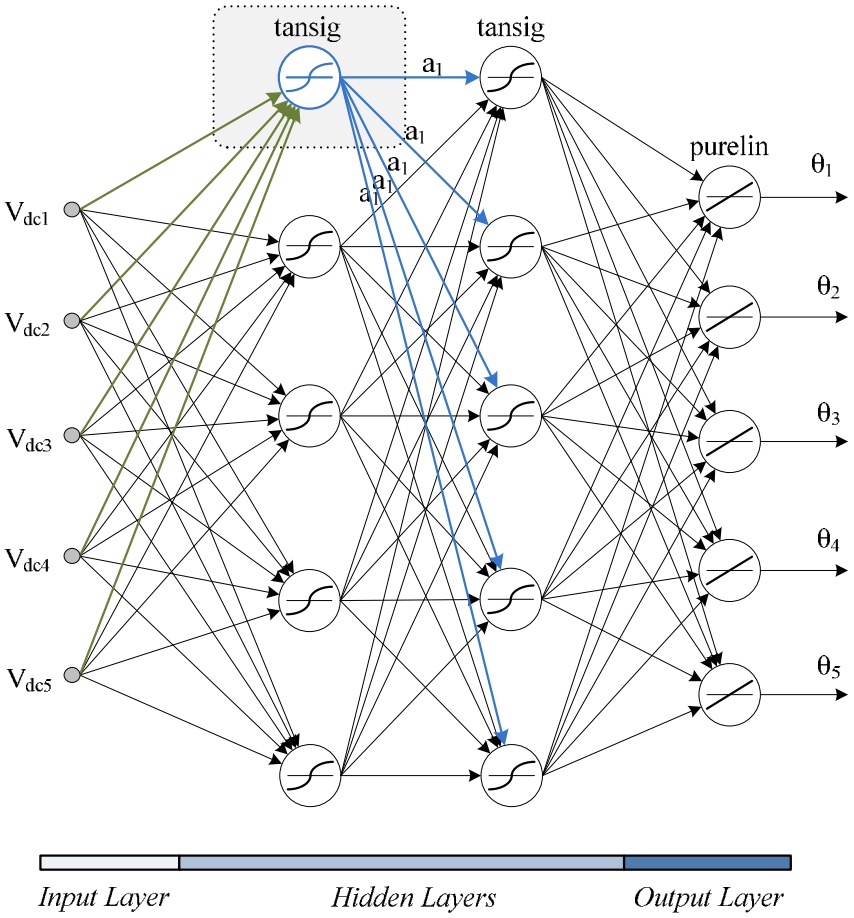


Figure 23 – Multilayer feed-forward perceptron neural network topology.

Figure 23 highlights the basic computational model of a biological process, showing its interconnections in the network. The inputs of these interconnections

are the five voltage magnitudes measured at the terminals, and its output is the input for all the neurons in the next layer. At the final layer, the switching angles are the outputs for the inverter logic control.

Each neuron a_j in Figure 23 computes a weighted sum of its n inputs Vk, $k=1,2,\ldots,n$, and generates an output as shown in Equation (33).

$$a_j = tgsig\left(\sum_{k=1}^{n} w_k V_k + bias\right) \tag{33}$$

The output is given by the tangent-sigmoid of the resultant weighted sum that usually has a bias associated to it that can be considered as an additional input. In Equation (33) w_k represents the synapse weight associated to each one of the n inputs.

3.3.1 Learning from data

Given the dataset of inputs and desired outputs, a network is required that can not only generate the desired output for the trained data, but also has the ability to generalize for points inside the hypercube space determined by the data. Learning for the computational neuron entails basically updating the network weights according to the data presented so as to efficiently represent and generalize the data set.

Performance is measured by calculating the mean squared error (MSE) as shown in Equation (34).

$$e = \frac{1}{p}\sum_{i=1}^{p}\left\| y^{(i)} - d^{(i)} \right\|^2 \tag{34}$$

where,

p: number of training data entries

y: ANN output vector

d: desired output vector

This error function is used by the back-propagation training algorithm to update the weights in order to obtain the desired results. The more neurons are used, the more complex nonlinearities can be solved. The number of neurons and layers is in most cases a trial-and-error process, as shown in Figure 24 for an 11-level cascade inverter. This figure shows how the MSE changes according to the number of neurons in the hidden layers. Note that for the SHE dataset, more than 100 neurons total will not give a good neural network response, as the data used for validation will have an error comparatively greater than the error with the trained data. Figure 25 illustrates the case for a 7-level cascade inverter. In this case one hidden layer is enough to map the data set from input to output. More than 40 neurons will cause the ANN to get into the over fitting range witch is not desired. Simulation results for this ANN will be shown in the next chapter.

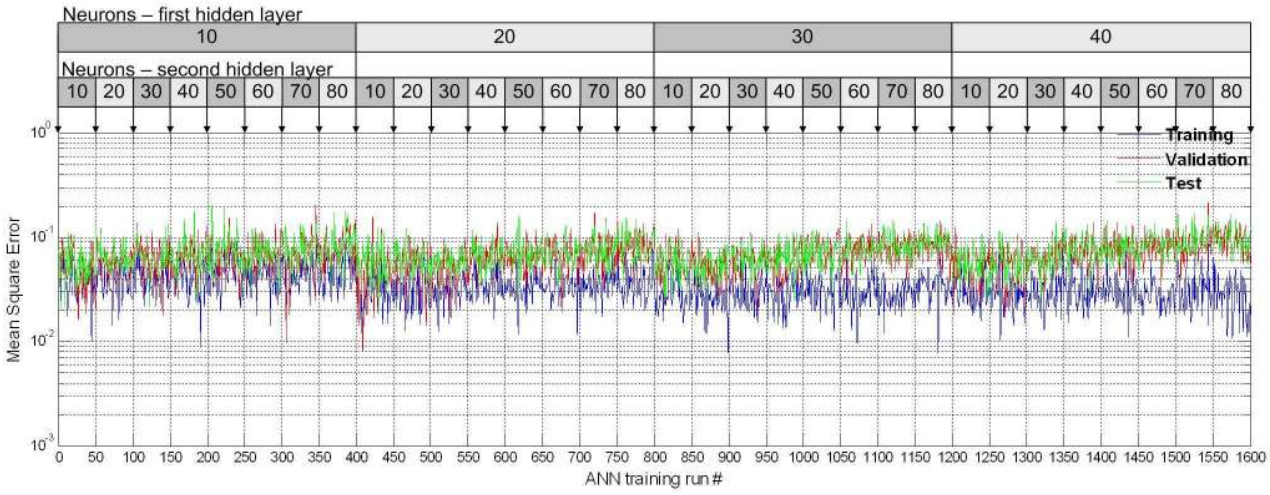


Figure 24 – ANN performance results for different number of hidden layer neurons in an 11-level inverter.

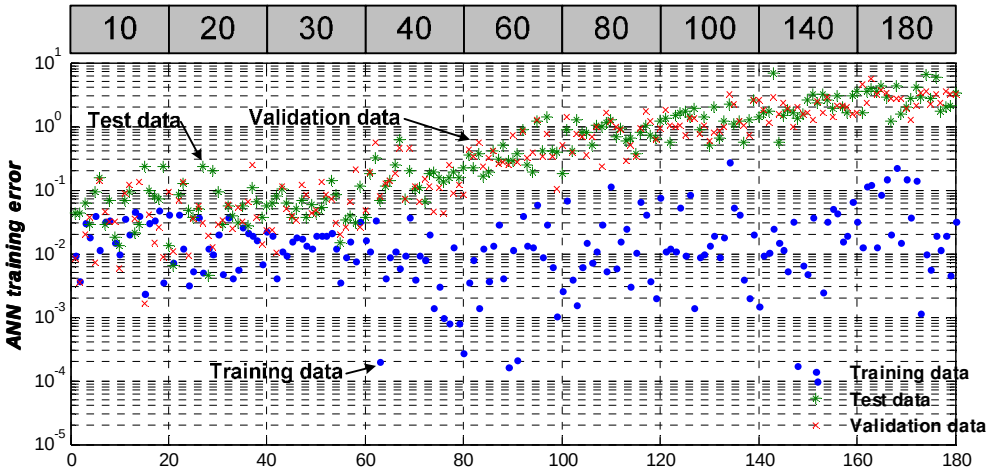


Figure 25 – ANN performance results for different number of hidden layer neurons in an 7-level inverter.

3.4 Chapter summary

The basic principles behind GA, its algorithm work flow and settings were presented. A single run using GA was shown to illustrate algorithm efficiency in

finding a solution. For the operation point used, the proposed search method returned satisfactory results. The same settings can be used for different operation points which were not shown due to the amount of data. The ANN topology and principles were introduced and illustrated. This topology was chosen based on the application in this work. The number of neurons per layer and data set size will ultimately determine performance as shown in Figure 24 and Figure 25.

Chapter 4

Multilevel cascade H-bridge inverter DC voltage estimation through output voltage sensing

This chapter presents an approach to determine the input voltage value of each cell in a cascade H-bridge multilevel inverter using a sensor at the output of the inverter to eliminate all the dc voltage sensors measuring the individual source voltages. The input voltages can be equal or unequal. The MOSFET device datasheet, the ambient temperature, and the modulation strategy are utilized to estimate the switch voltage drop to compensate for the measurement. The output voltage is then processed by a DSP unit that uses the signals that command the switches to estimate the voltage at each cell. Simulation and experimental results will be shown for a seven-level cascade multilevel inverter operating under a RLC load.

4.1 Introduction

In grid-connected or standalone applications, the DC source supplying each cell needs to be sensed and processed by the control system as the inverter power supply may vary. For example, interface of solar panels or fuel cell to the grid or for stand-alone systems requires voltage-sensing feedback to the control system [65]. Voltage sensors are also required in photovoltaic (PV) systems to accomplish maximum power point tracking (MPPT) and ensure power delivery maximization [66]. The CHB topology, with its multiple isolated power supplies, needs an individual sensor for each DC power supply. The number of sensors increases with

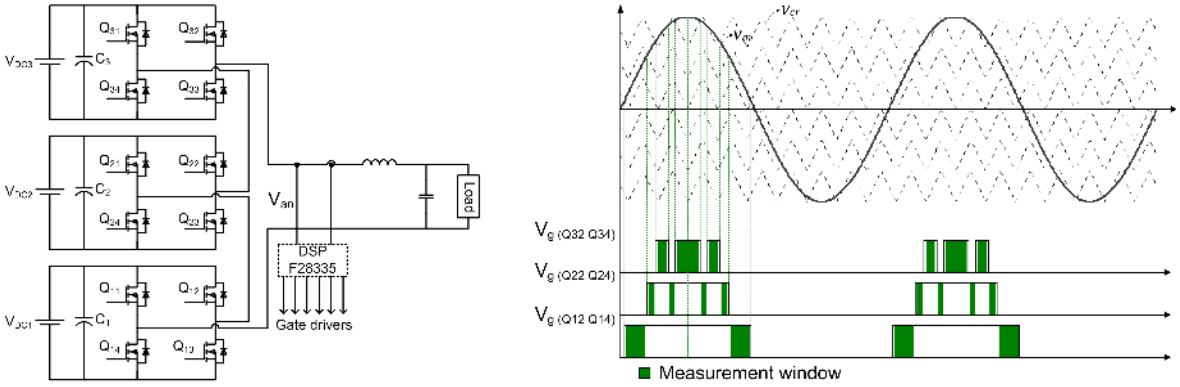
an increasing number of levels. Additionally, the sensors on the upper levels require isolation due to the independent DC sources in the topology.

The methodology proposed here calculates the individual input voltages using a single sensor at the output instead of a sensor for each H-bridge in the topology. This method will reduce the number of voltage sensors required in a multilevel topology by the number of H-bridges. One disadvantage comes from the fact that the sensor has to compensate the measured voltage with the effect of the on-state resistance, voltage drop, and stray inductance of the switches used. The approach to compensate the measured output voltage will be explained for a MOSFET-based seven-level CHB.

4.2 Level voltage estimation

The 7-level cascade inverter topology is presented in Figure 26 (a). It has three full bridge series connected configuration with three isolated input DC supplies that may have different voltage levels. In order to determine the voltage level of each voltage input (V_{DCx}, where x is 1, 2 or 3), the voltage and current before the LC filter are sensed and processed to estimate the individual voltage levels. The same logic signals that are sent to the gate drivers are used by the control system to determine the individual voltage levels. The internal control system logic function takes into account the rise time, fall time, on-state resistance, and forward voltage drop. Level-shifted carriers v_{cr} are compared with the modulating signal v_m to generate the gate signals to the H-bridges. Those logic signals are taken to derive the

measurement window where the output voltage is measured to determine the individual level. This is illustrated in Figure 26 (b).

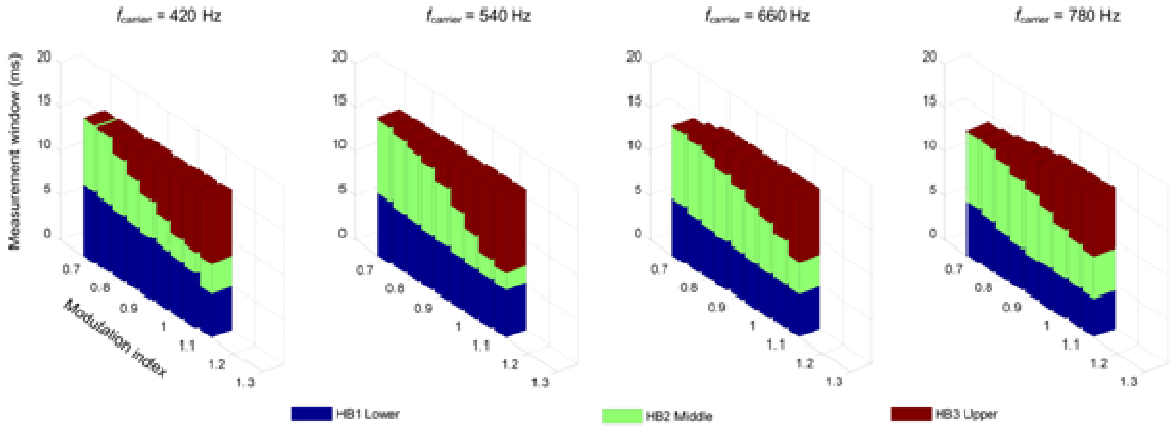


(a) *(b)*

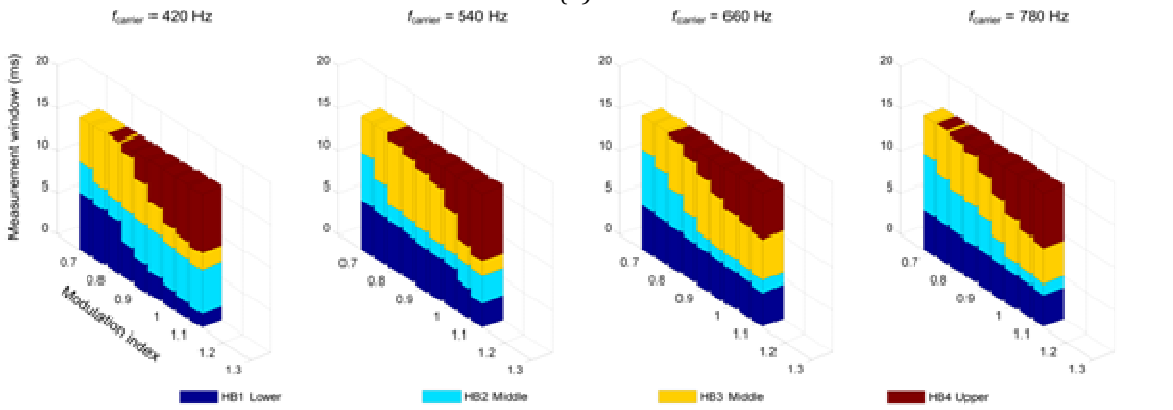
Figure 26 – Seven-level cascade multilevel inverter (a) and level-shifted modulation at f_{cr} = 540 Hz (b).

The time available for voltage measurement of each level can be determined based on the modulation index and carrier frequency. In Figure 26, a 540 Hz carrier frequency is illustrated with three cascade H-bridges (CHB) where switches Q_{1x} correspond to the lower HB and Q_{3x} the upper HB. Assuming that configuration, the total time available for each level to do a measurement is presented in Figure 27 for 7, 9 and 11 level configurations. The height of the bar indicates the amount of time spent on that level. In Figure 27 (a) the blue bar (lower) indicates the time spent on HB1, the green bar (middle) indicates the time HB1 and HB2 are both on and the red bar (upper) the time all the levels are on. The total time adds up to less than 60 Hz because of the level zero. In Figure 27 (a) for a 540 Hz carrier frequency the smallest window available is approximately 2 ms for a modulation index greater than 0.8. This is equivalent to 100 measurements using a sample time of 20 µs (50 kHz)

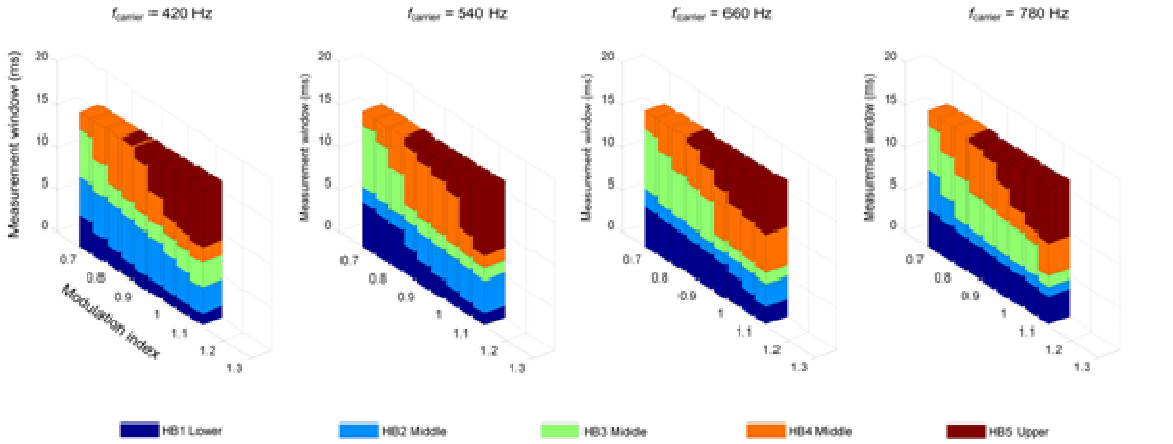
during one cycle. The plots in Figure 27 vary slightly depending on the way the carrier is generated. Additionally, a low modulation index may bypass the upper levels.



(a)



(b)



(c)

Figure 27 – Measurement window for a full cycle using level-shifted modulation at different carrier frequencies in an (a) 7 level, (b) 9 level and (c) 11 level multilevel cascade inverter.

4.3 On-state resistance

The switch on-state resistance will cause a voltage drop that needs to be compensated by the sensor. In the n-channel enhanced mode, the on-state resistance is proportional to the rate of change between the drain-to-source voltage v_{ds} and current i_{ds}.

$$R_{DS(ON)} = \left.\frac{\partial v_{ds}}{\partial i_{ds}}\right|_{V_{GS}=const.} \tag{35}$$

Then, the forward voltage drop at a given drain current I_D can be written as:

$$V_{drop} = I_D R_{DS(on)} \tag{36}$$

The inverter current is readily available at the output. However, the switch on-state resistance is dependent on the junction temperature that can be estimated if the ambient temperature and the thermal resistance over the thermal heat path can be determined. An equivalent thermal model is shown in Figure 28 where the different thermal resistances are modeled as series resistors and the transients are modeled by the capacitors.

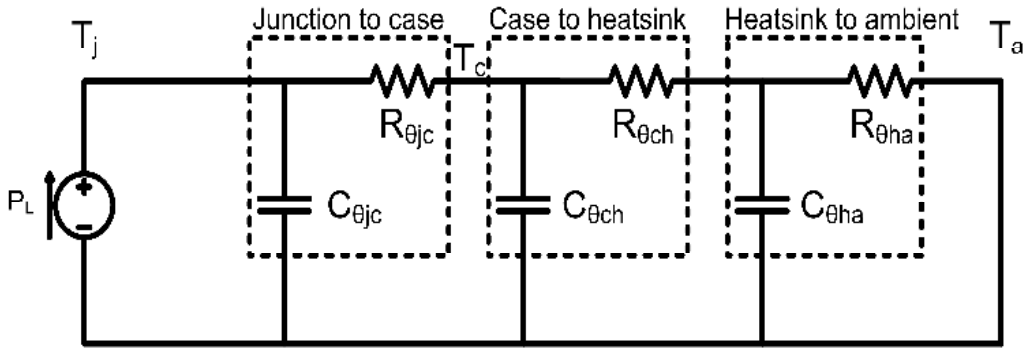


Figure 28 – System equivalent thermal path model.

Since steady state is being analyzed, the parallel capacitors will not be included in the model. The power loss (P_L) in the switch is modeled in the circuit of Figure 28 as a current source, and the ambient (T_a) and junction (T_j) temperatures are represented as the node voltages. The thermal resistances are represented by resistors $R_{\theta jc}$, $R_{\theta ch}$, $R_{\theta ha}$.

The junction temperature can be estimated in steady state for each switch by using (37),

$$T_j = T_a + P_L (R_{\theta jc} + R_{\theta ch} + R_{\theta ha}) \tag{37}$$

where,

$R_{\theta jc}$: Junction-to-case thermal resistance.

$R_{\theta ch}$: Case-to-heatsink thermal resistance.

$R_{\theta ha}$: Heatsink-to-ambient thermal resistance.

With the approximate junction temperature (T_j), the on-state resistance can be determined according to the datasheet curve. The main parameters of the power MOSFET switch used in this work are presented in Table 8.

Table 8. IRFS4127 power MOSFET relevant parameters.

Parameter	Value
Breakdown voltage (V_{dss})	200 V
Drain current (I_{ds})	72 A
On-state resistance (R_{ds})	18.2 Ω
Junction-to-Ambient thermal resistance ($R_{\theta Ja}$)	40 ºC/W
Turn-off delay time ($t_{d(on)}$)	56 ns
Fall time (t_f)	22 ns

The value of resistance shown in Table 8 is for 25°C at the junction. This semiconductor has the resistance dependence as depicted in Figure 29 that can be used to estimate the on-state resistance. From ambient temperature (25ºC) to 100ºC, the on-state resistance almost doubles.

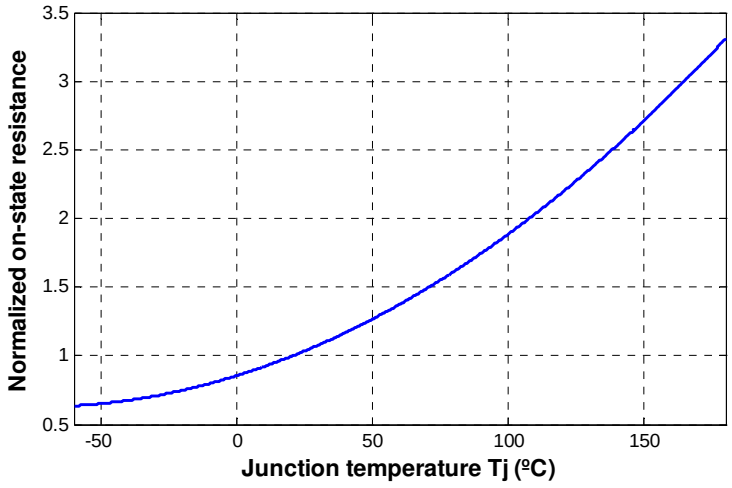


Figure 29 – On-state resistance dependence on junction temperature.

4.4 Conduction loss estimation

When operating at low carrier switching frequencies the dominant losses will be due to conduction [67-70]. The average switching frequency of each device will be inversely proportional to the number of levels *m* [45] as defined in (38),

$$f_{sw,dev} = \frac{f_{cr}}{(m-1)} \tag{38}$$

Control of a CHB requires that at any time if the level is not on (in series), a current path must exist. At any time during inverter operation, two switches will be on. If duty cycle swapping is used for a 7-level CHB, then each switch will have an average power loss as shown in (39).

$$P_L = \frac{1}{12}\left(6R_{DS(on)}\right)I^2_{D(RMS)} \tag{39}$$

Note that the switch diode voltage drop is not included since during inverter normal operation condition it does not conduct current. At any time two switches must be on to provide the voltage level ($+V_{dc}$ or $-V_{dc}$) or a current path (zero level).

4.5 Control algorithm

The control algorithm measures the output voltage before the LC filter over the first quarter of the output waveform using the gate driver signals as a reference. This is illustrated in Figure 26 (b). The measurement window shown is shorter than the signals that command the gate drivers to avoid influence of voltage transient on the switches. Such transients can be caused by stray inductances from *dv/dt* and/or

di/dt. Over the measurement window shown in Figure 26 (b) the inverter output voltage is acquired, and the voltage of each individual H-bridge is calculated based on the control algorithm shown in Figure 30. In order to determine the voltage level V_{dc1} based on the signals sent to Q_{11}, Q_{12}, Q_{21}, Q_{22}, Q_{31} and Q_{32}, the logic shown in (40) is evaluated.

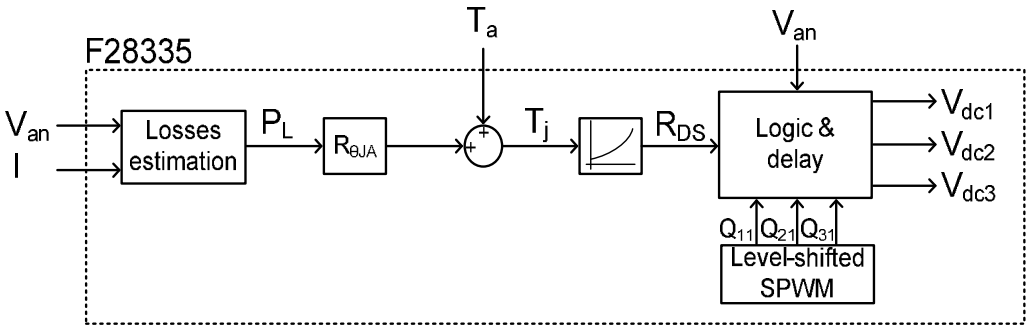


Figure 30 – Control algorithm for voltage level estimation.

$$V_{an} = V_{dc1} \xrightarrow{if} (Q_{11} XOR\, Q_{12}) \,\&\, (Q_{21} XNOR\, Q_{22}) \,\&\, (Q_{31} XNOR\, Q_{32}) \quad (40)$$

The upper levels can be determined indirectly as shown in (41) and (42).

$$(Q_{11} XOR\ Q_{12}) \,\&\, (Q_{21} XOR\ Q_{22}) \,\&\, (Q_{31} XNOR\ Q_{32}) \Rightarrow (V_{dc1} + V_{dc2}) \quad (41)$$

$$(Q_{11} XOR Q_{12}) \,\&\, (Q_{21} XOR Q_{22}) \,\&\, (Q_{31} XOR Q_{32}) \Rightarrow (V_{dc1} + V_{dc2} + V_{dc3}) \quad (42)$$

where,

& : Logic AND operator.

XOR : Logic exclusive OR operator.

XNOR : Logic inverse of exclusive OR operator.

The voltage and current values are measured to estimate the losses at each individual switch. The thermal resistance of the path can be determined by the

physical characteristics and specification of the components used. A temperature sensor provides the ambient temperature so that the junction temperature can be estimated using (37) and (39). Next, the on-state resistance is obtained to correct the difference between the actual inverter output voltage and the switches' voltage drop. This corrected output voltage is the basis for determining the voltage of each individual level.

4.6 Experimental results on cells voltage estimation

An 11-level cascade multilevel inverter was used for this experiment. The three lower H-bridges are switched as in a 7-level multilevel while the upper two H-bridges are bypassed to avoid effect of their series switches. Results using the power MOSFET presented in Table 8 for a seven-level inverter are shown in Figure 31. In Figure 31 the upper three waveforms are the gate signals for the first half of the fundamental frequency and the bottom waveform indicates the measurement window for calculating the voltage level for the lower H-bridge.

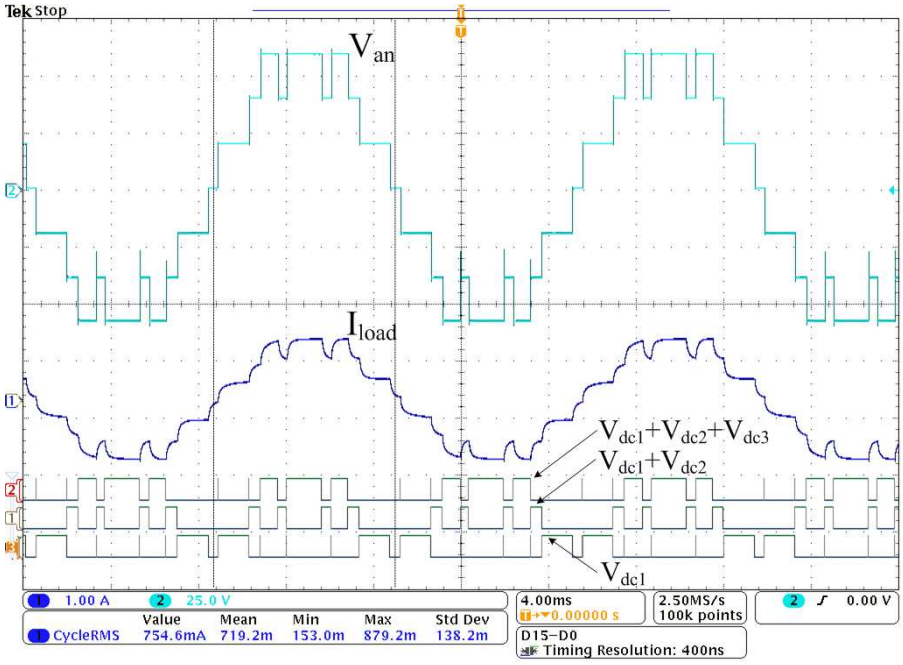


Figure 31 – CHB output voltage, current, and switching signals for the measurement window (botton).

In Figure 31 all three full bridges are operating with a 20V power supply. The measured voltages and the estimated cell voltages using this approach are presented in Table 9 for the case pictured in Figure 31. This table shows the standard deviation for the number of sample acquired. It can be noticed that a better estimation of the voltage level is obtained for the V_{dc1} due to the direct measurement of this level.

Table 9. Estimated individual cell voltage for Figure 31.

	Estimated		***Actual***
	mean	***Standard deviation***	
V_{dc1}	**19.77V**	0.0544V	**20V**
$V_{dc1}+V_{dc2}$	39.37V	0.0925V	40V
V_{dc2}	**19.60V**		**20V**
$V_{dc1}+V_{dc2}$ V_{dc3}	58.38V	0.0432V	60V
V_{dc3}	**19.01V**		**20V**

A detailed view of the waveform of Figure 31 is presented in Figure 32 where it can be compare how the pulses width are arranged in order to avoid measuring voltage during transients. A sample time of T_s=20 us is shown in this plot as dead-time between concurrent digital pulses.

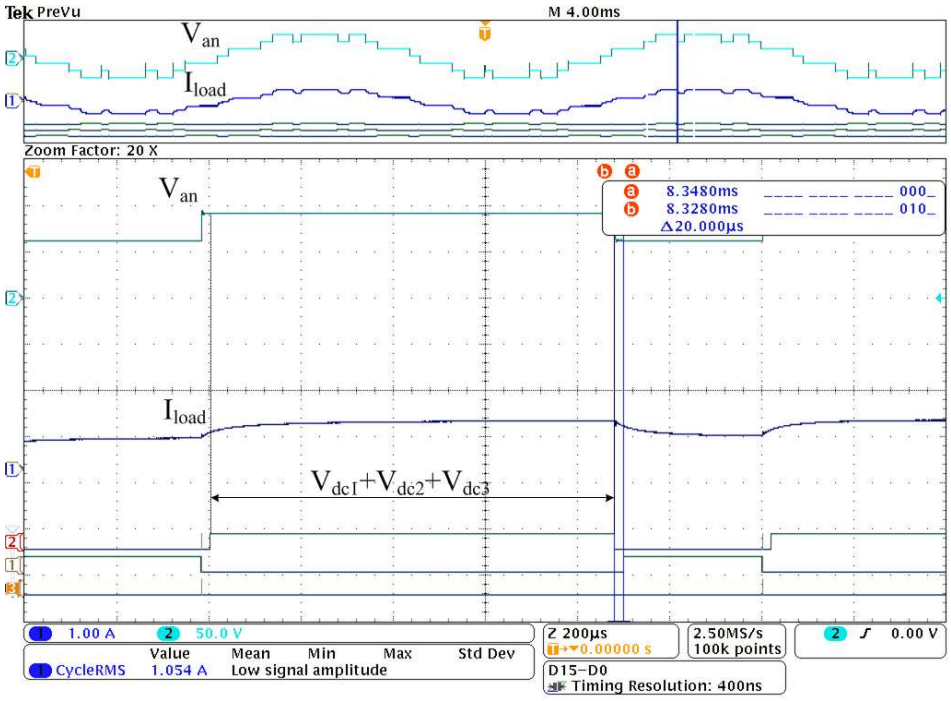


Figure 32 – Detailed view for the waveform of Figure 31 (Ts=20 us).

In Figure 33 the output voltage and the conditioned voltage to be sent to the analog input of the controller board is shown. The output waveform can be measured through a resistor network and then conditioned, using operational amplifiers, to the 3 V range of a typical controller. If measurements are done during half of the cycle as shown in Figure 33, then a resistor diode network may be used. Isolation amplifiers are another option as long as the measurements are compensated due to the sensor delay. In Figure 33 all three full bridges are operating with a 24V power supply. The measured voltages by the controller, bottom plot on Figure 33, were HB1=23.74 V, HB2=23.8 V and HB3=23.85 V averaged over the fundamental switching cycle.

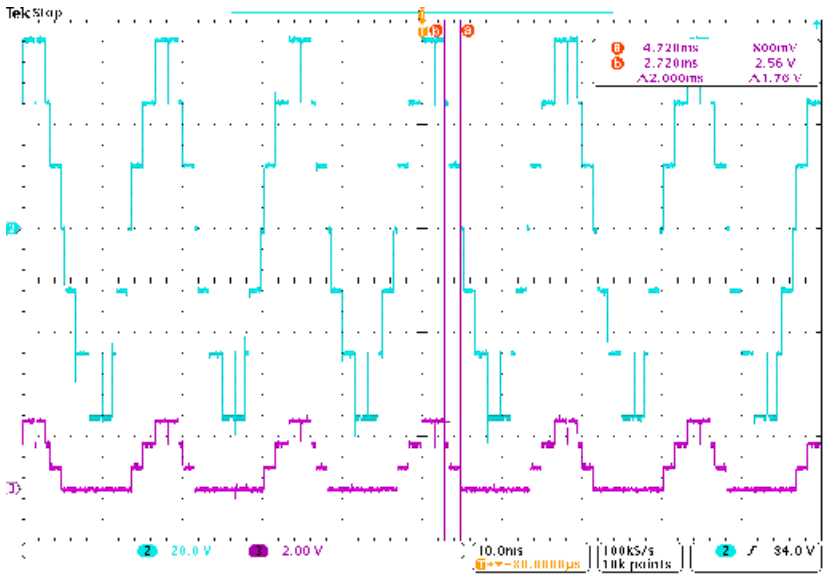


Figure 33 – Output voltage waveform (blue) at 540Hz and signal processed by the DSP (purple).

4.7 Chapter summary

Voltage estimation using multilevel inverter output voltage sensing was shown in this section. This approach can reduce the number of sensors used in the CHB topology and it can also be used together with the harmonic minimization as a way to further reduce costs. Due to the nonlinearities involved in this approach, the voltage cannot be determined as precisely as if a sensor was at the input, but this method can achieve higher cost savings for high level converters. In chapter 5 the ANN based system operating in real-time will be presented together with experimental results. This system uses sensor to determine the cells voltage.

Chapter 5

Real-time angle generation experimental results

This chapter is focused on the results obtained from using GA and ANN. Experimental and simulated data will be presented using the methodology proposed, and discussion on the results will be carried out.

5.1 Photovoltaic cell model

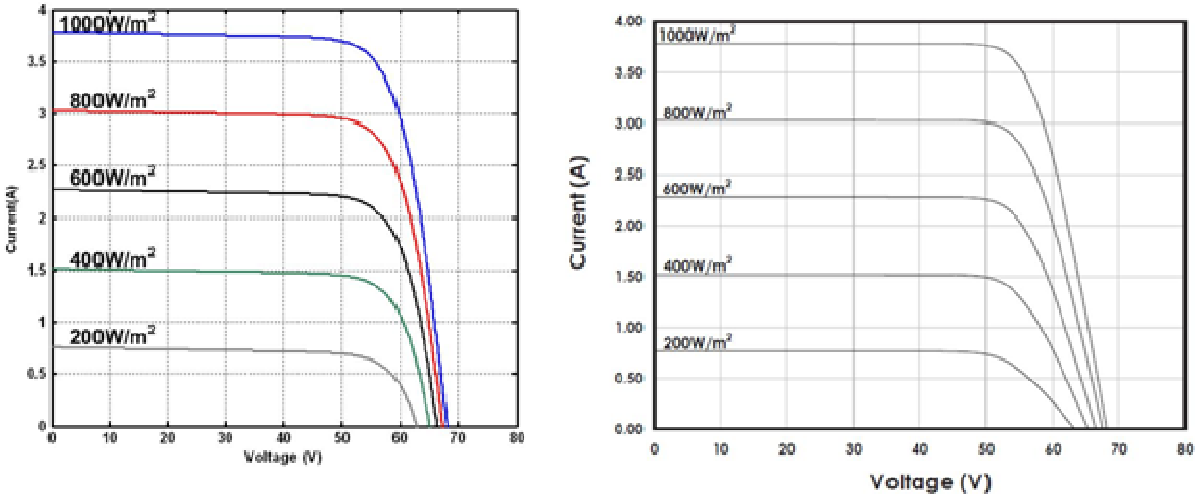
The experiments will not be restricted to power supplies. Solar panels will be used as they do not have a steady voltage profile. The solar panels to be connected to the H-bridge inverter are Sanyo HIT 195W. Its specifications and simulated parameters for use with (18) are shown in Table 10 and Table 11, respectively.

Table 10. Simulated parameters for equation 17.

Parameter	Value
I_{pv}	3.794 A
I_0	9.68×10^{-10} A
V_t	2.466 V
a	1.25
R_s	1.0973 Ω
R_p	1060.0 Ω

Table 11. Sanyo HIT photovoltaic electrical specifications.

Model	HIP-195BA19
Rated Power (Pmax)	195 W
Max. Power Voltage (Vpm)	55.3 V
Max. Power Current (Ipm)	3.53 A
Open Circuit Voltage (Voc)	68.1 V
Short Circuit Current (Isc)	3.79 A
Temperature Coefficient (Voc)	-0.17 V/ºC
Temperature Coefficient (Isc)	0.87 mA/ºC



(a) *(b)*

Figure 34 – Simulated (a) and experimental (b) I-V curves for Sanyo HIT 195 photovoltaic module.

Using the procedure previously shown where the manufacturer's datasheet is used to derive a model for use in simulation, the parameters in Table 10 were obtained. Figure 34 compares the model obtained from the PV datasheet with the manufacturer's experimental curve to show the performance of the model. The power versus voltage curve is shown in Figure 35 for five different irradiation levels. As indicated in Figure 35, the maximum power point voltage and current for standard test conditions (STC) irradiation level matches the one from the manufacture's datasheet. The fill factor was precisely matched as shown in Table 12.

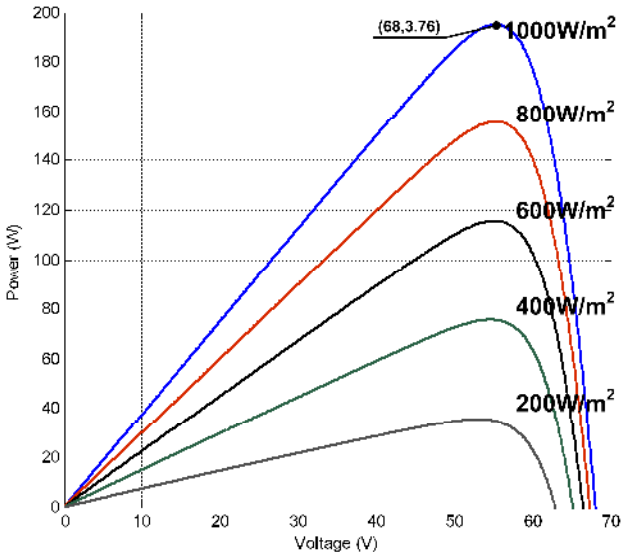


Figure 35 – Power versus voltage for Sanyo HIT 195 photovoltaic module.

Table 12. Experimental and simulated Fill Factor.

Parameter	**Value**	
	Manufacturer	Model
Fill Factor	0.7563	0.7627

The temperature influence in the curves was also implemented as shown in Figure 36 where the experimental data obtained from the manufacturer's datasheet and model is compared. The simulated curves were taken from the Simulink model implemented to run the inverter simulations.

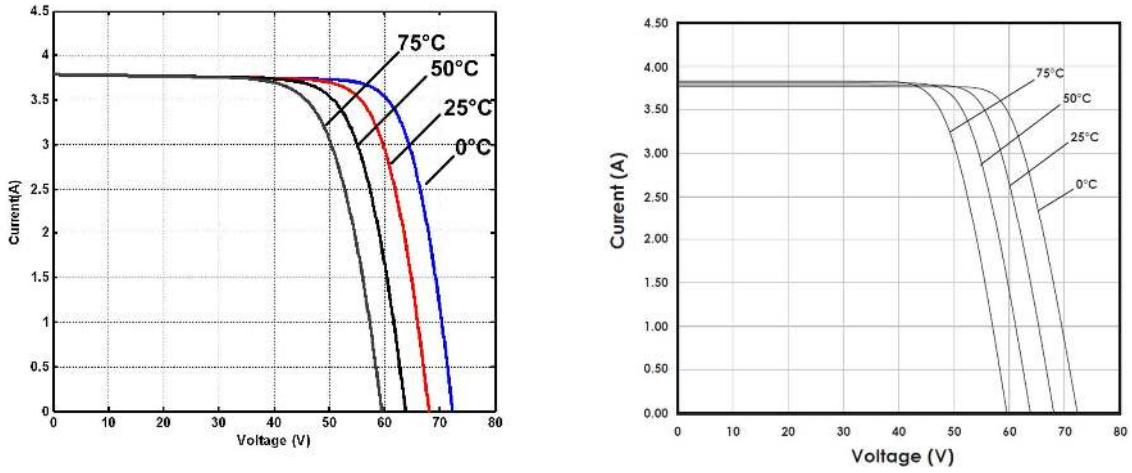


Figure 36 – Temperature variation of simulated (a) and experimental (b) I-V curves for Sanyo HIT 195 photovoltaic module.

5.2 Genetic algorithm settings

Finding the setting for a specific GA application is a trial-and-error process, and so it was for the SHE problem. Even when working on the same problem, small changes in the boundaries and/or cost function may require the algorithm's basic parameters to be set again. The Matlab GA toolbox was used in this work and the tuned setting for the SHE problem is shown in Table 13. The actual parameters may vary slightly from those in Table 13, as the cost function is changed over this work. Additionally, these same settings can be used for the 11-level and 7-level cascade configurations.

Table 13. Genetic algorithm initial settings.

Parameter	**Value**
Population size	1000
Number of generations	80
Fitness function	Scaling rank
mutation	uniform
crossover	Intermediate/fraction
selection	Normalized roulette
Fitness limit	≤1

The fitness function looking from the evolutionary point of view relates to how fit that individual is in the environment and its chance of survival. That

translates to the algorithm as a solution that produces as close as possible to the fundamental voltage while canceling the low order harmonic components as shown in Equation 43.

$$fitness = k_1\left|V_{fund} - 120\right| + k_3\left|V_{3rd}\right| + k_5\left|V_{5th}\right| + k_7\left|V_{7th}\right| + k_9\left|V_{9th}\right| \quad (43)$$

A different choice for k_n (n =1, 3, 5, 7 or 9) will change the way the fitness function is weighted and as a consequence the final solutions. This freedom to choose the coefficients can be used to make choices such as keeping the voltage close to the fundamental and allows for a certain level of harmonics to be present. That is illustrated in Figure 37 for a case where preference is given to harmonic minimization and the fundamental voltage is accepted to be within 5% range. Figure 38 shows a case where a stronger bias is given towards the fundamental allowing the harmonics to have higher values. Choice of the coefficients has some degree of subjectivity and the application requirements should be taken into account to determine the best approach to the problem.

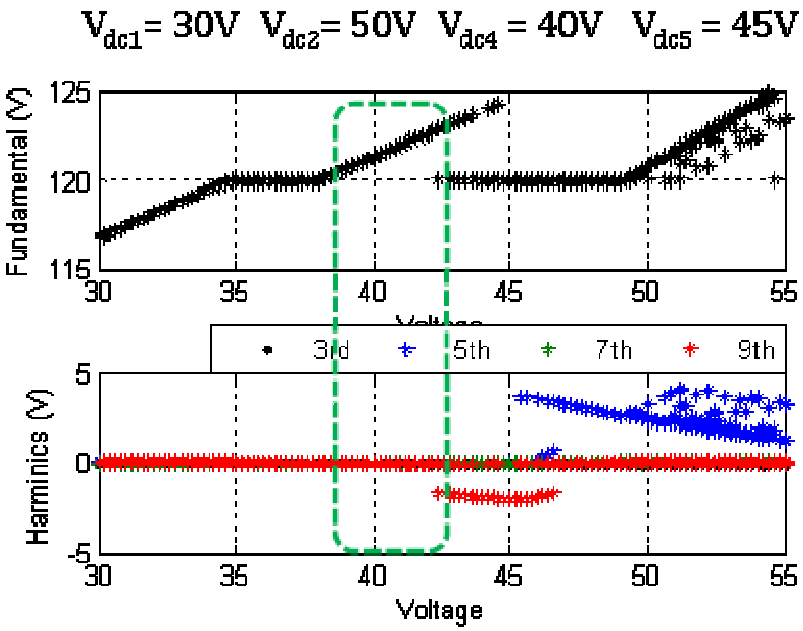


Figure 37 – Fundamental component (upper) and harmonics (lower) under Vdc3 variation.

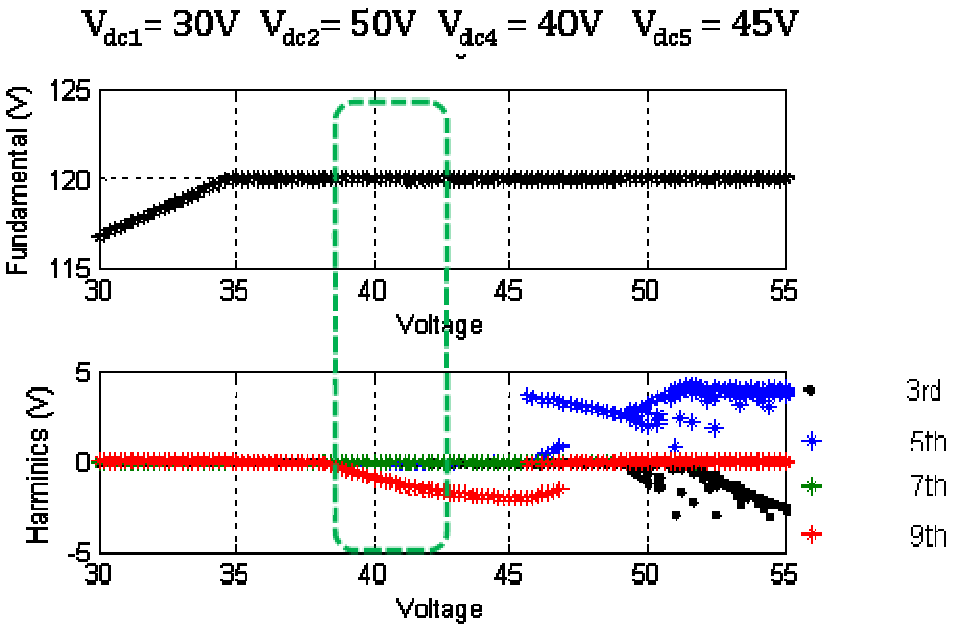


Figure 38 – Fundamental component (upper) and harmonics (lower) under Vdc3 variation with fitness function weighted towards fundamental voltage.

One of the possible choices for the coefficients of Equation (43) is shown in Table 14. Here, trial and error was utilized to determine the value of the coefficients.

Table 14. Objective function coefficients used in Figure 37 and Figure 38.

Objective function coefficients	**Value** (Figure 37)	**Value** (Figure 38)
k_1	10	10
k_2	1000	100
k_3	1000	100
k_4	1000	100
k_5	1000	100

5.3 Data set size

The solution of Equations (10-16) by GA requires a set of switching angles to be found for each combination of the input voltages. This is a combinatorial problem that can be treated with or without replacement. The resolution of the DC input sources for the data set will define the size of the data set for neural network training. For example, in a seven-level CHB inverter with DC sources that can only have two values 40 V and 42 V, the data set size can be defined as a combination of the two voltage levels ($n=2$) in groups of three ($k=3$) taken with replacement. This is shown in the first column of Table 15; a data set size of 2^3 (n^k) elements will be obtained. A second possibility is to use a combination with replacement (C_{wr}) for the

two voltage levels (*n=2*) in groups of three with replacement (*k=3*), as shown in Equation 44.

$$C_{wr} = \frac{(k+n-1)!}{k!(n-1)!} \tag{44}$$

Using Equation (44), a dataset size of 4 is obtained and is shown in the second column of Table 15. Both the sets [40V 40V 42V] and [40V 42V 40V] on the first column are considered as one entry in the second column. One disadvantage of using combination with replacement, shown in the second column, is that duty-cycle swapping is no longer possible. On the other hand, the dataset will provide an ANN that is easy to be trained and small in size which ultimately will lead to a fast algorithm execution on hardware level.

Table 15. Combinatorial possibilities for seven-level CHB with 40 V and 42 V levels.

Permutation with replacement	**Combination with replacement**
[40 40 40]	[40 40 40]
[40 40 42]	[40 40 42]
[40 42 40]	
[40 42 42]	[40 42 42]
[42 40 40]	
[42 40 42]	
[42 42 40]	
[42 42 42]	[42 42 42]

5.4 Dataset obtained through a GA run

The data set in Table 16 and Table 17 shows part of the dataset that was used to train the neural network. A feedforward ANN was used for this dataset, with a tangent-sigmoid function activation hidden layer and a linear activation function output layer. Different feedforward topologies were taken under different training methods to investigate which one best fits this application. This ANN takes the real DC source values normalized and gives the switching angles for the control system.

Table 16. Eleven-level CHB dataset for ANN training.

Input voltage (V)	**Switching angles (°)**
[25 25 25 25 25]	[0.4 9.8 19.4 26.0 41.6]
[25 25 29 35 39]	[5.0 16.5 19.8 35.7 58.4]
..	..
[33 35 35 35 39]	[7.2 28.9 41.4 52.1 73.5]
[35 35 37 37 39]	[17.7 31.4 48.8 57.5 67.7]
[36 38 40 40 40]	[21.5 37.5 51.7 58.8 70.8]
..	..
[40 40 40 40 40]	[24.9 42.2 52.1 61.1 71.9]

Table 17. Seven-level CHB dataset for ANN training.

Input voltage (V)	Switching angles (°)
[55 55 55]	[13.1 25.9 56.6]
[55 55 60]	[20.8 20.9 59.4]
..	..
[60 60 55]	[22.6 22.7 65.8]
[60 60 60]	[23.4 23.5 67.2]
[60 60 65]	[24.1 24.2 68.5]
..	..
[65 65 65]	[24.2 24.4 68.5]

5.4.1 Trained ANN obtained through the GA dataset

The ANN output angles can be seen in Figure 39. Two situations are presented in this figure through the variation of one of the five DC sources, while keeping the other four at a constant value. The top of Figure 39 shows the variation of one DC source while the other four sources are kept constant. The angles' variation under those conditions, shown for the ANN outputs (θ_1, θ_2, θ_3, θ_4 *and* θ_5), is smooth. Under this condition, the fundamental output voltage was kept in its nominal voltage (120 V) with no more than 1 V of deviation. The harmonic levels of individual 3rd, 5th, 7th and 9th harmonics are kept at very low values, as shown in Figure 40.

The eleven-level line voltage output waveform simulation using the feed-forward trained ANN is shown in Figure 41 for a random value chosen for the DC input voltages. The output waveform has 22 levels with triplen harmonics canceled out in the line voltage as shown in Figure 42. This ANN updates the angles during each cycle of the fundamental frequency. The frequency spectrum of the output voltage is shown in Figure 42 for a cycle of the fundamental frequency. Here, the 3rd, 5th, 7th and 9th harmonics are minimized using the angles provided by the ANN, and a peak line output voltage of 208 V is achieved. An analysis of the outputs of the neural network shows that in the worst case situations the individual voltage harmonics do not exceed 1.5% of the fundamental output voltage.

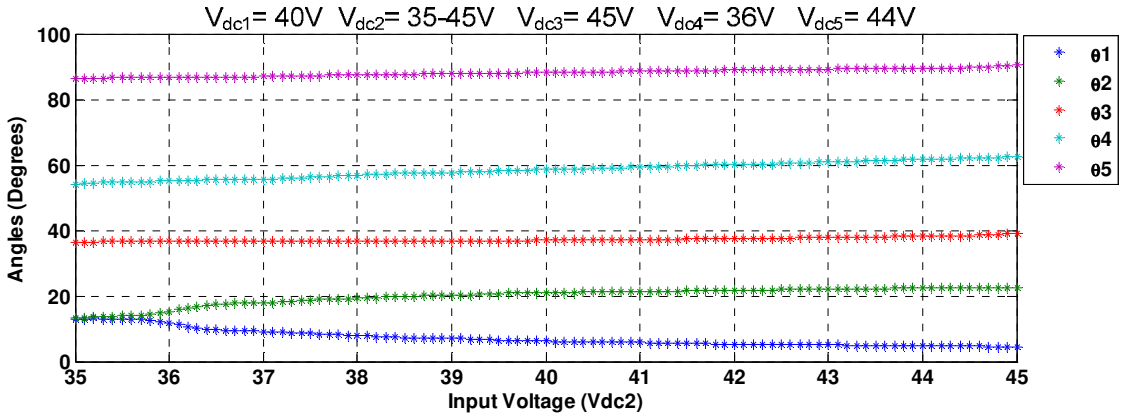


Figure 39 –Neural network generalized angles output under DC input voltage variation .

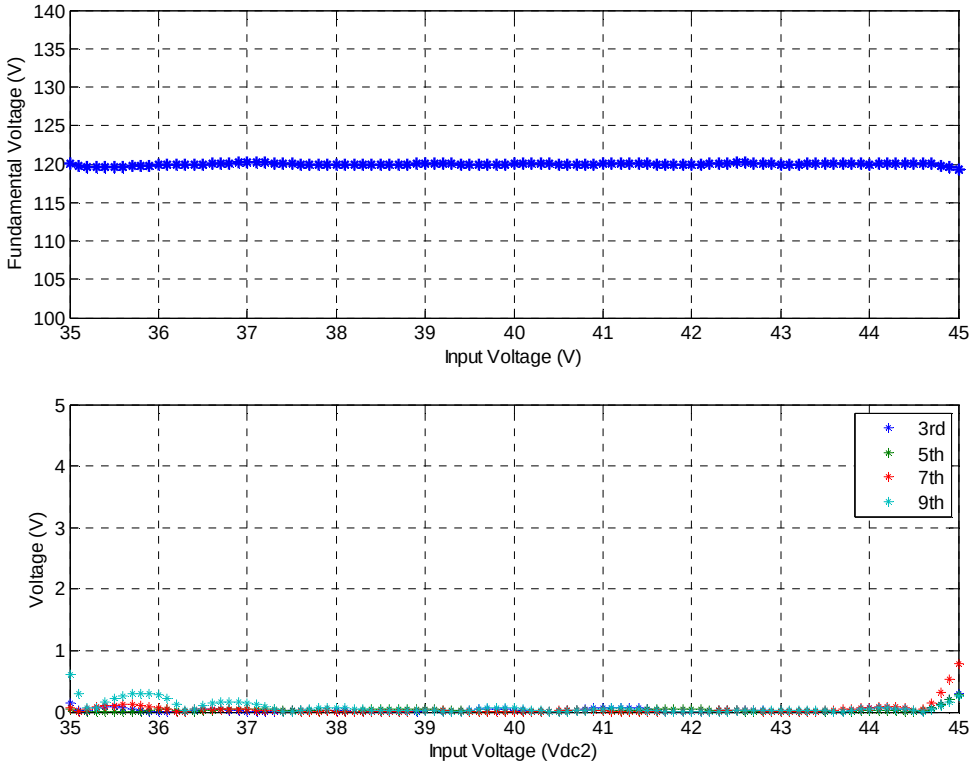


Figure 40 –Output voltage characteristics (upper) and harmonic content (lower) for angles generated by Figure 39.

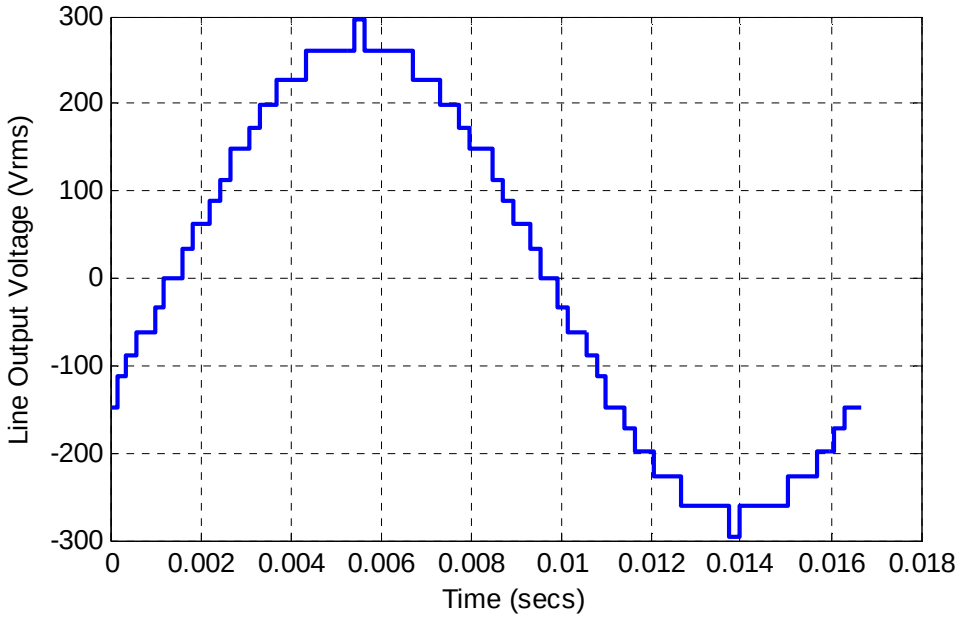


Figure 41 – Multilevel inverter line output voltage waveform.

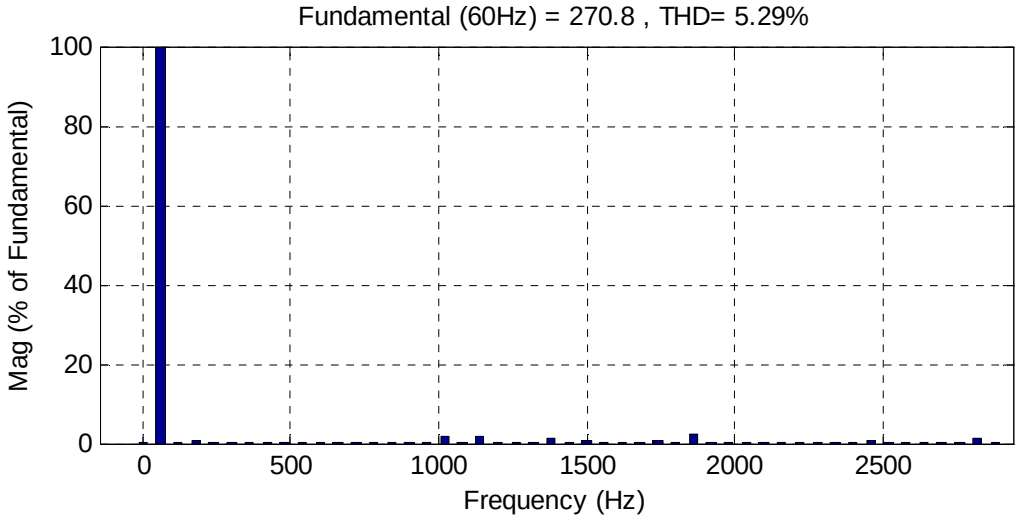


Figure 42 – Output voltage frequency spectrum for Figure 41.

The new ANN trained for the 7-level case is shown Figure 43. One case is presented in this figure through the variation of one of the three DC sources, while keeping the other two at a constant value. The top graph shows switching angles for one DC source varying, while the other two sources are kept constant. The angles' variation under those conditions, shown for the ANN outputs (θ_1, θ_2 *and* θ_3), is smooth. Under this condition, the fundamental output voltage was kept in its nominal voltage (120 V) with no more than 2 V of deviation. The harmonic levels of individual 3rd and 5th harmonics are kept at very low values, as shown in this figure.

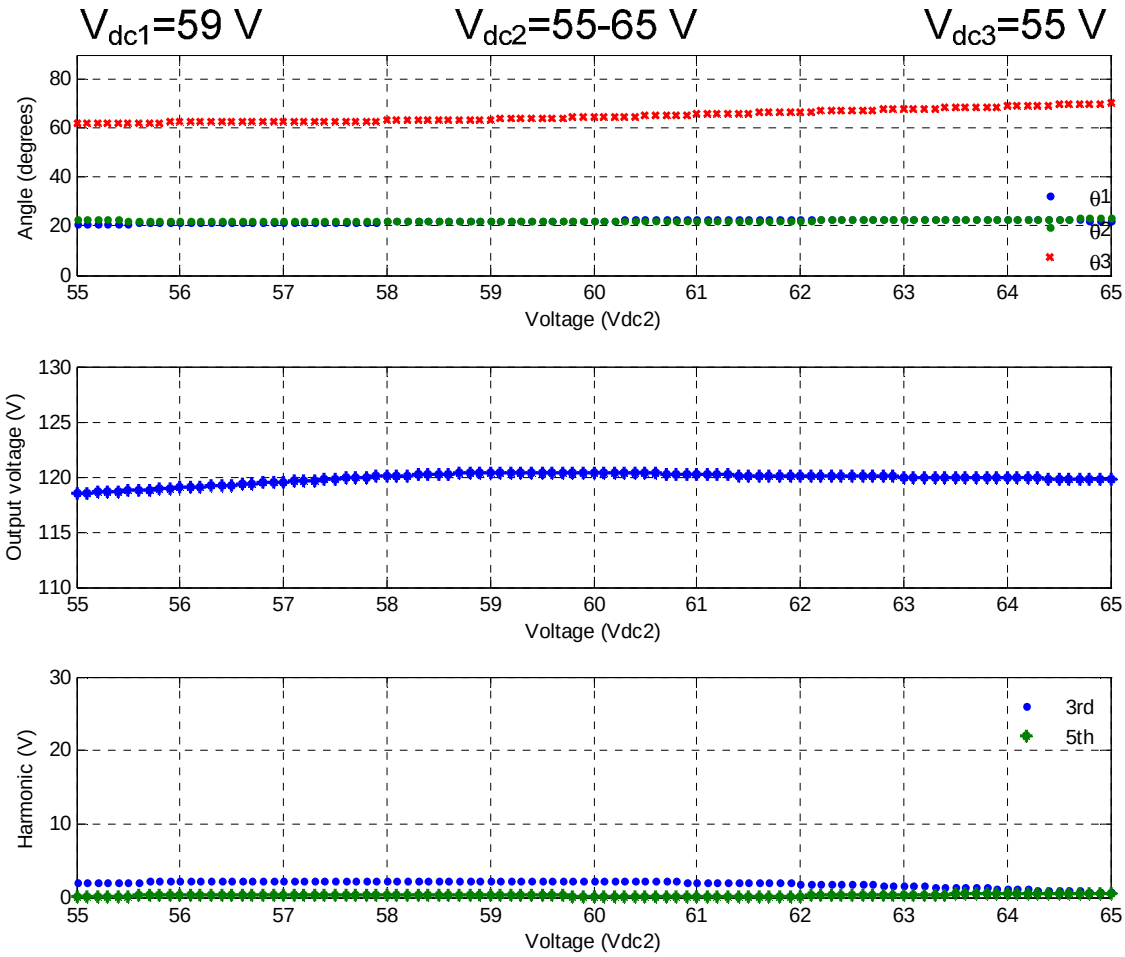


Figure 43 –Neural network generalized angles, output voltage and harmonic content for cascade 7-level inverter.

The Simulink model that generated the above figure is illustrated in Figure 44. It includes the solar panel model, the ANN trained, the load and the cascade multilevel inverter. This model can be uploaded in a DSpace or DSP system for real-time emulation.

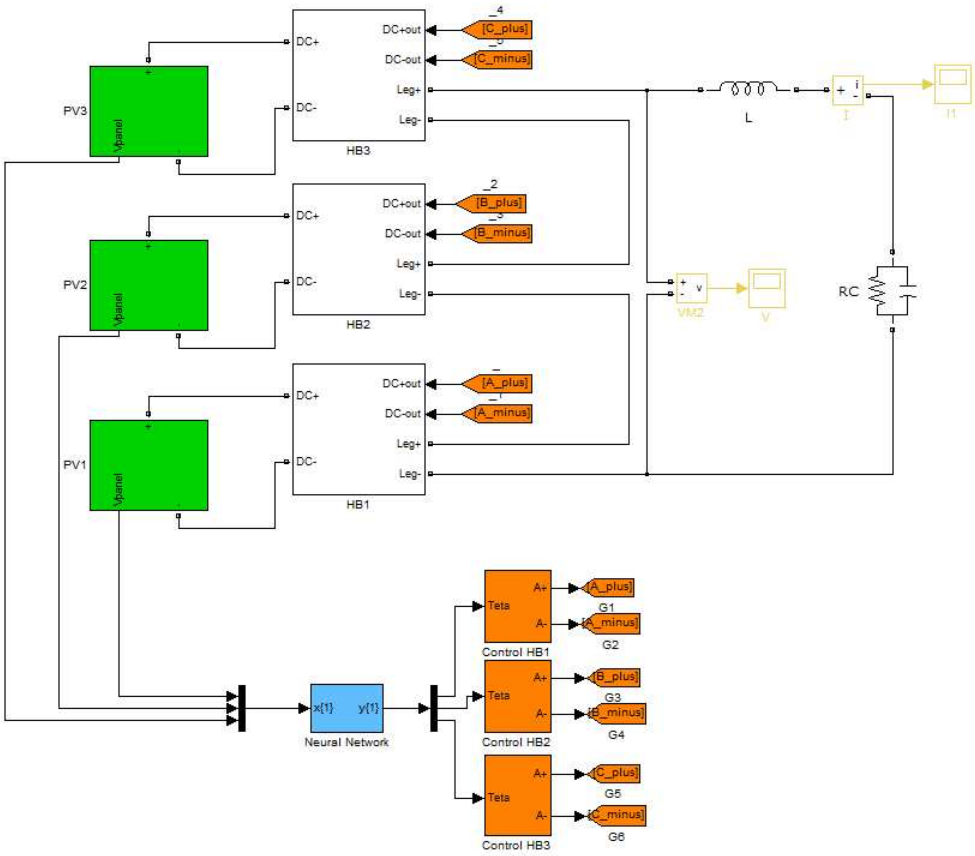


Figure 44 –Simulink model of the overall real time system: multilevel inverter, neural network and solar panels.

5.4.2Fitting performance of ANN compared to GA found results

The purpose of the ANN is to learn from the data it is presented to. In a 7-level cascade inverter the dataset to be used for the ANN for training consists of three input voltages that are related to three output switching angles. This mapping from three voltages to three angles is the three-dimensional mapping the ANN has to accomplish. Performance is evaluated during training as show in Figure 45. The

plot shows that an ANN with 30 neurons can give the best performance with minimum number of neurons for both training and validation data.

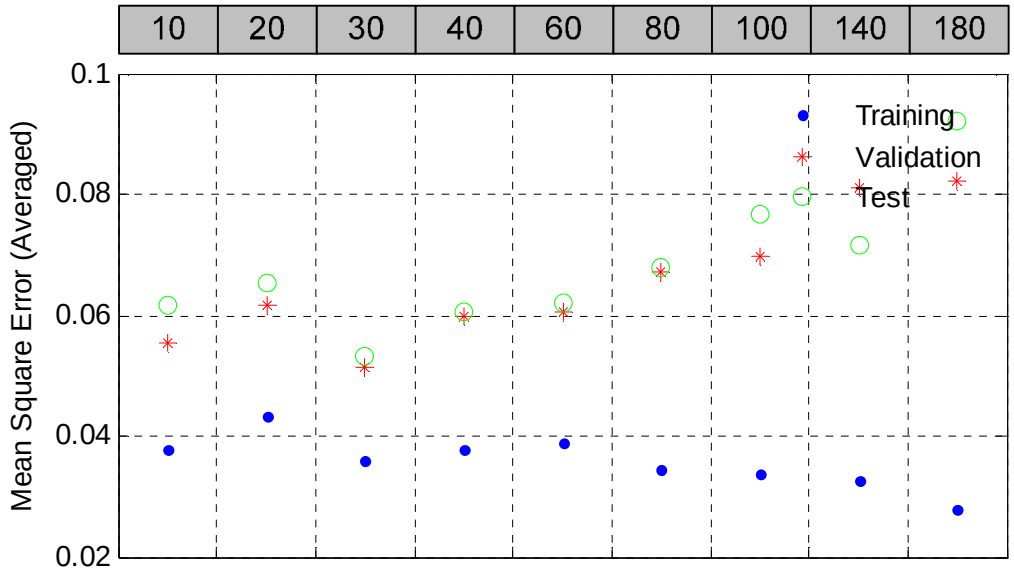


Figure 45 –ANN performance results for different number of neurons in a 7-level inverter.

A perfect fitting is not achievable using this technique for most cases as it involves the use of interpolation, extrapolation and not all the data is presented to the network.

GA is in charge of find the solutions for a set of input voltages presented. This dataset is used to train the ANN. The ANN chosen here is the one presented in Figure 45 with 30 neurons. The comparison between the angles generated by this Network and the target angles found by GA are presented in Table 18. This approximation is sufficiently close for the purpose of harmonic minimization. The average error is 1.5° between GA exact solution and ANN output angles.

Table 18. Exact and ANN approximation of the output switching angles.

Voltage $[V_{dc1}\ V_{dc2}\ V_{dc3}]$	Switching angles (GA) $[\theta_1\ \theta_2\ \theta_3]$	Switching angles (ANN) $[\theta_1\ \theta_2\ \theta_3]$
[55 55 54]	[09.08 28.81 55.25]	[9.84 27.75 55.12]
[55 56 54]	[12.46 26.73 56.80]	[14.35 24.67 56.72]
[55 57 54]	[15.35 24.73 58.12]	[17.84 22.40 57.99]
[55 58 54]	[20.50 20.50 59.39]	[19.71 21.34 58.85]
[55 59 54]	[20.67 20.67 60.02]	[20.46 21.17 59.50]
[55 60 54]	[20.84 20.84 60.77]	[20.65 21.42 60.03]

Another performance indicator is the output voltage generated by the trained ANN that is expected to be close to 120V and also the THD measured until the 5th harmonic. This performance indicator is shown in Table 19. The last three lines of this table shows that a close solution was found by GA which the ANN tries to fit in with some error in the process of training. This approximation feature of ANN is what causes the difference seen on the 4th and 5th column of this table. As a result the THD calculated using the ANN outputs may have higher values than the one calculated by GA.

Table 19. GA and ANN performance for fundamental voltage and THD until the 5th harmonic.

Voltage $[V_{dc1}\ V_{dc2}\ V_{dc3}]$	Fund. Voltage (V_{rms}) GA	Fund. Voltage (V_{rms}) ANN	THD_5 (%) GA	THD_5 (%) ANN
[55 55 54]	120.00	120.42	0	0.5
[55 56 54]	120.00	120.47	0	0.6
[55 57 54]	120.04	120.35	0	0.4
[55 58 54]	120.05	120.40	0.01	0.4
[55 59 54]	120.33	120.60	0.1	0.5
[55 60 54]	120.50	120.91	0.3	0.6

Table 19 reflects the overall error behavior of the ANN chosen based on Figure 45 and is the same ANN used when running the experiments. It indicates that the quality of fitting is excellent for the purpose of minimizing harmonics while keeping the fundamental.

5.5 GA exploration of the search space

The set of equations from (10) to (16) do not have solutions for all the range, which means that at some input voltages, there are no solutions to satisfy the criterion desired for the fundamental and to completely cancel the low-order harmonics. However, in this case the GA will look for an approximate solution that is nearer the requirement. This will introduce a set of solutions that partially satisfy the set of Equations (10) to (16). The procedure here will allow the fundamental to be around its nominal value (user defined 5%) and/or a low order harmonic that is

not canceled but instead is very low. This characteristic is very important for the neural network training process and is shown in Figure 46 with only one of the DC sources varying. Beginning at 39 V, the GA cannot find a solution because none exists in that range. This means that a zero fitness value cannot be reached. This figure shows an increase in the output voltage caused by the approximated solution found (a small fitness function value that is acceptable). In this case the 5th, 7th, 11th and 13th harmonics are minimized to less than 1% with the output voltage close (<5%) to its nominal value.

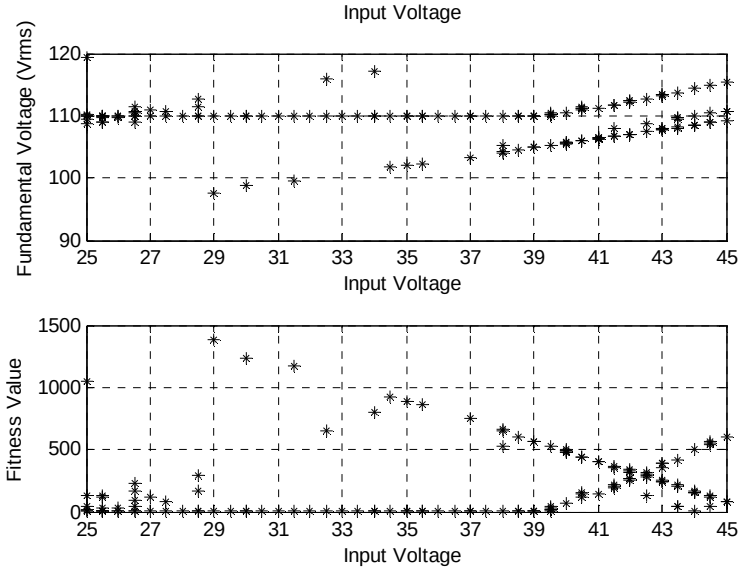


Figure 46 – Output voltage as a function of DC source input variation and quality of solutions measured by genetic algorithms fitness value.

Figure 47 shows how the GA can be weighted towards harmonics or fundamental voltage. In this figure only V_{dc3} is varying while the other sources are kept at the indicated values. As highlighted by the green rectangle on the right plot once the GA is set to keep fundamental the harmonic content start to increase for

the 9th harmonic. On the other hand, if the fundamental voltage is allowed to be within a range as shown on the left plot the harmonics can be eliminated or greatly minimized.

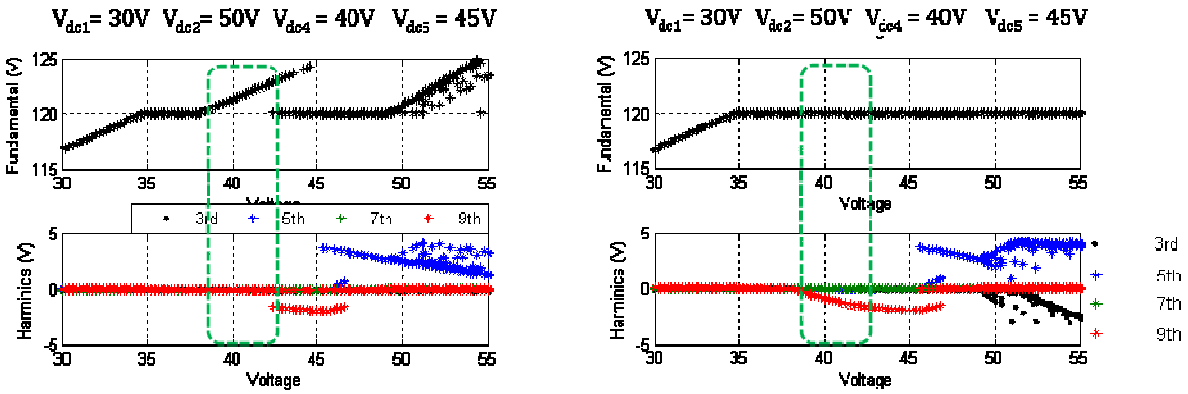


Figure 47 – Fundamental component (upper) and harmonics (lower) under Vdc3 variation for different GA search parameters.

5.6 Neural network real time implementation

The control system was implemented using DSpace DS1103 board, a real-time computing platform. The number of I/O interfaces makes the DS1103 a versatile controller board. It provides a selection of interfaces, including 50 bit-I/O channels, 36 A/D channels, and 8 D/A channels. For additional I/O tasks, a DSP controller unit built around Texas Instruments'TM320F240 DSP is used as a subsystem.

Figure 48 – DS1103 PPC controller board.

This allows the Simulink model to be compiled and uploaded in the processor without need for major changes or need to rewrite the source code. The DSpace processor is responsible for data acquisition of the DC source voltages fed to the ANN that performs the calculation of the appropriate switching angles. The second processor generates the corresponding pulses. The step size employed in the computation was 50 μs. For DSP compilation, Target Support Package (TSP) for Simulink was used so that a similar procedure can be used to compile the Simulink code into the DSP.

Because the modulation is software-synchronized there is a little fluctuation in the pulses width by a couple hundred nanoseconds. This is due to the imprecision associated with a software timer for a real-time operating system such as the one

running at the target computer. That does not compromise the stability of the overall system, and has little impact on the harmonic elimination performance.

5.7 Experimental results

The implemented system test bench is pictured in Figure 49. The solar Panel's connection and control is not shown in this figure. Each full bridge in the cascade topology has a 1mF DC electrolytic capacitor and four 200V/40A MOSFETs. The switches are placed into sockets so they can be changed for different applications. The capacitors can be optimized for each specific application to minimize its size. The focus in this work is on harmonic control and so capacitor optimization is suggested as a future work.

DSpace or DSP are the hardware-in-the-loop (HIL) system that allows real-time control of the system. The control topology used in this experiment uses two systems: one is the main station where Simulink® is installed, and the control is implemented, the second is the DSP or DSpace where the analog and digital I/Os to control the inverter and acquire signals. Compared to code composer, this system has a shorter implementation and debugging time as a result of a user-friendly interface; however, this comes at the cost of a sample time that can range from 30 us to 150 us in this setup.

Figure 49 – Eleven-level cascade multilevel inverter setup.

In Figure 50 a more detailed view of the single phase multilevel inverter prototype built for this dissertation is shown. Among the features it has a flexibility to use different control platform, snap-in sockets for power semiconductors, IC socket for easy removal of components, heat sink capable and the capacitors can be easily changed if needed. A thorough schematic view of the board, including all components used and its specification, in presented in Figure 51 and Figure 52.

Figure 50 – Eleven-level cascade multilevel inverter hardware.

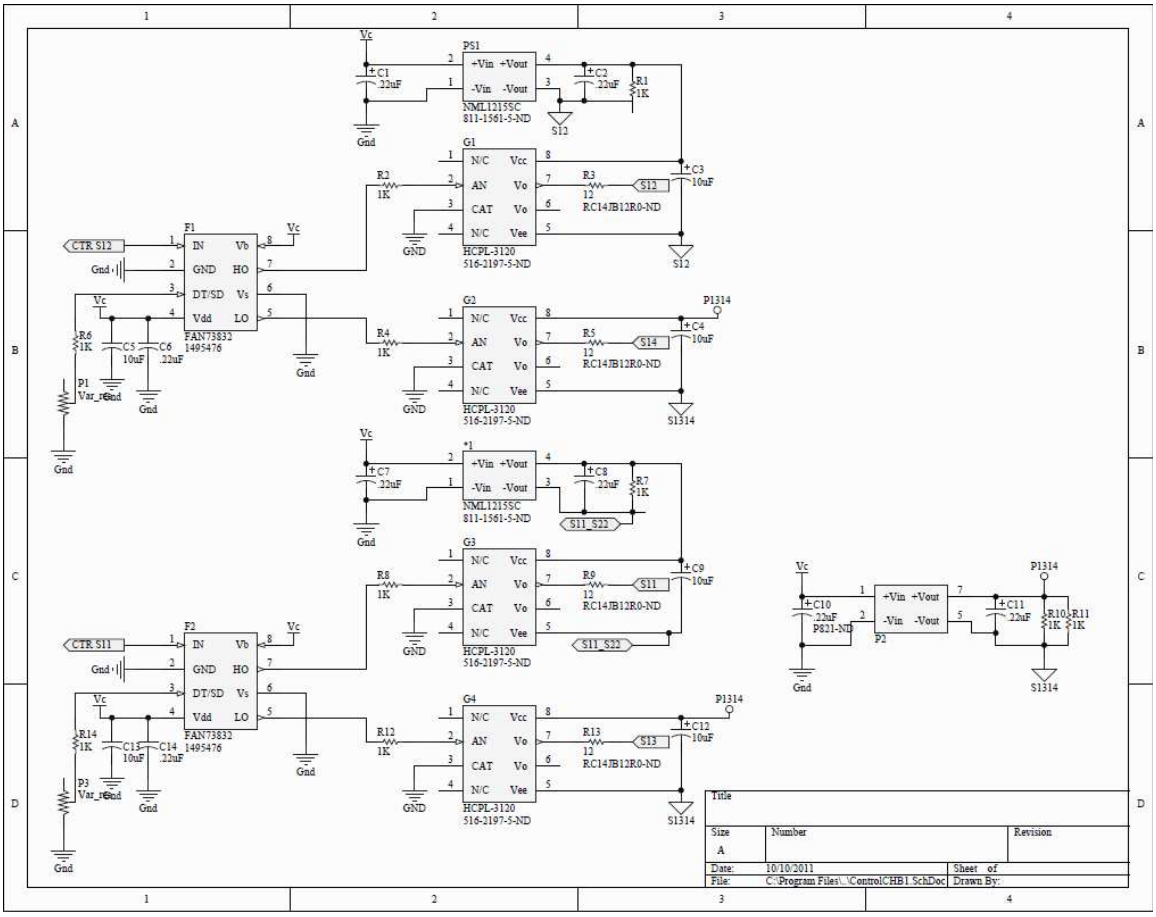


Figure 51 – Eleven-level cascade multilevel schematic view of the logic control.

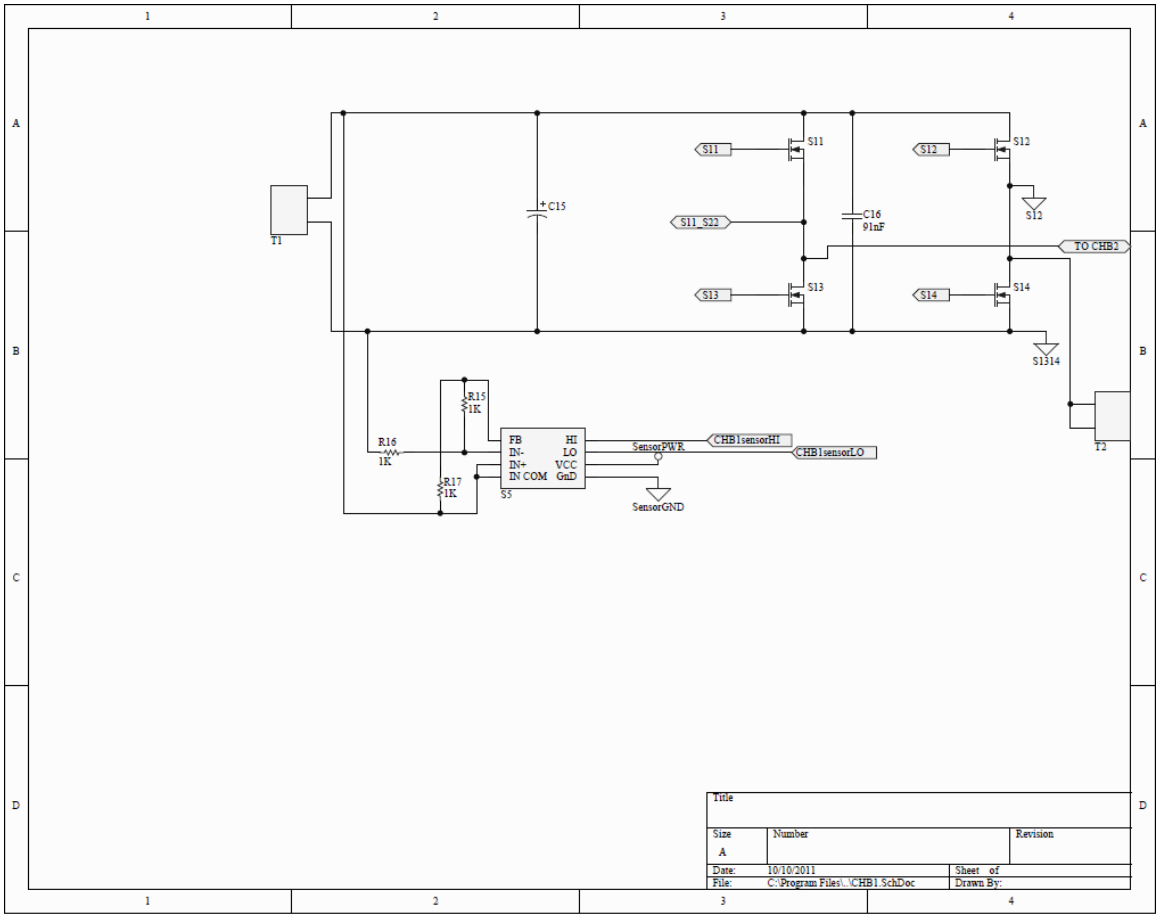


Figure 52 – Eleven-level cascade multilevel schematic view of one H-bridge and the voltage sensor.

The solar panel installation is shown in Figure 53. It consists of five 192W Sanyo solar panels. Both positive and negative connections are available to be used with the inverter.

Figure 53 – Photovoltaic panels' setup.

The cascade multilevel inverter prototype used can be configured to operate as a single-phase 11-level H-Bridge inverter that is controlled by a DSP or DSpace. The controller has analog and digital I/O boards for data acquisition, processing and control of the prototype

In Figure 54, experimental results for an eleven-level inverter operating with unequal DC sources are shown with the voltage values indicated. The blue line (darker line) shows the voltage variation, and points *a* and *b,* indicated in this figure, show that the angles were successfully updated after the step. The frequency spectrum for the steady voltage waveform of Figure 55, is shown in Figure 56,

where it can be noticed that the target harmonics were minimized to less than 1% with exception of the 13th harmonic, which is around 1.2% with a THD of 8.7%. This same figure shows a high value of the 3rd and 9th harmonics, those harmonics were not the target harmonics. Figure 57 shows experimental results for a new ANN trained to minimize the 3rd, 5th and 7th. This figure shows that the target harmonics are below 1% of the fundamental. A new ANN can always be trained to a new dataset so harmonics can be arbitrarily chosen.

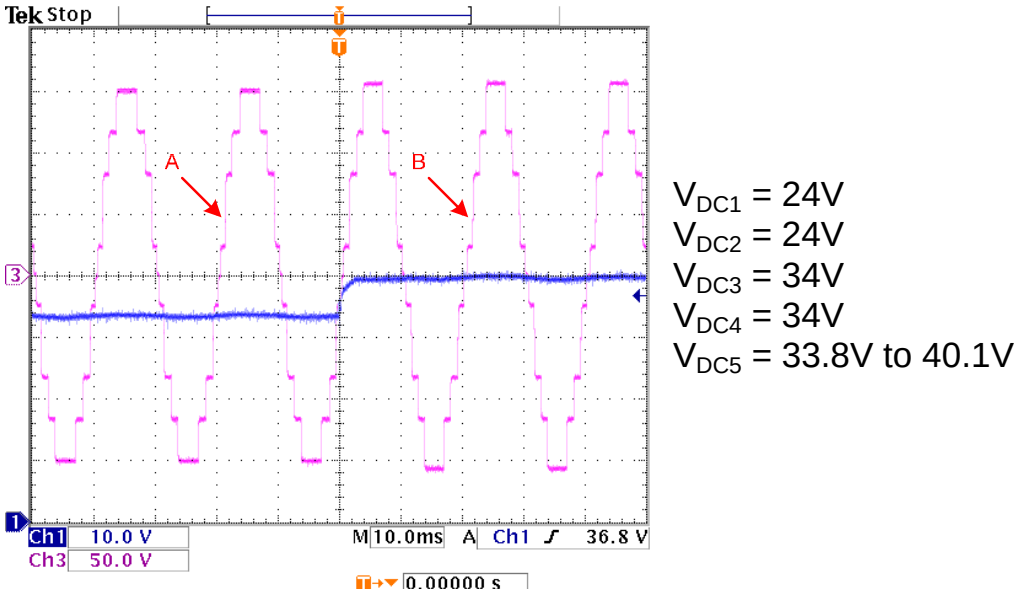


Figure 54 – System response to a DC input source step change (blue) and the inverter output voltage (purple) reconfiguration response.

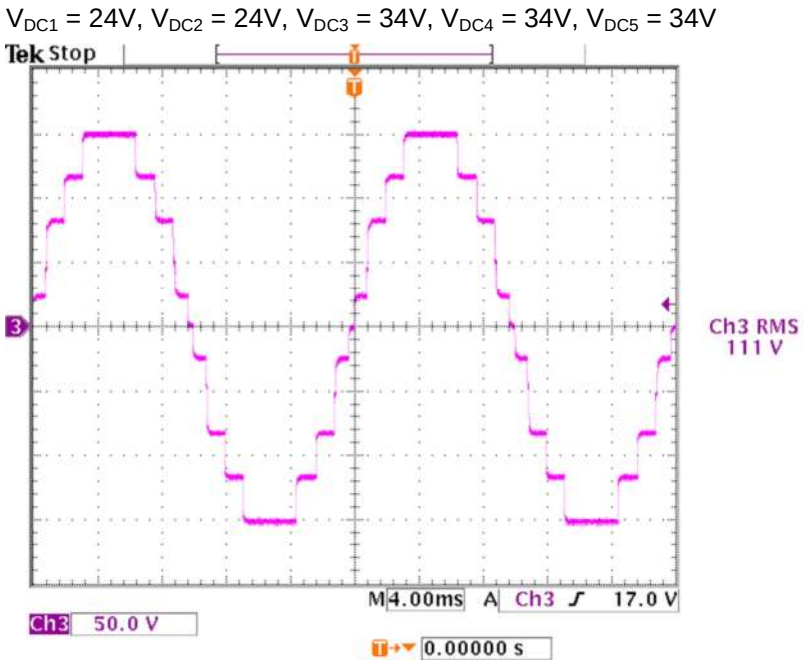


Figure 55 – Experimental output voltage waveform.

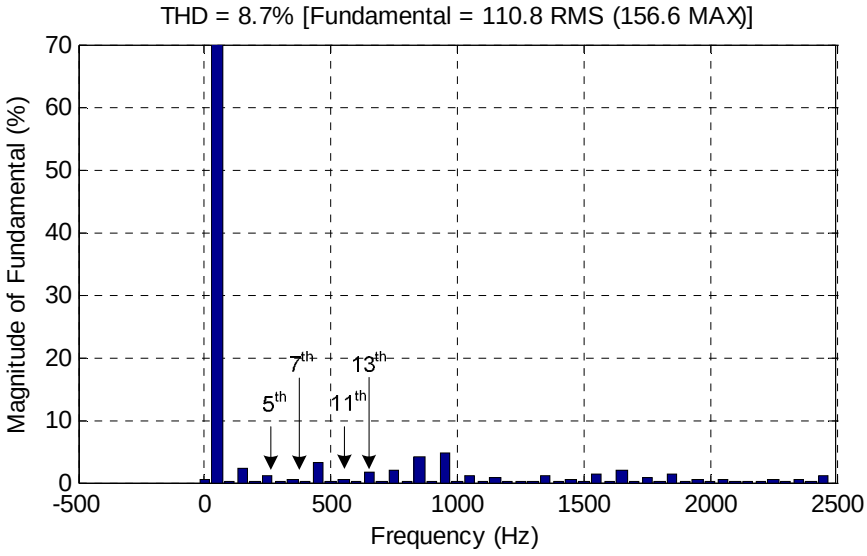


Figure 56 – Frequency spectrum of output voltage waveform for Figure 55.

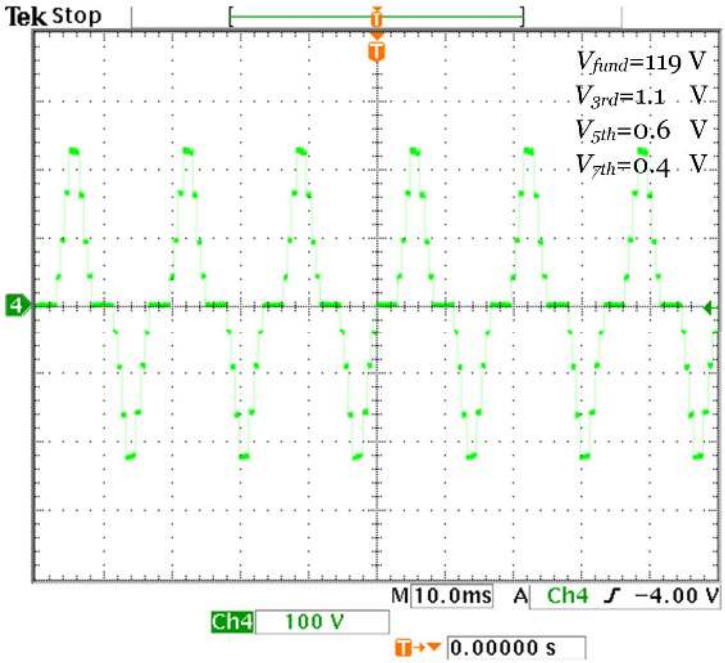


Figure 57 – Multilevel CHB output voltage and harmonic content.

This system has the ability to update the angles in real time at speeds higher than the line frequency (1/60 sec), but the angle update is done at the end of a cycle of the low frequency to avoid even harmonics. It is assumed that a substantial step variation in the magnitude of the DC source inputs may occur for this approach, so that the system should be able to adapt its output. This case is shown in Figure 54, where a step change is applied to one DC source which steps it from 33.8 V to 40.1 V. This figure shows that after one cycle of the output waveform the angles are adapted to the new condition; the two points indicated by the arrows. The ANN placed a small decrease in the angles to adapt to the new condition. This step change value was chosen also because it is visually apparent just after the DC step change. Due to the low computation time required by the neural network, the angles are

always available long before a cycle ends, but they are updated only at the end of the cycle.

5.7.1 Experimental results with load

In order to validate the approach, experimental results of the system operating at different load conditions as well as different number of levels were obtained. Table 20 shows two load conditions used. For all experimental tests with load, the values of C and L were kept with resistance values being switched on and off. Figure 58 shows the circuit connection to run the load tests shown in Table 20. The voltage output waveform will be shown before the filter (V_{an}) as indicated in this figure and the load current (I_{load}) is the resistor current as indicated.

Table 20. Parameters used for LC and RLC loads.

Parameter	**Value Case 1**	**Value Case 2**	**Value Case 3**
L	5 mH	5 mH	5 mH
R		107.1 Ω	107.1 Ω
C	10 uF	10 uF	

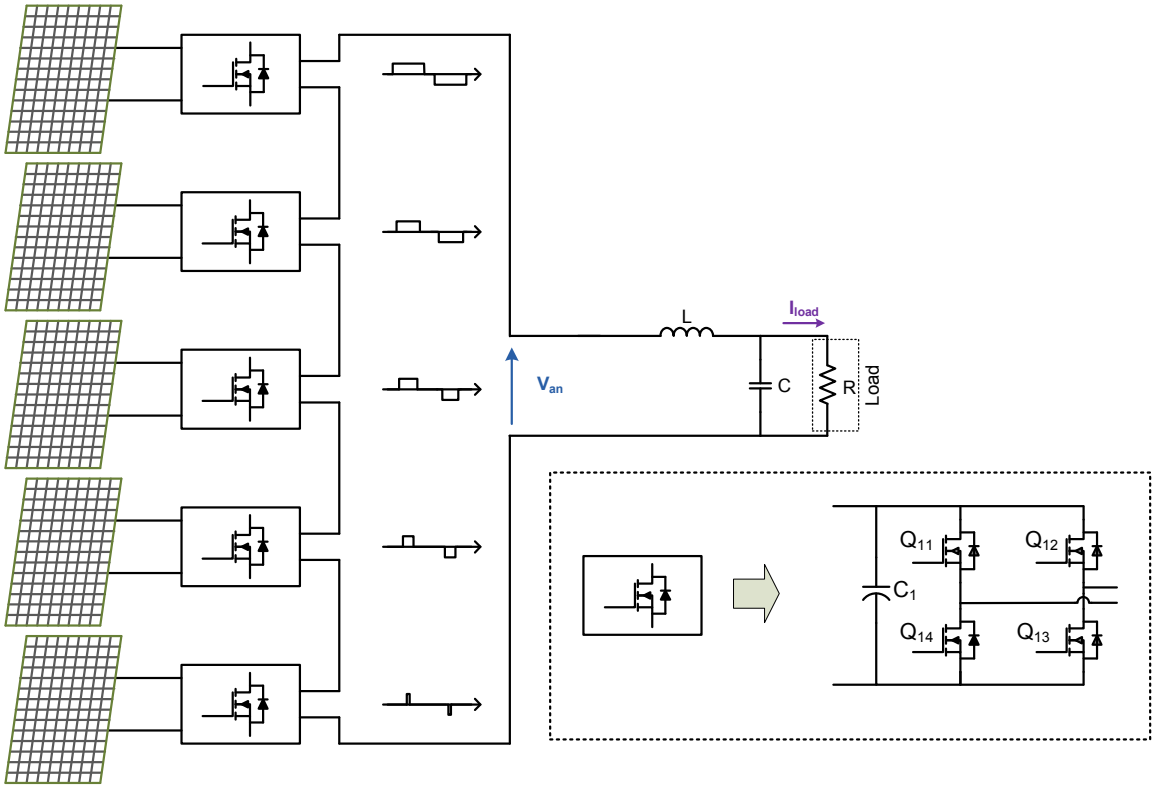


Figure 58 – Multilevel inverter connection diagram for load test in Table 20.

An 11-level output voltage using load conditions of case 1 is illustrated in Figure 59 with load current shown in the bottom half of the graph.

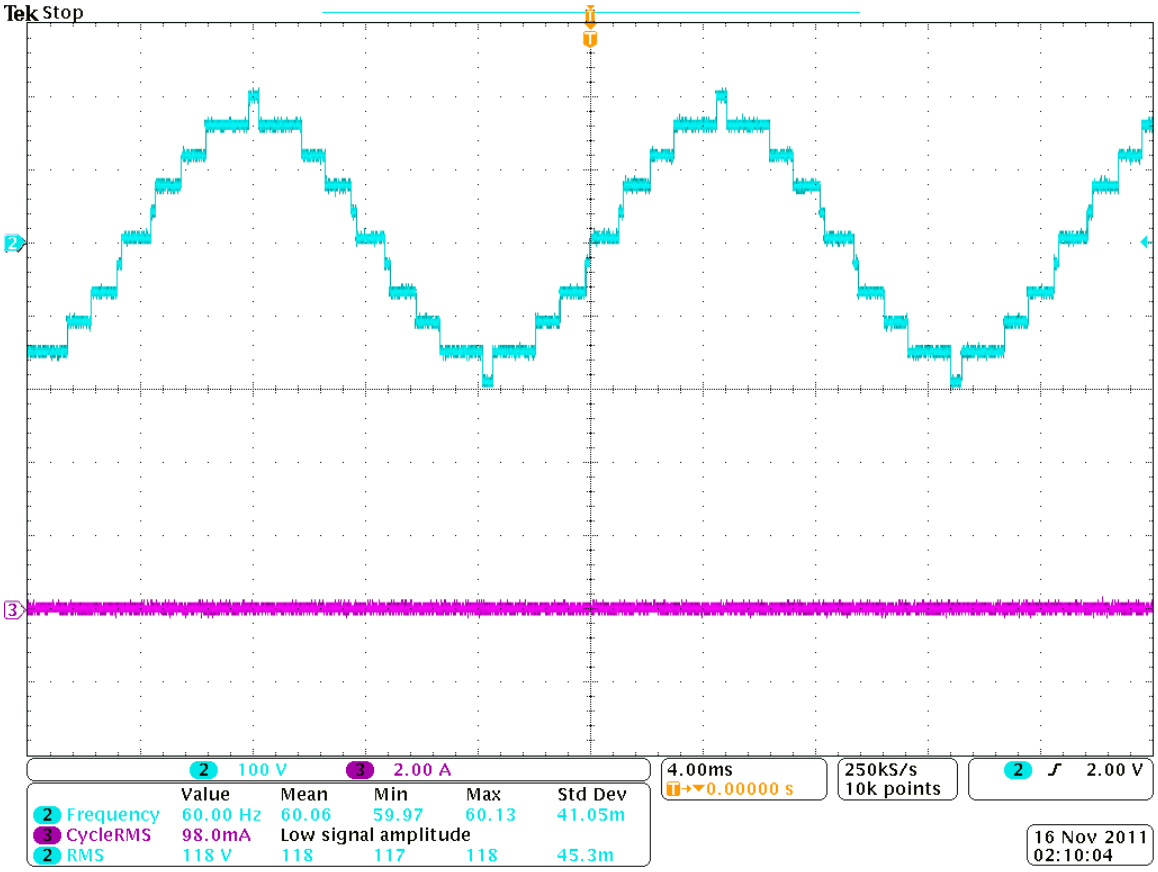


Figure 59 – Output voltage (cyan) and load current (purple) for case 1 in Table 20.

Figure 60 shows the frequency spectrum where it can be noticed that the lower order harmonics were minimized.

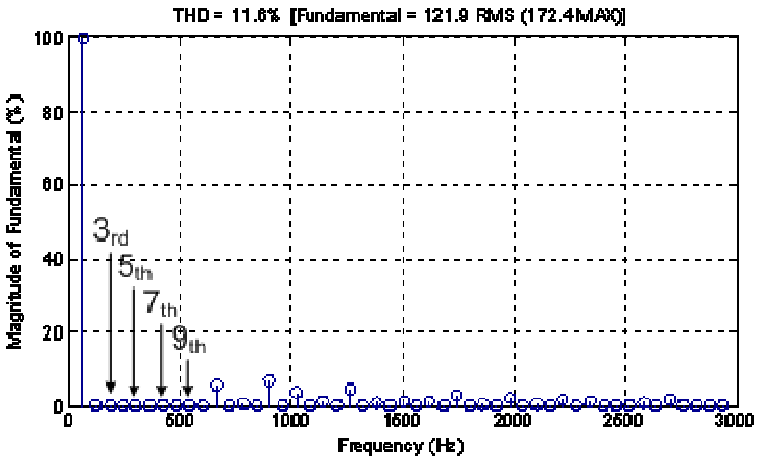
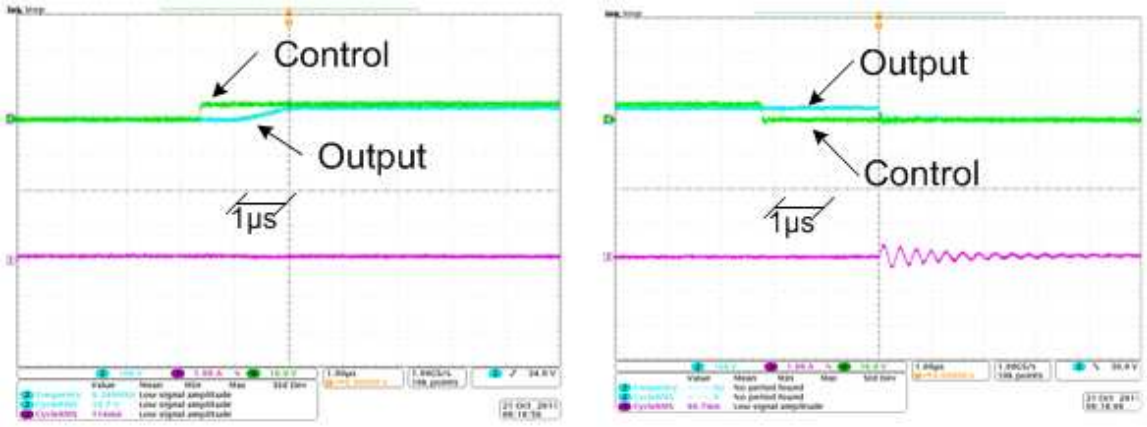


Figure 60 – Output voltage frequency spectrum of Figure 59.

Signal delay propagation was measured as shown in Figure 61 for load case 1. The green line is the signal coming out of the control board and the cyan line is measured at the output before the inductor (staircase waveform). This figure shows that the output waveform will be 1 to 2 μs longer than it was supposed to be. That difference does not affect the results.



(a) (b)

Figure 61 – Signal delay propagation during (a) turn-on and (b) turn-off.

Case 2 is illustrated in Figure 62 with current shown in the bottom part of the graph.

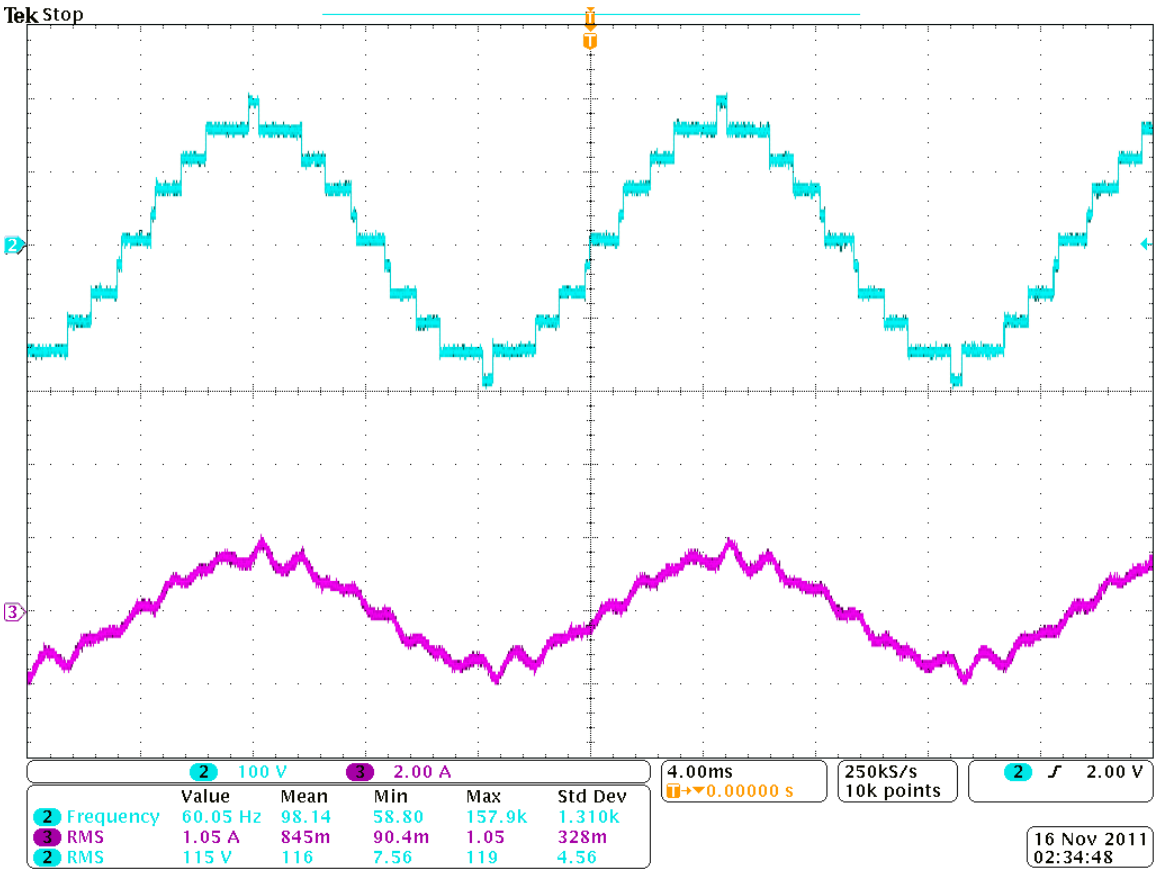


Figure 62 – Output voltage (cyan) and load current (purple) for case 2 in Table 20.

The output voltage spectrum is shown in Figure 63 and delay propagation shown in Figure 64.

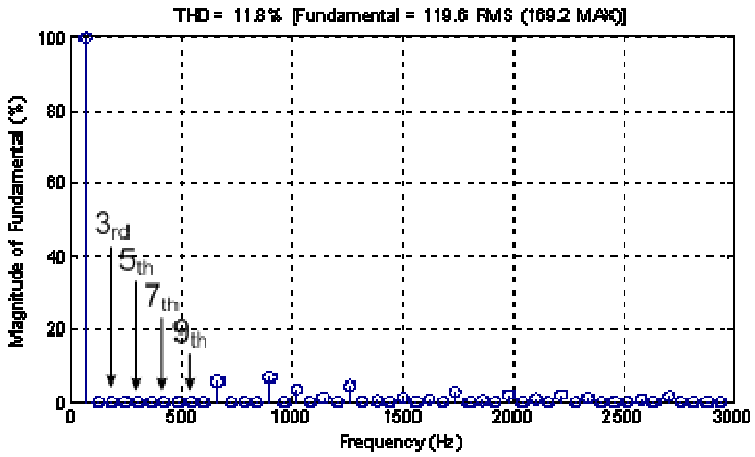
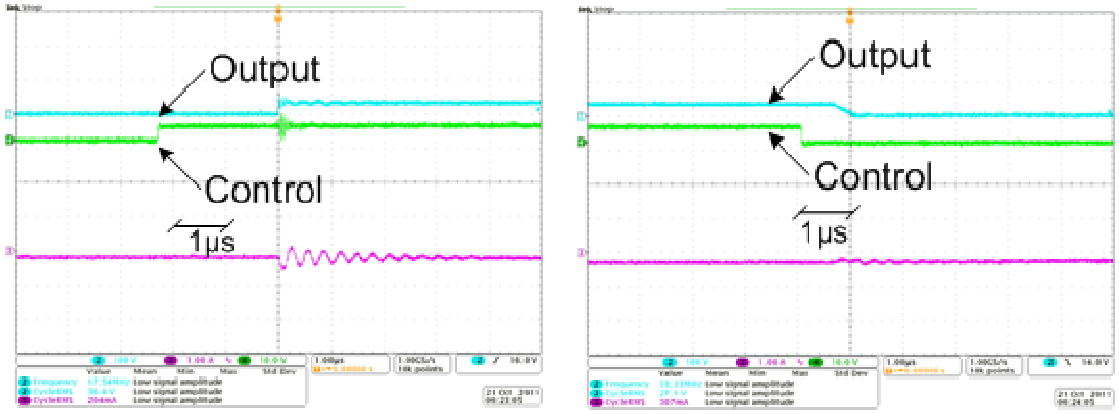


Figure 63 – Output voltage frequency spectrum of Figure 62.



(a) *(b)*

Figure 64 – Signal delay propagation during (a) turn-on and (b) turn-off under RLC load of case 2.

A RL load is illustrated in Figure 65. In this figure it can be noticed the near sinusoidal current. The harmonic content for voltage before the filter has similar harmonic characteristics as shown previously.

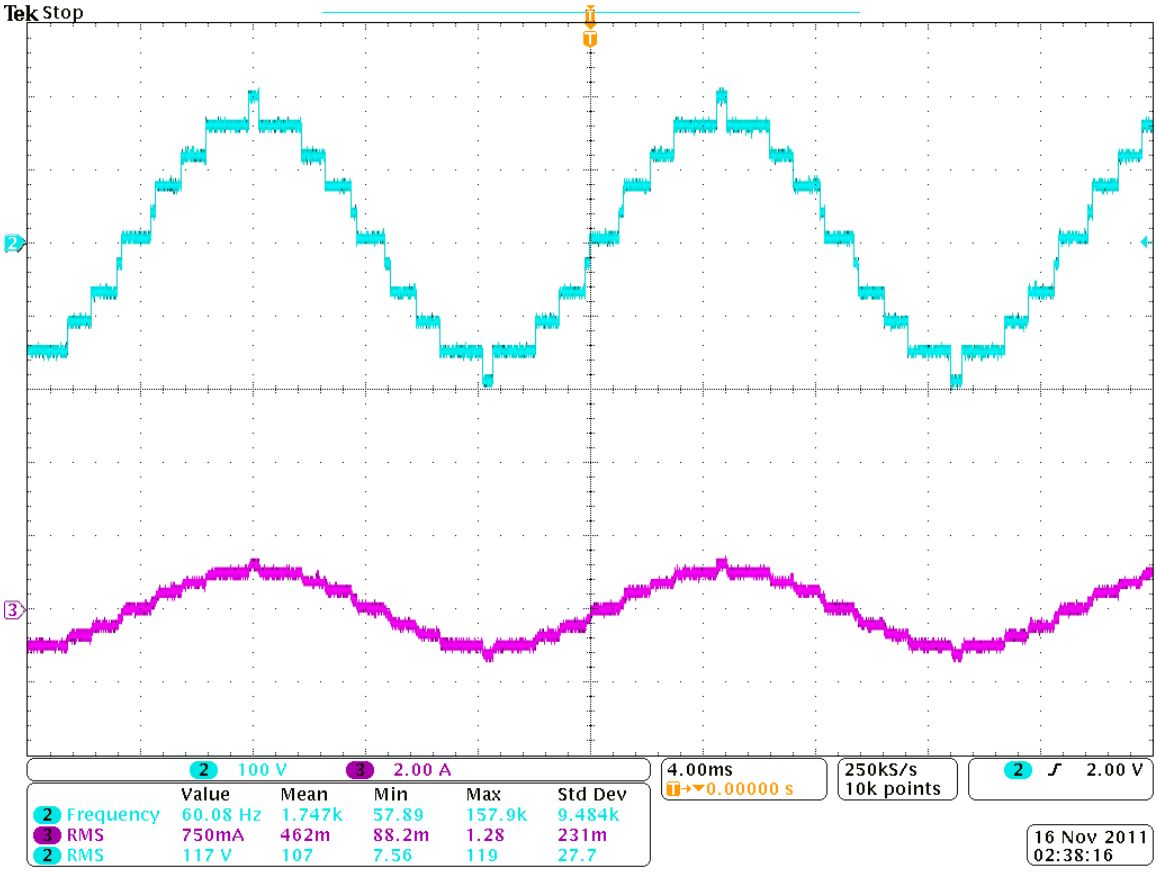
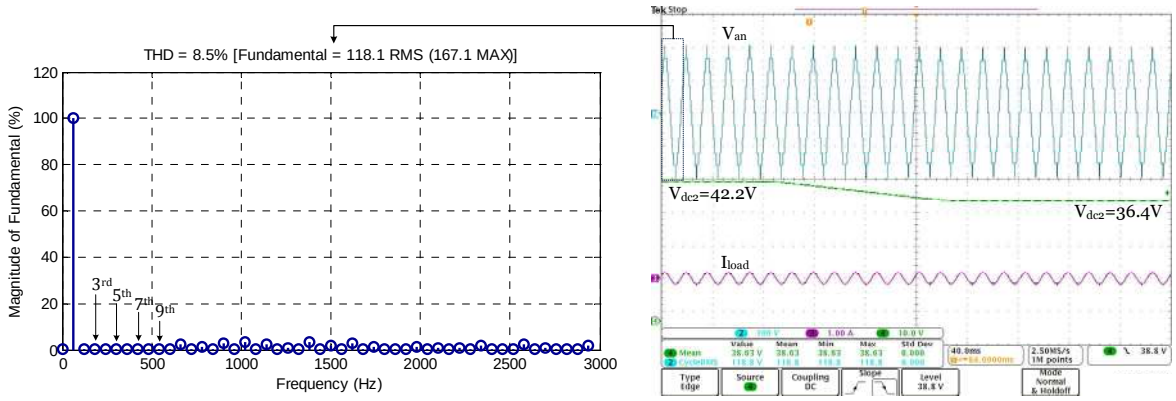


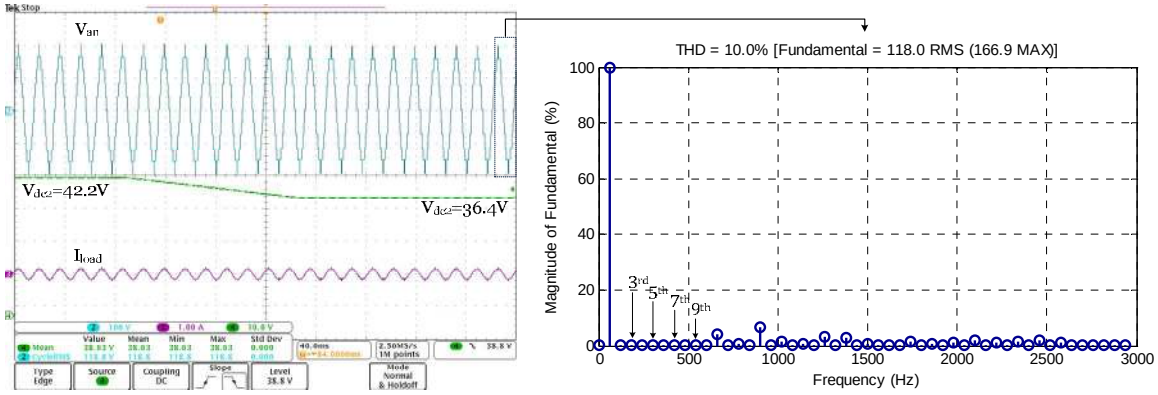
Figure 65 – Output voltage (cyan) and load current (purple) for R=107 Ω and L=5 mH.

Another real-time case is illustrated in Figure 66 with V_{dc2} transition from 42.2 V to 36.4 V. In this figure the THD spectrum of the output voltage is shown before the voltage change in V_{dc2} where the target harmonics were successfully minimized. In Figure 67 the harmonic spectrum is shown after the change in V_{dc2} where the harmonics were also minimized.



(a) *(b)*

Figure 66 – Output voltage harmonic content (a) and real-time ANN response (b) before V_{dc2} variation.



(a) *(b)*

Figure 67 – Output voltage harmonic content (a) and real-time ANN response (b) after V_{dc2} variation.

5.7.2 Seven-level experimental results with solar panels

Real-time ANN based results for a 500 Ω using the same LC parameters (5 mH, 10 µF) is shown in Figure 68.

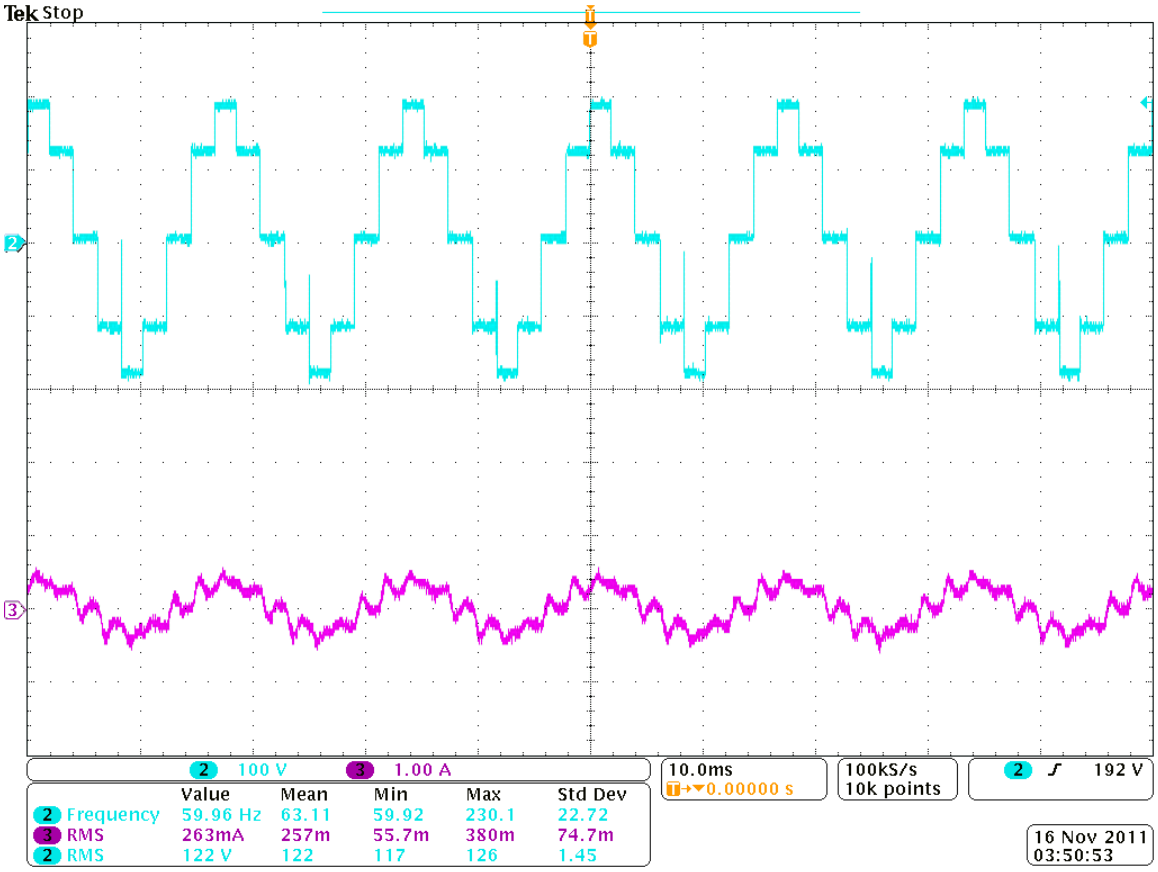


Figure 68 – Output voltage (green) and load current (purple) for 7-Level cascade under load condition (500 Ω;5 mH;10 μF).

As presented in Figure *69* the target low-order harmonics were minimized and the fundamental was kept close to 120 V.

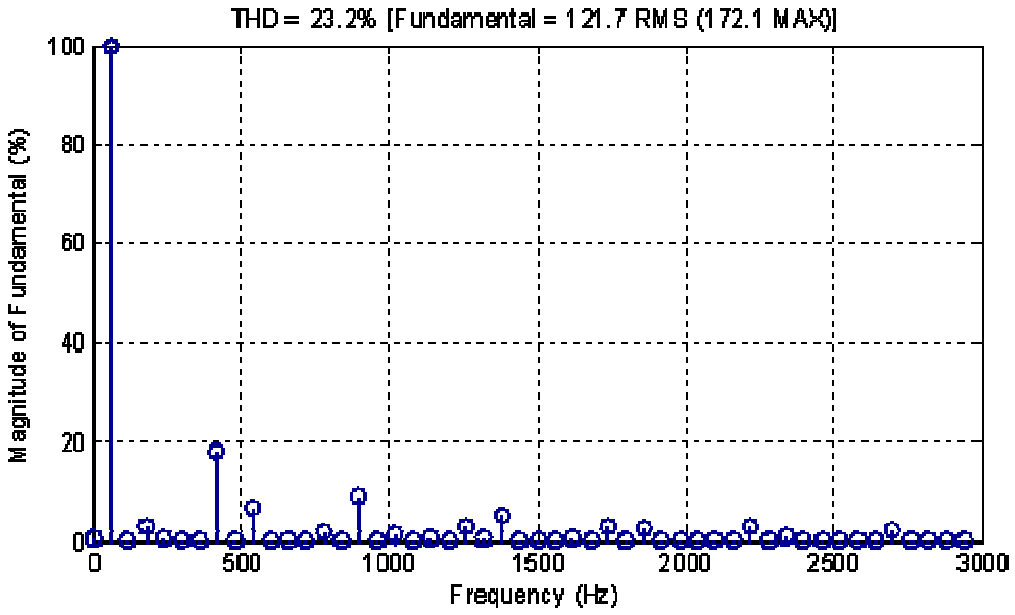


Figure 69 – Output voltage frequency spectrum of Figure 69.

A more demanding load condition is presented in Figure 70 under 333.3 Ω. The output voltage spectrum is shown in Figure 71.

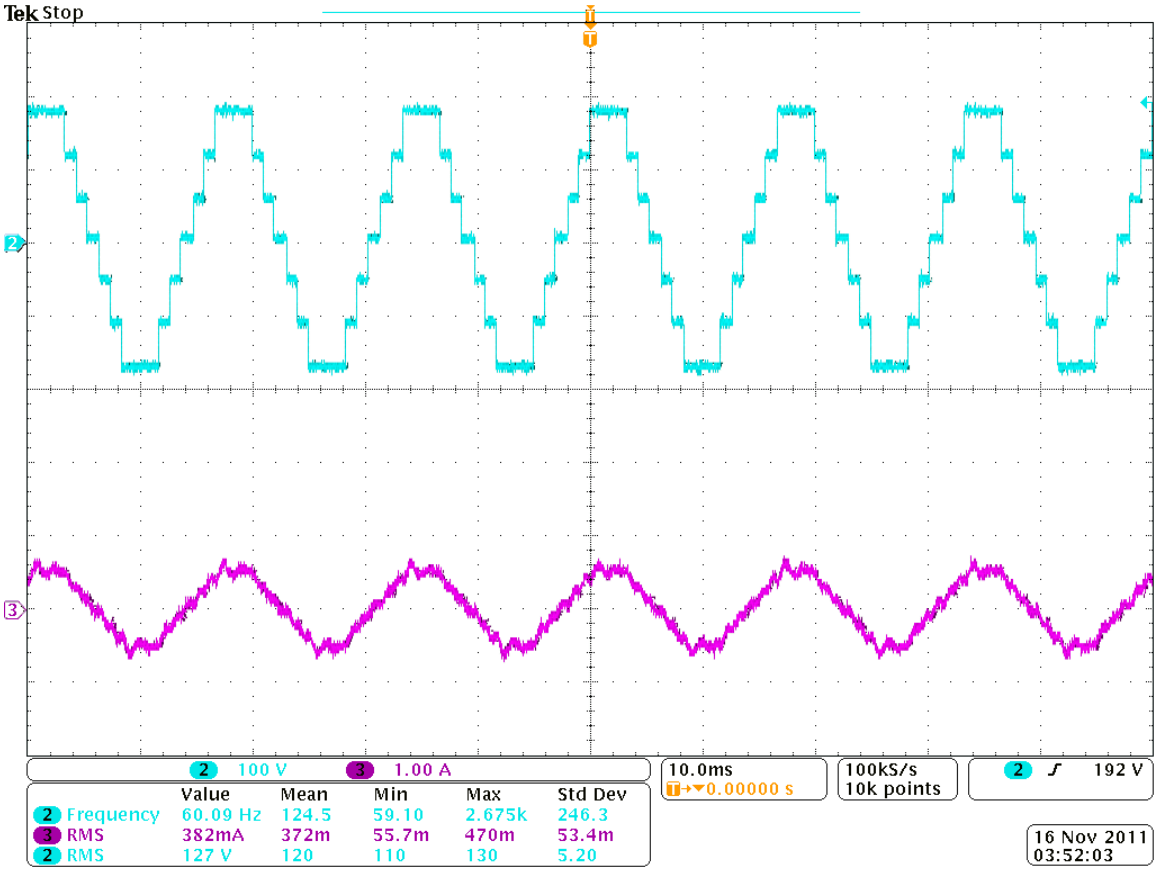


Figure 70 – Output voltage (green) and load current (purple) for 7-Level cascade under load condition (333.3 Ω;5 mH;10 µF).

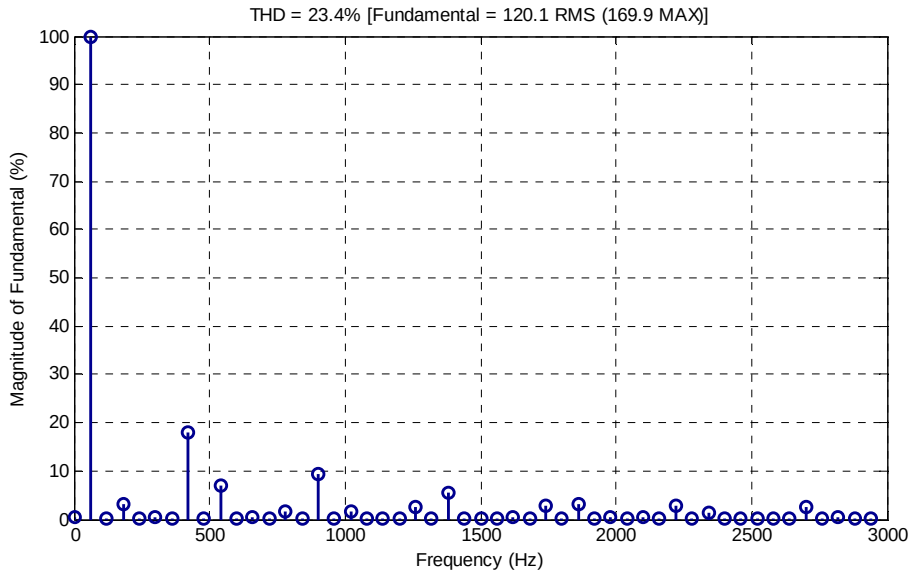


Figure 71 – Output voltage frequency spectrum of Figure 70.

5.8 Chapter summary

This chapter presented experimental results for a real-time ANN-based harmonic minimization system. This approach was able to provide the angles in-cycle (50 Hz or 60 Hz) implemented in hardware for harmonic minimization. The ANN was trained with a mixed data set that has eliminated harmonics and, for those points where a solution does not exist, minimized harmonics. The real time performance was shown to validate the proposed approach.

Chapter 6

Conclusions and future steps towards harmonic control

6.1 Conclusions

A new approach for real time computation of switching angles using artificial neural networks was presented. This approach has not been documented in the literature for the SHE problem as a methodology to obtain the switching angles. The solutions were found off line using genetic algorithms to obtain a data set for use during the training process of the neural network. GA was also used so as to explore the advantages of approximate solutions. The trained neural network was used then for on-line real-time determination of the angles.

The output angles returned by the ANN may not provide a satisfactory result, or harmonic elimination, at some points as it generalizes; however, a fast result can be obtained and more angles can be easily added to provide a better output waveform. Parallel networks can be used to accomplish better performance also.

Experimental results were shown to validate this approach. A real time system was implemented using the neural network previously obtained on both DSpace and DSP platform. The angles are updated at the same frequency of the fundamental output voltage due to the low computation required for the neural network.

The analytic calculation of the angles in real time for harmonic elimination is still being studied and approached by researchers through different paths. This work investigated ANNs as a tool to provide the angles in-cycle (50 Hz or 60 Hz)

that also can have DSP implementation but at the cost of minimization of harmonics instead of elimination. The ANN was trained with a mixed data set that has eliminated harmonics and, for those points where a solution does not exist, minimized harmonics. The real time performance was shown to validate the proposed approach.

The output angles returned by the ANN may not provide a satisfactory result, or harmonic elimination, at some points, as it generalizes; however, a fast result can be obtained and more angles can be easily added to provide a better output waveform. Parallel networks can be used to accomplish better performance also.

6.1.1 ANN improvement

To explore ANN ability to provide angles, an incremental training was done. A smaller dataset (subset) made of permutations with replacement (first column of Table 7) was initially adopted. Using part of this dataset, an ANN was trained, and its performance was evaluated.

The main purpose of this approach was to find a minimum data set and the size for the network. Also, as dataset size increases it was desired to observe if a satisfactory network could be found.

6.1.2 Stochastic search methods

GA has been successfully applied to this application. Current average time to find an off-line solution is 8-10 seconds. This might take up to four hours in a dataset size of 1500 since the GA has to run more than once for the same point to look for diversified solutions. Population size, genetic operator settings and fitness

function are the main parameters subject to change. For this specific problem it was observed that small changes on the crossover coefficient can speed up the search.

6.1.3 DSpace and DSP implementation

A Simulink program was implemented and loaded to the DSP's flash memory using Target Support Package (TSP) for Simulink. TSP allows compilation of a Simulink program into DSP language, which can be loaded and executed in a standalone environment. A TMDSeZ28335 floating point DSP was used for the experiments. The same principle works for the DSpace platform using Simulink to directly upload the program to the controller

6.1.4 Experimental results

Experimental results were conducted for 7-, 9- and 11-level cascade inverter under different load conditions showing the output voltage waveform, current waveform and the respective THD.

6.1.6 Main contributions summary

The impact and main contributions of this work can be summarized as follows:

- Real-time use of Artificial Neural Networks to generate the switching angles in a multilevel inverter powered by varying DC input sources. The angles can be chosen such that the fundamental can be kept constant and the low order harmonics minimized or eliminated in real-time in a cycle-by-cycle basis or faster if needed.

- Use of Genetic Algorithms to obtain the angles in cases where analytical approaches do not return a solution. GA solves the system for the angles and obtains the data set for the ANN training. This method provides a set of acceptable solutions in the space where solutions do not exist by analytical methods.
- The approach proposed here can now be applied whenever real-time harmonic control is needed as one candidate for the application in study.
- Generalized methodology: The number of switching angles, number of levels and modulation index can be varied according to the application and a new ANN for real-time operation can be trained.
- A low cost methodology to estimate the voltage level of each individual cell by using the output voltage and current. Although a direct measurement is not made, the voltage estimation avoids use of voltage sensors on each individual H-bridge.

6.1.5 Future work

Future work points in the direction of implementation and performance evaluation over a greater number of angles. This would allow for harmonic control while keeping the switching frequency minimum and complying with THD standards. The literature review also pointed the possibility of determining what the minimum number of angles needed is in order to comply with certain THD level.

Additionally an efficient way to combine ANN and maximum power point tacking of solar panels with enough angles to comply with grid codes is an interesting topic for future research.

List of References

[1] J. Rodriguez, J. Lai, F. Z. Peng, "Multilevel inverters: a survey of topologies, control and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[2] A. Pandey, B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, D. P. Kothari, "A review of multilevel power converters," *Institute of Engineers Journal (India)* , pp. 220-231, vol. 86, March 2006.

[3] S. Kouro,M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, J. I. Leon, "Recent advances and industrial applications of multilevel converters, " *IEEE Transactions on Industrial Electronics,* vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[4] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine,* vol. 2, no. 2, pp. 28-39, June 2008.

[5] R. Rangarajan, F. E. Villaseca, "A switching scheme for multilevel converters with non-equal DC sources, " *39th North American Power Symposium,* pp. 308-313, Sept. 2007.

[6] B. Ozpineci, L. M. Tolbert, J. N. Chiasson, "Harmonic optimization of multilevel converters using genetic algorithms," *IEEE Power Electronics Letters*, vol. 3, no. 3, pp. 92-95, Sept. 2005.

[7] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, Z. Du, "A unified approach to solving the harmonic elimination equations in multilevel converters," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 478-490, Mar. 2004.

[8] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, Z. Du, "Elimination of harmonics in a multilevel converter using the theory of symmetric polynomials and resultants," *IEEE Transactions on Control Systems Technology*, vol. 13, no. 2, pp. 216-223, March 2005.

[9] Z. Du, L. M. Tolbert, J. N. Chiasson, H. Li, "Low switching frequency active harmonic elimination in multilevel converters with unequal DC voltages," *Annual Meeting of the IEEE Industry Applications Society*, pp. 92-98, Oct. 2005.

[10] Z. Du, L. M. Tolbert, J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Transactions on Power Electronics,* vol. 21, no. 2, pp. 459-469, March 2006.

[11] D. Ahmadi, Jin Wang, "Selective harmonic elimination for multilevel inverters with unbalanced DC inputs," *IEEE Vehicle Power and Propulsion Conference,* pp. 773-778, Sept. 2009.

[12] M. Dahidah, V. G. Agelidis, "Selective harmonic elimination multilevel converter control with variant DC sources," *IEEE Conference on Industrial Electronics and Applications,* pp. 3351-3356, May 2009.

[13] M. G. H. Aghdam, S. H. Fathi, G. B. Gharehpetian, "Elimination of harmonics in a multi-level inverter with unequal DC sources using the homotopy algorithm," *IEEE International Symposium on Industrial Electronics*, pp. 578-583, June 2007.

[14] T. Tang, J. Han, X. Tan, "Selective harmonic elimination for a cascade multilevel inverter," *IEEE International Symposium on Industrial Electronics*, pp. 977-981, July 2006.

[15] J. R. Wells, B. M. Nee, P. L. Chapman, P. T. Krein, "Selective harmonic control: a general problem formulation and selected solutions," *IEEE Transactions on Power Electronics,* vol. 20, no. 6, pp. 1337-1345, Nov. 2005.

[16] M. S. A. Dahidah, V. G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula," *IEEE Transactions on Power Electronics,* vol. 23, no. 4, pp. 1620-1630, July 2008.

[17] D. W. Kang, H. C. Kim, T. J. Kim, D. S. Hyun, "A simple method for acquiring the conducting angle in a multilevel cascaded inverter using step pulse waves," *IEE Proceedings on Electric Power Applications*, vol. 152, pp. 103-111, Jan. 2005.

[18] Y. Liu, H. Hong, A. Q. Huang, "Real-time calculation of switching angles minimizing THD for multilevel inverters with step modulation," *IEEE Transaction on Industrial Electronics*, vol. 56, no. 2, pp. 285-293, Feb. 2009.

[19] F. J. T. Filho, L. M. Tolbert, Y. Cao, B. Ozpineci, "Real time selective harmonic minimization for multilevel inverters connected to solar panels using artificial neural network angle generation," *IEEE Energy Conversion Congress and Exposition,* pp. 594-598, Sept. 2010.

[20] U. Boke, "A simple model of photovoltaic module electric characteristics," *European Conference on Power Electronics and Applications,* pp.1-8, Sept. 2007.

[21] O. Gil-Arias, E. I. Ortiz-Rivera, "A general purpose tool for simulating the behavior of PV solar cells, modules and arrays," *11th Workshop on Control and Modeling for Power Electronics*, pp. 1-5, Aug. 2008.

[22] R. Ramaprabha, B. L. Mathur, "MATLAB based modelling to study the influence of shading on series connected SPVA," *2nd International Conference on Emerging Trends in Engineering and Technology*, pp. 30-34, Dec. 2009.

[23] M. G. Villalva, J. R. Gazoli, E. R. Filho, "Comprehensive approach to modeling and simulation of photovoltaic arrays," *IEEE Transactions on Power Electronics,* vol. 24, no. 5, pp. 1198-1208, May 2009.

[24] J. J. Hopfield, "Artificial neural networks," *IEEE Circuits and Devices Magazine,* vol. 4, no. 5, pp. 3-10, Sep. 1988.

[25] R. Aggarwal, Y. Song, "Artificial neural networks in power systems II: types of artificial neural networks," *Power Engineering Journal*, vol. 12, no. 1, pp. 41-47, Feb. 1998.

[26] R. Aggarwal, Y. Song, "Artificial neural networks in power systems I: general introduction to neural computing," *Power Engineering Journal*, vol. 11, no. 3, pp. 129-134, Jun. 1997.

[27] M. J. Willis, C. Di Massimo, G. A. Montague, M. T. Tham, A. J. Morris, "Artificial neural networks in process engineering," *IEE Procedings in Control Theory and Applications,* vol. 138, no. 3, pp. 256-266, May 1991.

[28] A. K. Jain, Jianchang Mao, K. M. Mohiuddin, "Artificial neural networks: a tutorial," *Computer* , vol. 29, no. 3, pp. 31-44, Mar 1996.

[29] B. K. Bose, "Neural network applications in power electronics and motor drives—An introduction and perspective," *IEEE Transactions on Industrial Electronics,* vol.54, no.1, pp.14-33, Feb. 2007.

[30] S. Haykin, Neural networks: A comprehensive foundation. Prentice Hall, 2nd. Ed., 1998.

[31] M. H. Hassoun, Fundamentals of artificial neural networks. MA: MIT Press, 1995.

[32] S. Jung, S. Kim, "Hardware implementation of a real-time neural network controller with a DSP and an FPGA for nonlinear systems," *IEEE Transactions on Industrial Electronics,* vol.54, no.1, pp.265-271, Feb. 2007.

[33] M. Bouzid, G. Champenois, N. M. Bellaaj, L. Signac, K. Jelassi, "An effective neural approach for the automatic location of stator interturn faults in induction motor," *IEEE Transactions on Industrial Electronics,* vol.55, no.12, pp.4277-4289, Dec. 2008.

[34] H. C. Lin, "Intelligent neural network-based fast power system harmonic detection," *IEEE Transactions on Industrial Electronics,* vol.54, no.1, pp.43-52, Feb. 2007.

[35] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*. New York: Wiley, 1995.

[36] D. E. Goldberg, Genetic Algorithms in Search, Optimization, and Machine Learning. MA: Addison-Wesley, 1989.

[37] K.F. Man, K.S. Tang, S. Kwong, "Genetic algorithms: concepts and applications [in engineering design]," *IEEE Transactions on Industrial Electronics,* vol.43, no.5, pp.519-534, Oct 1996.

[38] C. R. Houck, J. A. Joines and M. G. Kay, "A genetic algorithm for function optimization: A Matlab implementation," Technical Report NCSU-IE-TR-95-09, North Carolina State University, Raleigh, NC (1995).

[39] M. Srinivas, L. M. Patnaik, "Genetic algorithms: a survey, " *IEEE Computer Society Press.*, vol. 27, no. 6, pp. 17-26, Jun 1994.

[40] C. M. Fonseca, P. J. Fleming, "Genetic algorithms for multiobjective optimization: Formulation, discussion and generalization," *Proc. of the fifth conference on Genetic Algorithms*, July 1993.

[41] A. Wright, "Genetic algorithms for real parameter optimization," *Foundations of Genetic Algorithms*, Morgan Kaufmann, pp. 205–218.

[42] R. L. Haupt, S. E. Haupt, *Practical Genetic Algorithms*. New York: Wiley, 1998.

[43] J. R. Wells, P. L. Chapman, P. T. Krein, "Generalization of selective harmonic control/elimination," *IEEE Power Electronics Specialists Conference*, pp. 1358-1363, June 2005.

[44] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. Perez, J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters, " *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[45] B. Wu, *High-Power Converters and AC Drives*. Piscataway, NJ: IEEE Press, 2006.

[46] RT-LAB, Opal-RT Technologies (2001): http://www.opal-rt.com.

[47] V. G. Agelidis, A. Balouktsis, "On applying a minimization technique to the harmonic elimination PWM control: the bipolar waveform, " *IEEE Power Electronics Letters,* vol. 2, no. 2, pp. 41- 44, June 2004.

[48] Jin Wang, D. Ahmadi, "A Precise and practical harmonic elimination method for multilevel inverters," *IEEE Transactions on Industry Applications,* vol. 46, no. 2, pp. 857-865, March-april 2010.

[49] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930-2945, Dec. 2007.

[50] Lie Xu, V. G. Agelidis, "VSC transmission system using flying capacitor multilevel converters and hybrid PWM control," *IEEE Transactions on Power Delivery,* vol. 22, no. 1, pp. 693-702, Jan. 2007.

[51] Wanmin Fei; Xinbo Ruan; Bin Wu, "A Generalized Formulation of Quarter-Wave Symmetry SHE-PWM Problems for Multilevel Inverters," *IEEE Transactions on Power Electronics,* vol. 24, no. 7, pp. 1758-1766, July 2009.

[52] E. I. Ortiz-Rivera, F. Z. Peng, "Analytical model for a photovoltaic module using the electrical characteristics provided by the manufacturer data sheet," IEEE 36th Power Electronics Specialists Conference, pp. 2087-2091, June 2005.

[53] E. B. Baum and D. Haussler, "What size net gives valid generalization?," *Neural Computation*, vol. 1, no. 1, pp. 151–160, Cambridge, MA: MIT Press, Mar. 1990.

[54] M. T. Hagh, H. Taghizadeh, K. Razi, "Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization," *IEEE Transactions on Power Electronics,* vol. 24, no. 10, pp. 2259-2267, Oct. 2009.

[55] V. N. Vapnik and A. Y. Chervonenkis, "On the uniform convergence of relative frequencies of events to their probabilities," *Theory of Probability and Its Application,* vol. 16, no. 2, pp. 264–280 Philadelphia, PA: SIAM, 1971.

[56] S. Mohagheghi, R. G. Harley, T. G. Habetler, D. Divan, "Condition monitoring of power electronic circuits using artificial neural networks," *IEEE Transactions on Power Electronics,* vol. 24, no. 10, pp. 2363-2367, Oct. 2009.

[57] E. I. Ortiz-Rivera, F. Z. Peng, "Analytical model for a photovoltaic module using the electrical characteristics provided by the manufacturer data sheet," *IEEE 36th Power Electronics Specialists Conference*, pp. 2087-2091, June 2005.

[58] http://www.solarelectricpower.org

[59] http://solarbuzz.com/facts-and-figures/retail-price-environment/module-prices

[60] http://www1.eere.energy.gov

[61] Reneable Energy Policy Network for the 21st Century (REN21), "Renewable Global Status Report 2009 Update", available at www.ren21.net.

[62] S. Khomfoi, L. M. Tolbert, "Fault diagnosis and reconfiguration for multilevel inverter drive using AI based techniques," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2954-2968, Dec. 2007.

[63] C. Zang, Z. Pei, J. He, G. Ting, J. Zhu, W. Sun, "Comparison and analysis on common modulation strategies for the cascaded multilevel STATCOM," *IEEE International Conferences on Power Electronics and Drive Systems*, pp. 1439-1442, 2009.

[64] W. Song, A. Q. Huang, "Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM," I*EEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2700-2708, 2010.

[65] B. Ozpineci, L. M. Tolbert, Zhong Du, "Multiple input converters for fuel cells," in *Proc. 39th IEEE Industry Applications Conference*, vol. 2, pp. 791- 797, Oct. 2004.

[66] Feel-Soon Kang, Sung-Jun Park, Su Eog Cho, Cheul-U Kim, T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems," *IEEE Transactions on Energy Conversion*, vol. 20, no. 4, pp. 906- 915, Dec. 2005.

[67] R. Sternberger, D. Jovcic, "Analytical modeling of a square-wave-controlled cascade multilevel STATCOM," *IEEE Transactions on Power Delivery*, vol. 24, no. 4, pp. 2261-2269, Oct. 2009.

[68] H. Radermacher, B. D. Schmidt, R. W. Doncker, "Determination and comparison of losses of single phase multi-level inverters with symmetric supply," in *Proc.*

35th IEEE Power Electronics Specialists Conference, vol. 6, pp. 4428-4433, Nov. 2004.

[69] R. Gupta, A. Ghosh, A. Joshi, "Switching characterization of cascaded multilevel-inverter-controlled systems," *IEEE Transaction on Industrial Electronics*, vol. 55, no. 3, pp. 1047-1058, March 2008.

[70] Tae-Jin Kim, Dae-wook Kang, Yo-Han Lee, Dong-Seok Hyun, "The analysis of conduction and switching losses in multilevel inverter system," in *Proc. 32nd IEEE Power Electronics Specialist Conference*, vol. 3, pp. 1363-1368, Jun. 2001.

[71] http://sempragenerationcom/energy-solutions/solar-copper-mountain-solar.html.

[72] http://www.pv-ech.org/news/new_mexicos_30mw_cimarron_solar_plant_begins_commercial_operation.

Vita

Faete Filho (S'08) received his B.S. and M.S. degrees in electrical engineering from the Federal University of Mato Grosso do Sul, Brazil, in 2004 and 2006 respectively. He is currently a PhD Student at the University of Tennessee, Knoxville.

He worked as Associate researcher at the Batlab Research Laboratory, Brazil in 2007. He was awarded outstanding educational impact and first place in the 2005 and 2007 IEEE Future Energy Challenge competition, respectively. He worked as a student leader designing and building a house for the University of Tennessee team on the 2011 Solar Decathlon competition. He is an active representative in the student graduate senate and an occasional reviewer for IEEE transactions and conferences. His current areas of interest include multilevel inverters, power converters for distributed energy resources, and artificial intelligence techniques and applications to power electronics.