Real-Time Temperature Estimation for Power MOSFETs Considering Thermal Aging Effects

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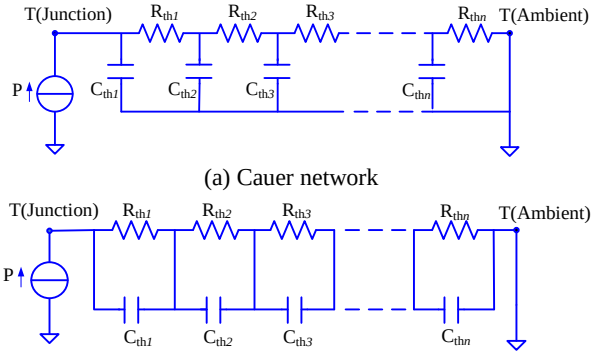
***Abstract*— This paper presents a novel real-time power device temperature estimation method which monitors the power MOSFET's junction temperature shift arising from thermal aging effects and incorporates the updated electrothermal models of power modules into digital controllers. Currently, the real-time estimator is emerging as an important tool for active control of device junction temperature as well as on-line health monitoring for power electronic systems but its thermal model fails to address the device's ongoing degradation. Because of a mismatch of coefficients of thermal expansion between layers of power devices, repetitive thermal cycling will cause cracks, voids and even delamination within the device components, especially in the solder and thermal grease layers. Consequently, the thermal resistance of power devices will increase, making it possible to use thermal resistance (and junction temperature) as key indicators for condition monitoring and control purposes. In this paper, the predicted device temperature via threshold voltage measurements is compared with the real-time estimated ones and the difference is attributed to the aging of the device. The thermal models in digital controllers are frequently updated to correct the shift caused by thermal aging effects. Experimental results on three power MOSFETs confirm that the proposed methodologies are effective to incorporate the thermal aging effects in the power device temperature estimator with good accuracy. The developed adaptive technologies can be applied to other power devices such as IGBTs and SiC MOSFETs, and have significant economic implications.**

***Index Terms*—Circuit topology, converters, monitoring, MOSFET switches, prognostics and health management, reliability testing, thermal management.**

I. INTRODUCTION

IN power electronic converters, the junction temperature of semiconductor devices is of critical importance for thermal management. Owing to the different coefficients of thermal expansion (CTEs) of materials used to form the layers of power devices, repetitive thermal cycling will cause cracks, voids and even delamination within the device components, especially in the solder and thermal grease layers. This in turn gives rise to their thermal resistance and junction temperature which may be detected and employed as key indicators for condition monitoring and control purposes**.**

The junction temperature of power devices is traditionally calculated using thermal resistance-capacitance (RC) networks that represent an equivalent heat transfer process from the source (power chips) to the heatsink, whose temperature is monitored by a temperature sensor [1]. In the literature, a trend is to move towards real-time power device junction temperature estimation [2]-[5] based on certain thermal models. Typical models of a single-chip power module are in the form of either Cauer network [6][7] or Foster network [8][9], as shown in Fig. 1. In essence, the Cauer model can represent the internal physical structure of the device layers but is computationally complex to implement. In contrast, the Foster-network is easier to be complemented but cannot provide temperature changes in the internal layers of the device. In this work, the focus is placed on the junction temperature (in relation to the total thermal impedance) rather than the thermal distribution in the internal layers. Since the change in the total thermal impedance arising from aging effects can be detected from the terminal characteristics, the two methods can offer identical solutions in this regard.



(a) Cauer network

(b) Foster network

Fig. 1. Two typical thermal RC models.

In addition, the electrical models are also found in use to compute the power dissipation of the device for a given operational condition. When combined with a thermal model, an electrothermal model of power devices can be attained and implemented in a digital signal processor (DSP) for condition monitoring and thermal management. Because of the continuous improvement in these models and the parameter identification, the power device junction temperature can now be determined with reasonable accuracy. As a result, electrothermal models have become an important tool for health monitoring and active control of power electronic converters [10]-[16]. However, these models all adopt fixed

thermal resistances throughout the device's lifespan so that the degradation of the materials in the thermal path during the device aging process is overlooked [17]-[22]. Without updating thermal models, it became increasingly difficult to predict the thermal performance of the device as the operating time goes on. This is especially true when safety margins are added in the datasheet provided by the device manufacturers so that temperature estimation can be a far cry from reality. In this paper, a new technique is developed to estimate the junction temperature of power devices by continuously correcting the effect of thermal ageing. This has not been reported previously and is a novelty of this work.

Furthermore, the considerable increase in the thermal resistance caused by aging in turn gives rise to the likelihood of device failures and the need for unnecessary overrating of the device. Clearly, accurate information of the device's temperature over its lifespan is highly desired to enable a regulation of the device's maximum temperature and thermal cycles [23]-[25]. Fundamentally, the effective temperature control in both steady-state and transient conditions can help reduce thermo-mechanical stress and failure rates of the device.

It becomes clear that real-time temperature estimation with online correction is critically important for understanding the through-life failure models and for improving reliability and maintainability of power electronic devices, especially for safety-critical applications. The creation of a PN diode on the FET chip to be used as a temperature sensor is an alternative but this would reduce the active chip area and thus power capacity of the device. Moreover, this needs additional measuring circuits and also a consensus from all original design manufacturers (ODMs).

This work considers the aging effect of MOSFET power devices in their junction temperature estimation by a data-driven adaptive method. The information of thermal resistance is used to correlate with the process of thermal path degradation and to calibrate the power device thermal models. The estimated device temperatures from the thermal model are also compared with the experimental ones derived from the measured MOSFET threshold voltage. If a sufficient discrepancy (i.e. degradation) between the two temperatures is detected, the thermal model needs to be updated to accommodate this change.

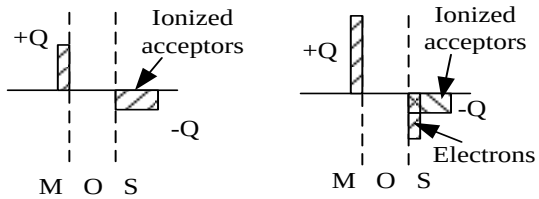
II. Measurements of TSEPs and TTICs

In general, MOSFET chips are encapsulated in a plastic case by the moulding compound. Direct measurement of the junction temperature requires removal of the plastic case and compound in order to gain an access to the chip surface, which is often impractical. Therefore, measuring TSEPs in the chip to estimate the junction temperature is an attractive alternative as long as their correlation can be established correctly.

A. Choice of the TSEP

In the literature, the drain-body diode forward voltage, on-state resistance and threshold voltage are three well known TSEPs of power MOSFETs [26]-[29]. The first two indicate the temperature in the intrinsic body diode area and in the active drain region, respectively. Thus they are less accurate in detecting the junction temperature. In contrast, the third parameter has a linear relationship with the device temperature (-2 to -6 mV/ºC) at small drain currents (<10mA), resulting from temperature variations of the Fermi level in the channel region of the MOSFET.

For an *n*-channel (*p*-bulk) power MOSFET, there are no electric charges inside the ideal metal-oxide-semiconductor (MOS) structure under equilibrium conditions. When a bias voltage (V_G) is applied, charges appear in the metal (*M*) and semiconductor (*S*) near the metal-oxide and oxide-semiconductor interfaces.



(a) Depletion $V_{th} > V_G > 0$. (b) Inversion $V_G > V_{th} > 0$.

Fig. 2. Charging diagrams of the *n*-channel MOSFET [30].

The application of positive bias voltage $V_G > 0$ places positive charges on the MOS metal or gate, which in turn repels holes from the oxide-semiconductor interface and exposes the negatively charged acceptor sites, which is known as depletion (Fig. 2a). As V_G increases to balance out the charges, electrons are drawn towards the oxide-semiconductor interface. Finally, the electron concentration in this surface region rises to the same level of the hole concentration in the *p* bulk region (i.e. $V_G = V_{th}$), the surface is no longer depleted. This point is the onset of inversion and the corresponding gate bias is termed the threshold voltage (V_{th}). Further increases in the positive bias ($V_G > V_{th}$) will change this surface region (channel) from a *p*-type to an *n*-type (called inversion), as shown in Fig. 2(b).

The threshold voltage of a power MOSFET is affected by the doping density of the body region, thickness of the gate oxides, and more importantly, junction temperature (*T*). As *T* increases, electrons become more active: to raise the intrinsic carrier concentration, and thus to reduce the threshold voltage. The relationship of V_{th} and *T* is given by [31]:

$$\frac{dV_{th}}{dT} = \frac{d\psi_B}{dT}\left(2 + \frac{1}{C_{OX}}\sqrt{\frac{\varepsilon_{Si} q N_A}{\psi_B}}\right) \quad (1)$$

where

$$\frac{d\psi_B}{dT} \approx \frac{1}{T}\left[\frac{E_g(0)}{2q} - |\psi_B|\right] \quad (2)$$

ψ_B is the difference in potentials between the Fermi level and the mid-gap, ε_{Si} is the dielectric constant of silicon, N_A is the doping density, $E_g(0)$ is the band-gap energy at $T = 0$K, and C_{OX} is the gate oxide capacitance per unit area.

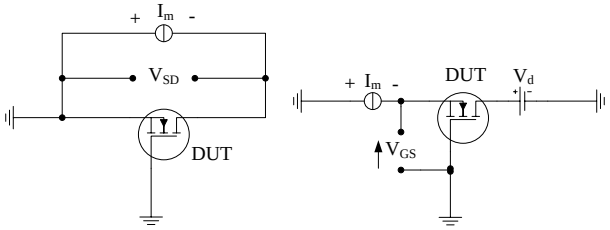
The threshold voltage is found to be able to provide an accurate junction temperature and a high signal-to-noise ratio [29], and is thus chosen as the TSEP in this work.

B. Calibration curves

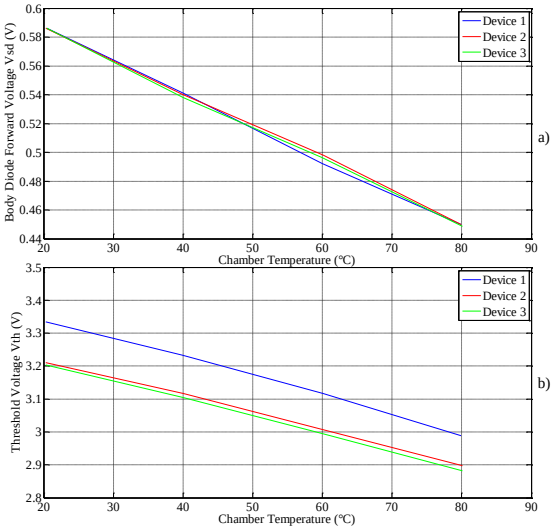
In this paper, three identical power MOSFETs (IRFI640GPbF) and a Texas Instruments floating-point DSP (TMS320C6701) are used. The MOSFETs have a breakdown voltage of 200V, a continuous drain current of 9.8A (at 20°C

case temperature) and an on-state resistance of 0.18Ω [32]. The MOSFET devices are tested in a standard temperature-controlled environmental chamber (Binder MKF720).

The body diode forward voltage $V_{SD}(T_j)$ and gate threshold voltage $V_{th}(T_j)$ are calibrated at four set temperatures of 20°C, 40°C, 60°C and 80°C. As shown in Fig. 3(a), $V_{SD}(T_j)$ is firstly calibrated by injecting a 10mA current followed by $V_{th}(T_j)$ at a 5mA drain current and a 15V drain-source voltage. On the one hand, the current needs to be large enough to ensure an effective conduction of the switching devices. On the other hand, the current should be low enough to avoid excessive self-heating which affects the calibration precision.



(a) Measurement circuitry for V_{SD} and V_{th}



(b) Calibration curves for V_{SD} and V_{th}

Fig. 3. Calibration testing circuit and test results.

Calibration results in Fig. 3(b) exhibit an approximately linear relationship between the diode forward voltage drop and ambient temperature with a slope of -2.2mV/°C. Similarly, the threshold voltage is linear with the ambient temperature with a slope of -5.8mV/°C. It is obvious that V_{th} has better temperature sensitivity than V_{SD} if used as a TSEP.

Test results from the MOSFETs can also give their junction temperature by

$$T_j = \frac{(3.459 - V_{th})}{0.0058} \tag{3}$$

C. Transient thermal impedance curves

In order to obtain a TTIC, the device is heated by a constant power to reach its steady state, and is then switched off to measure the cooling response of the junction temperature through the TSEP (i.e. V_{th} in this case).

With measured junction temperatures, the thermal impedance $Z_{th(c)}(t)$ can be calculated by [33]:

$$Z_{th(c)}(t) = \frac{T_{js} - T_{jc}(t)}{P} \tag{4}$$

where $T_{jc}(t)$ is the instantaneous junction temperature of the device at the time t after removing the constant power P, T_{js} is the junction temperature of the device at thermal equilibrium.

Fig. 4 illustrates the simplified circuit for V_{th} measurement, which utilizes the existing gate driver and DSP/microcontroller capabilities. When the switch S_1 is closed, the MOSFET is in the heating mode. When S_1 is open, the MOSFET is isolated from the DC link and is in the cooling mode for measurements.

It is crucial to choose a right value for the gate resistor R_G: the MOSFET should be driven into the active operating region in the heating mode, and there is only a small drain current I_D flowing through the MOSFET in the cooling mode. Through trial and error, a 2.2kΩ gate resistor is selected in this study. During the heating mode, $V_{DS(on)}$=7.6V with a drain current of 4.3A. This results in a power input of 32.68W (note: rated power 40W). In the cooling mode, $I_D \approx$5mA with V_{GG}=15V applied (nearly the same condition as the calibration measurement).

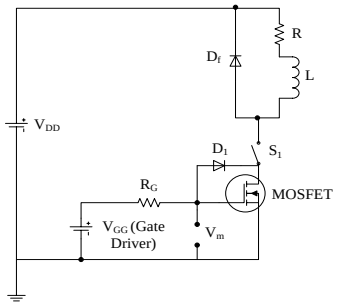


Fig. 4. Simplified circuit for threshold voltage measurement.

After a steady state is reached, S_1 is switched off so that the cooling responses of V_{th} as well as the heatsink temperature T_{ref} can be measured and recorded by the DSP at a sampling interval of 15μs. During the cooling response tests, the heatsink temperature is almost constant. After correcting the non-thermal switching transients for $T_{jc(t)}$ and T_{ref} [29], the TTIC is attained, as is plotted in Fig. 5. It can be seen that the obtained junction-to-heatsink thermal resistance $Z_{th(c)}$ is approximately 1.6°C/W. However, this parameter in the MOSFET datasheet is 3.1°C/W [32], nearly twice as the measured value. Clearly, the device manufacturer has added a considerable safety margin to the transient thermal impedance and this is not uncommon in semiconductor industry [34].

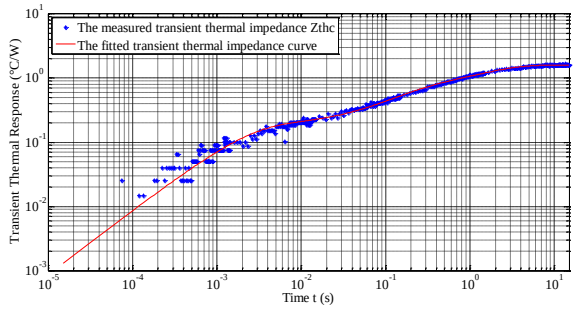


Fig. 5. The measured transient thermal impedance curves.

III. Online Measurements of the Threshold Voltage

Online measurements of the threshold voltage are first carried out at switching transients and then at steady state.

A. Measurements during switching transients

Early attempts [35] to measure the threshold voltage suffer from rapid transient changes in the turn-on time. As a preliminary improvement, the gate-source voltage rise and drain current rise are directly sampled and monitored by the DSP in this paper. Moreover, the gate drive circuit is also modified to prolong the turn-on process. A 470kΩ gate resistor R_{G2} is added, and the switch S_1 and the diode D_1 are rearranged as depicted in Fig. 6. In this diagram, S_1 is an optocoupler which can be directly driven by the DSP output but cannot conduct in reverse.

At normal operating mode, S_1 is turned on by the DSP. Then the driver IC can charge the gate of the device through R_{G1} and S_1. Since the MOSFET gate cannot discharge through S_1, D_1 is arranged anti-parallel with S_1 to allow current to flow back to the driver IC. The on-state voltage drops of S_1 and D_1 are approximately 0.15V and 0.6V, respectively, so that their impact on the normal switching process is negligible.

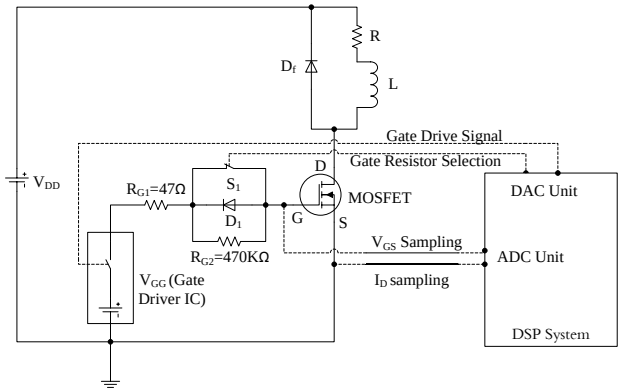


Fig. 6. Modified threshold voltage measurement.

When V_{th} is measured, S_1 is turned off by the DSP and the gate charging current flows through R_{G1} and R_{G2}. Because R_{G2} is much larger than R_{G1}, the turn-on process of the MOSFET is greatly slowed down. During this period, the gate source voltage and drain current are continuously sampled by the DSP until a zero-crossing point of I_D is detected. The gate source voltage at this instant is identified as the threshold voltage.

Experimental tests are performed under the following conditions: 100V DC link voltage, 30Ω load resistance, 10mH load inductance, 20°C heatsink temperature, and 15μs sample interval. From test results plotted in Fig. 7, the threshold voltage reads as 3.9V, indicating a 20% measurement error in the measurement.

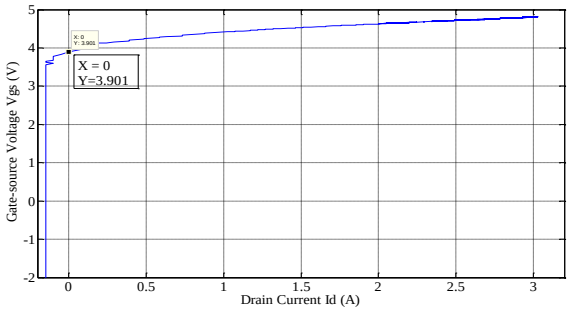


Fig. 7. Test results of the gate-source voltage and drain current.

Clearly, the modified threshold voltage measurement still needs to detect the exact drain current rise moment during the turn-on process, which is both prone to measurement noise and V_{ds} bias effects. Given this particular experimental challenge, the modified topology in Fig. 6 is not recommended and better alternatives need to develop.

B. Measurement during a steady state

In fact, the threshold voltage can also be measured at a steady state condition. During the measurements, the DC link and the load are momentarily isolated from the MOSFET to eliminate their influence on the power device. Next, the driver IC supplies a small drain current (less than 10mA) to the MOSFET. The gate source voltage under this condition is recorded and considered to be the threshold voltage.

Fig. 8 illustrates the proposed circuit setup for the threshold voltage measurement. A switching device (C_1) is used as the circuit contactor to momentarily disconnect the power MOSFET from the DC link voltage during measurements. Moreover, an optocoupler (S_2) and a power diode (D_2) are added to connect the gate to the drain during threshold voltage measurements and to disconnect them during normal operations. Furthermore, R_{G2} is changed from 470kΩ to 2.2KΩ while the drain current is controlled to be 5mA during measurements.

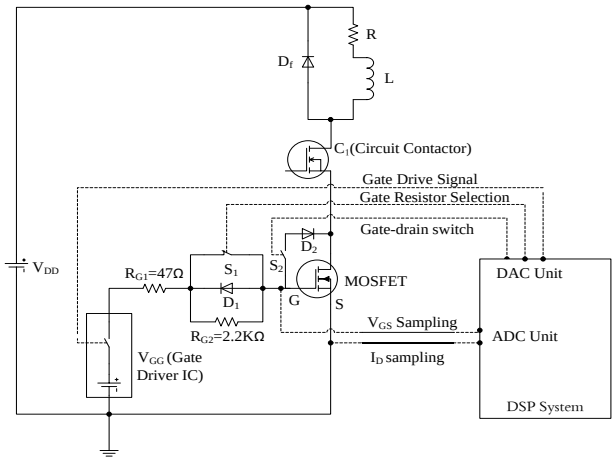


Fig. 8. Proposed circuitry for threshold voltage measurement.

IV. Real-Time Temperature Estimator

Compared to a Cauer-network, the Foster-network is easier to be extracted from TTICs using the curve fitting technique [33][36], and easier to be implemented in DSP with less computational costs. This paper derives the Foster RC thermal model from measured TTICs using a cooling curve and a curve fitting technique. In this test, it takes less than 3μs to run a third-order Foster-network in the DSP, which is only 30% of the processing time for an equivalent third-order Cauer-network. Again, it needs to stress that the Foster thermal model is a mathematical description rather than a physical representation of the structure of the device.

A. Derivation of the thermal model

Based on the cooling response, a Foster-network can be constructed with a series of RC cells in subsets with decoupled time constants [37]. For each subset, an optimized model code can be obtained, and then a complete model code can be pieced together by summing the exponential terms in a closed form of the simple analytical expression [38]:

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{R_i C_i}}\right) \tag{5}$$

where $Z_{th}(t)$ is the transient thermal impedance, R_i and C_i are the thermal resistance and capacitance of the cell i in the Foster-network, respectively.

The measured transient thermal impedance $Z_{th(c)}$ is fitted to a third-order Foster-network to obtain corresponding RC values by using a Matlab program. The results are shown in Fig. 9. This curve-fitted TTIC is plotted on the measured one, as given in Fig. 5. A good degree of reproductivity of the Foster-network by this third-order expression is clearly demonstrated in the figure.

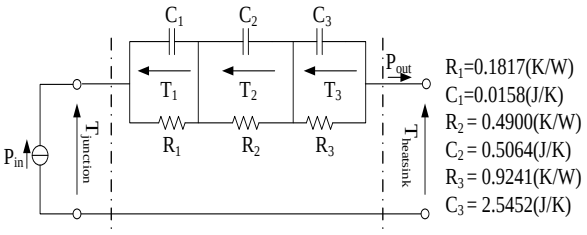


Fig. 9. The derived third-order Foster-network and its parameters.

B. Update on the thermal model

The above analysis is based on an assumption that thermal resistances do not change with time but this is not true in reality. To account for the aging effect in a multi-layer power device over its lifetime, the parameters in the Foster-network model need to be frequently updated. This update process can be carried out online at a chosen shift in thermal resistance or a chosen time interval.

By the nature of device aging, a linear approximation of thermal resistance upon the number of its thermal cycles can be assumed. This study proposes a linear estimation method to correlate thermal resistance and aging as follows,

$$R_{i(aged)} = R_i \left(1 + \frac{T_{j(measured)} - T_{j(estimated)}}{PR_{total}}\right) \tag{6}$$

where $R_{i(aged)}$ is the updated thermal resistance in the degraded thermal path, $T_{j(measured)}$ and $T_{j(estimated)}$ are the measured and estimated junction temperatures, and R_{total} is the sum of the thermal resistances without aging effects.

On the contrary, thermal capacitance is different to thermal resistance upon device aging. By definition, the thermal capacitance C_{th} is given by [39]:

$$C_{th} = \rho c_p l A \tag{7}$$

where ρ is the material density, c_p is the specific heat, l and A are the length and cross-sectional area in the thermal path, respectively.

Although thermal deterioration may also lead to some voids within die-attach solder layers in the device, the change in thermal capacitance is significantly less than that in thermal resistance. In this study, voids are modeled as an aggregate parameter [40] to reflect its inhomogeneous structure as opposed to commonly used air pockets. The properties of solder and voids are tabulated in Table I.

TABLE I
PARAMETERS OF VOIDS AND SOLDER IN THE MODELING

Material	Density	Specific Heat	Thermal conductivity
Solder (95Pb/Sn)	11,000 kg/ m^3	134 J/kg°C	32.3 W/m°C
Voids	2,340 kg/ m^3	820 J/kg°C	1 W/m°C

Solder and voids are important parts in the thermal modeling of the device. In principle, the thermal resistance of voids is 32 times greater than solder for the same size while their thermal capacitances are similar. Furthermore, the thermal capacitance of solder layers (0.004 J/K) is much smaller than that of the silicon substrate layer (0.0729 J/K) [4] and even smaller than that of the silicon active device layer (0.0044 J/K). As a result, the thermal capacitance of solder layers is considered less sensitive to void growth in the course of device aging.

C. Implementation of the real-time temperature estimator

In this test, the DC link is set to 190V, and the load current is 4.22A. In order to increase the switching heat power for an appreciable junction temperature rise, a gate resistor of 2.2kΩ is used. The switching power loss is measured off-line and the conduction loss is attained online by measuring V_{DS} and I_L. The test results from real-time temperature estimation (without model update) are shown in Fig. 10. There are two kinds of fluctuations which can be observed. The fast temperature fluctuations (less than 0.5ms) are caused by the switching events of the device, and the slow temperature fluctuations (over 200ms) are caused by variations of the load current and/or heatsink temperature. During the device on-time, a maximum of 15 junction temperature estimations can be produced. During the off-time, this is reduced to 5.

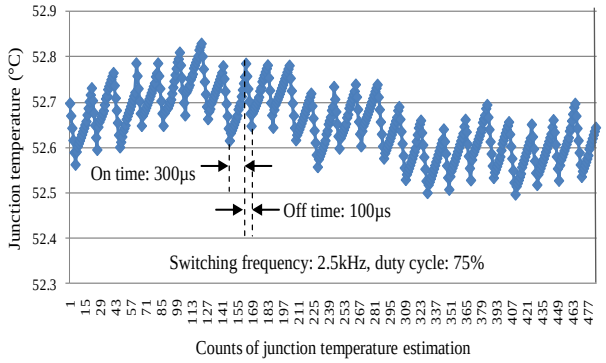
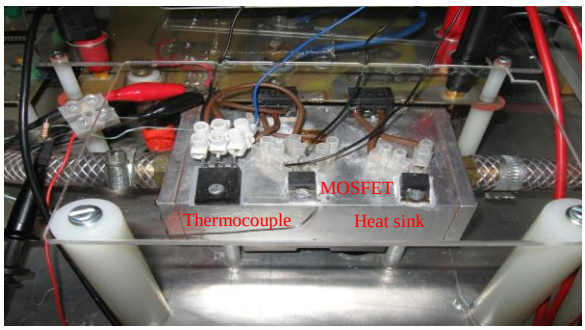


Fig. 10. Test results from the real-time junction temperature estimator.

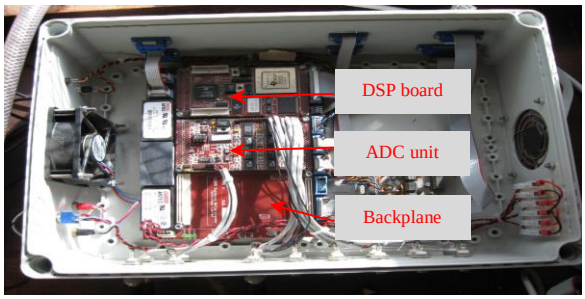
V. Experimental Setup and Procedure

An experimental test rig is set up for real-time junction temperature estimation, as presented in Fig. 11. The test rig consists of devices under test (i.e. MOSFETs), a measurement circuit, a control system, a DSP system, several temperature sensors and a temperature-controlled cold plate.

To emulate the aging in the thermal path of the device, the thermal grease between the power MOSFET and the heatsink is intentionally removed. Consequently, the thermal path between the silicon die and the heatsink is degraded to represent certain degree of device aging.



(a) Test base



(b) DSP system

Fig. 11. Experimental setup for real-time temperature estimation.

The thermal model update program is implemented in the DSP system and its procedure is illustrated in Fig. 12. The function generator produces the gate drive signal and the DSP system will simultaneously sample V_{DS}, I_L, V_{GS} and heatsink temperature T_{ref} at a 2.5 kHz switching frequency and a 75% duty cycle. Two hardware interrupt service routines (ISRs) are composed and implemented inside the DSP. One is triggered by the ADC unit by the end of every sampling process and another by the internal timer. The ADC ISR performs functions of both real-time junction temperature estimation and thermal model update. In this test, the junction temperature is estimated in real time every 20μs and the timer interrupt is triggered every 500μs. After the timer ISR runs 120,000 cycles, it will send a signal to the ADC ISR to start the thermal model update (i.e. every minute). However, the interval of the model update can be easily defined in the timer ISR at will. Ideally, the thermal model update should be trigged by events such as significant increases in junction temperature or thermal resistance. Alternatively, the update can be conducted at given time intervals (such as monthly) and more frequently when the devices approach their end-of-life period.

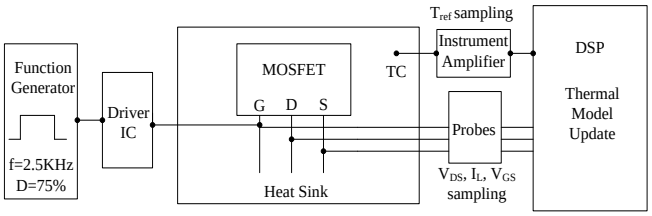


Fig. 12. Schematic diagram for online thermal model update.

VI. Results and Discussions

Following the method described in Section III-B, the threshold voltage is measured. The first 10 samples are discarded to remove non-thermal switching transients while further 15 samples are used to compute the junction temperature using Eq. 3. Then the thermal resistances are updated to reflect the degradation in the thermal path by Eq. 6.

A. Online update on the thermal model

Fig. 13 presents a comparison between the measured and estimated junction temperatures without an update on the thermal model. The former is based on V_{th} measurement and the latter on the Foster-network from the cooling curves of the "aged" MOSFET. By comparing the aged MOSFET with a new one, the error in temperature estimation is found to be as much as 20°C, which is well over the measurement tolerance. Obviously, traditional methods are increasingly difficult to measure the junction temperature with precision as thermal aging of the power device take places.

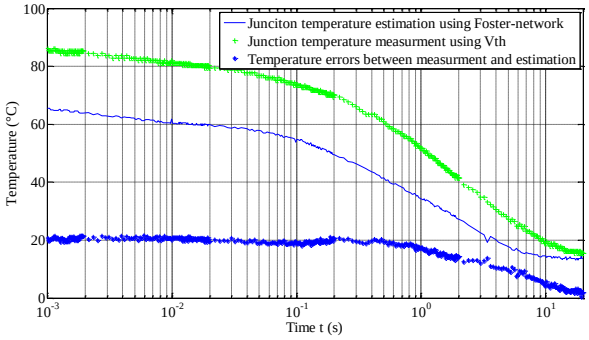


Fig. 13. Measured and estimated junction temperature without thermal model update.

This paper takes aging effects into account by measuring the change in thermal resistance and updating the thermal RC model for temperature estimation. During experimental tests, three consecutive thermal model updates are conducted at a 1-minute interval, and the log files are tabulated in Table II.

TABLE II
THERMAL MODEL UPDATE TEST (WITH THERMAL GREASE REMOVED)

Parameter	Update 1	Update 2	Update 3
Measured T_j (°C)	71.21	71.21	69.53
Estimated T_j (°C)	52.59	65.14	70.06
V_{th} (V)	3.05	3.05	3.06
ΔT (°C)	18.62	6.07	-0.53
ΔR (°C/W)	0.636	0.229	-0.017
R_1 (°C/W)	0.254	0.280	0.278
R_2 (°C/W)	0.685	0.756	0.750
R_3 (°C/W)	1.292	1.425	1.415

Three measurements from Updates 1-3 are used to minimize the measurement uncertainty (by convergence) in detecting the thermal deterioration of the device related to the removal of the thermal grease in this case.

The data for Update 1 show that the temperature difference (ΔT) between measurements and estimations is 18.62°C, the change in thermal resistance (ΔR) is 0.636°C/W, which is 40% of the original value due to the removal of the thermal grease. Thus the thermal resistances R_1 to R_3 increase by 40% accordingly by the thermal model updater. Since Update 2 uses the data from Update 1, the temperature difference is reduced to 6.07°C and the thermal resistance change is reduced to 0.229°C/W. Similarly, For Update 3, the temperature and resistance differences become negligible: -0.52°C and -0.017°C/W, respectively. The minus sign here indicates an overshooting occurrence in the previous update. Obviously, three successive measurements are sufficient to trace and correct a thermal change and to update the Foster-network model accurately. Although the updating can be achieved continuously, it is only needed to do so once a reasonable level of device degradation is generated (e.g. months).

These estimated junction temperature results are then compared to the measured ones using V_{th} through the cooling phase. As depicted in Fig. 14, the temperature error is consistently lowered (less than 2°C) after thermal model updates. This significant improvement confirms the effectiveness of the proposed methodology for the accurate junction temperature estimation.

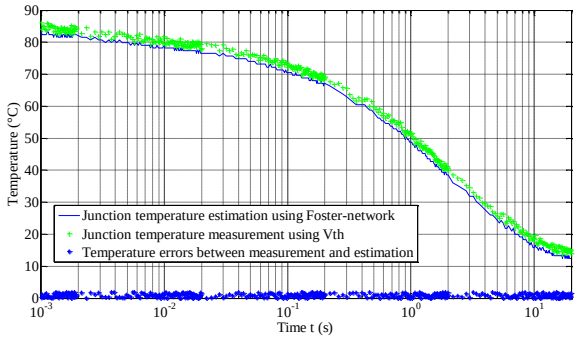


Fig. 14. Measured and estimated junction temperatures with thermal model updated.

B. Discussions

A fundamental principle behind the proposed technique is that solder layer degradation will not affect the linear relationship of the junction temperature and TSEPs. Because solder sits in the transitional layers between the silicon region and the base plate, the void growth within the solder layers does not impact on the physical characteristics of the silicon region. Therefore, it is feasible to use measured TSEP results to correct the estimated junction temperature generated from the thermal models.

It should be noted that TSEPs are measured under similar conditions of conducting the offline calibration so as to acquire accurate information of the junction temperature using TSEPs. In power MOSFETs, the variations of TSEPs are typically in a few millivolts whilst the threshold voltage may vary by 6mV/°C. Moreover, the actual conditions for threshold voltage measurement at a specific DC-link voltage and load scenario may be a far cry from the calibration measurement, resulting in measurement uncertainty of the junction temperature. Therefore, it is needed to conduct the calibration tests as close as possible to the operational conditions.

This paper is focused on the aging effects of power MOSFETs, particularly the solder layer degradation. The proposed techniques may not be suitable for correcting bonding wire-related failures because the relationship between the thermal resistance and bond wire failures is not yet established. The TSEPs are measured through the electric contacts of the power MOSFET via bonding wires but are not affected by partial failure of bond wires.

However, the method may be applied to other power devices such as insulated-gate bipolar transistor (IGBTs) and silicon carbide (SiC) MOSFETs which also have a MOS-gate structure and whose threshold voltage can also be used as a TSEP. The concepts demonstrated in this work are particularly relevant to high power IGBTs used in high-reliability applications where a complex gate driver design for power electronic devices is required for protection purposes.

It also needs to point out that the proposed online threshold voltage measurement technique uses the circuit contactor C_1 to momentarily isolate the Power MOSFET from the main circuit. Nonetheless, this can be overcome for multilevel converter applications (e.g. diode-clamped multilevel inverters) where a power device can be momentarily isolated from the load current path by other devices.

VII. CONCLUSIONS

The paper has presented a new real-time device temperature estimator. The novelty lies in the accurate thermal models to account for the aging effects of the power MOSFET and an experimental demonstration of the proposed methodologies.

In this study, the threshold voltage is proven to be an important temperature sensitive electrical parameter to detect the degradation of the power MOSFETs. However, it should not be measured at switching transients when it can be populated with electromagnetic interface (EMI), fluctuations of gate driver voltage and even dc-link voltage. It is possible to

enhance the accuracy of the estimated junction temperature in a model-based real-time estimator. Test results on power MOSFETs have shown that the proposed techniques are capable of detecting the increase in the thermal resistance of the device and correcting estimation errors (arising from aging of physical layers) in the thermal RC models.

The proposed technologies are based on power MOSFETs and their effectiveness is experimentally validated. In terms of MOS-gate structure, SiC MOSFETs and IGBTs also have similar turn-on characteristics, threshold voltage temperature dependency, and gate driver circuits. The proposed methods can be applied to IGBT-, SiC-based converters for on-line through-life health monitoring of power devices. In addition, they are useful for high power high reliability systems such as multi-level converter-based high-voltage direct current (HVDC) valves, flexible AC transmission systems (FACTs) (Statcom/SVG), and medium-voltage drives for power, petrol, chemical, and steel industries, locomotive and submarine traction drives. Other potential benefits may also include active control of the device junction temperature and reduced heatsink weight and volume.

In the future work, the proposed condition monitoring circuitry will be integrated into the existing driver circuits to further improve the reliability and controllability of the power devices. This will have significant economic implications in lowering the material and operational costs of power converters.

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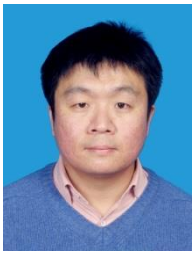

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