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ERKAN YUCE, SHAHRAM MINAEI, NORBERT HERENC SAR, JAROSLAV KOTON

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REALIZATION OF FIRST-ORDER CURRENT-MODE FILTERS WITH LOW NUMBER OF MOS TRANSISTORS

ERKAN YUCE

*Pamukkale University, Department of Electrical and Electronics Engineering,
Denizli, Kinikli 20070, Turkey
erkanyuce@yahoo.com*

SHAHRAM MINAEI*

*Dogus University, Department of Electronics and Communications Engineering,
Acibadem, Kadikoy 34722, Istanbul, Turkey
sminaei@dogus.edu.tr*

NORBERT HERENC SAR

*Brno University of Technology, Department of Telecommunications,
Purkynova 118, 612 00 Brno, Czech Republic
herencsn@feec.vutbr.cz*

JAROSLAV KOTON

*Brno University of Technology, Department of Telecommunications,
Purkynova 118, 612 00 Brno, Czech Republic
koton@feec.vutbr.cz*

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In this paper, a new current-mode (CM) circuit for realizing all of the first-order filter responses is suggested. The proposed configuration contains low number of components, only two NMOS transistors both operating in saturation region, two capacitors and two resistors. Major advantages of the presented circuit are low voltage, low noise and high linearity. The proposed filter circuit can simultaneously provide both inverting and non-inverting first-order low-pass, high-pass and all-pass filter responses. Computer simulation results achieved through SPICE tool and experimental results are given as examples to demonstrate performance and effectiveness of the proposed topology.

Keywords: NMOS, first-order filter, current-mode.

1. Introduction

The use of current-mode (CM) active devices offers some important potential advantages called as higher usable gain, more reduced voltage excursion at sensitive nodes, greater linearity, less power consumption, wider bandwidth, better accuracy and larger dynamic range compared to that of voltage-mode counterparts for example operational amplifiers¹⁻³. It is a well known fact that an all-pass filter (phase shifter) topology like previously reported first-order signal processing units⁴⁻¹⁸ finds wide

* Corresponding author

Table 1. Comparison with previously published CM all-pass filters

Properties Reference	Number of transistors	Number of R/C	Passive component matching constraint	Type of response	Technology	Power supplies
[10]	6	0/1	no	inverting	BJT	$\pm 1.5V$
[11]	3	2/2	no	Non-inverting	0.18 μm	+1.8V
[12]	7	0/1	no	Non-inverting	0.35 μm	+3.3V
[13]	12	0/1	no	Non-inverting	BJT	+3.0V
[14]	10	0/1	no	inverting	BJT	$\pm 5.0V$
[15]	38*	2/1	yes	Both **	0.35 μm	$\pm 2.5V$
[16]	38	1/1	no	Both simultaneously	0.5 μm	$\pm 2.0V$
[17]	32	1/1	no	Both ***	0.25 μm	$\pm 1.25V$
This work	2	2/2	yes	Both simultaneously	0.13 μm	$\pm 0.75V$

* Except four NMOS transistors used to obtain two tunable resistors

** There are two different circuits, one of which is inverting while other one is non-inverting.

*** Inverting response is obtained by RC-CR transformation.

application areas in analog signal processing systems, control engineering, etc. in order to shift phases of the signals while keeping their amplitudes unchanged. A first-order all-pass filter requiring at least one capacitive component and one resistive component has a pole on the left half s plane and a zero on the right half s plane. The pole and zero has the same value in magnitude. The filters of ⁴⁻⁹ use CMOS technology but operate in voltage-mode (VM). On the other hand, the circuits in ^{10, 13, 14} operate in CM but employ BJT technology. The CM filter of ¹¹, which is suitable for high frequency applications, contains three CMOS transistors, a floating resistor for biasing purpose and a large coupling capacitor for dc isolation of the load. The circuit reported in ¹² is a square-root-domain CM filter which needs two identical bias currents. It is worth to note that a simple square-root-domain integrator needs more than 30 transistors ¹². Further, many phase shifters like circuits in ¹⁵⁻¹⁸ using active building blocks such as second-generation current conveyors (CCII) have been reported in open literature. It should be noted that a CCII typically involves more than ten transistors.

In this paper, a novel CM circuit for simultaneously providing both inverting and non-inverting first-order low-pass, high-pass and all-pass filter responses is suggested. The developed filter structure includes a lower number of elements such as only two NMOS transistors, two capacitors and two resistors. The presented circuit enjoys low voltage, low noise and high linearity. However, it requires matching conditions for all-pass responses. Simulation results and experimental measurements are included to verify the theory. Table 1 summarizes the advantages and disadvantages of the previously published CM all-pass phase filters as well as the proposed one.

2. Proposed CM All-pass Filter

The proposed CM topology for realizing various first-order filters is shown in Fig. 1. It can be seen that it employs an inverting amplifier with the voltage gain of $-\beta$. The employed inverting amplifier should possess high input and low output impedances ideally. Such an amplifier with unity gain in magnitude can be found in ⁵ using two NMOS and three PMOS transistors or in ^{6, 8} using only two NMOS transistors with large

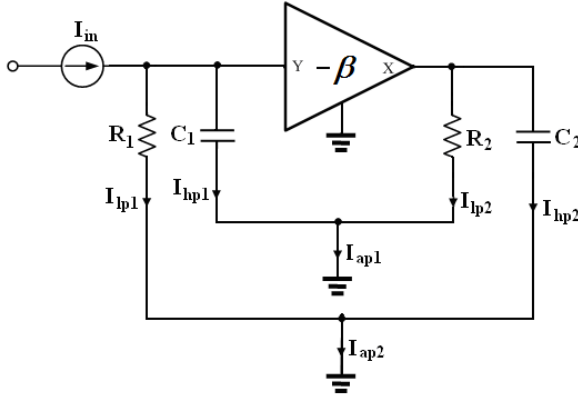


Fig. 1. Developed CM configuration for realizing first-order filters.

dimensions. Analysis of the proposed CM configuration of Fig. 1 gives the following responses:

i. Non-inverting low-pass transfer function (TF) and phase response

$$\frac{I_{lp1}}{I_{in}} = \frac{1}{1 + sC_1R_1} \quad (1a)$$

$$\phi_{lp1}(\omega) = -\tan^{-1}(\omega C_1R_1) \quad (1b)$$

ii. Non-inverting high-pass TF and phase response

$$\frac{I_{hp1}}{I_{in}} = \frac{sC_1R_1}{1 + sC_1R_1} \quad (2a)$$

$$\phi_{hp1}(\omega) = \frac{\pi}{2} - \tan^{-1}(\omega C_1R_1) \quad (2b)$$

iii. Inverting low-pass TF and phase response

$$\frac{I_{lp2}}{I_{in}} = -\frac{\beta \frac{R_1}{R_2}}{1 + sC_1R_1} \quad (3a)$$

$$\phi_{lp2}(\omega) = \pi - \tan^{-1}(\omega C_1R_1) \quad (3b)$$

iv. Inverting high-pass TF and phase response

$$\frac{I_{hp2}}{I_{in}} = -\frac{s\beta C_2R_1}{1 + sC_1R_1} \quad (4a)$$

$$\phi_{hp2}(\omega) = -\frac{\pi}{2} - \tan^{-1}(\omega C_1R_1) \quad (4b)$$

Here, the pole frequency of the filter from Fig. 1 is found as $\omega_0 = 1/(C_1R_1)$. Further, if $\beta = 1$ as for the inverting amplifiers in ^{5,6}, the following responses can be obtained:

v. Inverting all-pass TF and phase response if $R_2 = R_1$ as

$$\frac{I_{ap1}}{I_{in}} = \frac{I_{hp1}}{I_{in}} + \frac{I_{lp2}}{I_{in}} = -\frac{1 - sC_1R_1}{1 + sC_1R_1} \tag{5a}$$

$$\varphi_{ap1}(\omega) = \pi - 2 \tan^{-1}(\omega C_1R_1) \tag{5b}$$

vi. Non-inverting all-pass TF and phase response if $C_2 = C_1$ as

$$\frac{I_{ap2}}{I_{in}} = \frac{I_{lp1}}{I_{in}} + \frac{I_{hp2}}{I_{in}} = \frac{1 - sC_1R_1}{1 + sC_1R_1} \tag{6a}$$

$$\varphi_{ap2}(\omega) = -2 \tan^{-1}(\omega C_1R_1) \tag{6b}$$

It should be noted that the all-pass filters of ^{4-15, 17, 18} can realize only one all-pass response. In order to obtain output currents at high-output-impedance terminals from the structure in Fig. 1, a current buffer is required for each current. For this purpose a current follower (CF) ¹⁹ can be a good choice. However, a CF has an input parasitic resistance denoted by R_p . The output of the developed inverting all-pass filter connected to the input of a CF is shown in Fig. 2. Considering the required conditions for the inverting all-pass response as $R_1 = R_2$ and $\beta = 1$, the corresponding gain and phase responses are computed as

$$\frac{I_{ap1}}{I_{in}} = -\frac{1 - sC_1R_1}{1 + \frac{R_p}{R_1} + sC_1(R_1 + 3R_p)} \tag{7a}$$

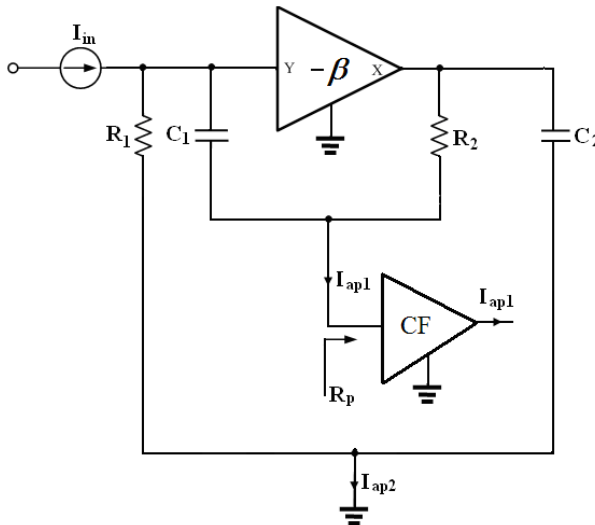


Fig. 2. The output of the suggested all-pass filter connected to the input of a CF.

$$\varphi_{ap1}(\omega) = \pi - \tan^{-1}(\omega C_1 R_1) - \tan^{-1}\left(\frac{\omega C_1(R_1 + 3R_p)}{1 + \frac{R_p}{R_1}}\right) \quad (7b)$$

From (7), one should select $R_1 \gg 3R_p$ to prevent the loading effect.

3. Parasitic effects

The parasitic of the employed amplifier can be considered as parallel capacitance and resistance at its input terminal ($R_y \parallel C_y$) and output resistance (R_o) in series at its output terminal as shown in Fig. 3. Since R_y and C_y appears in parallel with externally connected R_1 and C_1 , their effects can be neglected selecting $R_1 \gg R_y$ and $C_y \ll C_1$. Considering the output resistance R_o of the inverting amplifier, while the current responses I_{lp1} and I_{hp1} remain undisturbed, I_{lp2} and I_{hp2} and their corresponding phase responses convert to

$$\frac{I_{lp2}}{I_{in}} = -\frac{\beta R_1}{(1 + sC_1 R_1)(R_2 + R_o + sC_2 R_2 R_o)} \quad (8a)$$

$$\varphi_{lp2}(\omega) = \pi - \tan^{-1}(\omega C_1 R_1) - \tan^{-1}\left(\frac{\omega C_2 R_2 R_o}{R_2 + R_o}\right) \quad (8b)$$

$$\frac{I_{hp2}}{I_{in}} = -\frac{\beta s C_2 R_1 R_2}{(1 + sC_1 R_1)(R_2 + R_o + sC_2 R_2 R_o)} \quad (9a)$$

$$\varphi_{hp2}(\omega) = -\frac{\pi}{2} - \tan^{-1}(\omega C_1 R_1) - \tan^{-1}\left(\frac{\omega C_2 R_2 R_o}{R_2 + R_o}\right) \quad (9b)$$

It can be seen that a second pole appears in the TF of the filter due to the nonzero output resistance of the amplifier as

$$\omega_{p2} = \frac{R_2 + R_o}{C_2 R_2 R_o} = \frac{1}{C_2 R_o} + \frac{1}{C_2 R_2} \quad (10)$$

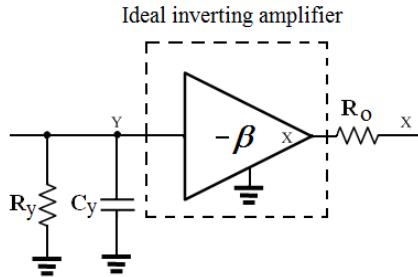


Fig. 3. Inverting amplifier with parasitic impedances

Thus one should select $R_o \ll R_2$ in order to neglect the effect of the second pole. Similarly, for the all-pass responses we can obtain

$$\frac{I_{lap1}}{I_{in}} = -\frac{R_1(\beta - sC_1(R_2 + R_o) - s^2C_1C_2R_2R_o)}{(1 + sC_1R_1)(R_2 + R_o + sC_2R_2R_o)} \quad (11a)$$

$$\varphi_{ap1}(\omega) = \pi - \tan^{-1}\left(\frac{\omega C_1(R_2 + R_o)}{\beta + \omega^2 C_1 C_2 R_2 R_o}\right) - \tan^{-1}(\omega C_1 R_1) - \tan^{-1}\left(\frac{\omega C_2 R_2 R_o}{R_2 + R_o}\right) \quad (11b)$$

$$\frac{I_{lap2}}{I_{in}} = \frac{R_2 + R_o - sC_2R_2(\beta R_1 - R_o)}{(1 + sC_1R_1)(R_2 + R_o + sC_2R_2R_o)} \quad (12a)$$

$$\varphi_{ap2}(\omega) = -\tan^{-1}\left(\frac{\omega C_2 R_2 (\beta R_1 - R_o)}{R_2 + R_o}\right) - \tan^{-1}(\omega C_1 R_1) - \tan^{-1}\left(\frac{\omega C_2 R_2 R_o}{R_2 + R_o}\right) \quad (12b)$$

Selecting $R_o \ll R_2$ with $R_2 = \beta R_1$ and $C_1 = \beta C_2$ in (11a) and (12a) one can obtain the ideal all-pass responses (5a) and (6a), respectively. Note that the proposed all-pass filter having no capacitor connected in series to the X terminal of the inverting amplifier; accordingly, it can be worked at higher frequencies²⁰.

4. Noise analysis

The inverting amplifier used in the structure of the proposed CM all-pass filter can be implemented with two NMOS transistors as shown in Fig. 4a⁸. The gain of the amplifier is found as

$$\frac{V_o}{V_{in}} = -\beta = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \quad (13)$$

where $(W/L)_i$ is the ratio of the channel width to channel length of the i -th ($i = 1, 2$) transistor.

The inverting amplifier including noise sources of the transistors is shown in Fig. 4b. The noise density sources of the transistors can be represented as:

$$\overline{dV_1^2} = 4kTR_{eff1}df \quad (14a)$$

$$\overline{dV_2^2} = 4kTR_{eff2}df \quad (14b)$$

Here, R_{effi} is the effective thermal noise resistance of the i -th transistor given as

$$R_{effi} = \frac{2}{g_{mi}} + R_{Gi} + R_{Bi}(n-1)^2 \quad (15)$$

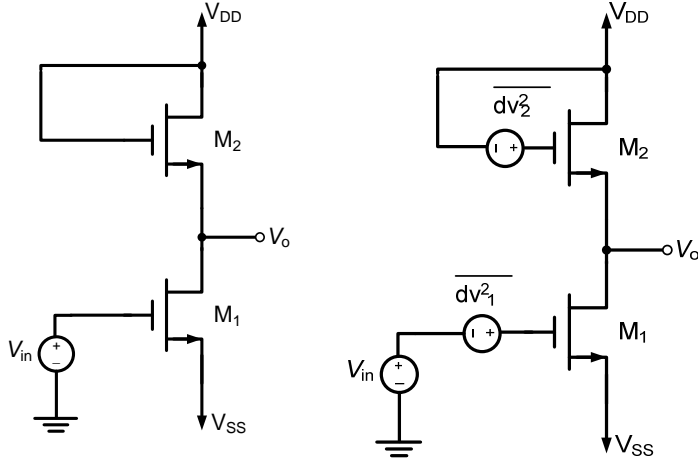


Fig. 4. (a) NMOS-based inverting amplifier (b) Noise model.

In (15), $\frac{2/3}{g_m}$ represents the channel noise effect, R_G is the poly gate resistor and R_B is the substrate resistance²¹. The substrate resistance is multiplied a factor of $(n-1)$ which is equal to the ratio of the bulk transconductance to the transconductance of the transistor, i.e. $\frac{g_{mb}}{g_m}$.

The total output current noise density of the inverting amplifier can be given as

$$\overline{di_{out}^2} = g_{m1}^2 \overline{dV_1^2} + g_{m2}^2 \overline{dV_2^2} \quad (16)$$

Thus the equivalent input noise density of the amplifier is found as

$$\overline{dV_{ieq}^2} = \overline{dV_1^2} + \frac{g_{m2}^2}{g_{m1}^2} \overline{dV_2^2} = \overline{dV_1^2} + \frac{1}{\beta^2} \overline{dV_2^2} \quad (17)$$

Considering matched transistors i.e. $g_{m1} \cong g_{m2}$ and consequently $\beta = 1$ the total equivalent input noise density is $\overline{dV_{ieq}^2} \cong 2\overline{dV_1^2}$.

For the all-pass filter of Fig. 1, there are additional thermal noises due to the external resistors R_1 and R_2 . Thus, the total equivalent input noise of the proposed CM all-pass filter can be given as:

$$\overline{dV_{ieq-allpass}^2} = 4kTR_1 df + 2\overline{dV_1^2} + \frac{1}{\beta^2} 4kTR_2 df \quad (18)$$

From (18), an equivalent input resistance (R_{ieq}) for noise calculation purpose can be defined as:

$$R_{ieq-allpass} = R_1 + 2R_{eff1} + \frac{1}{\beta^2} R_2 \quad (19)$$

The bandwidth (BW) of the equivalent input noise density is limited by the external capacitor C_1 . Thus the integrated noise of this resistor-capacitor combination (or all-pass filter) is found by taking the integral over all frequencies as

$$\overline{V_{ieq}^2} = \int_0^{\infty} \frac{dV_{ieq-allpass}^2}{1 + \left(\frac{f}{BW}\right)^2} = 4kTR_{ieq}BW \frac{\pi}{2} \quad (20)$$

where

$$BW = \frac{1}{2\pi R_{ieq} C_1} \quad (21)$$

Substituting (21) into (20), the integrated noise is simply found as kT/C_1 . For wideband systems the integrated noise is important, thus to reduce the noise we have to select larger capacitances which obviously will increase the power consumption²¹.

5. Simulation and experimental results

In this section, simulation results of the proposed first-order all-pass filter in Fig. 1 based on 0.13 μm IBM MOS technology parameters²² with ± 0.75 V dc power supply voltages are demonstrated. The aspect ratios of both NMOS transistors of inverting amplifier in Fig. 4⁶ are chosen as 104 $\mu\text{m}/0.13$ μm . The aspect ratio of the transistors are selected large to prevent loading effect. The non-ideality parameters of the structure given in Fig. 4 are found as $\beta = 0.852$, $R_o = 13.66$ Ω , $C_y = 221$ fF, $R_y \approx \infty$. Passive components of the all-pass filter depicted in Fig. 1 are taken as $R_1 = R_2 = 12$ k Ω and $C_1 = C_2 = 10$ pF to obtain the resonance frequency of $f_o \cong 1.32$ MHz. For this purpose, ideal and simulated magnitude and phase responses of the all-pass filter, I_{ap1} and I_{ap2} , are shown in Figs. 5 and 6, respectively. Time domain responses of I_{ap1} and I_{ap2} are demonstrated in Fig. 7. Total Harmonic Distortion (THD) variations versus amplitudes of peak values of input current are given in Table 2, where at the outputs of I_{ap1} and I_{ap2} . 20 Ω resistors are connected to simulate the effect of the current. Similarly, input and output noise variations against frequency for I_{ap1} and I_{ap2} are tabulated in Tables 3 and 4, respectively.

Monte Carlo analysis of the introduced all-pass filter with 20% variations of $C = 10$ pF is achieved after a hundred runs. In addition, the variations of the magnitude of all-pass filter at 1.32 MHz are demonstrated in Fig. 8. The magnitudes of I_{ap1} and I_{ap2} with respect to frequency are drawn in Fig. 9.

In order to confirm the simulation results, the behavior of the I_{ap1} response of the proposed all-pass filter has also been verified by experimental measurements using network-spectrum analyzer Agilent 4395A, function generator Agilent 33521A, and oscilloscope Agilent DSOX2014A. In measurements the readily available array transistors CD4007UB²³ by Texas Instruments with ± 15 V dc supply voltages have been used. To perform the measurements of the proposed current-mode filter, the circuit was extended by voltage-to-current and current-to-voltage converters realized by OPA860 ICs²⁴ by Texas Instruments with dc power supply voltages equal to ± 5 V as it is shown in²⁵.

Since the OPA 860 generally behaves as CCII+, the measured voltage compared to the I_{ap1} is shifted in the phase by 180° . The experiments have been performed with $R_1 = R_2 = 1.2 \text{ k}\Omega$ and $C_1 = C_2 = 100 \text{ pF}$ and the results are shown in Fig. 10. In this case the 90° phase shift is at $f_0 \cong 1.26 \text{ MHz}$, which is very close to the theoretical value of $f_0 \cong 1.3263 \text{ MHz}$. The time-domain response of the measured I_{ap1} response of the all-pass filter is shown in Fig. 11 in which a sine-wave input of 1 V peak-to-peak and frequency of 1.26 MHz was applied to the filter. From Fig. 11 it can be seen that the phase shift in the I_{ap1} output against the input is 91° .

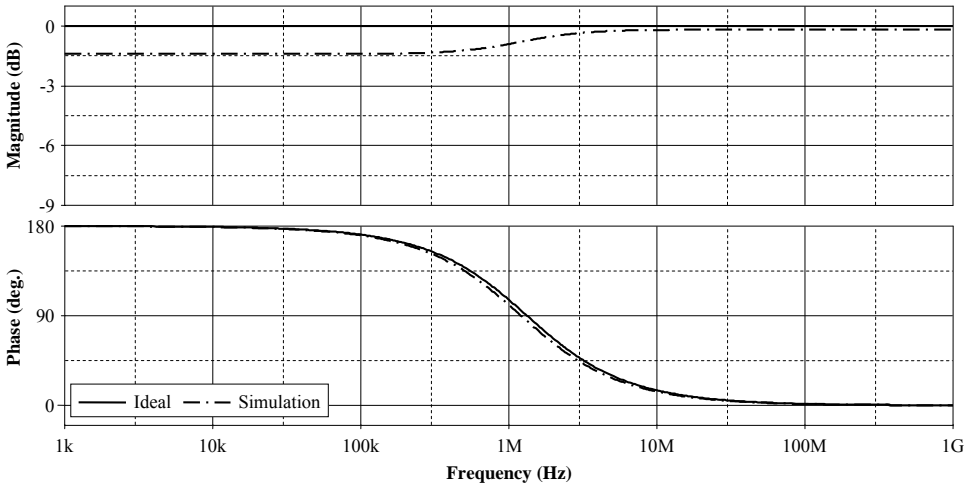


Fig. 5. Simulated magnitude and phase responses of the I_{ap1} .

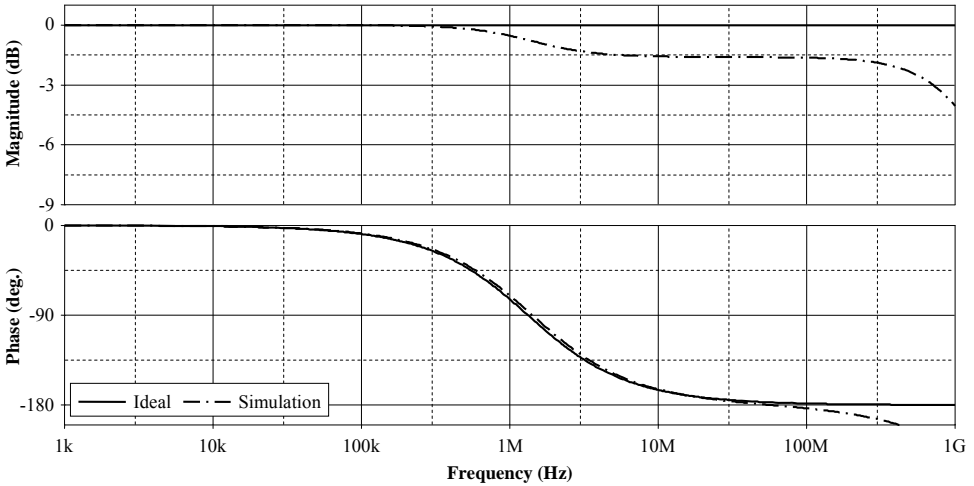


Fig. 6. Simulated magnitude and phase responses of the I_{ap2} .

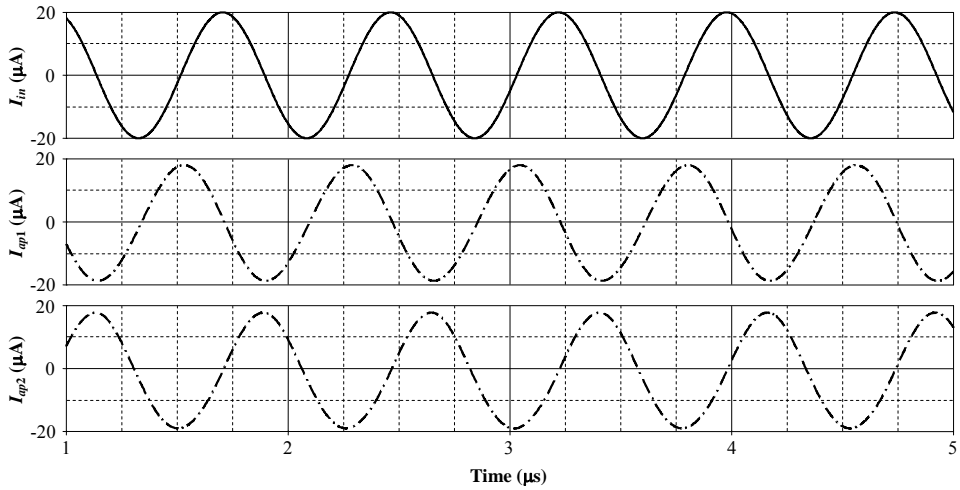


Fig. 7. Time domain responses of the all-pass filter.

Table 2. THD variations of all-pass responses of the filter in Fig. 1 at 1.32 MHz.

Magnitude of input current (μA)	I_{ap1} , THD (%)	I_{ap2} , THD (%)
1	0.379	0.628
5	0.582	1.242
10	1.119	2.306
15	1.609	3.275
20	2.046	4.072
25	2.353	4.684
30	2.581	5.192
35	2.782	5.639
40	2.955	6.050
45	3.114	6.490
50	3.232	7.103

Table 3. Input and output noises of the all-pass filter in Fig. 1 (I_{ap1}) against frequency.

Frequency (Hz)	Output noise ($\text{pV}/\sqrt{\text{Hz}}$)	Input noise ($\text{pA}/\sqrt{\text{Hz}}$)
1×10^3	575.64	33.81
1×10^4	575.64	33.81
1×10^5	575.63	33.78
1×10^6	575.04	31.98
1×10^7	574.04	29.54
1×10^8	574.02	29.48

Table 4. Input and output noises of the all-pass filter in Fig. 1 (I_{ap2}) against frequency.

Frequency (Hz)	Output noise (pV/ $\sqrt{\text{Hz}}$)	Input noise (pA/ $\sqrt{\text{Hz}}$)
1×10^3	575.77	28.79
1×10^4	575.77	28.79
1×10^5	575.77	28.82
1×10^6	575.72	30.67
1×10^7	575.59	34.69
1×10^8	572.45	35.11

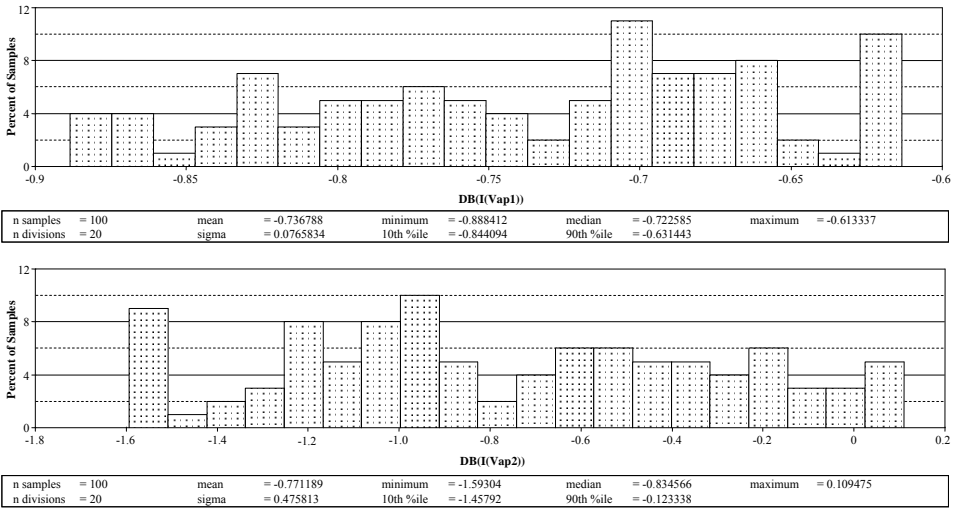


Fig. 8. Variations of the magnitude of all-pass filter at 1.32 MHz.

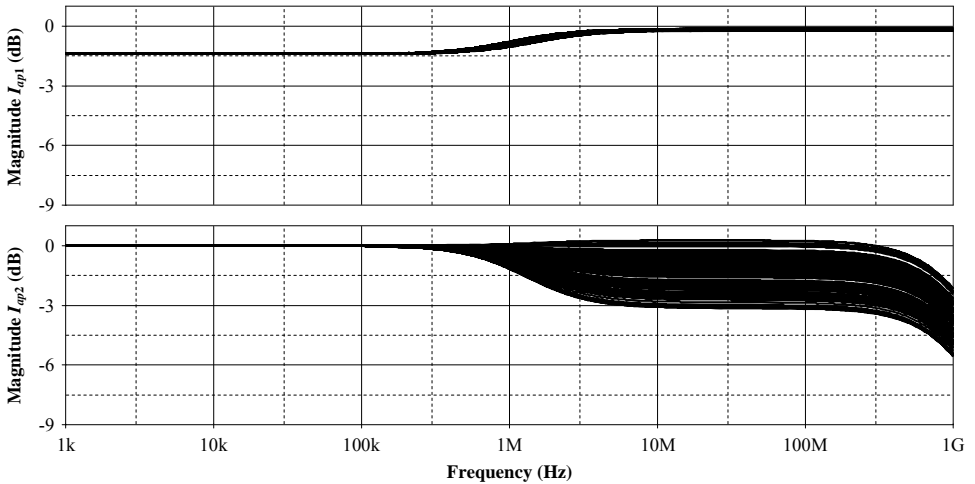


Figure 9. The magnitudes of I_{ap1} and I_{ap2} with respect to frequency.

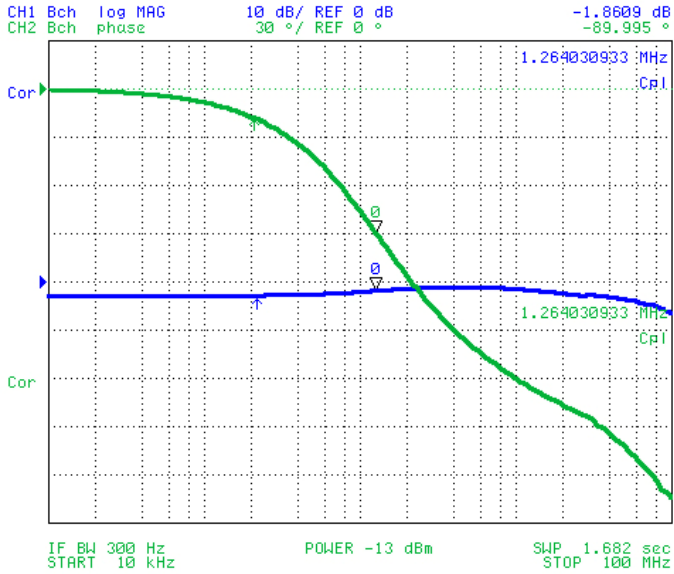


Fig. 10. Measured magnitude and phase responses of the I_{ap1} .

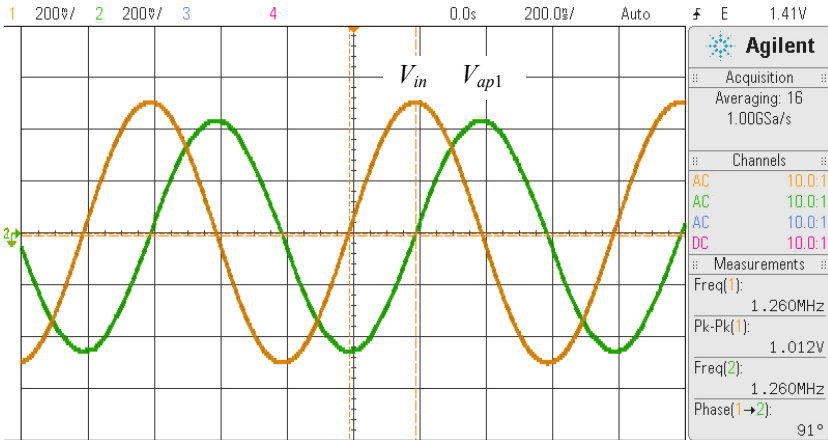


Fig. 11. Measured time domain response of the I_{ap1} .

It is observed from Figs. 5-7, 10, and 11 that the simulation and experimental results are in close proximity with the ideal ones as expected. Nevertheless, the discrepancy among ideal, simulation and experimental results fundamentally arises from non-idealities of NMOS transistors.

6. Conclusion

A new CM all-pass filter structure for simultaneously realizing inverting/ non-inverting first-order low-pass, high-pass and all-pass filter responses is developed in this paper. The suggested first-order filter consists of a lower number of components for example two NMOS transistors both in saturation region, two capacitors and two resistors. Major advantages of the proposed configuration are low voltage, low noise and

high linearity. Nevertheless, it needs matching constraints for all-pass characteristics. Simulation results accomplished via SPICE and experimental tests confirm the theoretical ones well as expected.

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