JSR Publications

Available Online

J. Sci. Res. **13** (1), 85-99 (2021)

JOURNAL OF SCIENTIFIC RESEARCH

www.banglajol.info/index.php/JSR

Realization of Inverse Active Filters Using Single Current Differencing Buffered Amplifier

T. K. Paul, S. Roy, R. R. Pal*

Department of Physics, Vidyasagar University, Midnapore 721102, West Bengal, India

Received 24 June 2020, accepted in final revised form 6 October 2020

Abstract

The authors introduce a new single current differencing buffered amplifier (CDBA) based inverse filter configuration. By appropriate selection of admittances, different inverse filter circuits like inverse high-pass (IHP) circuit, inverse low-pass (ILP) circuit, inverse band-reject (IBR) circuit and inverse band-pass (IBP) circuit can be realized from the same configuration. The capacitors used here are grounded/virtually grounded for all the realizations. The performances of the proposed filters have been judged by using CMOS structure of CDBA with TSMC 0.35 µm technology as well as by using the available IC of current feedback operational amplifier (CFOA) i.e. AD844 based CDBA. The simulation results agreed well with the theoretical results. Monte-Carlo simulation has also been performed to check the robustness of the proposed configuration.

Keywords: Inverse active filters; Current differencing buffered amplifier (CDBA); Analog signal processing.

doi: http://dx.doi.org/10.3329/jsr.v13i1.47766 J. Sci. Res. **13** (1), 85-99 (2021)

1. Introduction

Inverse filters which have an inverse transfer function of the original system are needed for correcting electrical signal distortions caused by the transmission system or signal processors and are used in control systems, communication and instrumentation [1,2]. Though there are several techniques for obtaining inverse digital filtering; only a few circuits are known for realizing continuous-time analog inverse filters. A single four-terminal floating nuller (FTFN) based inverse filter circuit has been reported by Wang and Lee [1], but the circuit is suitable only for all pass filter response. Also, it requires floating capacitor for its realization. Again, the single FTFN based inverse low-pass filter, introduced by Chipipop and Surakampontorn [2], uses floating capacitor and comparatively large number of resistors. However, the topology proposed by Abuelma'atti [3] is capable of realizing all the five inverse filter responses using single FTFN, but it is

* *Corresponding author*: rrpal@mail.vidyasagar.ac.in

unfit for IC implementation as it uses floating capacitor. Using current feedback operational amplifier (CFOA) as an active building block, few inverse active filters [4-7] have been reported but multiple CFOAs are needed for all of them. Further, the filters of Patil and Sharma [7] have the disadvantage of using floating capacitor and large number of resistors. The filter circuits (one each for ILP, IBP and IHP response) proposed by Herencsar *et al.* [8] require three differential difference current conveyors (DDCCs). Tsukutani *et al.* [9] introduced three inverse filter circuits, one each for IHP, ILP and IBP filter, but their circuits need three/four operational transconductance amplifiers (OTAs). Contrariwise, the inverse filter circuits based on second generation current conveyors (CCIIs) [10,11] have the limitations of excessive use of active building blocks and resistors. P. Kumar *et al*. [12] reported a unified filter topology to realize IHP, ILP, IBP and IBR filters, but it employs four voltage differencing transconductance amplifiers (VDTAs). Operational transresistance amplifier (OTRA) has also been employed to implement inverse filters [13-15]. However, these filters use two OTRAs and comparatively large number of passive elements.

Presently, a new active block namely current differencing buffered amplifier (CDBA) has been presented by Acar and Ozoguz. It offers all the advantages of current mode techniques and can be operated in several megahertz frequency range. The parasitic capacitance does not exist in this block as its input terminals are virtually grounded [16]. Furthermore, CDBA offers a low impedance voltage mode output, which is very needful for easy cascading. Various analog circuits such as inductor [16], multiplier [17], filter [18], oscillator [19] etc. are available using this versatile active building block.

Although, few attempts have already been made to realize inverse active filters by using CDBA as an active block [20-23], these circuits have some drawbacks. The inverse filter configuration reported by Nasir and Ahmad [20] has the limitation that it cannot realize IBR filter response. Furthermore, two CDBAs are necessary to implement this configuration. By contrast, Pandey *et al.* [21] introduced a topology which can realize all the inverse filter functions, but this topology also requires two CDBAs. Another inverse filter configuration has been presented by Bhagat *et al*. [22] employing two CDBAs. However, this configuration exhibits IBR and IAP filters only. Again, Bhagat *et al.* [23] reported an inverse filter topology using two CDBAs, but this design is only for ILP, IHP and IBP filter realizations.

In this paper, we propose a new single CDBA based inverse filter configuration which realizes inverse high-pass (IHP), inverse low-pass (ILP), inverse band-pass (IBP) and inverse band-reject (IBR) through the selection of proper admittances. The capacitors are grounded or virtually grounded in all the proposed functions. PSPICE simulation has been carried out by using CMOS as well as AD844 (commercially available IC) structure of CDBA for practical validation of the configuration. Simulation results are satisfactory. Robustness of the structure has been confirmed by Monte-Carlo analysis. The comparison of the reported inverse filter configuration with various previously proposed works are shown in Table 1.

Table 1. Comparison of previously reported inverse filter circuits and this work.

Ref.	No. and name of active blocks	Number of resistors (R)	Number of capacitors (C)	Standard filter functions
[1]	1 FTFN	4 R (1 G, 3 F)	2 C (1 G, 1 F)	IAP
[2]	1 FTFN	5 R (2 G, 3 F)	2 C (1 G, 1 F)	ILP
[3]	1 FTFN	2-4 R (1/2 G, 1/2 F)	2/3 C (1/2/3 G, 1/2 F)	IHP, ILP, IBP, IBR, IAP
[4]	3 CFOA	4 R (1/4 G, 3/4 F)	2 C (G)	IHP, ILP, IBP, IBR
[5]	3 CFOA	3-5 R (1/2/3 G, 1/2/3/4 F)	2 C (G)	IHP, ILP, IBP, IBR
[6]	3 CFOA	2-4 R (G)	2-4 C (G)	IHP, ILP, IBP
[7]	2 CFOA	4/6 R (2/4 G, 2/4 F)	2 C (1/2 G, 1 F)	IHP, ILP, IBP, IBR
[8]	3 DDCC	2 R (G)	2 C (G)	IHP, ILP, IBP
[9]	3/4 OTA	0	2 C (G)	IHP, ILP, IBP
[10]	3 CCII	2-5 R (1/2/3 G, 1/2 F)	2-5 C (1-3 G, 1/2 F)	IHP, ILP, IBP
[11]	3-6 CCII	3/4/6 R (G)	2 C (G)	IHP, ILP, IBP
[12]	2-4 VDTA	0	2 C (G)	IHP, ILP, IBP, IBR
[13]	2 OTRA	4 R (VG)	2/3 C (VG)	IHP, ILP, IBP
[14]	2 OTRA	4/5 R (VG)	2-4 C (VG)	IAP, IBR
[15]	2 OTRA	3/4 R (VG)	2/3 C (VG)	ILP, IBP
[20]	2 CDBA	2-4 R (1/2/3 G, 1 VG)	2-4 C (1/2/3 G, 1 VG)	IHP, ILP, IBP
[21]	2 CDBA	2-4 R (1/2 G, 2 VG)	2-4 C (1/2 G, 2/4 VG)	IHP, ILP, IBP, IBR, IAP
[22]	2 CDBA	4/5 R (VG)	2 C (1 G, 1 VG)	IBR, IAP
[23]	2 CDBA	4 R (2/3/4 VG, 1/2 F)	2 C (VG)	IHP, ILP, IBP
This work	1 CDBA	2/3 R (1 G, 1 VG, 1 F)	2/3 C (1 G, 2 VG)	IHP, ILP, IBP, IBR

G = Grounded, VG = Virtually Grounded, F = Floating.

2. Circuit Description

2.1. *CDBA*

CDBA is a current processing analog active building block which has greater linearity, large dynamic range, wide bandwidth etc. Furthermore, CDBA has no parasitic capacitances due to internally grounded input terminals [16]. Fig. 1(a) shows the circuit symbol of the CDBA, where p and n are the low impedance input terminals, w is low impedance output terminal and z is the high impedance output terminal [17]. The equivalent circuit of the CDBA is shown in Fig. 1(b). The port characteristics of this block can be expressed as $V_p = V_n = 0$, $V_w = V_z$ and $I_z = I_p - I_n$. The possible CMOS [17] and AD844 [19] based CDBA are depicted in Figs. 2(a) and 2(b) respectively.

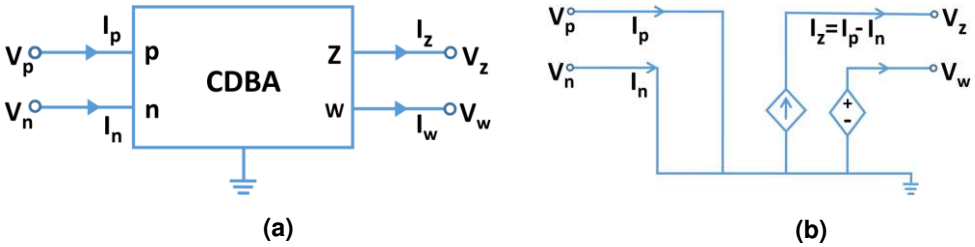

Fig. 1. The CDBA (a) block diagram (b) equivalent circuit.

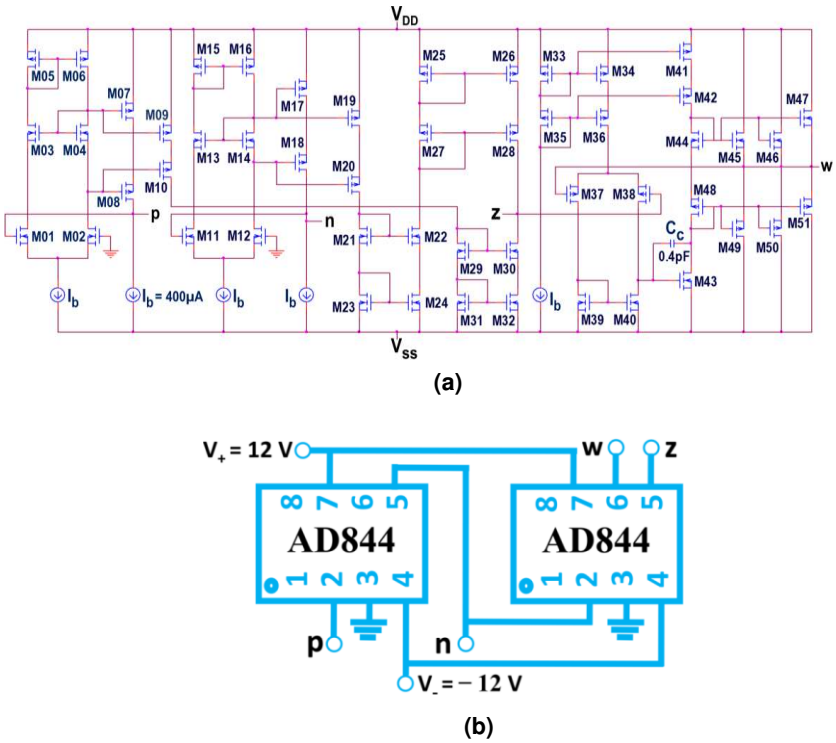

Fig. 2. Realization of the CDBA with (a) CMOS [17] and (b) AD844 [19].

2.2. *The proposed circuit configuration*

The proposed generalized configuration for realizing various inverse filters is shown in Fig. 3. This structure uses single CDBA and six admittances. The transfer function of the circuit of Fig. 3 obtained by routine analysis can be expressed as:

$$\frac{V_0(s)}{V_{in}(s)} = \frac{N(s)}{D(s)} = \frac{Y_1Y_2+Y_1Y_3}{(Y_2Y_6+Y_3Y_6-Y_2Y_3)+\frac{Y_4Y_5}{Y_4+Y_5}(Y_2+Y_3)} \tag{1}$$

If we choose the admittances, such that $Y_1 = sC_1 + \frac{1}{R_1}$, $Y_2 = sC_2$ and $Y_3 = \frac{1}{R_2}$, then the N(s) can be expressed as:

$$N(s) = s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1 \quad (2)$$

The required denominator functions $D(s)$ can be obtained by appropriate selection of admittances for Y_4, Y_5 and Y_6 as shown in Table 2. The transfer functions of various inverse filters are depicted in Table 3. It is clear from Table 3 that the IHP, ILP, IBP and IBR filter responses can be realized from the proposed configuration.

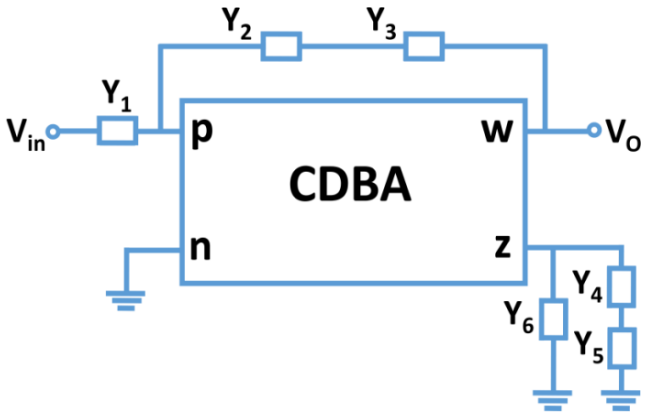

Fig. 3. Generalized design of a single CDBA based inverse filter realization.

Table 2. Selection of admittances and condition for different filter functions.

Filter response	Y_4	Y_5	Y_6	Condition
IHP	0	0	sC_3	$C_2 = C_3$
ILP	0	0	$\frac{1}{R_3}$	$R_2 = R_3$
IBP	$\frac{1}{R_3}$	sC_3	0	$C_3 = 2C_2, R_2 = 2R_3$
IBR	0	$\frac{1}{R_3}$	sC_3	$C_3 = C_1 = \frac{C_2}{2}, R_3 = R_1 = 2R_2$

Table 3. Transfer function of different filter responses.

Filter response	Transfer function
IHP	$\frac{V_0}{V_{in}} = \frac{1}{\frac{s^2C_2C_3R_1R_2}{s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1}}$
ILP	$\frac{V_0}{V_{in}} = \frac{1}{\frac{\frac{R_1}{R_3}}{s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1}}$

IBP	$\frac{V_0}{V_{in}} = \frac{1}{\frac{sC_2R_1}{s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1}}$
IBR	$\frac{V_0}{V_{in}} = \frac{1}{\frac{s^2C_1C_2R_1R_2 + 1}{s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1}}$

The circuit parameters ω_0 and Q for all the proposed filter responses are given by:

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_2}} \text{ and } Q = \frac{\sqrt{C_1C_2R_1R_2}}{C_1R_1 + C_2R_2} \tag{3}$$

3. Non-Ideal and Sensitivity Analysis

Practically, the effect of voltage and current tracking errors of CDBA will affect the performances of the proposed inverse filter responses. The non-ideal characteristic equation of CDBA is rewritten through a matrix, given in Eq. (4).

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 \\ 0 & 0 & 0 & \beta \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_w \\ V_z \end{bmatrix} \tag{4}$$

where α_p, α_n and β denote the non-ideal port transfer ratios of the CDBA.

Reanalyzing the designed circuit, taking into consideration of the non-ideal characteristic equation of CDBA, the revised transfer functions for the filter responses can be expressed as given in Table 4.

Table 4. Non-ideal transfer functions of various filter responses.

Filter response	Transfer function
IHP	$\frac{V_0}{V_{in}} = \frac{1}{\frac{s^2C_2C_3R_1R_2 + (1 - \alpha_p\beta)sC_2R_1}{\alpha_p\beta(s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1)}}$
ILP	$\frac{V_0}{V_{in}} = \frac{1}{\frac{(1 - \alpha_p\beta)sC_2R_1 + \frac{R_1}{R_3}}{\alpha_p\beta(s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1)}}$
IBP	$\frac{V_0}{V_{in}} = \frac{1}{\frac{(2 - \alpha_p\beta)sC_2R_1}{\alpha_p\beta(s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1)}}$
IBR	$\frac{V_0}{V_{in}} = \frac{1}{\frac{s^2C_1C_2R_1R_2 + (1 - \alpha_p\beta)sC_2R_1 + 1}{\alpha_p\beta(s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1)}}$

From Table 4, the modified parameters ω_0 and Q of the filters can be expressed as:

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_2}} \text{ and } Q = \frac{\sqrt{C_1C_2R_1R_2}}{C_1R_1 + C_2R_2} \tag{5}$$

From the Eq. (5), it may be concluded that the parameters ω_0 and Q for all the responses remain unchanged under non-ideal conditions. The sensitivity analysis of ω_0 and Q for the reported structure can be written as:

$$S^{\omega_0}_{C_1,C_2,R_1,R_2} = -\frac{1}{2};\ S^{Q}_{C_1,R_1} = \frac{1}{2} - \frac{C_1R_1}{C_1R_1 + C_2R_2};\ S^{Q}_{C_2,R_2} = \frac{1}{2} - \frac{C_2R_2}{C_1R_1 + C_2R_2} \tag{6}$$

Eq. (6) ensures that the sensitivities of ω_0 and Q with respect to different passive elements do not exceed ½ in magnitude.

4. Parasitic Analysis

Involving the different parasitics, the model of CDBA is shown in Fig. 4. The parasitic resistances R_p, R_n and R_o appear in series at the port p, n and w, respectively, whereas a resistance R_z in parallel with a capacitance C_z appears at the z-port [19]. Reanalyzing the reported circuit, taking into consideration the parasitics of CDBA, the revised transfer functions for the filter responses are depicted in Table 5.

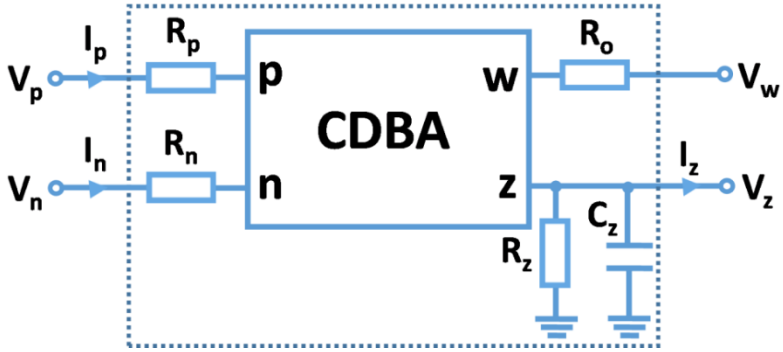

Fig. 4. Parasitic model of CDBA [19].

Table 5. Transfer functions of various filters including CDBA terminal parasitics.

Filter response	Transfer function
IHP	$\frac{V_0}{V_{in}} = \frac{1}{\frac{R_1'\left(\frac{1}{R_z} + sC_{3z}\right)(1 + sC_2R_2') - sC_2R_1}{(s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1)}}$
ILP	$\frac{V_0}{V_{in}} = \frac{1}{\frac{R_1'\left(\frac{1}{R_{3z}} + sC_z\right)(1 + sC_2R_2') - sC_2R_1}{(s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1)}}$

IBP	$\frac{V_0}{V_{in}} = \frac{1}{\frac{R_1'\left(\frac{1}{R_{3z}'} + sC_z\right)(1 + sC_2R_2') - sC_2R_1}{(s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1)}}$
IBR	$\frac{V_0}{V_{in}} = \frac{1}{\frac{R_1'\left(\frac{1}{R_{3z}} + sC_{3z}\right)(1 + sC_2R_2') - sC_2R_1}{(s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1)}}$

where $C_{3z} = C_3 + C_z$, $R_{3z} = R_3||R_z$, $R_{3z}' = (R_3 + \frac{1}{sC_z})||R_z$, $R_1' = R_1 + R_p$ and $R_2' = R_2 + R_o$.

It is clear from Table 5 that the transfer functions of the filters are affected by the non-idealities of CDBA. The so caused deviation from the ideal behaviour can be kept less if the values of all external resistors are kept much smaller than R_z but much higher than R_p, R_o. Likewise, the values of all external capacitors are selected much higher than C_z. Hence, all these parasitic components will be absorbed and they will not affect the circuit parameters.

5. Simulation Results

PSPICE simulation software has been used for practical verification of the proposed configuration. Initially, the functionality of the proposed circuit has been tested by using CMOS structure of CDBA [17]. For supporting hardware implementation of the designed filters, the CDBA block has also been realized employing market available ICs AD844 [19] and the simulation results for the same have been presented later.

5.1. *Simulation results using CMOS structure of CDBA*

The CMOS version of CDBA used for the purpose of simulations has been shown in Fig. 2(a) [17]. TSMC 0.35 µm technology has been used for this purpose. The aspect ratios of all the transistors used in Fig. 2(a) are given in Table 6 [17]. The supply voltages are chosen as ± 2.5 V. The chosen values of the capacitors and resistors for various filter responses are presented in Table 7. The ideal and simulated frequency response of IHP, ILP, IBP and IBR filters are depicted from Figs. 5(a) to 5(d), respectively.

Table 6. Dimensions of the transistors used in the CDBA circuit [17].

Transistors	Aspect ratio (µm/µm)
M01, M02, M11, M12	90/3
M03–M06, M13–M16, M21–M24	60/3
M07–M10, M17–M20, M25–M28, M39, M40	120/3
M33–M38, M41, M42	330/3
M29–M32	92/3
M43	217/3

Table 7. Values of circuit elements for realizing different filter responses.

Filter type	C_1 (pF)	C_2 (pF)	C_3 (pF)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)
IHP	30	30	30	5	5	–
ILP	30	30	–	5	5	5
IBP	30	30	60	5	5	2.5
IBR	30	60	30	5	2.5	5

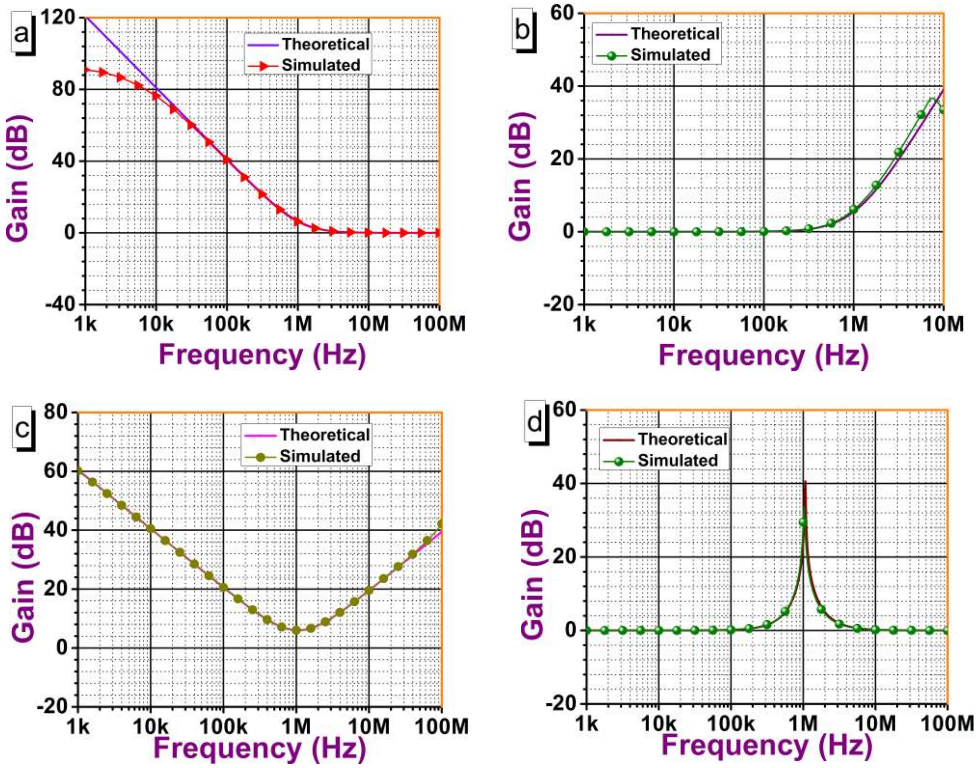

Fig. 5. Frequency responses of filter using CMOS structure of CDBA (a) IHP (b) ILP (c) IBP (d) IBR.

The f_0-tuning (f_0= $\frac{\omega_0}{2\pi}$) responses for the inverse band-reject filter for a particular Q value (Q = ½) are displayed in Fig. 6. The values of capacitors, resistors and corresponding values of f_0 are shown in Table 8. In order to determine the variation of centre frequency of IBR filter due to resistors and capacitors tolerance, the Monte Carlo analysis has been carried out. The analysis is done for 100 samples and tolerance is considered 5 % for resistors and capacitors which is shown in Fig. 7. It depicts that the center frequency varies from a minimum value 952.191 kHz to a maximum value 1.05042 MHz with standard deviation 17.2461 kHz. In order to inspect the dynamic range of the filter in their pass band, the output noise for IHP filter has been determined through PSPICE

simulation. The variation of output noise within pass band frequencies is demonstrated in Fig. 8, which depicts that noise is in considerable limit. For examining the transient analysis, a sinusoidal input of 100 kHz has been applied at the input terminal of the IBR filter and the obtained curves without significant distortion are depicted in Fig. 9. The IBR response of the proposed configuration has been tested for linearity by noting down the variations of total harmonic distortion (THD) with respect to amplitude of input signal. The result has been shown in Fig. 10. It is obtained from Fig. 10 that THD is increasing from 0.49 % to 2.59 % for the variation of input signal amplitude from 50 mV to 400 mV. From these simulation results it is concluded that the circuit can work excellently.

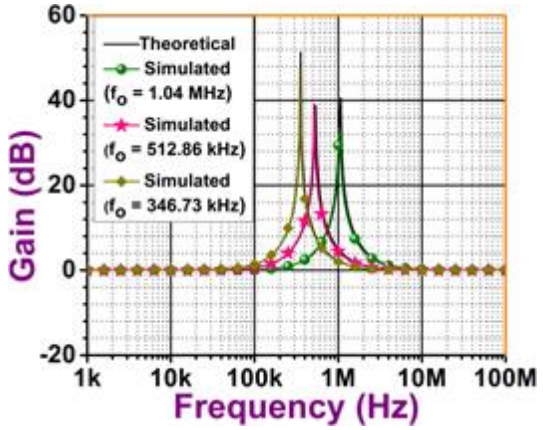

Fig. 6. f_0-tuning responses of IBR filter.

Table 8. Values of circuit elements for f_0-tuning of IBR filter.

C_1 (pF)	C_2 (pF)	C_3 (pF)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	Theoretical value of f_0	Simulation value of f_0	Frequency deviation (%)
30	60	30	5	2.5	5	1.06 MHz	1.02 MHz	3.8
30	60	30	10	5	10	530.79 kHz	512.86 kHz	3.4
30	60	30	15	7.5	15	353.83 kHz	346.73 kHz	2

5.2. *Simulation results using IC AD844*

The performance of all the filter responses has also been verified by using IC AD844 structure of CDBA with ± 10 V supply voltages. The implementation of CDBA using two AD844 ICs is shown in Fig. 2(b). The values of C_1, C_2, C_3 and R_1, R_2, R_3 are selected according to Table 7. The simulated frequency response of IHP, ILP, IBP and IBR filters are depicted from Figs. 11(a) to 11(d) respectively.

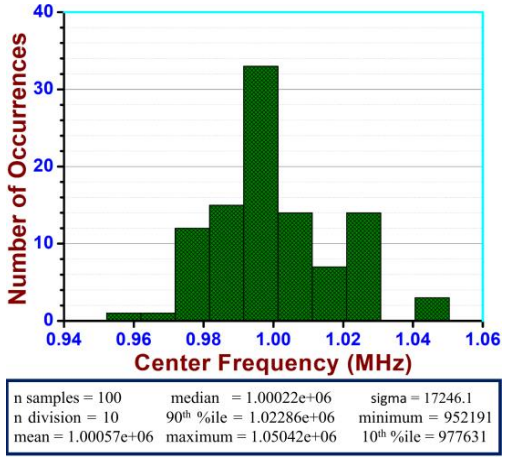

Fig. 7. Monte Carlo analysis of IBR filter for 100 samples.

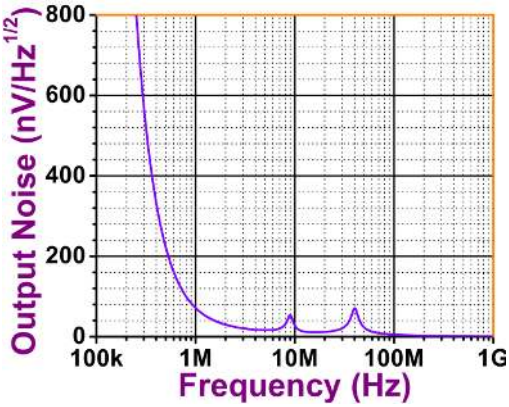

Fig. 8. Variation of output noise for IHP filter with respect to frequency.

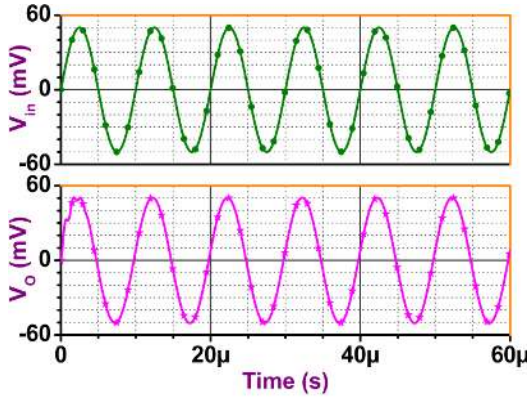

Fig. 9. Transient response of the IBR filter.

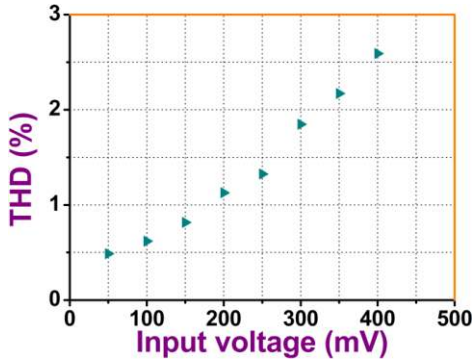

Fig. 10. THD plot for IBR filter function with input voltage.

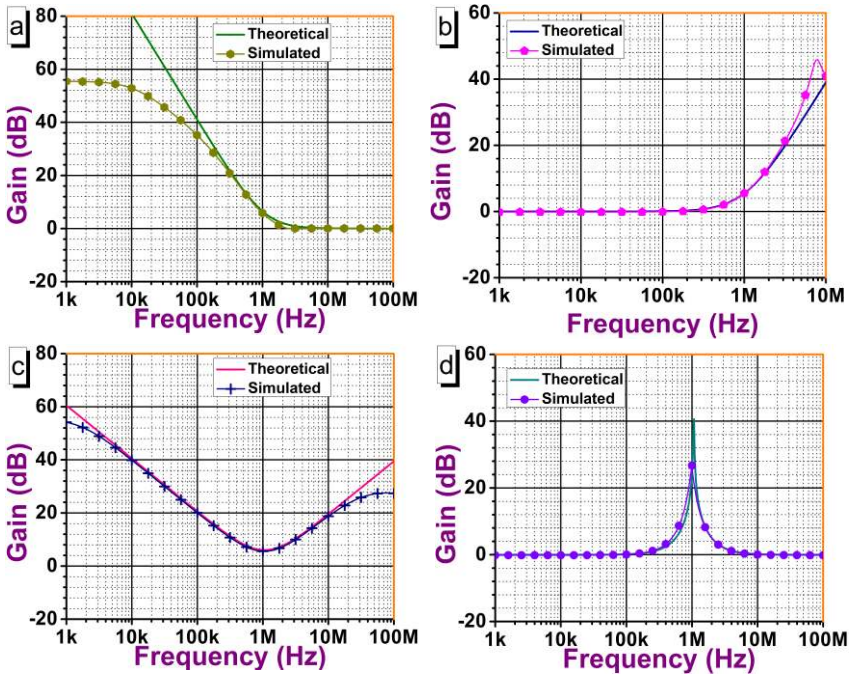

Fig. 11. Frequency responses of filter using AD844 IC (a) IHP (b) ILP (c) IBP (d) IBR.

The f_0 tuning of the inverse band-pass filter for Q = ½ is shown in Fig. 12. The selected capacitor, resistor values and the corresponding values of f_0 are shown in Table 9. To demonstrate the time domain behavior, a sinusoidal signal of 100 kHz, 100 mVp is applied at the IBR filter as input voltage. The input and output curves are depicted in Fig. 13. It is seen that the magnitude of output voltage is equal to input voltage. Fig. 14 depicts the THD variations of the IBR filter response with input signal amplitude. It is found that the THD is almost constant for the input range between 50 mV and 400 mV.

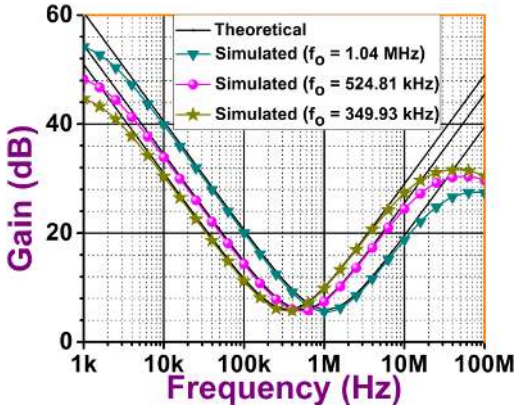

Fig. 12. f_0-tuning responses of IBP filter.

Table 9. Values of circuit elements for f_0-tuning of IBP filter.

C_1 (pF)	C_2 (pF)	C_3 (pF)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	Theoretical value of f_0	Simulation value of f_0	Frequency deviation (%)
30	30	60	5	5	2.5	1.06 MHz	1.04 MHz	1.9
30	30	60	10	10	5	530.79 kHz	524.81 kHz	1.1
30	30	60	15	15	7.5	353.83 kHz	349.93 kHz	1.1

It is found that the PSPICE simulation responses for both the CMOS and AD844 structure of CDBA are in close agreement with the theoretical results.

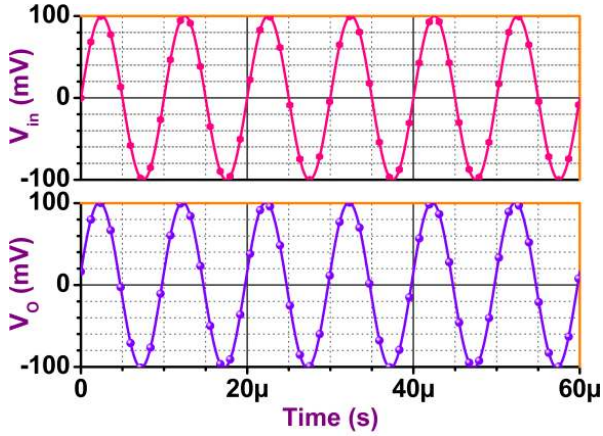

Fig. 13. Time-domain response of the IBR filter.

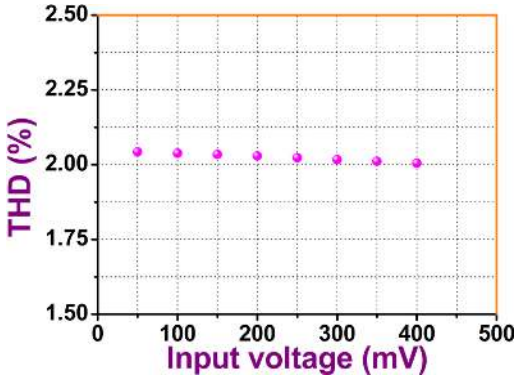

Fig. 14. Variation of THD with input voltage for IBR filter function.

5. Conclusion

We have reported a configuration of inverse filter using single CDBA block. Different filter responses can be realized by selecting proper passive elements. The workability of the proposed configuration has been verified using PSPICE simulation with CMOS structure of CDBA implemented with TSMC 0.35 µm process parameters. This configuration has also been tested through CDBA implemented with two AD844 ICs. The simulations results are in close agreement with theoretical prediction. The total harmonic distortion is found to be less than 2.59 % for the IBR filter response when simulated by CMOS based CDBA structure. For AD844 based CDBA structure, it is less than 2.04 %.

Acknowledgment

We are thankful to FIST-Department of Science and Technology, SAP-University Grants Commission, India for their continuous financial support to complete this work.

References

1. H. -Y. Wang and C. T. Lee, Electron. Lett. **35**, 1889 (1999). https://doi.org/10.1049/el:19991336
2. B. Chipipop and W. Surakampontorn, Electron. Lett. **35**, 690 (1999). https://doi.org/10.1049/el:19990495
3. M. T. Abuelma'atti, Frequenz **54**, 284 (2000).
4. S. S. Gupta, D. R. Bhaskar, R. Senani, and A. K. Singh, Electr. Eng. **91**, 23 (2009). https://doi.org/10.1007/s00202-009-0112-3
5. S. S. Gupta, D. R. Bhaskar, and R. Senani, Int. J. Electron. **98**, 1103 (2011). https://doi.org/10.1080/00207217.2010.547812
6. H. -Y. Wang, S. -H. Chang, T. -Y. Yang, and P. -Y. Tsai, Circuits Syst. **2011**, 14 (2011).
7. V. Patil and R. K. Sharma, Int. J. Sci. Res. Dev. **3**, 359 (2015).
8. N. Herencsar, A. Lahiri, J. Koton, and K. Vrba - *Proc. of 33rd Int. Conf. on Telecommunications and Signal Process.-TSP* 2010, 38 (2010).

9. T. Tsukutani, Y. Sumi, and N. Yabuki, Int. J. Electron. Lett. **4**, 166 (2014). https://doi.org/10.1080/21681724.2014.984636
10. C. K. Choubey, G. Tiwari, and S. K. Paul - *Int. Conf. on Adv. in Electron. Commun. and Comp. Technol. (ICAECCT)*, 160 (2016).
11. T. Tsukutani, Y. Kunugasa, and N. Yabuki, J. Electr. Eng. **6**, 212 (2018). https://doi.org/10.17265/2328-2223/2018.04.003
12. P. Kumar, N. Pandey, and S. K. Paul, J. Circuits, Syst. Comp. **28,** (2018). https://doi.org/10.1142/S0218126619501433
13. A. K. Singh, A. Gupta, and R. Senani, Adv. Electr. Electron. Eng. **15**, 846 (2017).
14. A. Pradhan and R. K. Sharma, Proc. Natl. Acad. Sci. India, Sect. A Phys. Sci. **90,** 481 (2019). https://doi.org/10.1007/s40010-019-00603-w
15. S. Banerjee, M. Ghosh, and P. Mondal - *Int. Conf. on Commun. and Signal Process*. **148** (2019).
16. J. K. Pathak, A. K. Singh, and R. Senani, Int. J. Electron. **103**, 1 (2015). https://doi.org/10.1080/00207217.2015.1020884
17. S. Roy, T. K. Paul, S. Maiti, and R. R. Pal, AEU-Int. J. Electron. Commun. **88**, 11 (2018). https://doi.org/10.1016/j.aeue.2018.03.002
18. T. K. Paul and R. R. Pal, Int. J. Comput. Eng. Res. **9**, 53 (2019).
19. T. S. Arora and S. Gupta, Eng. Sci. Technol. Int. J. **21**, 43 (2018).
20. A. R. Nasir and S. N. Ahmad, Int. J. Comput. Sci. Inf. Secur. **11**, 50 (2013).
21. R. Pandey, N. Pandey, T. Negi, and V. Garg, ISRN Electron. **2013**, 1 (2013). https://doi.org/10.1155/2013/181869
22. R. Bhagat, D. R. Bhaskar, and P. Kumar, Int. J. Eng. Res.Technol. (IJERT), **8**, 9 (2019).
23. R. Bhagat, D. R. Bhaskar, and P. Kumar, Int. J. Recent Technol. Eng. (IJRTE), **8**, 8844 (2019). https://doi.org/10.35940/ijrte.D9476.118419