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Realization of Unified Power Quality Conditioner for Mitigating All Voltage Collapse Issues

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Abstract

This paper proposes about a powerful control mechanism of UPQC (Unified Power Quality Conditioner) work on voltage source inverter which can effectively compensate source current harmonics and also mitigate all voltage collapse such as dip, swell, voltage unbalances and harmonics. The consolidation of series and parallel active power filters sharing mutual DC bus capacitor forms UPQC. PI (Proportional Integral) controller is mainly used in order to maintain continual DC voltage along with the hysteresis current controller. The parallel and series power filters were designed using 3-phase voltage source inverter. The reference signals for shunt and series active power filters were obtained by Synchronous Reference Frame (SRF) theory and Power Reactive (PQ) theory respectively. By using these theories, reference signals were obtained which was fed to the controllers for generating switching pulses for parallel and series active filters. The UPQC dynamic performance is obtained through testing terms like the compensation of voltage, current harmonics and all voltage distortion associated with 3-phase 3-wire power system which is simulated using MATLAB-Simulink software.

Keywords

Power Quality Conditioner, Voltage Sag (Dip), Voltage Swell, Current Harmonics Mitigation, Power Quality Improvement

1. Introduction

Due to increase in use of power electronics devices in industrial area as well as in customer loads which uses

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non-linear loads, non-linear loads at utility cause large supply of reactive power which pollutes the source side equipment largely. The main requirement of mitigation equipment is that they should be fast and dynamic response helps to reduce the source side harmonics. Due to increasing use of non-linear loads, nowadays active filters are replacing the olden days mitigation methods like switching capacitor and thyristor controlled inductor coupled with passive filters [1]-[4]. There are types of active power filters used: parallel active filter eliminates current harmonics and series active filter mitigates all types of voltage issues.

The Unified Power Quality Conditioner (UPQC) is a solution to mitigate current and voltage issues; it is the combined design of shunt and series active power filters coupled through mutual DC linkage capacitor which rejects the instabilities spread from the supply side and the interconnected supplementary loads. In general, the task of UPQC, parallel active filter estimates the reimbursing current harmonics called mitigating current harmonics and helps in VAR generation using the control circuitry [5]-[8]. The series active filters are able to mitigate all voltage issues. The device used to control the series active power filter analyzes the reference voltage to be inoculated by matching the voltage at terminal against the reference voltage.

From the literature review of various works done so far, describing the balanced or unbalanced source conditions by voltage either dip or rise. In this work, different kind of voltage based PQ issues such as sag, swell, transients, interruption and current harmonics are simultaneously mitigated under balanced and unbalanced source conditions as well as linear and non-linear loading conditions.

This article proposes about three-phase three-wire system having voltage source inverter using streamlined control method. The series active filter is maintaining load voltage, dip/swell, harmonics and flickers. The voltage on DC capacitor is maintained constant by parallel active filters. UPQC performances are simulated and verified using MATLAB tool.

The Right Shunt type Unified Power Quality Conditioner (UPQC) with voltage source inverter is acted as a filter and its modelling is deliberated in Section 2. The proposed control method based on hysteresis controller for series and parallel active filter is explained in Section 3. A Simulink model and its detailed result and discussion of the projected control scheme are described in Section4 for two different source conditions. The conclusion of the work is summarized in Section 5.

2. Unified Power Quality Conditioner (UPQC)

This system proposes about the 3-phase source coupled to a power system feeding non-linear load. **Figure 1** shows the UPQC, and it has a dual voltage source inverters having one shunt and other is series active power filter. The series filter is connected between supply and DC common link through a single phase transformers on each phase having turns ratios 1:1. These transformers act as a filter to eliminate the switching ripples actively mitigate from series filter. The voltage source inverters are constructed using IGBT's (Insulated Gate Bipolar Transistors). Synchronous Reference frame theory for parallel (shunt) filter and instantaneous reactive power theory were used as control algorithm for UPQC. A series filter composed of inductance along with capacitance is connected with transformers which mitigate ripple contents [6] [7] [9]-[11].

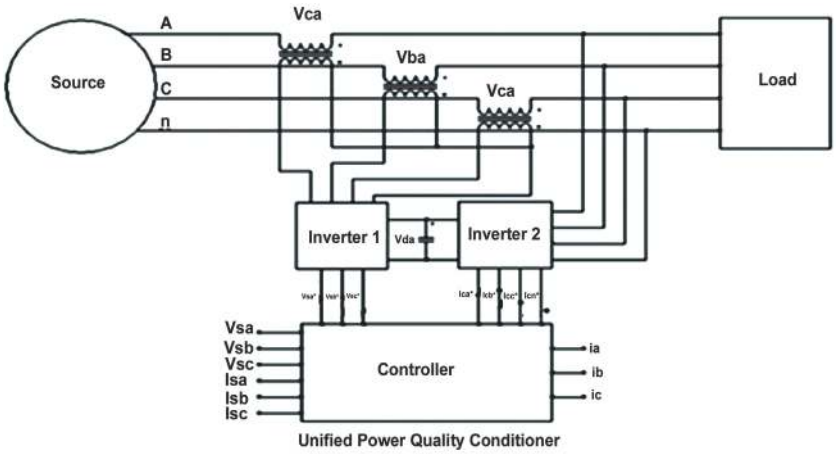

Figure 1. UPQC configuration system.

2.1. Voltage Source Inverter

From olden days, several inverters have been used due to different applications. Voltage Source inverters have wide applications which include drive control strategy, STATCOM, HVDC transmission, and more important is that the interfacing of renewable energy resources. In Power Quality improvement voltage source topology was widely used in SVC's, UPQC's, etc. due fast and dynamic response characteristics [8] [11]. Moreover, in UPQC, voltage source converters certain unbalance DC link voltage due fast short duration operation. The advantages of voltage source inverter are:

-Produce pure sinusoidal current waveforms by reducing unwanted harmonics.

-Lessens the overvoltage produce by refection on extended cable.

-Ripple is two times normal the switching frequency in the first set.

Figure 2 shows the Voltage source inverter (VSI) topology as an active filter .This topology permits switches to tolerate higher DC voltage input on the sites that the switches will not elevate the level of withstanding voltage [6] [10].

2.2. Hysteresis Controller

Conventional control topology for parallel active filter controlled by the hysteresis scheme in voltage source inverter is shown in **Figure 3** and its modeling is defined as follows.

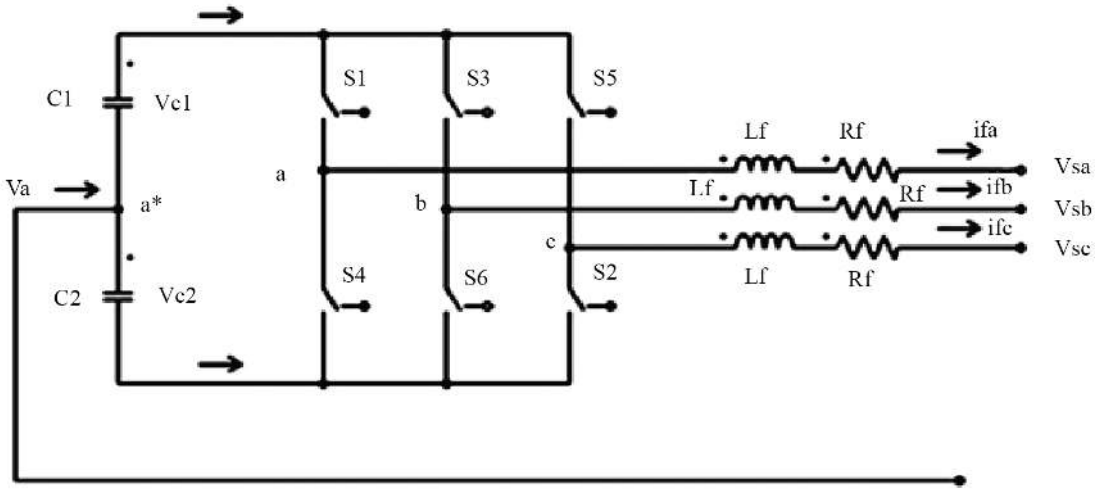

Figure 2. Voltage source inverter.

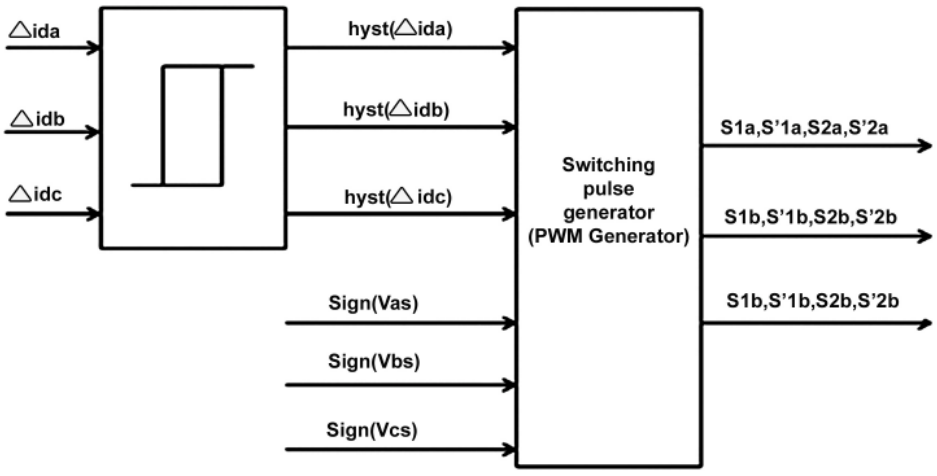

Figure 3. Voltage source inverter hysteresis control.

Three phase voltage is given as:

$$\left.\begin{aligned} V_{as} &= V \cdot \sin(\omega t) \\ V_{bs} &= V \cdot \sin\left(\omega t - \frac{2\pi}{3}\right) \\ V_{cs} &= V \cdot \sin\left(\omega t + \frac{2\pi}{3}\right) \end{aligned}\right\} \tag{1}$$

where V is the line voltage measured across three phases a, b, c correspondingly. Hysteresis Current Controller is helping to identify the mitigated reference current. Then the inside and outside of hysteresis comparator are stated as:

$$hysteresis(\Delta i_{dx}) = \begin{cases} 1, & \text{if } \Delta i_{dx} > h \\ 0, & \text{if } \Delta i_{dx} < -h \end{cases} \tag{2}$$

$$\Delta i_{dx} = i_{dx}^{*} - i_{dx}; x = a, b, c \tag{3}$$

Effective switching pulses are used to generate three different voltages on the AC side of the active filter. Upper and lower voltages existing in the negative and positive phase voltages of the inverter acted as an active filter. In optimistic side voltage produced on two levels, 0 and $U\,l/2$, and the destructive side voltage level produced are, $-U\,l/2$ and 0. A Voltage $-U\,l/2$ is produced in order to increase the level of compensating voltage, whereas the level of voltage on high side 0 is to reduce compensated voltage. Thus, for every half cycle in switching high and low level voltage was selected alternately in order to select compensated current for each thyristor [6] [12]-[14].

$$T_{a1} = sign(V_{as})\left[1 - hysteresis(\Delta i_{da})\right] \tag{4}$$

$$T_{a2} = \left[1 - sign(V_{as})\right] hysteresis(\Delta i_{da}) \tag{5}$$

$$S_a = sign(V_{as}) \cdot hysteresis(\Delta i_{da}) + \left[1 - sign(V_{as})\right] \cdot \left[1 - hysteresis(\Delta i_{da})\right] \tag{6}$$

$$T_{b1} = sign(V_{bs})\left[1 - hysteresis(\Delta i_{db})\right] \tag{7}$$

$$T_{b2} = \left[1 - sign(V_{bs})\right] hysteresis(\Delta i_{db}) \tag{8}$$

$$S_b = sign(V_{bs}) \cdot hysteresis(\Delta i_{db}) + \left[1 - sign(V_{bs})\right] \cdot \left[1 - hysteresis(\Delta i_{db})\right] \tag{9}$$

$$T_{c1} = sign(V_{cs})\left[1 - hysteresis(\Delta i_{dc})\right] \tag{10}$$

$$T_{c2} = \left[1 - sign(V_{cs})\right] hysteresis(\Delta i_{dc}) \tag{11}$$

$$S_c = sign(V_{cs}) \cdot hysteresis(\Delta i_{dc}) + \left[1 - sign(V_{cs})\right] \cdot \left[1 - hysteresis(\Delta i_{dc})\right] \tag{12}$$

where $sign(V_{sx}) = 1$, if $V_{sx} > 0$; or 0 if $V_{sx} < 0$ and $x = a, b, c$.

2.3. Logic Control

Logic control is used in controlling the both Active Power Filters for providing gate signals. The Difference between the injected and reference current gives a reference modulation waveform. The inverter control is determined by two strategies [12] [13]. Determination of intermediate signals V_{im1} and V_{im2}:

- If $E_c \geq 1$ at that time $V_{im1} = 1$
- If $E_c \geq 1$ at that time $V_{im1} = 0$
- If $E_c \geq 1$ at that time $V_{im2} = 0$
- If $E_c \geq 1$ at that time $V_{im2} = 1$

where V_{im1} and V_{im2} are midway signal, E_c is the modulation reference error signal.

3. Control Approach

The control approach for generation of the reference signal is based upon error signal generation and time delay basis for effective compensation of UPQC. The time delay and reference current generation mainly to compensate distortions, unbalance voltages and current during any fault conditions. The proposed control approach is most suitable and effective for mitigating current and voltages during undesirable conditions.The control strategy for parallel and series active filters are shown in **Figure 4** and **Figure 5** respectively.

3.1. Parallel Active Filter Control

The main aim of this control approach is to compensate current harmonics which usually based upon the synchronous reference frame detection method [3]. The control approach is based upon the load currents i_{la}, i_{lb}, i_{lc}, are converted into 3 phase (a,b,c) reference frame and then to two phase ($\alpha-\beta$) stationary reference frame currents i_α and i_β using: [15]-[20].

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{13}$$

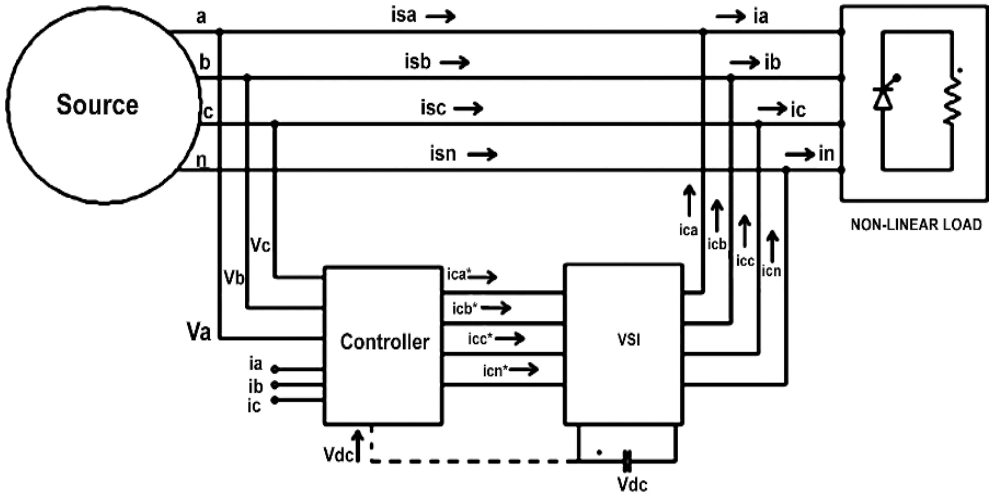

Figure 4. Parallel active filter control strategy.

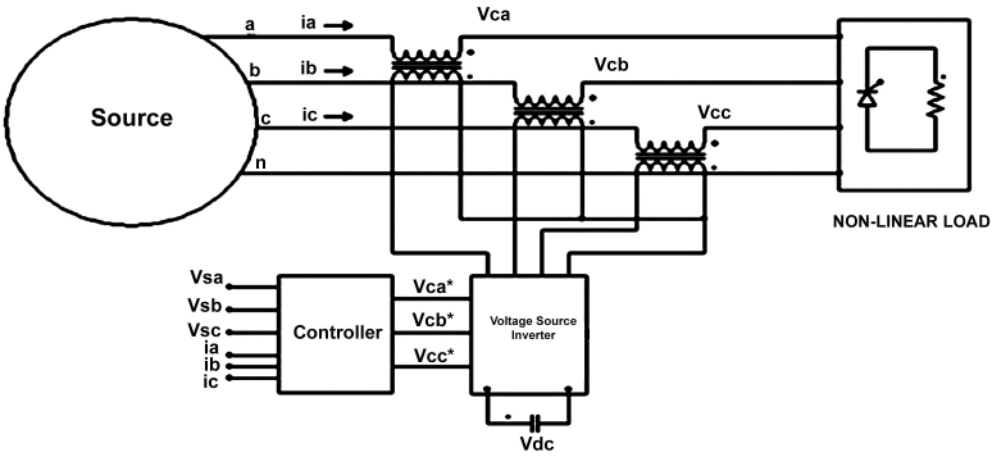

Figure 5. Series active filter control strategy.

By means of phase locked loop (PLL), that make possible for generations of $\cos(\theta_{et})$ and $\sin(\theta_{et})$ from phase voltages such as, V_{as}, V_{bs}, and V_{cs}.

The i_α and i_β currents obtained from (d-q) reference frame are written as:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \sin(\theta_{et}) & -\cos(\theta_{et}) \\ \cos(\theta_{et}) & \sin(\theta_{et}) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{14}$$

The i_d and i_q current are transformed into DC components and using a low pass filter harmonic components are obtained:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \overline{i_d} + \overline{i_d} \\ i_q \end{bmatrix} \tag{15}$$

The equation for the reference current i_α-ref and i_β-ref as,

$$\begin{bmatrix} i_\alpha - ref \\ i_\beta - ref \end{bmatrix} = \begin{bmatrix} \sin(\theta_{et}) & -\cos(\theta_{et}) \\ \cos(\theta_{et}) & \sin(\theta_{et}) \end{bmatrix}^{-1} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{16}$$

$$\begin{bmatrix} i_\alpha - ref \\ i_\beta - ref \end{bmatrix} = \begin{bmatrix} \sin(\theta_{et}) & \cos(\theta_{et}) \\ -\cos(\theta_{et}) & \sin(\theta_{et}) \end{bmatrix} \begin{bmatrix} \overline{i_d} + \overline{i_d} \\ i_q \end{bmatrix} \tag{17}$$

The *abc* reference frame is given as:

$$\begin{bmatrix} i_{a-ref} \\ i_{b-ref} \\ i_{c-ref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_\alpha - ref \\ i_\beta - ref \end{bmatrix} \tag{18}$$

Finally, the compensation currents are obtained as;

$$\begin{cases} i_{acomp} = i_{a-ref} - i_{La} \\ i_{bcomp} = i_{b-ref} - i_{Lb} \\ i_{ccomp} = i_{c-ref} - i_{Lc} \end{cases} \tag{19}$$

In order to mitigate, initially the inverter losses are reduced and then normalize the DC link voltages using a PI voltage controller [21]. The loop produces an equivalent current given as:

$$I_{c,los} = k_p \cdot \Delta U_{DC} + K_i \int \Delta U_{DC} \cdot \mathrm{d}t \tag{20}$$

3.2. Series Active Filter Control

For generating reference frame for series active filter depending upon the PQ theory, we assume phase voltages are symmetric and distorted: [3] [15] [17] [19]. The **Figure 5** shows the series active filter control for generating the filter reference voltage at the time of distortion occurred in the supply voltage.

$$\begin{bmatrix} U_A \\ U_B \\ U_C \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} \sqrt{2} U_n \sin(n\omega t + \theta_n) \\ \sum_{n=1}^{\infty} \sqrt{2} U_n \sin\left[\left(n\omega t - \frac{2\pi}{3}\right) + \theta_n\right] \\ \sum_{n=1}^{\infty} \sqrt{2} U_n \sin\left[\left(n\omega t - \frac{2\pi}{3}\right) + \theta_n\right] \end{bmatrix} \tag{21}$$

The U_n and θ_n are rms voltages and primary phase angle, n is the harmonic order. When $n = 1$, it means that the fundamental 3-phasesupply voltage;

$$\begin{bmatrix} U_A \\ U_B \\ U_C \end{bmatrix} = \begin{bmatrix} \sqrt{2}U_1 \sin\left(\omega t + \theta_1\right) \\ \sqrt{2}U_1 \sin\left[\left(\omega t - \frac{2\pi}{3}\right) + \theta_1\right] \\ \sqrt{2}U_1 \sin\left[\left(\omega t - \frac{2\pi}{3}\right) + \theta_1\right] \end{bmatrix} \tag{22}$$

Equation (10) is converted into reference frame:

$$\begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix} = C_{32} \begin{bmatrix} U_A \\ U_B \\ U_C \end{bmatrix} = \sqrt{3} \begin{bmatrix} \sum_{n=1}^{\infty} U_n \sin\left(n\omega t + \theta_n\right) \\ \sum_{n=1}^{\infty} \mp U_n \sin\left(n\omega t + \theta_n\right) \end{bmatrix} \tag{23}$$

$$C_{32} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{24}$$

The fundamental 3-phase current is framed as:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\left(\omega t\right) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{25}$$

Equation (10) is transformed to ($\alpha - \beta$) reference frame:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = C_{32} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \sin\left(\omega t\right) \\ -\cos\left(\omega t\right) \end{bmatrix} \tag{26}$$

The DC components are obtained by passing P and Q in low pass filter (LPF), then

$$\begin{bmatrix} \overline{p} \\ \overline{q} \end{bmatrix} = \sqrt{3} \begin{bmatrix} U_1 \cos\left(\theta_1\right) \\ U_1 \sin\left(\theta_1\right) \end{bmatrix} \tag{27}$$

From the above equation the transformation is made as:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} U_\alpha & U_\beta \\ U_\beta & -U_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix} \tag{28}$$

The DC mechanisms of p and q as:

$$\begin{bmatrix} \overline{p} \\ \overline{q} \end{bmatrix} = \begin{bmatrix} U_{\alpha f} & U_{\beta f} \\ U_{\beta f} & -U_{\alpha f} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} U_{\alpha f} \\ U_{\beta f} \end{bmatrix} \tag{29}$$

The fundamental reference frame is given as:

$$\begin{bmatrix} U_{\alpha f} \\ U_{\beta f} \end{bmatrix} = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix}^{-1} \begin{bmatrix} \overline{p} \\ \overline{q} \end{bmatrix} \tag{30}$$

The three-phase fundamental voltages are given as:

$$\begin{bmatrix} U_{Af} \\ U_{Bf} \\ U_{Cf} \end{bmatrix} = C_{23} \begin{bmatrix} U_{\alpha f} \\ U_{\beta f} \end{bmatrix} = \sqrt{2} \begin{bmatrix} U_1 \sin(\omega t + \theta_1) \\ U_1 \sin\left[\left(\omega t - \frac{2\pi}{3}\right) + \theta_1\right] \\ U_1 \sin\left[\left(\omega t - \frac{2\pi}{3}\right) + \theta_1\right] \end{bmatrix} \tag{31}$$

$$C_{23} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \tag{32}$$

4. Simulation Results and Discussion

4.1. UPQC Performance for Voltage Compensation for Balanced Source Voltage

Here both shunt and series power filters are put into operation at different time instants. Considering nonlinear load for simulation source parameters considered are as follows. Input source voltages: V_a = 230 V, V_b = 230 V, V_c = 230 V. The load element and filters with VSC has been built using MATLAB /SIMULINK. The following observations are drawn from the simulation outcomes. The control algorithm provides reactive and harmonic power compensation.

Here balanced source voltage is considered and after compensation balanced source current is prescribed in following results. **Figure 6** shows the three phase balanced source voltages which is being supplied to the system. **Figure 7** depicts the three phase error voltage which is generated due to the load connected to UPQC.

At time instant for t = 0 to 0.05 sec system is working without any issues, which does not require any compensation and after t = 0.05 voltage dip is introduced, in this time period series filter comes into operation for compensating voltage harmonics. The voltage dip occurs till 0.1 sec, the system is again at normal working condition. Then a short time interruption is led which occur from t = 0.14 to 0.15 sec, following the interruption

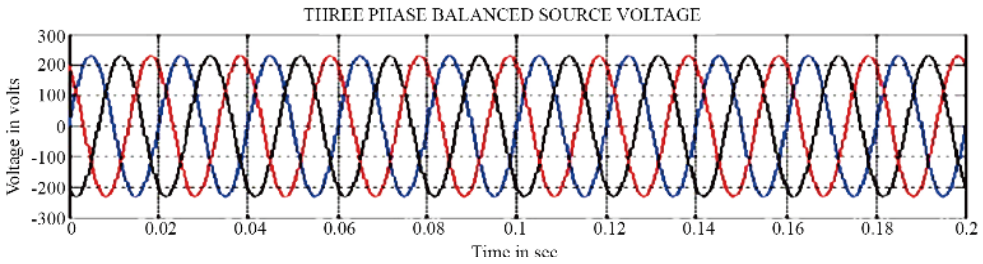

Figure 6. Three phase balanced source voltage.

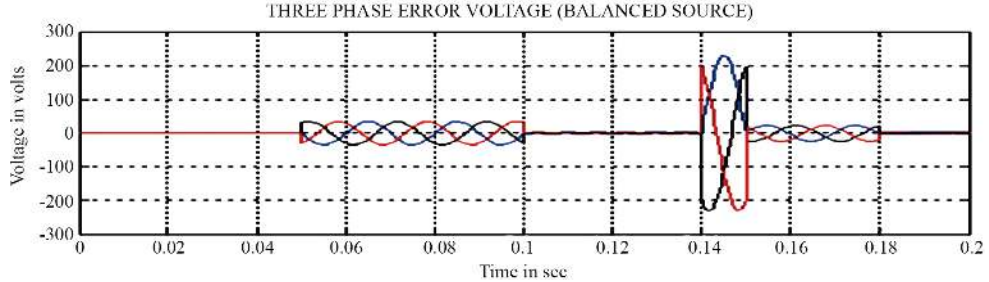

Figure 7. Three phase error voltage.

voltage swell is hosted from t = 0.15 to 0.18 sec at that time shunt filter comes into operation for compensating harmonics due rise in voltage, then the system voltage come back to its normal working condition.

In **Figure 8** voltage from t = 0 to 0.05 sec remain zero because of normal operation at time 0.05 sec voltage dip arise the reference voltage generator generates required amount of voltage to compensate dip which occur till 0.1 sec. At t = 0.14 sec there is a small interruption for 0.01 sec so reference voltage generator generates the necessary voltage to maintain source voltage as normal. At t = 0.15 sec there is 10% rise (V_s = 253 volt) in voltage till 0.18 sec. So reference voltage generator generates the required voltage in the opposite direction for mitigation.

Three phase actual (generated) error voltage which is being added to the system error voltage to obtain the compensated source voltage of 230 volts for an entire operating period, it is shown in **Figure 9**.

In **Figure 8** and **Figure 9** there are few overshoots at t = 0.5 secs, t = 0.1 secs, t = 0.14 ecs, t = 0.18 secs respectively. This overshoots are due to sudden injection of reference components (voltage/Current) while mitigating the *pq* issues like sag, swell and etc., in the respective fault points. The duration of this overshoot exist for few milli or micro seconds. These overshoots can be reduced by selecting suitable values of L and C of the active filters and its controllers in the proposed UPQC.

The supply current before compensation is non-sinusoidal due to the non-linear load connected to the system which is shown in **Figure 10**.

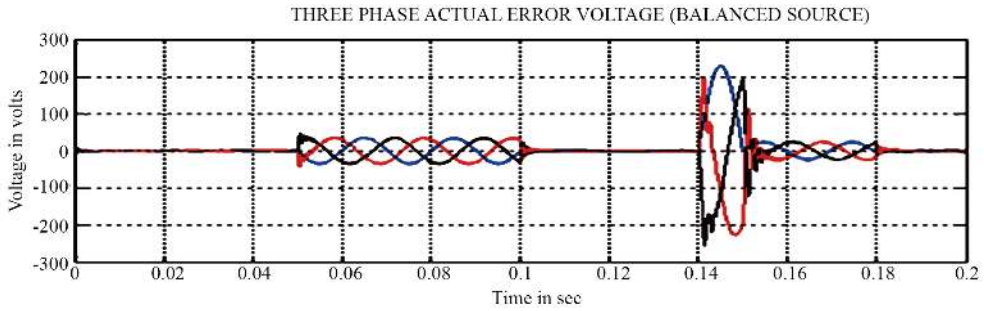

Figure 8. Three phase actual error voltage.

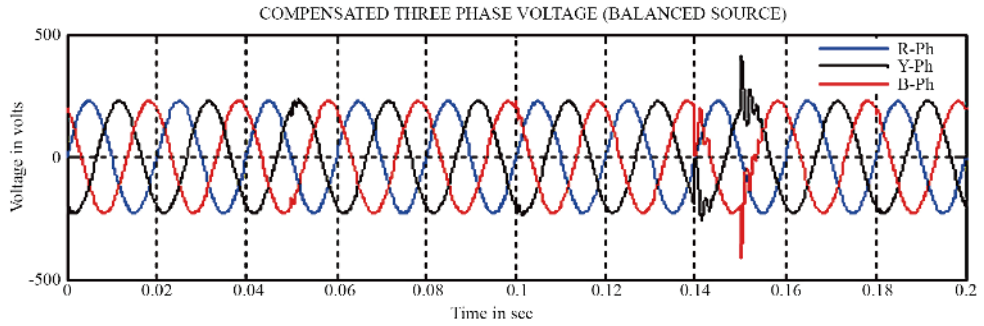

Figure 9. Compensated Source voltage after compensation.

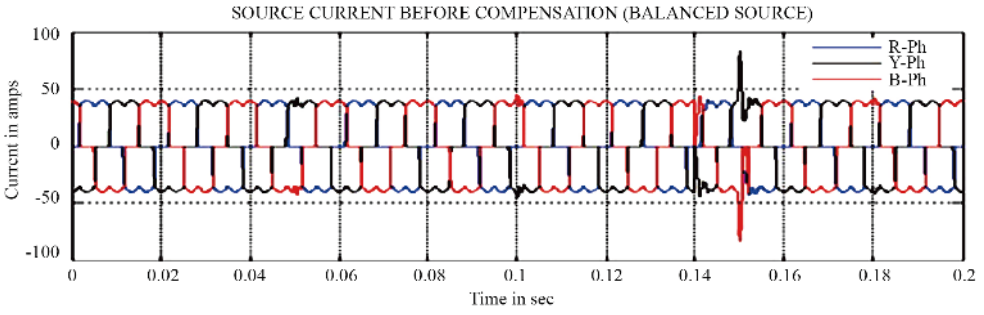

Figure 10. Source current before compensation.

The generated reference current for compensation using hysteresis controller is exactly follows the reference filter current shown in **Figure 11**. It is generated by the synchronous reference current generator and is presented in **Figure 12**.

The generated reference current **Figure 12** is injected into the source current at the load terminal (normally at the point of common coupling). It results sinusoidal current which is in phase with the source voltage shown in **Figure 13**. Hence the Total Harmonic Distortion (THD) is improved from 30.59% to 0.83%.

There is a small disturbance in time t = 0.05, 0.1, 0.14 and 0.15 respectively, which is due the operation of controller during the mitigation process of dip, interruption and swell.

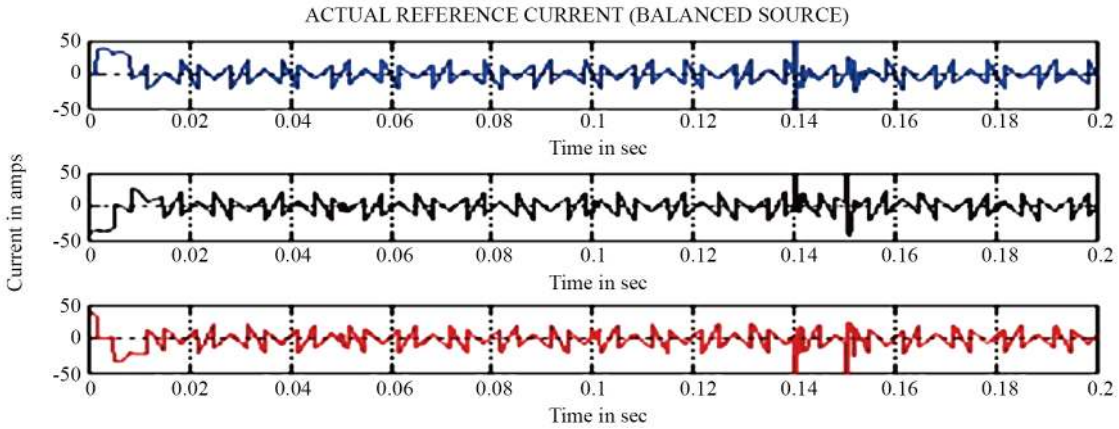

Figure 11. Filter reference current.

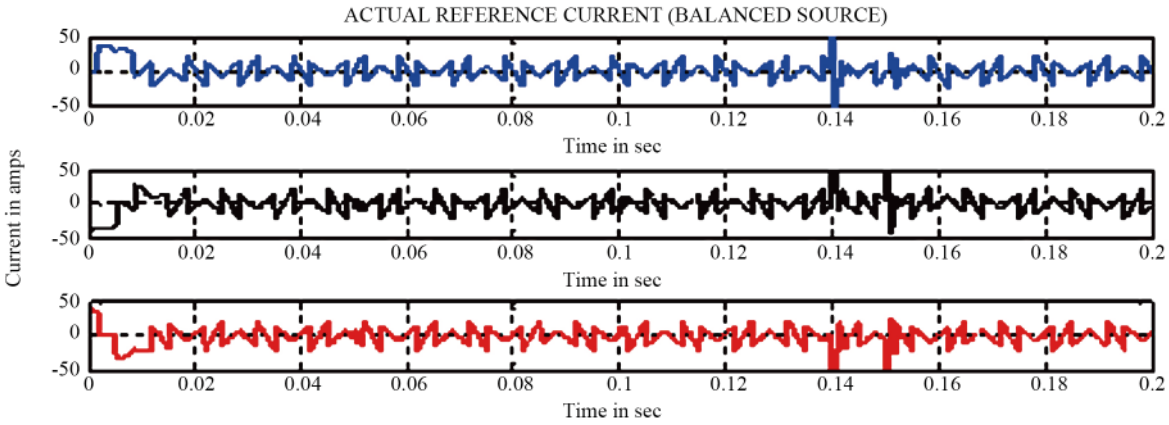

Figure 12. Actual filter current.

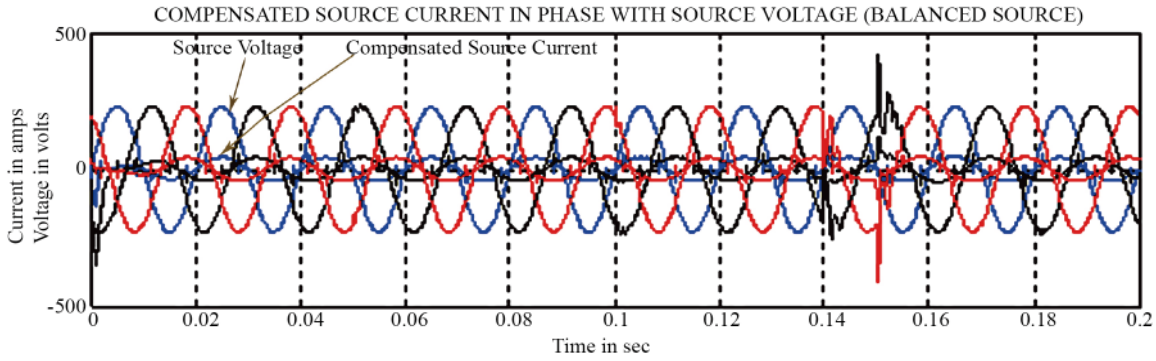

Figure 13. Compensated source voltage in phase with the source current after compensation.

4.2. UPQC Performance for Voltage Compensation for Unbalanced Source Voltage

Considering same simulation load parameters, but having unbalanced sources are as follows. Input source voltages: V_a = 230 V, V_b = 220 V, V_c = 230 V.

From t = 0.05 sec voltage dip is introduced, in this time period series filter comes into operation for compensating voltage harmonics. Then a short time interruption is led which occur from t = 0.14 to 0.15 sec, following the interruption voltage swell is hosted from t = 0.15 to 0.18 sec at that time shunt filter comes into operation for compensating harmonics due rise in voltage, then the system voltage come back to its normal working condition.

Here unbalanced source voltage is considered and after compensation balanced source current is prescribed in following results. **Figure 14** shows the three phase unbalanced source voltages which are supplied to the system. **Figure 15** and **Figure 16** are the error voltage and its corresponding actual error voltage generated by using proposed control strategy.

Three phase actual (generated) error voltage shown in **Figure 16**, which is being added to the system error voltage to obtain the compensated source voltage of 230 volts for an entire operating period, it is shown in **Figure 17**.

Figure 18 shows the supply current before compensation and which is in non-sinusoidal due to non-linear

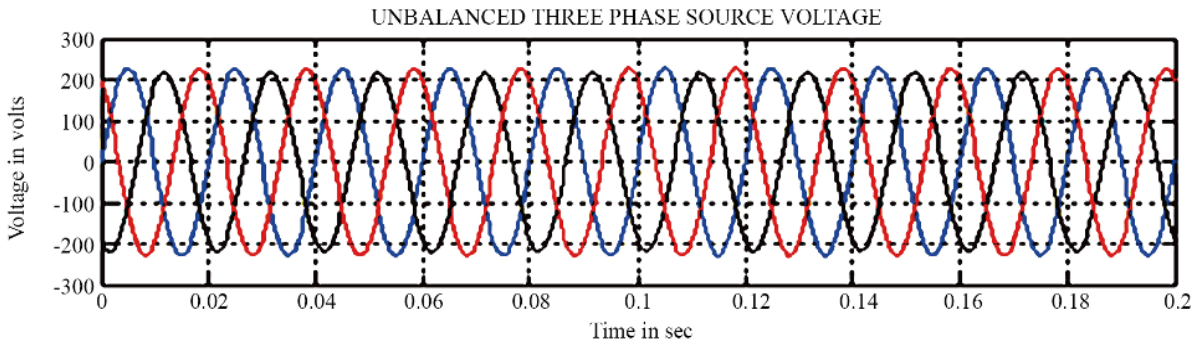

Figure 14. Unbalanced source voltages.

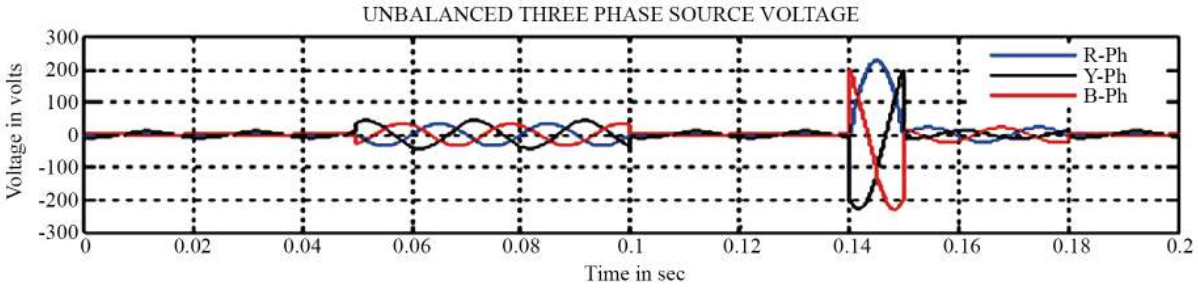

Figure 15. Three phase error voltages.

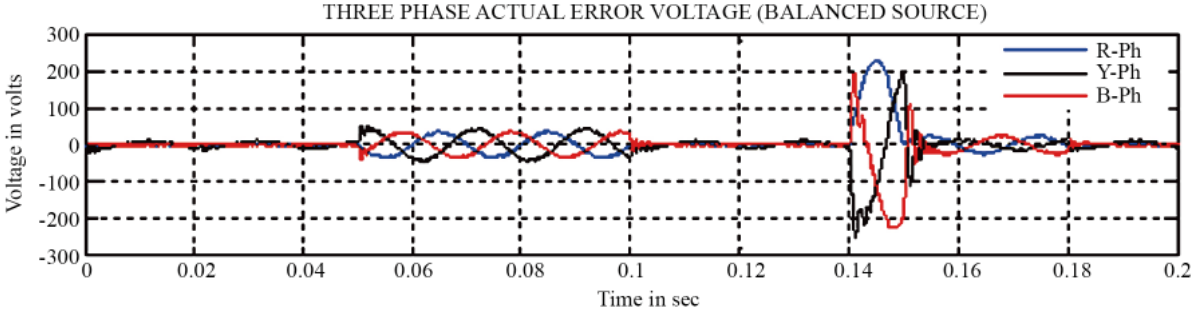

Figure 16. Three phase actual error voltages.

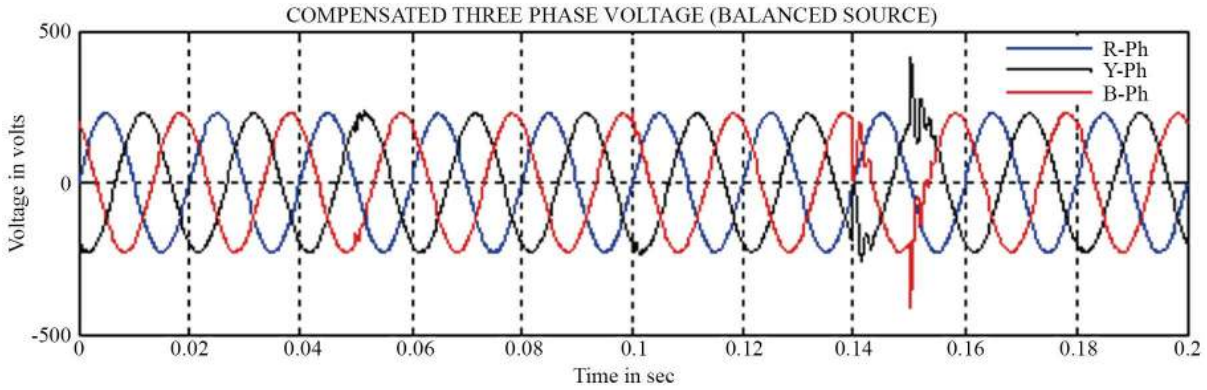

Figure 17. Compensated three phase source voltages.

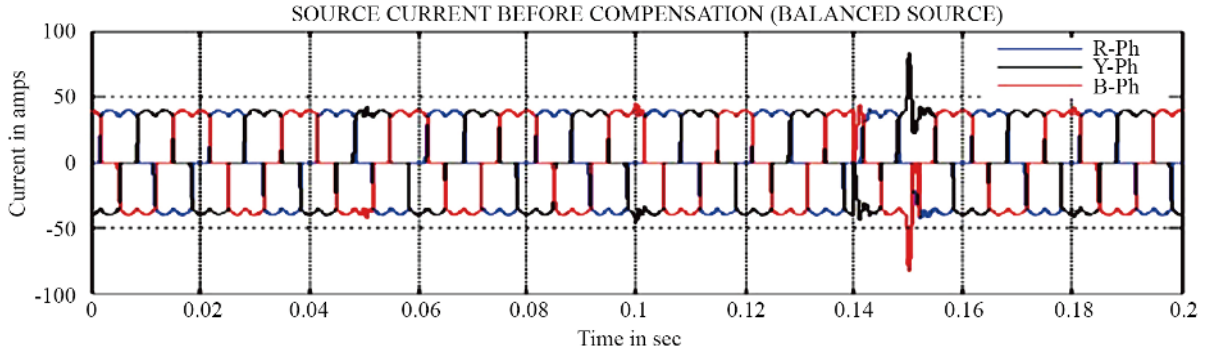

Figure 18. Uncompensated source current.

load connected to the system. The actual filter current generated by the synchronous reference current generator using hysteresis controller for the connected non-linear load is shown in **Figure 20**. It is exactly matched with source reference current shown in **Figure 19**.

Figure 20 shows compensated source voltage in phase with the source current which is obtained by injection of generating reference current to source current at load terminal. There is a small ripple in the compensated current waveform shown in **Figure 21** is due to the injection of reference current and voltages at various points at the point of common coupling. By designing a suitable filter component, the short duration ripples are quenched quickly.

The above tasks are analyzed by using MATLAB Simulink for two different operating conditions such a balanced and unbalanced source voltage conditions. The amount of harmonic distortion reduction is up to the benchmark level and its results are tabulated in **Table 1**. **Table 1** shows the numerical statistics of the THD values under before and after compensation of the current in the proposed system. The THD improvement in both operating conditions is more satisfactory with the standard of IEEE value.

5. Conclusion

For the improvement of power quality issues in the source current due to harmonics delivered by the nonlinear loads, a new UPQC configuration is constructed. The voltage source inverter topology is proposed to mitigate the issues by acting as a filter. The control approach is based on the power instantaneous method for series filter and synchronous reference frame topology for parallel filter is proposed. UPQC configuration is proposed and validated using MATLAB/SIMULINK software. UPQC configuration is satisfactory observed for different power quality issues such as current harmonics mitigation, voltage sag and voltage swell and unbalance compensation. Anyhow, in the proposed work the performance of UPQC has been agreed for various power quality mitigations like dip, swell and interruption under balanced and unbalanced condition of the considered nonlinear load. The improvement of THD in the source current is improved from 30.59% to 0.83% for balanced source voltage and unbalanced source voltage THD value is improved from 42.05% to 0.92%. Thus the prospective

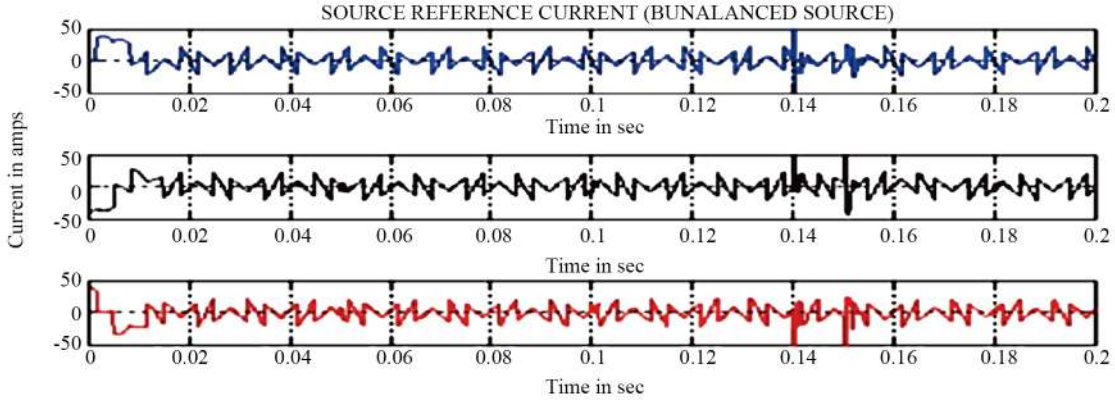

Figure 19. Reference filter current.

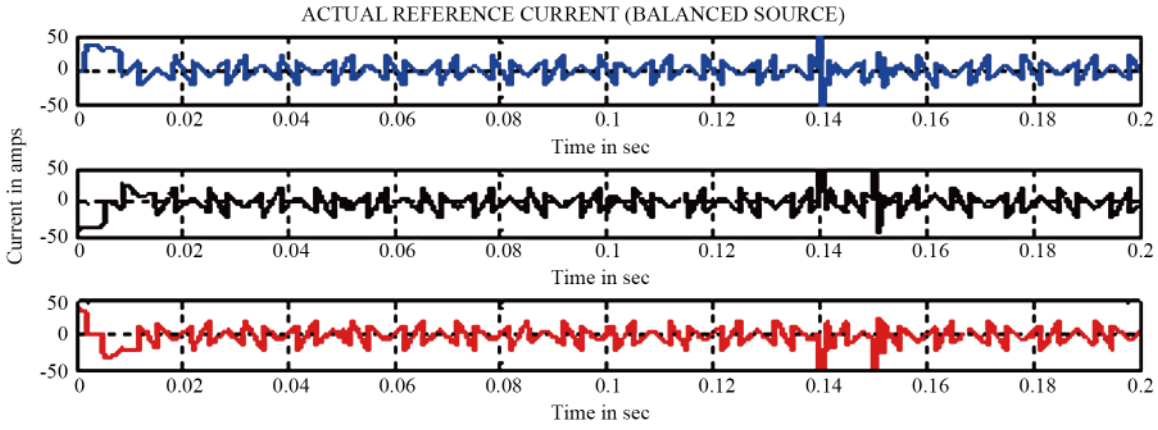

Figure 20. Actual Reference current.

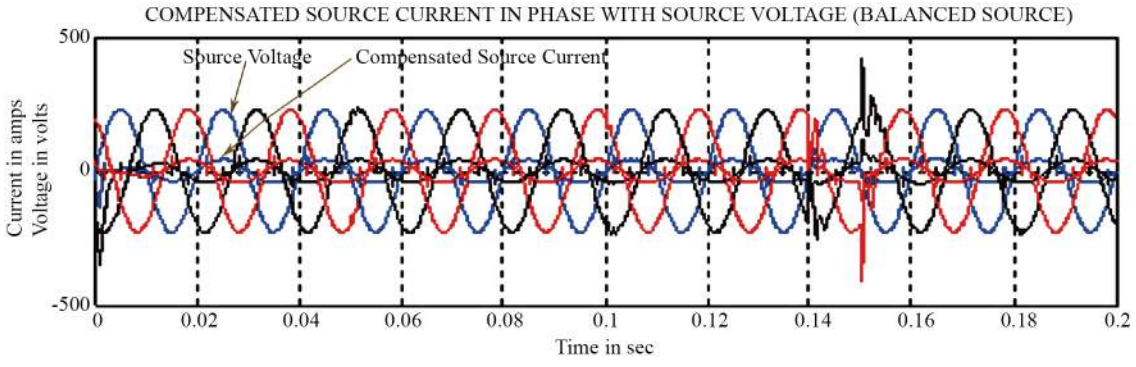

Figure 21. Compensated source current in phase with source voltage.

Table 1. Table of comparison of results before and after compensation.

S.No	Total Harmonic Compensation	Before Compensation	After Compensation
1	Balanced Source Voltage	30.59 %	0.83%
2	Unbalanced Source Voltage	42.05%	0.92%

performance of the UPQC control approach could be replaced by intelligent control strategy and it is useful for potential usage of UPQC under many circumstances.

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