Mater. Res. Soc. Symp. Proc. Vol. 970 © 2007 Materials Research Society 0970-Y01-02

Recent Advances in 3D Integration at IMEC

Piet De Moor, Wouter Ruythooren, Philippe Soussan, Bart Swinnen, Kris Baert, Chris Van Hoof, and Eric Beyne
IMEC, Kapeldreef 75, Leuven, B-3001, Belgium

ABSTRACT

IMEC is focusing its 3D-integration technology developments in 3 distinct directions: 3D-System-in-a- Package (3D-SiP), 3D-Wafer-Level-Packaging (3D-WLP) and 3D-Stacked-IC (3D-SiC). First, the background of these separate approaches will be given. Next the materials and technologies involved, the typical characteristics and the ongoing developments will be discussed. Finally, the roadmap for the 3D-integration in IMEC will be presented.

INTRODUCTION

Advantages of 3D integration

A large number of good reasons to use 3D integration are present today [1-3]. Summarizing, the main drivers are: performance enhancement and form factor reduction.

In terms of performance, 3D stacked dies can benefit of (relatively) short interconnects between e.g. functional blocks, as compared to fairly long horizontal global interconnects on a classical CMOS chip. Even more important (and extending the field of CMOS by far) is the concept of heterogeneous integration: instead of combining different technologies on one die (which is in general costly – if feasible at all), dies emerging from different technologies can be assembled using short interconnects. This has two major advantages: first, due to the drastically reduced parasitic capacitance, higher speed and lower power consumption is obtained. Moreover, the two (or more) different technologies can be optimized independent in terms of technology and specifications. Historical examples where this vertical integration is used are detector systems, such as X-ray or infrared detectors – often using non-Si materials - hybridized on readout circuits. But there are many other applications of heterogeneous integration, such as logic and memory, MEMS sensors or actuators and read-out electronics.

The achievable form factor reduction using 3D-integration is obvious: today's advanced thinning technology enables Silicon thinning to less than 50 um, enabling very thin yet performing systems. Moreover, as Si becomes flexible at such dimensions, the fabrication of flexible and even stretchable devices become feasible.

Risks

Apart from the extra cost involved in 3D-integration, there are a number of risks that could hamper the break-through of 3D-integration. As in standard packaged systems, the reliability needs to be addressed. Moreover, most 3D integrated systems use aggressive substrate thinning, possibly resulting in (catastrophic) influence on the device properties. There are a number of yield considerations as well – which translate directly into cost. Finally, the thermal management of a 3D stack will require even more attention than that of a classical package.

Reliability of 3D stacks depends very much on the design, materials and technology used. The problems are however quite similar to the standard packaging and hybridization reliability issues: mismatch of coefficient of thermal expansion of different materials, and as a consequence stress build-up and failure through e.g. delamination, crack initiation [4]. Careful design driven by thermo-electrical simulations can solve most of the problems.

Thinning induced damage in Si, and its consequences for the device properties are a more fundamental limitation. A typical technique such as backside grinding is known to produce damage at the back side of the wafer, both at the surface as well as deeper into the bulk Si, depending on the type of grinding wheels. When thinning to a final thickness of less than 50 micron, properties of devices at the front side may start changing. To complicate things, this influence is very dependent on the type of devices and the technology used to produce them. Further fundamental study of the induced damage (and how to avoid or remove it) is required. For the flexible or stretchable devices, the variable nature of the induced stress, as well as damage propagation needs to be understood in order to be able to provide reliable products.

Finally, yield assessment is even more important than in traditional 2-dimensional systems. Evidently, the vertical interconnect yield must be very high, i.e. the stacking technology must be controlled very well. But this is only one part of the compound yield. In order to produce a fully operational 3D-stack, also the individual components must be yielding. This leads to a trade-off between two different approaches to realize the vertical interconnections: wafer-to-wafer bonding or die-to-wafer (or die-to-die) bonding. When the yield of the individual components is very high (or when this yield cannot be determined easily), the wafer-to-wafer bonding is the most economically solution. However, if the component yield is not close to 100 %, the die-to-wafer approach rapidly gains interest in terms of compound yield (and hence cost): it makes no sense to have a triple stack device with excellent interconnection yield, and only 2 (out of 3) operational dies.

Thermal management in current technologies and packages is already today a challenge. Stacking different dies in a very small volume using extreme substrate thinning will create overheating in a number of applications. Enhancing the external cooling as well as optimizing the device design taking into account the power dissipation will help, but might not be sufficient. This means that at the technology side solutions must be provided. This can be achieved in minimizing the thermal resistance between the different layers, by e.g. decreasing the polymer glue thickness or providing dummy electrical interconnects [5].

3D integration approaches

When discussing the multiple advantages of 3D integration one should not forget one possible show stopper, which is increased cost! Hence, it is extremely important to use cost-effective process technologies. Moreover, by using processes which are available in commercial foundries, large scale production becomes possible, resulting in low cost. Hence the many different possible schemes for 3D integration should be 'filtered' into categories which are using different technology platforms [3]. "Back-end" packaging services typically are equipped with advanced wire bonding, printed circuit board (PCB) technology and high throughput pick and place and flip-chip integration. On this platform, 3D-System-in-a-package (3D-SiP) applications can be produced. If the application requires a higher density of vertical interconnects, typically some processing on wafer level is required. Here the main difference is whether this is done in a post-processing way, or whether this involves changing the initial process flow of the devices. Foundries supplying wafer-level-packaging technology (for e.g. integrated passive devices) are positioned well to post-process on finished wafers from different sources. They can provide the necessary technology and equipment for the 3D-Wafer-Level-Packaging (3D-WLP) approach. For the highest vertical interconnect density, one needs to change the process flow of devices. This can be typically done only in (CMOS-)foundries. This type of vertical integration is the 3D-Stacked-IC (3D-SiC). The 3 different 3D approaches will be discussed in more technical detail in the next sections.

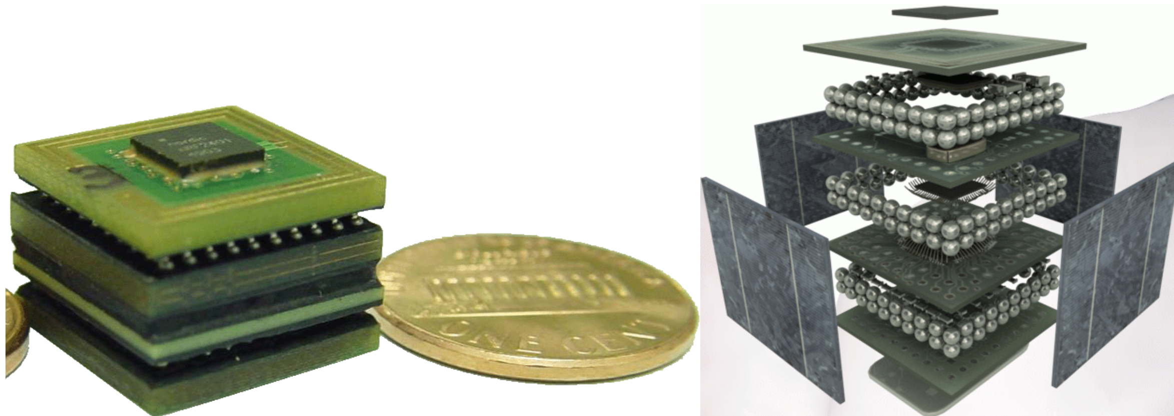

Fig. 1: Example of a 3D-SiP assembly: a EEG/ECG wireless node within a volume of 1 cm^3.

3D-SYSTEM-IN-A-PACKAGE (3D-SiP)

The 3D-SiP technology typically uses solder balls to stack different subsystems (typically PCB's) containing individual packaged dies and/or components. A wide variety of assembly techniques can be used: e.g. wire bonding, flip-chip, underfill materials. In order to enable the use of thick components on individual layers, often multiple solder ball interconnects are required [6]. Typical vertical interconnection densities are rather modest: 2-3/mm in peripheral interconnects, 4-11/mm^2 when using area redistribution.

The main advantage of this approach is the use of commercial available and thus generic assembly technology, leading to the excellent manufacturablility. Moreover, the different layers

can be tested separately before final assembly, resulting in a good compound yield. A lowlight is the lack of standardization in package types and dimensions.

The main application for 3D-SiP assemblies are intelligent wireless sensor nodes. The different layers possibly contain totally different functionalities: sensors, actuators, batteries, power scavengers, read-out electronics, wireless tranceiver, antenna, … Once assembled, a complete system is obtained. Fig. 1 shows the Electro Encefalogram/Electrocardiogram (EEG/ECG) 3D-SiP demonstrator that has been assembled in IMEC. It combines multi-channel preamplifiers, digitalization and wireless transmission of the signals in a volume less than 1 cm^3 [6].

A more advanced 3D-SiP technology consists of embedding pre-thinned dies into PCB's using lamination techniques. The contacts to the die are made by laser micro vias and Cu plating. The interconnect density obtained is basically limited by the PCB manufacturing technology.

3D-WAFER-LEVEL-PACKAGING (3D-WLP)

In the 3D-WLP approach processing is done at wafer level, but after completion of the normal wafer processing, i.e. post the IC passivation. As a consequence, there is no interference of the 3D integration process with the device processing. However, the post-processing approach limits to some extent the maximum vertical interconnect density, which is 1-50/mm when using peripheral interconnects and 100- 2500/mm^2 when using area redistribution. Two different technologies are being developed at IMEC: die stacking and thin film embedding (Fig. 2). 3D-WLP applications include 3D sensor integration and 3D RF(-MEMS) stacks, as well as flexible and/or stretchable electronics for e.g. on the body applications when using thin film embedding technology.

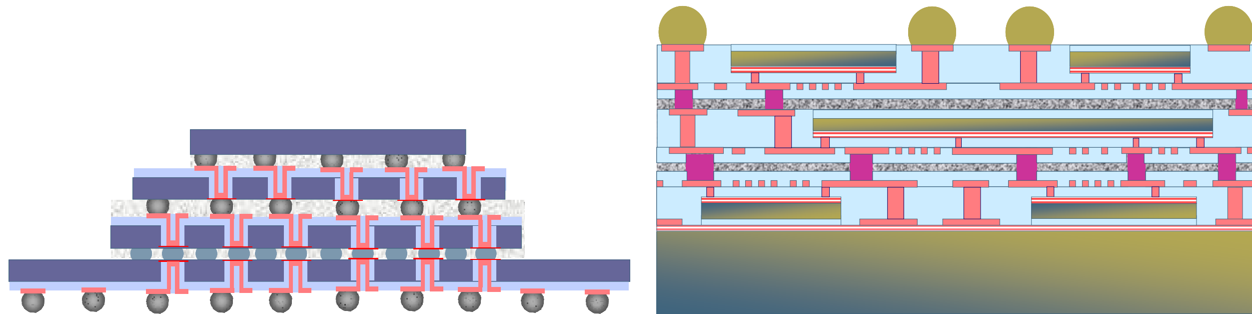

Fig. 2: The different approaches in 3D-WLP integration: die stacking (left) and ultra thin chip embedding (right).

Both the die stacking and the thin film embedding approach require thinning of the Si substrate to 100 micron and even down to 15 micron. As Si becomes flexible and highly fragile, we process these wafers after gluing them on a carrier wafer. Critical process parameters are the total thickness variation of the carrier substrate, the glue layer and the grinding process [7]. In the die stacking flow, after thinning to approximately 100 micron, 50-100 micron wide vias are etched in the Si, and subsequently the insulator material is etched in order to reach the contact pad. Next an insulator material is being deposited and patterned. Finally, a seed layer is

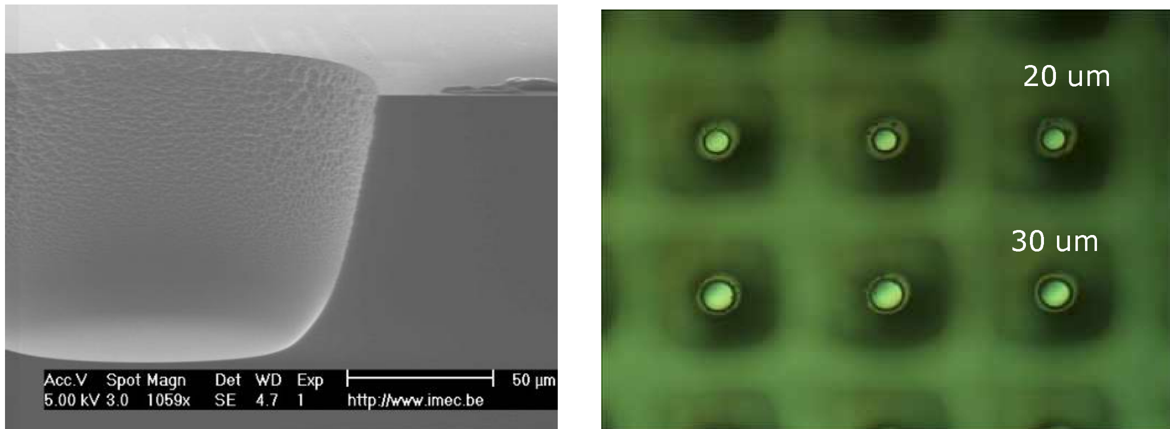

Fig. 3: 3D-WLP technology results: sloped via etch (left), patterning of resist inside a 50 um wide via using spray coating (right).

sputtered, followed by Cu plating [8]. As opposed to many other 3D technologies, we are not filling the vias completely with Cu, as this may cause reliability issues due to the large mismatch in CTE with Si [9]. Optionally, the via can be filled using a polymer such as BCB. More detailed information on critical processes such as the sloped via etching and the insulator patterning using resist spray coating are found in [10,11]. For the integration of different wafers or dies containing through wafer vias, typically solder bumps are used. Traditional solder materials such as Sn alloys or In can provide very high densities [12] but have the disadvantage of being reflown multiple times when assembling a multiple die stack. This problem can be overcome when using transient liquid phase bumps. These bumps contain initially a small amount of solder material, but during the flip-chip assembly the solder material is completely consumed by the UBM material, resulting in an intermetallic compound. The latter has the advantage of a having a higher melting point than the initial solder material. TLP bumps based on Co-Sn and Cu-Sn intermetallics are under investigation at IMEC.

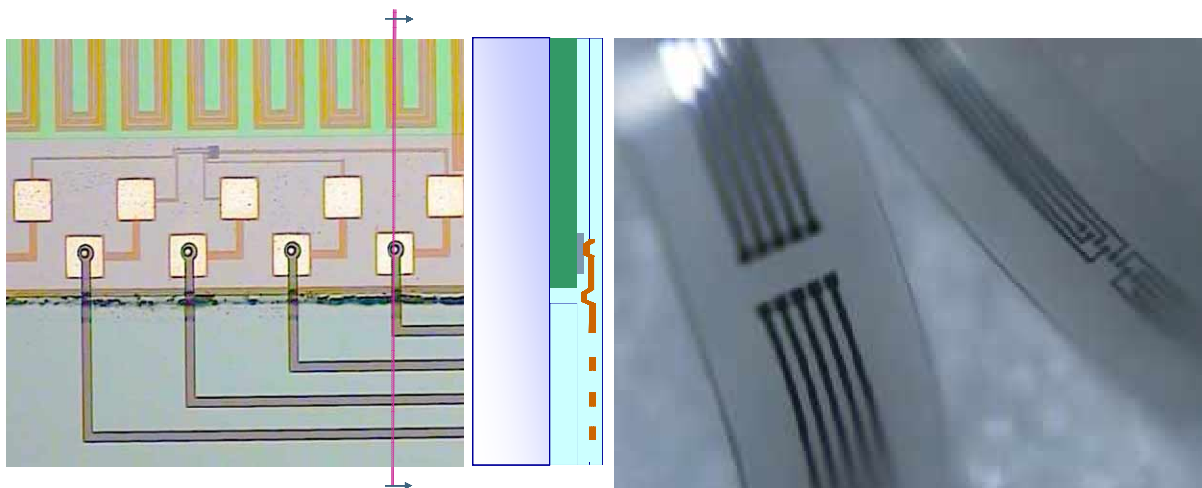

Fig. 4: Examples of 3D-WLP ultra thin die embedding: a 15 um thin die is transferred to a host substrate and electrically connected (left), metal interconnects embedded in flexible Silicone (right).

The thin film embedding process uses thin film technology using BCB dielectric and electroplated Cu to interconnect embedded dies of a thickness of ~ 15 micron. Critical processes involved are the singulation of extreme thin dies and the die transfer from the carrier to the final host substrate. Fig. 4 shows an example of an embedded and electrically interconnected thin die [13]. When applying a sacrificial layer at the beginning of this process, and a sacrificial layer etch at the end, flexible electronics with embedded active dies are obtained [14].

3D-STACKED-IC (3D-SIC)

The 3D-SiC process is a part of the device wafer fabrication: the 5 micron wide vias are etched 25 um deep in the Si and Cu electroplated after completion of the front end of line (FEOL), and before starting the back-end of line (BEOL) process. This requires full compatibility of these processes with the normal device process, but has the advantage not to consume any area in the BEOL (Fig. 5). Vertical interconnection densities of up to $10000/mm^2$ are possible. After the completion of the device process, the wafers are glued to a carrier wafer, and thinned down to ~ 25 um. A combined Si and CMP process [15] reduces further the thickness and exposes and planarizes the bottom of the vias. After an additional Si recess etch, ~ 1 micron Cu "nails" are ready to be bond to the Cu landing pad on the next wafer (or die). We have been investigating the process window of Cu-Cu thermocompression bonding as a function of the bonding temperature, bonding force and Cu surface preparation [16]. The best Cu-Cu bonding results are obtained at a bonding temperature of 300 – 350C using a citric acid Cu surface preparation. Yielding daisy chains of up to 10000 vias have been obtained [17]. A thermal analysis of the 3D-SiC assembly is given in [5].

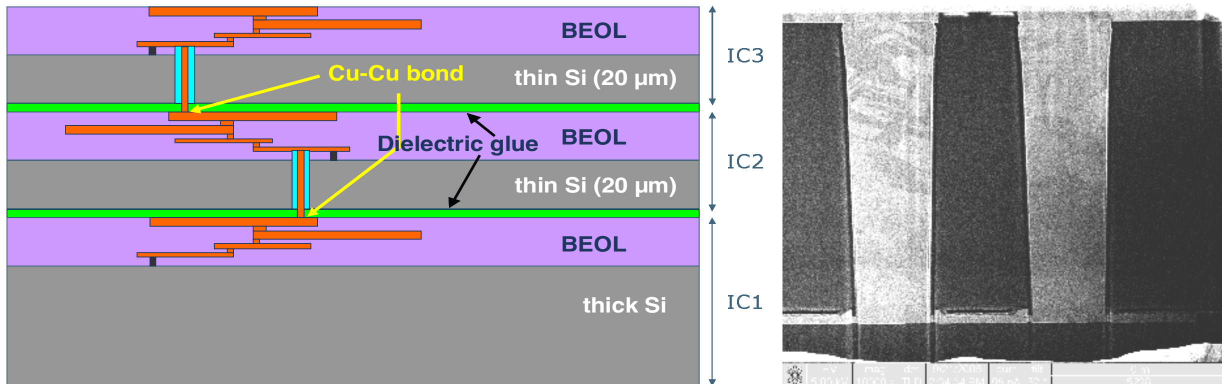

Fig.5: 3D-SiC integration: scheme (left) and demonstration of daisy chains using Cu-Cu interconnects (right).

IMEC 3D ROADMAP

Figures 6 and 7 show the IMEC roadmap for 3D integration and its associated specifications such as via dimensions and densities [3]. It is clear that as a function of time the interconnect density and therefore the interconnect complexity will increase – for the 3 different 3D integration approaches.

In 3D-SiP increasing the vertical interconnect density is difficult. The vertical dimension however can be still reduced by going from wire bonded subsystems to Chip Scale Package (CSP) type of interconnections. Finally, the most compact form factor and the highest density can be achieved when embedding the dies into the PCB boards.

When higher vertical via interconnect densities are required, the 3D-WLP technology is required. For die stacking, the via density is increased by reducing the wafer thickness. Multiple dies will be stacked on top of each other resulting in intelligent heterogeneous systems within a very small volume. A basic design limitation in die stacking is the typical 'wedding cake' form factor: is it difficult to put a (very thin) die on top of a smaller die. This disadvantage is not present in the die embedding approach. Multiple dies with different dimensions can be embedded next to each other and on top of each other. The latter will be possible thanks to the stacking of Ultra Thin Flex Substrates (UTCF) containing embedded dies. In order to overcome the somewhat limited vertical interconnect density on the embedded dies, the final goal is to embed thin dies with through wafer vias.

At the cost of interfering in the device (e.g. CMOS) processing, the 3D-SiC approach offers the highest interconnect density. Again stacking of multiple dies in this manner suffers from the 'wedding-cake' limitation. Therefore the ultimate 3D interconnect performance, i.e. minimal size and maximal vertical interconnection density, is obtained when embedding dies with 3D-SiC through wafer vias in flexible substrates, and subsequently stacking them.

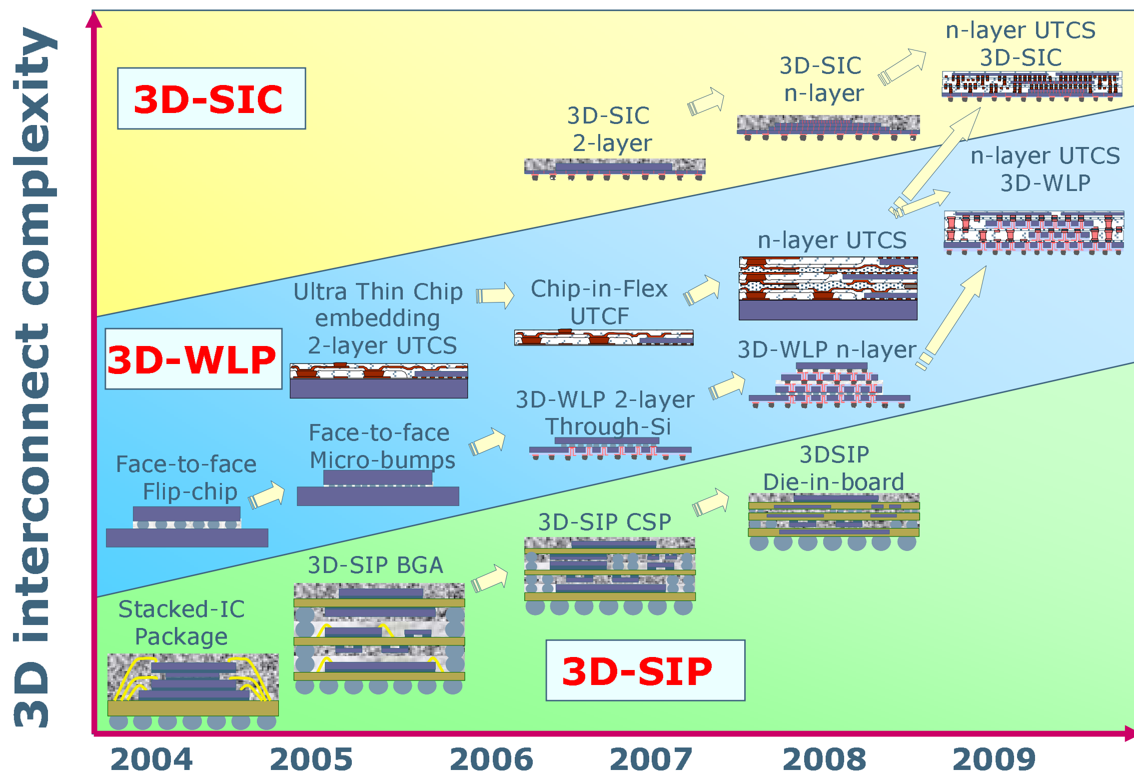

Fig. 6: The IMEC roadmap for 3D integration.

	3D-SIP	3D-WLP		3D-SIC
Technology	Package interposer	WLP, Post-passivation		Si-foundry, Post FEOL
3D interconnect	Package I/O	UTCS Embedded die	Si-through vias	Si-through "Cu nail" vias
Intercon. Density	'package-to-package'	'around' die	'through' die	'through' die
Peripheral	2 - 3 /mm	10 - 50 /mm	10 - 25 /mm	25 -100 /mm
Area-array	4 - 11/mm²	100 -2.5k/mm²	16 - 100/mm²	400-10k/mm²
3D Si Via pitch	-	-	40 – 100 µm	< 10 µm
3D interconnect pitch	300 – 500 µm	20 – 100 µm	-	-
3D Si Via diameter	-	-	25 - 100 µm	1 - 5 µm
Die thickness	> 50 µm	10 - 20 µm	50 - 100 µm	10 - 20 µm

Fig. 7: Typical dimensions of the different 3D integration approaches.

CONCLUSIONS

The breakthrough of 3D integration in industrial products will depend on the combination of enhanced performance, reliability and low cost. These considerations have already to be taken into account during the technology development. IMEC's 3D integration approaches and roadmap focus on 3 different technologies, each closely linked to a technology platform: 3D-SiP, 3D-WLP and 3D-SiC. Each of them has a different vertical interconnect density and hence different applications. While the 3D-SiP is using state-of-the art technology, it is closest to the market. 3D-WLP and 3D-SiC technologies require further developments, but first results are encouraging.

ACKNOWLEDGMENTS

The work presented here is the result of a collaboration between many groups and sections within IMEC, while the 3D integration strategy is mainly originating from Eric Beyne. This work is supported by many different companies (including the IMEC core partners), as well as by EC and local government projects.

REFERENCES

1. Proc. of the 1st, 2nd and 3rd conf. on "3D Architectures for Semiconductor Integration and packaging", RTI international, Burlingame, California, April 13-15, 2004; Tempe, Arizona, June 13-15, 2005; Burlingame, California, October 31 – November 2, 2006
2. E.Beyne, "3D Interconnection and packaging: impending reality or still a dream?" proceedings of the IEEE International Solid-State Circuits Conference, ISSCC2004, 15-19 February 2004; San Francisco, CA, USA, IEEE, 2004, pp.138-145.
3. E.Beyne, "System-Driven Approaches to 3D Integration", The 4th International Symposium on Microelectronics and Packaging, Seoul, S-Korea, September 28, 2005, p 25 – 34.
4. C. Noritake, P. Limaye, M. Gonzalez and B.Vandevelde, "Thermal Cycle Reliability of 3D Chip Stacked Package Using Pb-free Solder Bumps: Parameter Study by FEM Analysis", 7th Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Microelectronics and Microsystems – EuroSimE, April 2006, Como (Italy).
5. Liu Caroline Chen, Bart Vandevelde, Bart Swinnen, Eric Beyne, "Enabling SPICE-Type Modeling of the Thermal Properties of 3D-Stacked ICs", EPTC 2006, Singapore, December 6-8, 2006
6. Bert Gyselinckx, "3D System-in-Package Integration of Wireless Sensor Nodes" , invited paper at ISSCC, February 11-15 2007, San Francisco
7. Koen De Munck, Lieve Bogaerts, Deniz S. Tezcan, Piet De Moor, Bart Swinnen, Kris Baert, and Chris Van Hoof, "Wafer Level Temporary Bonding/Debonding for Thin Wafer Handling Applications", IMAPS International Conference and Exhibition on Device Packaging, Scottsdale, March 2006

8. Deniz Sabuncuoglu Tezcan, Nga Pham, Bivragh Majeed, Kris Baert , Piet De Moor and Wouter Ruythooren, “Sloped Through Wafer Vias for 3D Wafer Level Packaging”, accepted for publication at ECTC 2007, Reno, USA , May 29 -June 1 2007.
9. M.Gonzalez et al, “influence of dielectric materials and via geometry on the thermomechanical behaviour of silicon through interconnects” ”. Proc. of 10th Pan Pacific Microelectronics Symposium, SMTA, Hawaii, January 25-27, 2005.
10. Deniz Sabuncuoglu Tezcan, Koen De Munck, Nga Pham, Ole Luhn, Arno Aarts, Piet De Moor, Kris Baert and Chris Van Hoof, “Development of Vertical and Tapered Via Etch for 3D Through Wafer Interconnect Technology”, EPTC 2006, Singapore, December 6-8, 2006
11. Nga P. Pham, Mathieu Vanden Bulcke , Piet De Moor, “Spray Coating of Photoresist for Realizing Through-Wafer Interconnects”, EPTC 2006, Singapore, December 6-8, 2006
12. Koen De Munck, Deniz Sabuncuoglu Tezcan, Tom Borgers, Wouter Ruythooren, Piet De Moor, Sherif Sedky, Cinzia Toccafondi, Jan Bogaerts and Chris Van Hoof, “High performance Hybrid and Monolithic Backside Thinned CMOS Imagers realized using a new integration process”, IEDM 2006, December 11-13 2006, San Francisco
13. E.Beyne, “Technologies for very high bandwidth electrical interconnects between next generation VLSI circuits”, IEEE-IEDM 2001 Technical Digest, December 2-5, Washington, D.C., S23-p3, 2001.
14. Vanden Bulcke, M. et al, "Active Electrode Arrays by Chip Embedding in a Flexible Silicone Carrier," Engineering in Medicine and Biology Society, 2006. IEEE-EMBS 2006. 28th Annual International Conference of the, vol., no.pp. 2811-2815, 30 Aug.-03 Sept. 2006.
15. K. De Munck, J. Vaes, P. De Moor, C. Van Hoof, B. Swinnen, “Grinding and Mixed Silicon Cupper CMP of Stacked Patterned Wafers for 3D Integration”, MRS Fall Meeting, November 27 – December 1 2006, Boston
16. Wouter Ruythooren, Serguei Stoukatch, Konstantina Lambrinou, Piet De Moor, Bart Swinnen, “Direct Cu-Cu Thermo-Compression Bonding for 3D-Stacked IC Integration”, IMAPS 2006, October 8-12, San Diego
17. B. Swinnen, W. Ruythooren, P. De Moor, L. Bogaerts, L. Carbonell, K. De Munck, B. Eyckens, S. Stoukatch, D. Sabuncuoglu Tezcan, Z. Tőkei, J. Vaes, J. Van Aelst, E. Beyne, “3D integration by Cu Cu thermo-compression bonding of extremely thinned bulk-Si die containing 10 µm pitch through-Si vias.”, IEDM 2006, December 11-13 2006, San Francisco