Jae Choon Kim
Test & System Package,
Samsung Electronics,
Hwasung 18448, South Korea

Zongqing Ren
Mechanical and Aerospace Engineering,
University of California, Irvine,
Irvine, CA 92617

Anil Yuksel
IBM Systems,
IBM Corporation,
Austin, TX 78758

Ercan M. Dede
Electronics Research Department,
Toyota Research Institute of North America,
Ann Arbor, MI 48105

Prabhakar R. Bandaru
Mechanical and Aerospace Engineering,
University of California, San Diego,
San Diego, CA 92093

Dan Oh
Test & System Package,
Samsung Electronics,
Hwasung 18448, South Korea

Jaeho Lee[1]
Mechanical and Aerospace Engineering,
University of California, Irvine,
Irvine, CA 92617
e-mail: jaeholee@uci.edu

Recent Advances in Thermal Metamaterials and Their Future Applications for Electronics Packaging

Thermal metamaterials exhibit thermal properties that do not exist in nature but can be rationally designed to offer unique capabilities of controlling heat transfer. Recent advances have demonstrated successful manipulation of conductive heat transfer and led to novel heat guiding structures such as thermal cloaks, concentrators, etc. These advances imply new opportunities to guide heat transfer in complex systems and new packaging approaches as related to thermal management of electronics. Such aspects are important, as trends of electronics packaging toward higher power, higher density, and 2.5D/3D integration are making thermal management even more challenging. While conventional cooling solutions based on large thermal-conductivity materials as well as heat pipes and heat exchangers may dissipate the heat from a source to a sink in a uniform manner, thermal metamaterials could help dissipate the heat in a deterministic manner and avoid thermal crosstalk and local hot spots. This paper reviews recent advances of thermal metamaterials that are potentially relevant to electronics packaging. While providing an overview of the state-of-the-art and critical 2.5D/3D-integrated packaging challenges, this paper also discusses the implications of thermal metamaterials for the future of electronic packaging thermal management. Thermal metamaterials could provide a solution to nontrivial thermal management challenges. Future research will need to take on the new challenges in implementing the thermal metamaterial designs in high-performance heterogeneous packages to continue to advance the state-of-the-art in electronics packaging. [DOI: 10.1115/1.4047414]

Keywords: thermal management, electronics cooling, heat guiding, heterogeneous package

1 Introduction

Metamaterials are structures that are artificially engineered to obtain properties that are not available in nature. For instance, advances in optical metamaterials have allowed sophisticated control over light or electromagnetic waves. As one of the most influential and popular benchmarks, an invisibility cloak, has been achieved at both microwave regimes [1,2] and optical frequencies [3–8] based on the theory of transformation optics. Coordinate transformation-based methodologies connect metamaterial properties with thermal dissipation in devices, which further inspires the study of thermal metamaterials for heat control. Various thermal metamaterials that are conduction-based have been demonstrated through numerical [9–11] or experimental [12–15] studies under steady-state or transient conditions. Additionally, scattering cancelation-based bilayer thermal cloaks have been experimentally demonstrated in 2D [16,17] or 3D [17,18]. Topology optimization-based finite element methods have also been explored to enable heat flow control in arbitrary (e.g., noncircular or nonspherical) geometries [19,20] and bifunctional cloaking [21]. The combined manipulating of thermal and dc fields [22], as well as, thermal-composite design optimization methods for thermal management of printed circuit board (PCB)-based electronics [23] have been considered. Thermal radiation-based metamaterials have been actively studied [24] but not been reviewed in this paper due to their limited relevance to electronic packaging at the present.

Indeed, thermal metamaterials can make an impact on electronic packaging [25]. With rapid development of nanoelectronics, 3D-integrated circuits (ICs), and flexible electronics, thermal management is becoming more challenging [26]. For example, in 2.5D packages, the logic power as well as the number of high band width memory (HBM) layers continue to increase [27,28]. One critical challenge in 2.5D packages is thermal crosstalk as the logic chip and HBM are placed close to each other while they require different operating temperatures [29,30]. Thus, thermal metamaterials are needed to facilitate heat dissipation and protect temperature-sensitive components [31–33]. In 3D packages, thermal resistances and operating temperatures continue to increase. Conventional thermal management approaches include through-silicon-via optimization [34–40] and single- or two-phase cooling with microchannels [41–46].

In this paper, we review and summarize the recent progress, and outlook, of thermal metamaterials as related to challenges in thermal management of electronic packaging. In Sec. 2, we review thermal metamaterials with a focus on anisotropic heat spreaders and diffusers, thermal cloaking and isolating, and heat guiding and bending devices. This section discusses theoretical and experimental advancements and thermal metamaterials that are related to packaging applications. In Sec. 3, we review the thermal management challenges in heterogeneous integration with

[1]Corresponding author.
Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the Journal of Electronic Packaging. Manuscript received February 29, 2020; final manuscript received May 16, 2020; published online June 29, 2020. Assoc. Editor: Ronald Warzoha.

a focus on multichip implementations and multilayer stacking. In Sec. 4, we discuss package-level cooling capacities and implications of thermal metamaterials for packaging applications and potential research directions in the future.

2 Recent Progress in Thermal Metamaterials

In the last decade, there have been significant advances in the field of thermal metamaterials. The trend in thermal metamaterials has been toward practical demonstrations such as thermostats [47], thermal camouflage [48], dual-function thermal metamaterials [49], and active heat flow control [50,51]. In this section, we review the recent progress in conduction-based thermal metamaterials that are relevant to potential applications in electronic packaging.

2.1 Anisotropic Heat Spreader. The ability to control thermal energy through mediums has significant implications beyond fundamental study. The controlled transmission of heat is hard to achieve in one material or device because heat is carried by a broad spectrum of high-frequency (terahertz) phonons that are hard to control [52]. Moreover, microscale heat transport in solids is diffusive based on the Fourier's law of heat conduction: $q_i = -k_{ij}\nabla T_j$, where k_{ij} represents the second-order thermal-conductivity tensor. Here, q_i and ∇T_j are the heat flux and temperature gradient in the ith and jth directions, respectively. The path of heat conduction can be controlled by engineering an artificial material with prescribed anisotropy in its thermal-conductivity tensor.

With respect to functional devices based on thermal passage, Chang et al. first fabricated thermal diodes using carbon nanotubes and boron nitride nanotubes [53]. The nonuniform mass deposited along the tube yielded a higher conductance when heat flows from the high-mass region to the low-mass region. Some 2D materials like black phosphorous had also shown thermal-conductivity anisotropy arising from the anisotropic phonon dispersion relation [54,55].

In recent studies, silicon nanostructures with vertically etched holes, or holey silicon, had demonstrated significant thermal-conductivity reductions and anisotropic thermal conductivity in the in-plane and cross-plane directions [56–58]. Ren and Lee had shown that the unique thermal-conductivity anisotropy in holey silicon is ideal for thermoelectric cooling (TEC) to address on-chip hot spots [59,60]. In the in-plane direction, the neck size dominated phonon boundary scattering reduces the thermal conductivity (k_x and k_y), which sustains a large temperature gradient for enhanced thermoelectric effects. In the cross-plane direction, the low frequency (long wavelength) phonons are less susceptible to surface disorder. The persistent long wavelength phonons lead to a high cross-plane thermal conductivity (k_z), which facilitates heat dissipation. To address such increasingly severe hot spot issues in nanoscale and high-power electronics, a lateral TEC design based on holey silicon is shown in Fig. 1(*a*). The heat generation by electronics was modeled by a combination of a $70\,\mathrm{W\cdot cm^{-2}}$ background heat flux and a $700\,\mathrm{W\cdot cm^{-2}}$ hot spot heat flux as representative values for future electronics. The top of holey silicon undergoes convective heat transfer to 25 °C ambient air with a constant/equivalent convection coefficient value of $8700\,\mathrm{W\cdot m^{-2}K^{-1}}$, which represents the use of an advanced heat exchanger [61]. With an optimal applied current, the hot spot temperature of the holey silicon-based TEC was 15 °C lower compared to that of the bulk silicon-based TEC; see Fig. 1(*d*). Holey silicon-based TEC can be potentially used to provide localized cooling to power electronics and optoelectronic devices [16,61].

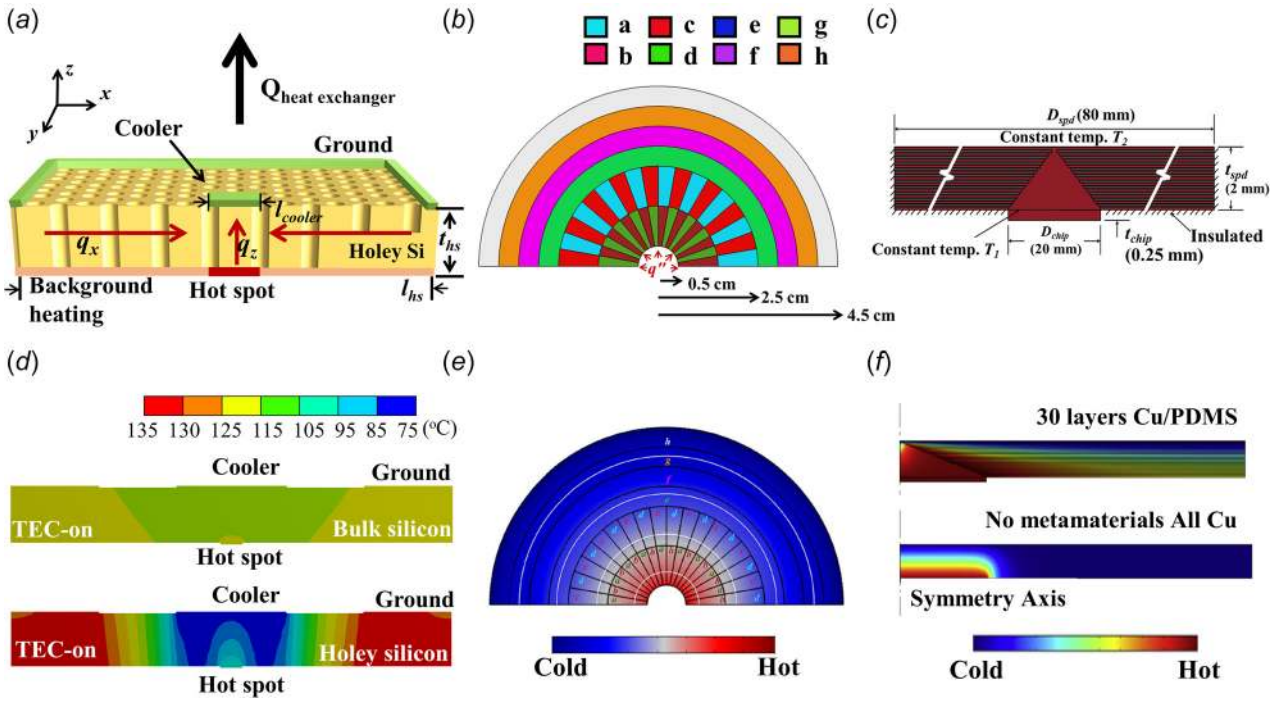

Fig. 1 (*a*) The holey silicon-based lateral TEC design. The black arrows indicate the convectional heat flux. The cooler size (l_{cooler}), holey Si chip thickness (l_{hs}), and holey Si chip size (l_{hs}) are in the range of 50–500 μm, 50–150 μm, and 1–12 mm, respectively. (*b*) The design of the perfect thermal diffuser with an input heat flux $q'' = 2\times10^6\ \mathrm{W\cdot m^{-2}}$. The symbols refer to the materials with isotropic thermal conductivities, i.e., $k_a = 282\,\mathrm{W\cdot m^{-1}K^{-1}}$, $k_b = 12\,\mathrm{W\cdot m^{-1}K^{-1}}$, $k_c = 118\,\mathrm{W\cdot m^{-1}K^{-1}}$, $k_d = 29\,\mathrm{W\cdot m^{-1}K^{-1}}$, $k_e = 110\,\mathrm{W\cdot m^{-1}K^{-1}}$, $k_f = 31\,\mathrm{W\cdot m^{-1}K^{-1}}$, $k_g = 169\,\mathrm{W\cdot m^{-1}K^{-1}}$, and $k_h = 20\,\mathrm{W\cdot m^{-1}K^{-1}}$. (*c*) Schematic of the cross-sectional view of the bilayer thermal metamaterial spreaders. (*d*) Cross-sectional temperature profiles of bulk silicon and holey silicon-based TEC with an optimal applied current ($I = 0.9$ A) that balances the Peltier effect and Joule heating. (*e*) Temperature profiles of (*b*). (*f*) Temperature profile comparison of (*c*) with metamaterial spreader and all Cu designs (Figures reprinted with permission (*a*) and (*d*) from Ren and Lee [59], Copyright 2017 IOP Publishing; (*b*) and (*e*) from Vemuri and Bandaru [62], Copyright 2016 Springer Nature; (*c*) and (*f*) from Hamed and Ndao [63]. Copyright 2017 Elsevier B.V.).

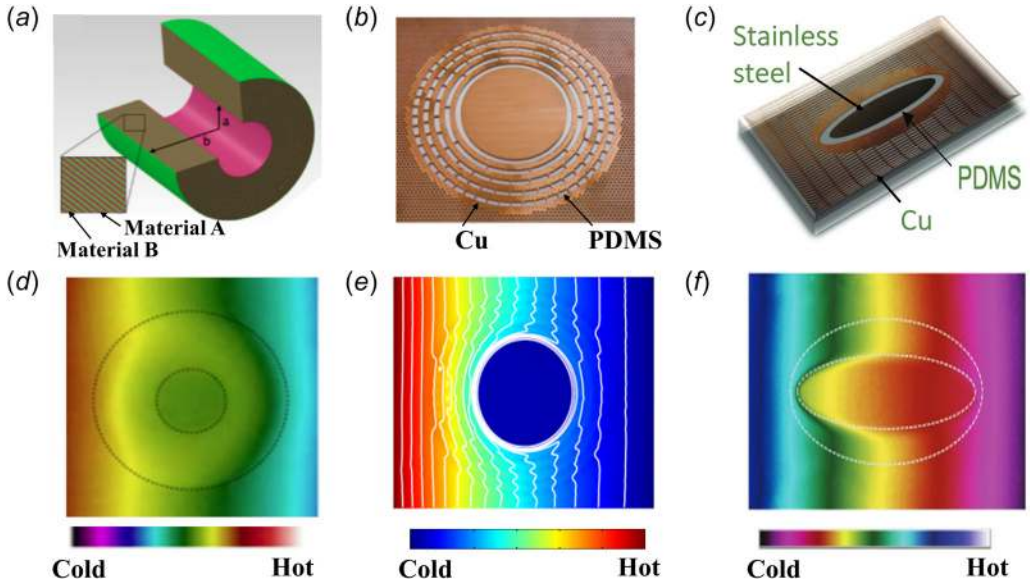

Fig. 2 (*a*) The steady-state thermal cloak composed of latex rubber film (material A) and silicone elastomers (material B) with agar-water as the background material. $a = 0.8$ cm and $b = 2.7$ cm. (*b*) The transient thermal cloak composed of Cu and PDMS. (*c*) The omnidirectional elliptical thermal cloak composed of a stainless steel object, a Cu shell, and a PDMS insulating layer. (*d*) The measured temperature profile of (*a*). (*e*) The measured temperature profile of (*b*) at $t = 120$ s. (*f*) The measured temperature profile of (*c*) at $t = 5$ min. (Figures reprinted with permission (*a*) and (*d*) from Ref. [12], Copyright 2012 American Physical Society; (*b*) and (*e*) from Schittny et al. [13]. Copyright 2013 American Physical Society; (*c*) and (*f*) from Han et al. [65]. Copyright 2018 John Wiley & Sons, Inc.).

Anisotropic heat spreaders/diffusers can also be designed through the metamaterial approach for passive cooling applications. Vemuri and Bandaru reported a perfect thermal diffuser by rationally placing constituent materials in the radial and the azimuthal directions [62]. Figure 1(*b*) shows the design of thermal diffuser. When a hot spot heat flux is applied at the center, the isotherm lines are equally spaced through the spreader; see Fig. 1(*e*). The source temperature of the anisotropic heat spreader is significantly lower compared to that obtained using a single material with isotropic thermal conductivity. The advantage of such designs includes the regularization of heat transport, so as to control the path of heat transfer, e.g., to obtain a uniform temperature distribution avoiding hot spots. The facilitating methodology involves a metamaterial architecture, constituted from individual *thermal meta-atoms* at any given point in the diffuser and with spatially varying values for the thermal conductivity. Hamed and Ndao designed a bilayer thermal diffuser based on coordinate transformation to increase the thermal spreading efficiency [63]. Figure 1(*c*) shows the cross-sectional view of the heat spreader design with alternating layers of copper ($k_{\text{Cu}} = 400\,\text{W}\cdot\text{m}^{-1}\text{K}^{-1}$) and polydimethylsiloxane (PDMS, $k_{\text{PDMS}} = 0.15\,\text{W}\cdot\text{m}^{-1}\text{K}^{-1}$). With constant temperatures applied to the chip ($T_1 = 80\,^{\circ}\text{C}$) and spreader ($T_2 = 27\,^{\circ}\text{C}$) surfaces, the metamaterial heat spreader allows for much higher heat spreading to guide heat in the lateral direction compared to a pure Cu spreader reference, see Fig. 1(*f*).

In additional to cooling, efficient heat expanders are designed through coordinate transformation to provide a large surface of uniform temperature when there is a small hot spot. Liu et al. developed a plate heater based on transformation thermodynamics that can transiently provide a large and homogeneous-temperature surface powered by a thermal source whose area is 100 times smaller compared to that of the surface [64]. Han et al. constructed a thermal expander based on an elliptical thermal cloak that works as a high-efficiency point-to-plane heat source convertor with excellent transient performance [65].

2.2 Heat Cloaking and Isolating. Thermally sensitive elements, electronic circuits, components, or systems may be arranged to be in a region with minimum thermal disturbances, i.e., where the thermal gradient across the elements may be as close to zero as possible, irrespective of the temperature variations in the surroundings. A region where such a gradient may be established may be defined as a *thermal cloak*. The bending of the heat flux, through individual materials arrangement in a *metamaterial* immediately suggests applications [12] to thermal concentrators or thermal cloaks [11], where the temperature gradient could be engineered to be equal to zero in the *cloaked* region. Experimentally, a temperature gradient less than 0.004 K/cm was measured over the cloaked region [66]. Thermal invisibility cloak reduces temperature disturbance in the cloaked region and has the potential for many thermal management functions [22,67]. A majority of thermal cloaking research focuses on hiding the object from external heat flow. Fan et al. [68] and Chen et al. [69] first investigated thermal cloaking based on coordinate transformation methodologies, which indicates the required transformed properties in the physical space to realize invisibility [67]. Li et al. developed a bifunctional cloak possessing both electrical and thermal cloaking functionalities. The desired anisotropic thermal conductivity for coordinate transformation is obtained by filling nanoparticles into a substrate based on effective medium theory [9]. Guenneau et al. adopted coordinate transformation to thermodynamics and designed a multilayered thermal cloak consisting of homogeneous isotropic materials with realistic diffusivities [10].

The first experimental demonstration of thermal cloaking was shown by Narayana and Sato [12]. Multilayered composites are used to achieve thermal cloaking as well as thermal concentration and flux rotation in a steady-state condition. Figure 2(*a*) shows the multilayer-based thermal cloak with 40 alternating layers of latex rubber (material A, $k_A = 0.13\,\text{W}\cdot\text{m}^{-1}\text{K}^{-1}$) and silicone elastomers (material B, $k_b = 2.6\,\text{W}\cdot\text{m}^{-1}\text{K}^{-1}$). The host background material is agar-water block with $k_{\text{hb}} = 0.56\,\text{W}\cdot\text{m}^{-1}\text{K}^{-1}$ and $k_h^2 \sim k_A k_B$ is the key to achieve the least perturbation [12]. The steady-state temperature profile with a lateral temperature gradient is shown in Fig. 2(*d*). Dede et al. fabricated multilayer-based thermal cloak using a standard PCB manufacturing process [15]. Schittny et al. [13] and Ma et al. [14] experimentally realized

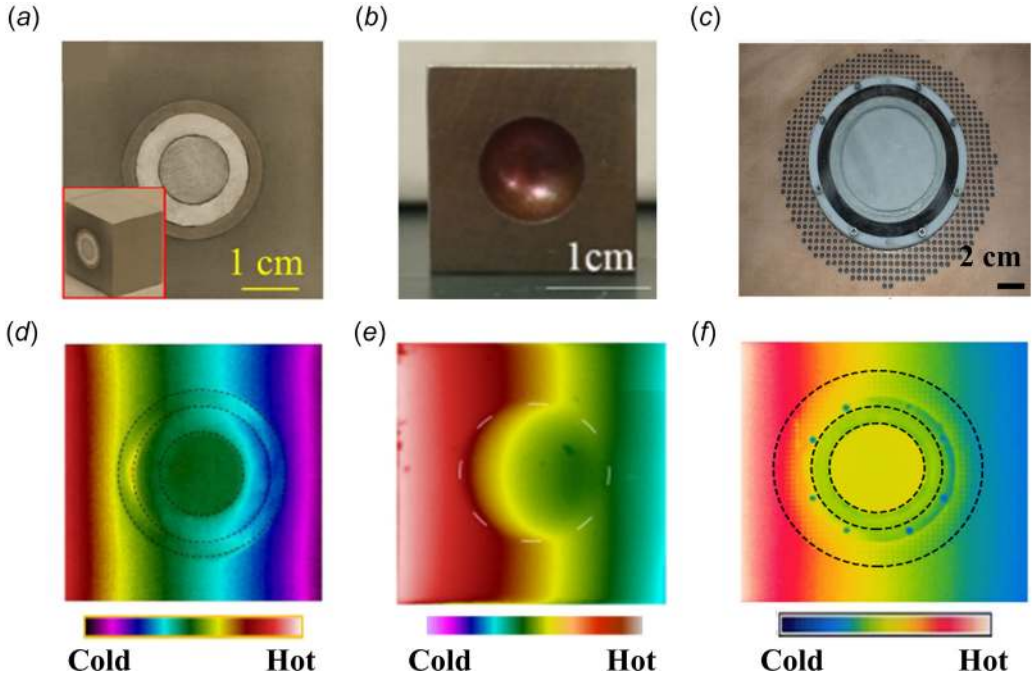

Fig. 3 (*a*) The 2D bilayer thermal with sealant as the background material (2.3 $W \cdot m^{-1}K^{-1}$). The inner and outer layers are polystyrene and Inconel 625 alloy with thermal conductivity of 0.03 and 9.8 $W \cdot m^{-1}K^{-1}$, respectively. The object in the center is an Al cylinder. (*b*) The 3D bilayer thermal cloak with stainless steel as the background material and Cu thin disk punched into the hemispherical hole. (*c*) Thermal zero-index cloak with Cu as the background material and stainless steel as the clocked object. The outer layer is Cu with drilled holes and the inner layer is a channel filled with water. (*d*) The measured temperature profile of (*a*). (*e*) The measured temperature profile of (*b*). (*f*) The measured temperature profile of (*c*). (Figures reprinted with permission, (*a*) and (*d*) from Han et al. [17]. Copyright 2014 American Physical Society. (*b*) and (*e*) from Xu et al. [18]. Copyright 2014 American Physical Society. (*c*) and (*f*) from Li et al. [74]. Copyright 2019 Springer Nature.)

transient thermal cloaks that allow real-time thermal protection to the object. The design of a Cu-based transient thermal cloak is shown in Fig. 2(*b*). The temperature profile with a lateral temperature gradient applied for 120 s is shown in Fig. 2(*e*), where the temperature in the cloaked region is smaller than its surroundings. However, in the long-time limit, a small amount of thermal energy will diffuse into the cloaked region due to the finite thermal conductivity of the insulating layers. The temperature of the cloaked region will eventually heat up and approach the steady-state temperature [13]. Han et al. established a general design method to create steady-state thermal cloaks by using only homogeneous and natural materials [11]. He and Wu designed an open cloak, in which the temperature of the cloaked object can be sharply reduced compared to the closed cloak when the window is located at the low-temperature side [31]. Coordinate transformation-based thermal cloaks commonly rely on parameter simplification or directional functions for anisotropic geometries. Han et al. demonstrated an omnidirectional thermal cloak that is derived directly from the conduction equation without approximation [48]. The elliptical thermal cloak is shown in Fig. 2(*c*). The thermal cloak works along arbitrary directions of heat flow and its performance is validated in the time-dependent case as shown in Fig. 2(*f*) (temperature profile at $t = 5$ min). Moreover, a thermal cloak sensor, which is capable of cloaking itself and receiving the incoming signal simultaneously can also be achieved.

Another approach to construct a thermal cloak is scattering cancelation as discussed by Alu and Engheta to apply metamaterials for reducing the total scattering cross section of spherical and cylindrical objects [70]. The bilayer thermal cloak consists of two concentric shells, the inner layer is a thermal insulator to block heat flux from entering the object, and the outer layer minimizes the temperature distortion introduced by the inner layer. This technique was further developed in the experimental realization of a bilayer thermal cloak with only homogeneous and isotropic materials in 2D [17] and 3D [18] scenarios, as shown in Figs. 3(*a*), 3(*b*), 3(*d*), and 3(*e*). In addition to thermal cloaking, Ma et al. experimentally demonstrated an electric-thermal bifunctional cloak based on the same method [16].

Yet another strategy in constructing thermal cloaks for steady-state heat conduction is to use gradient-based homogenization design and optimization. Here, a thermal composite may be designed by representing the explicit heterogeneous microstructure of the composite via homogenized effective anisotropic material properties. In such a way, an optimization objective function is defined, and a gradient-based optimizer is exploited in minimizing the functional through the local design of the anisotropic material thermal-conductivity layout. This method was first proposed for thermal-composites by Dede [19] and then extended by Dede et al. [20], where optimal thermal composite annular structures were independently designed to realize effective heat flux cloaking, focusing, or reversal/guiding devices. The benefit of this numerical method is that it is highly geometrically flexible and can be applied to the design of arbitrarily shaped thermal metamaterials, as explained in Ref. [20]. Such material optimization techniques have been further applied by Fachinotti et al. [71] in the fabrication of anisotropic heat flux manipulation devices. Additionally, following He and Wu [39], the material design optimization technique has been employed in Ref. [40] for the useful design of "open" (i.e., cold side open) thermal cloaks for temperature-sensitive device cloaking or shielding in multilayer PCBs.

Despite this progress, in practice, the capability of the thermal metamaterial is limited because of the narrow range of thermal conductivities in natural solid materials, which ranges about four orders of magnitude from 0.1 to 1000 $W \cdot m^{-1}K^{-1}$ at room temperature [72]. For thermal cloak designs based on coordinate

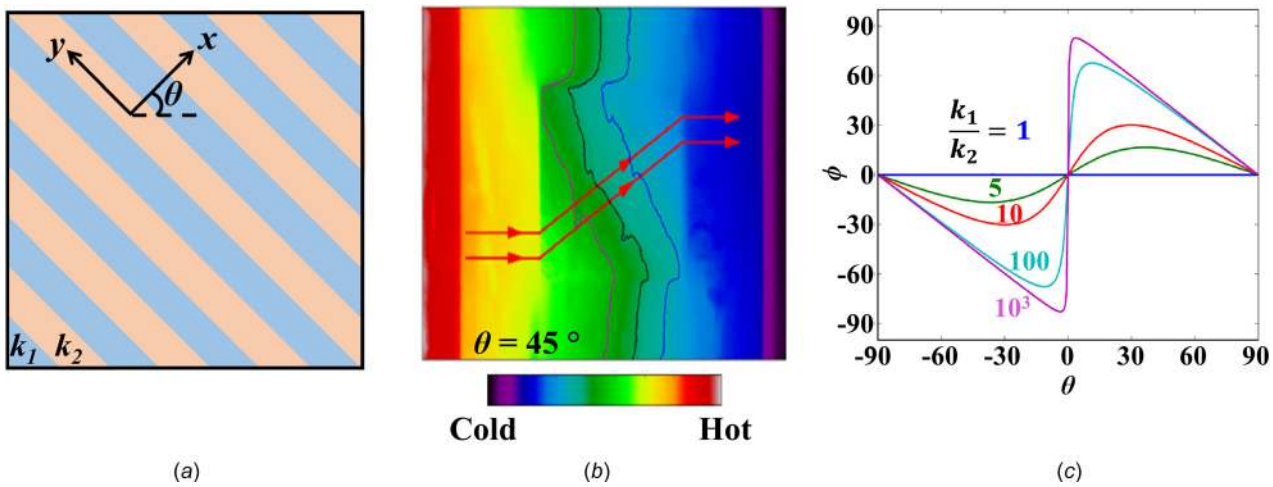

Fig. 4 Heat flux rotation as a function of composite sample orientation. (*a*) The rotated layer orientation with $\theta = 45$ deg. *x* and *y* correspond to the coordinate systems. k_1 and k_2 are the thermal conductivities of the stacked layers. (*b*) Steady-state temperature profile measured when $\theta = 45$ deg. The upward bended heat flux is evident with a horizontally applied temperature gradient. (*c*) The variation of the heat flux bending angle ϕ with composite layer orientation θ at different thermal-conductivity ratios (k_1/k_2). (Figures reprinted with permission (*b*) from Vemuri et al. [66]. Copyright 2014 AIP Publishing LLC; (*c*) from Vemuri and Bandaru [76]. Copyright 2013 AIP Publishing LLC.)

transformation, scattering cancelation, or gradient-based design optimization methods, the thermal conductivity of the conductive or inner layers needs to be much larger than that of the background substrate. To minimize the perturbation of the heat flux at the interface with the background, the metamaterial-based composite needs to be embedded in a background corresponding to the geometric mean of the thermal conductivities of the metamaterials' constituents [73]. Consequently, most of the thermal cloaks cannot operate when the background substrate is a high-thermal-conductivity material, e.g., Li et al. designed a thermal cloak that works in high-thermal-conductivity-backgrounds [74]. They identified an equivalence between zero index in Maxwell's equation and infinite thermal conductivity in Fourier's law and theoretically proved that the integrated high-speed fluid field is equivalent to a material with an infinitely large thermal conductivity. A near thermal zero-index cloak is constructed with a solid conductor embedded with circulating fluid as shown in Fig. 3(*c*). Their thermal cloak works with Cu as the background material and acts as a transient temperature sensor as the temperature of the object follows the environmental changes as shown in Fig. 3(*f*).

2.3 Heat Guiding and Bending. With the trend toward high packaging density of electronics, it becomes severely important to dissipate heat in a well-defined path to reduce thermal crosstalk between adjacent devices and protect thermally sensitive components. While an extensive number of fundamental studies about thermal metamaterials have shown heat flow manipulation, the ideal thermal metamaterials are usually composed of curved lines or complex structures that are costly to fabricate [75]. On the other hand, thermal shifters composed of two isotropic materials have shown the ability to bend heat flux on demand with good manufacturability [66,76]. Considering two alternatively stacked isotropic materials with thermal conductivities of k_1 and k_2 as shown in Fig. 4(*a*). The heat flux rotation is a function of the composite layer orientation. Assuming material 1 is Cu ($k_1 = 390\,\mathrm{W \cdot m^{-1}K^{-1}}$) and material 2 is stainless steel ($k_2 = 42\,\mathrm{W \cdot m^{-1}K^{-1}}$), the heat flux can be bended upward by 26 deg when composite layer orientation $\theta = 45$ deg; see Fig. 4(*b*) [66]. Figure 4(*c*) shows the relationship between heat flux rotation, thermal-conductivity ratio of two materials, and the rotation angle of the composite. A large thermal-conductivity ratio leads to a large heat flux rotation [76].

The thermal shifter could be used as a unit cell to enable multifunctional thermal metamaterials such as a thermal cloak, concentrator, etc. [75,77]. Figure 5(*a*) shows the design of a tunable thermal cloak by the diverse assembly of 4×4 thermal shifters with orientations of ± 15 deg, ± 45 deg, and ± 75 deg. The thermal shifter unit cell was composited of Cu and PDMS; see Fig. 5(*b*). Figure 5(*c*) shows that the thermal shield has a reduced temperature gradient in the center when subject to a lateral temperature gradient. Kang et al. reported a temperature-responsive thermal cloak that can induce dynamic changes in thermal energy distribution by integrating phase-change materials (PCMs) [33]. The thermal cloak was constructed by 4×4 thermal shifters with a similar design as shown in Fig. 5(*a*). The two materials are stainless steel and *n*-octadecane filled with multiwalled carbon nanotube (MWCNTs) and Cu power, which is used as the phase-change nanocomposite (PCNC) to provide a modulation of thermal conductivity with respect to ambient temperature; see Fig. 5(*d*). The transition temperature of PCNC is 28 °C, and the thermal conductivity of PCNC is 5.0 and $0.75\,\mathrm{W \cdot m^{-1}K^{-1}}$ at 20 and 35 °C, respectively. Figures 5(*e*) and 5(*f*) show the temperature profiles of the thermal cloak at low and high ambient temperatures with respect to a lateral temperature gradient. At a low-temperature range of 20–24 °C, PCNC is in the solid-state phase and has a comparable thermal conductivity to stainless steel, the thermal cloaking is at off-mode. On the contrary, at a high-temperature range of 30–41 °C, PCNC transforms into a liquid phase state and with a much lower thermal conductivity, which acts as a thermal insulator and protects the cloaked region (thermal cloaking at on-mode). The temperature responsive thermal cloak can be potentially applied to protect temperature-sensitive devices through related isolation as well as dissipation.

3 Thermal Management Challenges in Heterogeneous

Thermal management has long been considered as one of the keys to maximize device performance and reliability. Compared to conventional MCPs (multichip packages) and SIP (system in package), advanced heterogeneous packages face more challenges in thermal management due to the targeted finer pitches, 3D stacks, more inputs/outputs (I/Os), higher densities, higher power consumptions, and higher performance applications [78–81].

Thermal management challenges in heterogeneous packages can be understood from two points of view. First, high-

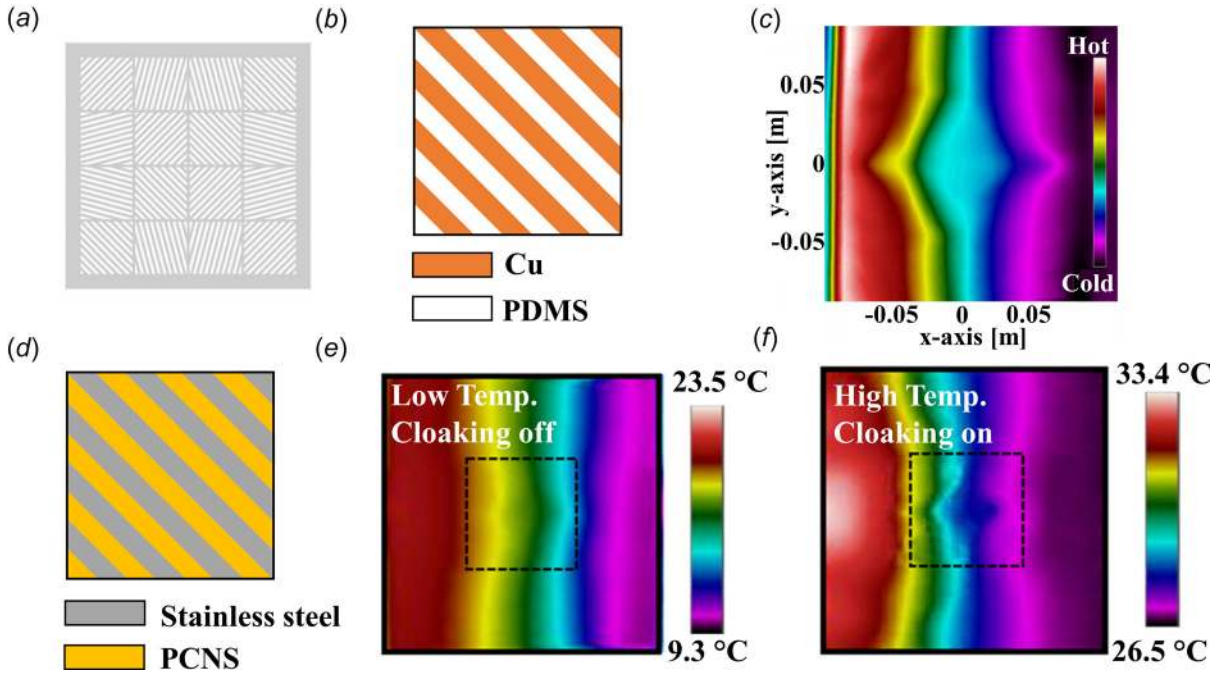

Fig. 5 (*a*) Thermal cloak design with 4 × 4 thermal shifters; (*b*) the unit cell of the steady-state thermal cloak; (*c*) the steady-state temperature profile of (*b*) with respect to a lateral temperature gradient; (*d*) the unit cell of the temperature-sensitive thermal cloak; (*e*) the temperature profile of the temperature responsive thermal cloak at a low-temperature range. Thermal cloak is at off-mode and shows a linear temperature profile in the center. (*f*) The temperature profile of the temperature responsive thermal cloak at a high-temperature range. Thermal cloak is at on-mode and shows a cloaked region in the center. (Figures reprinted with permission (*a*) and (*c*) from Park et al. [75]. Copyright 2017 Springer Nature. (*e*) and (*f*) from Kang et al. [33]. Copyright 2019 Elsevier B.V.)

performance chips are laterally placed close to each other while their temperature-sensitivity and mechanical-reliability metrics are different. This is a common scenario in 2.5D package platforms [28,46,79,82–93]. Second, high-performance chips are vertically stacked, while the thermal resistance increases with the number of stacked chips. This is a common scenario in 3D package platforms such as TSV-SIP (through silicon via) and HBM [94–103]. These two categories of thermal management challenges are reviewed in Secs. 3.1 and 3.2.

3.1 Thermal Management Challenges Due to Multichip Implementations. In 2.5D package platforms, chips can be located in one interposer, regardless of which node process they are, to achieve enhanced performance, lower tolerance, and higher power efficiency, which are required for heterogeneous packages to achieve a minimal footprint. To minimize the package area, high power chips are located as close as possible. In this section, the details of thermal management challenges in side-by-side multichip implementations are reviewed with discussions of high power density requirements, thermal crosstalk, varying temperature criteria, thermal interface materials (TIMs), and substrate thermal resistance.

3.1.1 High Power Density. Thermal management challenge is mostly driven by the continuous increase in power density. Many of the 2.5D package platforms use a silicon interposer to interconnect logic chips and HBMs [78–80,88,93], which have a high heat flux more than $100\,\mathrm{W}\cdot\mathrm{cm}^{-2}$ in a single package [81,104,105]. This requires effective cooling very close to the heat source. However, some of the 2.5D packages have various layers, such as TIM and heat slug layers, between the heat source and the heat sink for reliability concerns at the board level [83,85,89,92]. When the heat sink has a rough contact surface and the 2.5D package has a large thermally induced or assembly warpage, the possibility of the active device cracking and failure increases after the heat sink is attached. Heat slugs and a TIM layer can be used to reduce the possibility of having a device crack for 2.5D packages but increases the thermal resistance between the heat sink and heat source. In the same time, the logic power is continuously increased with higher stacked HBMs for meeting performance requirements [27,28]. According to the international technology roadmap for semiconductors [106], the power density of the microprocessor has increased from about $40\,\mathrm{W}\cdot\mathrm{cm}^{-2}$ (in the present day) to about $100\,\mathrm{W}\cdot\mathrm{cm}^{-2}$ (in 2020). A high efficient cooling solution is needed at the system level to address the increased number of hot spots in a single package. The system-level solution refers to cooling with the casing and other systems, and the board-level solution refers to cooling without the casing. Thermal metamaterials may provide a better path for cooling through controlled heat flux transfer in the latter case.

3.1.2 Thermal Crosstalk. In advanced heterogeneous packages, heat generation in each device can affect neighboring units [28,46,78,81,83,107]. In the 2.5D package platform, the logic device and HBMs are placed within 500 μm because of signal integrity/power integrity (SI/PI) performance. Thermal crosstalk could have detrimental effects, such as an increase in leakage power [108]; see Fig. 6. In general, for logic devices whose current leakage significantly increases with temperature, heat generation from adjacent devices leads to increased current leakage, which could aggravate the self-heating and increase the temperature. To reduce the thermal crosstalk, the distance between the individual logic chips could be increased, a low-thermal-conductivity material mold could be employed to create a thermal barrier between the devices, or a thermal metamaterial design could be implemented to realize a thermal channel running from hot spots to heat sink.

3.1.3 Differences in Operating Temperature and Power Generation. In general, each device has a maximum operation temperature, such as 125 °C for a logic chip and 85 °C for a memory chip [29,30], that affects the reliability of operation

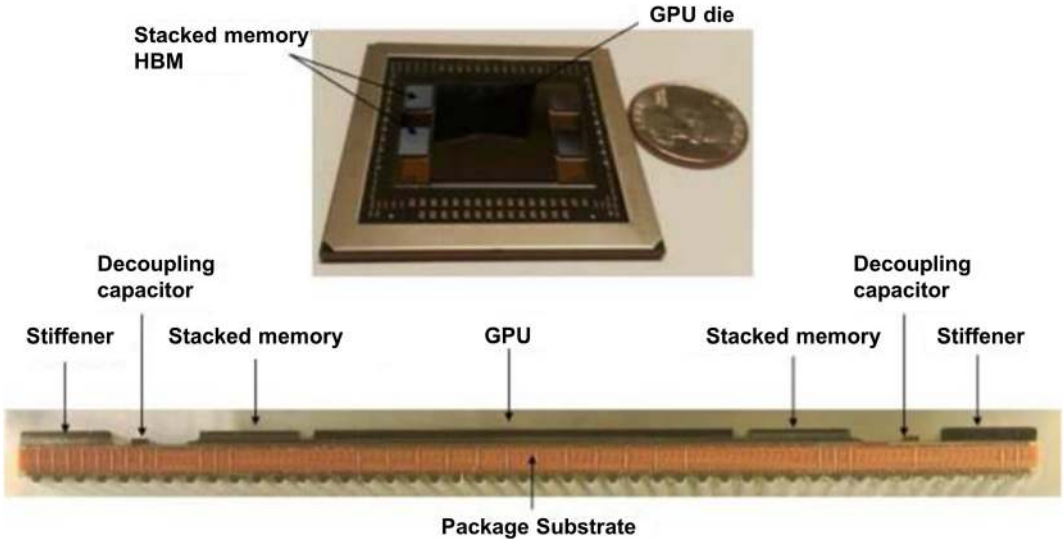

Fig. 6 Si Interposer with a 2.5D package. HBM size is 7.75 mm × 11.87 mm × 720 μm. (Figure reprinted with permission from Lee et al. [108]. Copyright 2016 Institute of Electrical and Electronics Engineers.)

[28,30,46,84,109]. These temperatures are considered as upper limits for reliable operations and performance and should not be exceeded. However, if devices with different operational temperature limits are placed adjacent to each other such as in 2.5D package platforms, the chip of a lower operation temperature limit could easily exceed the limitation due to the thermal crosstalk from a higher operating temperature chip. Also, the logic chip power is normally higher than that of the memory chip when they operate for high performance, which causes a significant thermal crosstalk from logic to memory. This thermal crosstalk effect can be observed from a power envelop graph.

Figure 7 shows the power envelop graphs for IPOP (interposer package on package) and FO-SIP (fan-out system in package) package platforms [28]. The inflection point is observed due to different maximum operation temperature limits of logic and memory chips. From the power envelope graph, the graph area can be considered as a metric scope of performance or efficiency and better thermal performance package shows larger power envelope area. Figure 7 shows that the FO-SIP's power envelope area is larger than IPOP's power envelop area, which means the FO-SIP is a thermally enhanced platform compared with IPOP. With the optimal thermal management solution, the logic chip and HBM could be placed closely with the maximum performance and operating temperatures close to 125 °C and 95 °C, respectively, and the power envelope area would be increased as shown in Fig. 7.

3.1.4 Thermal Interface Material Issues. Thermal interface materials are generally used between active devices and a cooling system, whose performance is related to the thermal conductivity and the bond layer thickness (BLT) [110–112]. High-thermal conductivity and low BLT are preferred for thermal management [113–115]. In 2.5D package platforms, TIMs are typically used on ASIC (application-specific) and HBM [85]. ASIC and HBM have different thermomechanical properties, because ASICs are made of a single chip, and HBMs are made of several chips with multilevel vertical stacks. Even with the same applied pressure, HBM is more vulnerable to mechanical stresses. For this reason, when the same TIM is applied on ASIC and HBM, the BLT is likely to be limited by the HBM's mechanical reliability. When the BLT is fixed, different TIMs could be used on each individual device to maximize the performance. Alternatively, the height of the devices could be modified to the TIM's compression characteristics for the heterogenous package [116], as shown in Fig. 8. In addition, due to the large size of the substrate, the TIM's performance is degraded by voiding, pumping out, and drying out by warpage depending on the operational temperature change. Material selection is facilitated through power thermal cycle inspection of the selected TIM to identify the least impact on performance degradation. Considering that metamaterials make use of an effective thermal medium approximation, the related design principles may be used to controllably fabricate a multilayer TIM.

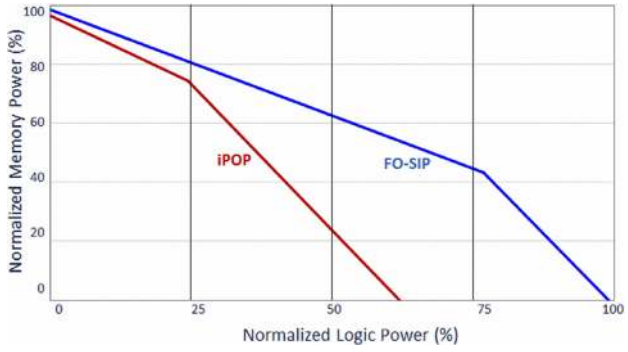

Fig. 7 A power envelope analysis chart. The inflection points are observed due to different maximum operation temperature limits of logic and memory chips. (Figure reprinted with permission from You et al. [28]. Copyright 2018 Institute of Electrical and Electronics Engineers.)

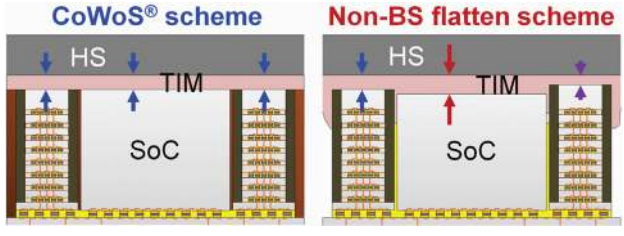

Fig. 8 Flatten backside can manage the BLT with same TIM at same time. However, because of the different mechanical reliability, the TIM's thermal-conductivity choice is restricted. If can control the logic chip and memory chip individually as like nonflattened backside, the TIM's thermal-conductivity choice is not restricted. (Figure reprinted with permission from Hou et al. [116]. Copyright 2017 Institute of Electrical and Electronics Engineers.)

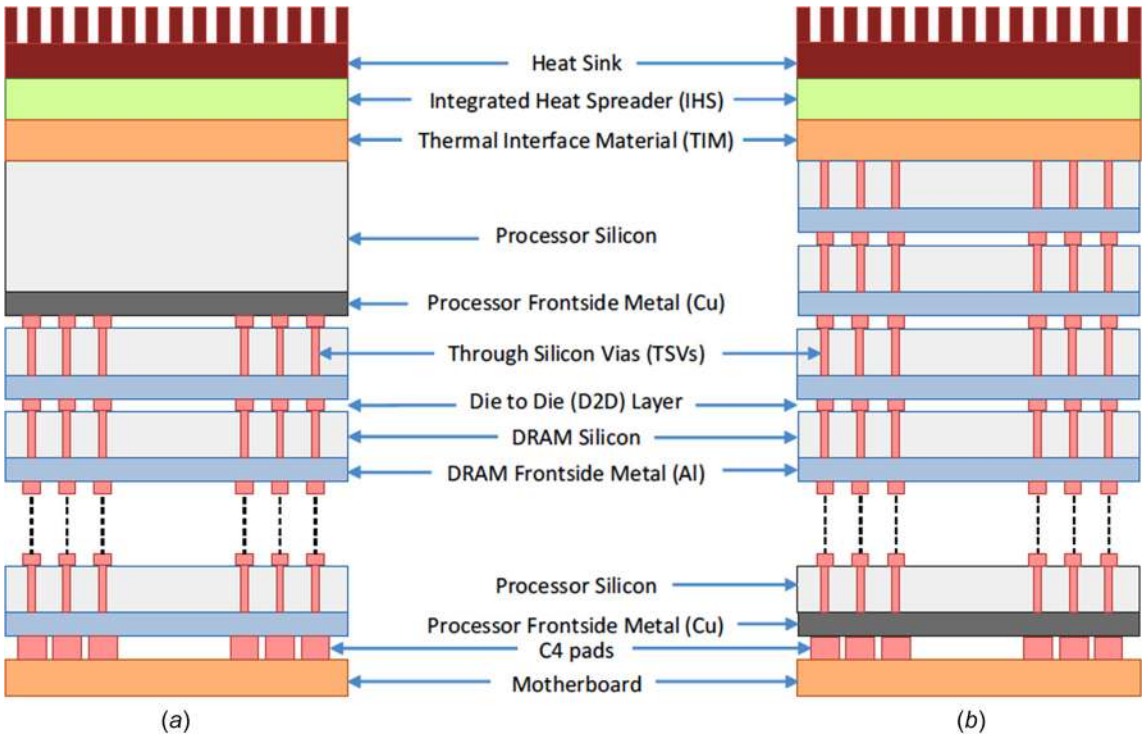

Fig. 9 Schematic of 3D stacked chips with two case (*a*) processor on top and (*b*) memory on top. Processor has higher power and temperature than memory. (Figure reprinted with permission from Agarwal et al. [118]. Copyright 2017 Association for Computing Machinery.)

3.1.5 Thick Substrate. For the advanced heterogenous package, multiple devices are placed on one substrate and thus the number of signal I/Os and power I/Os tend to increase the effective substrate thickness [80,81,117]. When substrates become thicker, the vertical thermal resistance is increased by the number of substrate dielectric layers that nominally have low-thermal conductivity. A thick substrate is one of the main thermal challenges for 2.5D integration. Thermal metamaterials can be considered to enhance heat transfer through the substrate, when integrated with interposer design, and other thermal solutions such as the thermal via, a metal core, and metal block solutions may also be considered.

3.2 Thermal Challenges Due to Three-Dimensional Implementation. Similar to 2.5D package platforms, 3D package platforms are designed to implement heterogeneous integration with a minimal footprint while providing advantages in lowering latency, reducing power consumption, and increasing interconnect bandwidth. With 3D interconnections, the stacked chips create complex thermal management challenges. In this section, the details of thermal management challenges and solutions are reviewed including heat removal through stacked chips, thermal resistance by joint layers, limited thermal spreading by thinned chips, and TSV solutions.

3.2.1 Heat Removal Through Stacked Chips. In 3D chip stacks, the hottest die is the one closest to the substrate due to I/O count or S/I and P/I performance reasons. The heat from the hottest chip is dissipated through the stacked devices, which causes challenges for thermal management because each stacked chip works as a thermal resistance, and the heat from the hottest chip affects the other chips; see Fig. 9. The hottest device should be located close to the cooling system or should have a direct heat path from the hottest chip to the cooling system to enhance cooling efficiency. Aditya et al. [118] shows that the thermal advantages in the TSV-SIP package platform.

3.2.2 Die Bonding. In the 3D stack platform, chip bonding is the main factor for increasing the vertical thermal resistance [100,102,119,120]. A 3D stack joint layer consists of microbumps and a nonconductive film (NCF). A microbump's thermal conductivity is about $60\,\mathrm{W\cdot m^{-1}K^{-1}}$ and the NCF thermal conductivity is about $0.5\,\mathrm{W\cdot m^{-1}K^{-1}}$, both of which are significantly lower than Si thermal conductivity of about $120\,\mathrm{W\cdot m^{-1}K^{-1}}$. So, both features contribute to dramatically increase the vertical thermal resistance. In addition, the chip back end of line layer has lower thermal conductivity than Si [121–123], which also contributes to increase the vertical thermal resistance. Moreover, the interface thermal contact resistance in the junction also contributes. Because of these reasons, the vertical thermal resistance increases rapidly with the number of interconnection layers as shown in Fig. 10.

3.2.3 Thinned Chip. If there is no limit to the package thickness, the chip thickness can be as thick as possible to increase the heat spreading of the hot spot inside the chip [124]. However, the package thickness is usually constrained by system design which affects the 3D stacked device height. In particular, for interconnection using TSVs, the chip thickness is restricted due to a design limitation of the TSV [125]. A chip thickness with TSVs can be much lower than the maximum thickness allowed for single-chips without TSVs (about 780 μm) [126], which can lead to limited lateral heat spreading or increased lateral thermal resistance.

3.2.4 Nonhomogeneous Three-Dimensional Connections. The TSV count, location, dimension, and thermal properties are considered as design parameters to enhance TSV heat transfer. Moreover, when the locations of TSVs are well aligned with other stacked chips, this could work as a thermal path from the heat source to the heat sink [38,127–134]. For example, thermal TSVs (TTSVs), either integrated with thermal metamaterials or designed using metamaterial principles, can be placed close to hot spot regions to facilitate enhanced heat dissipation in 3D ICs

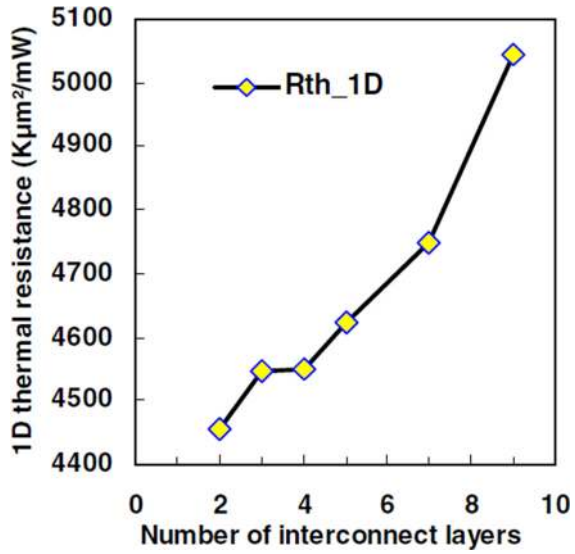

Fig. 10 Vertical thermal resistance is increased along with the number of interconnection layers. (Figure reprinted with permission from Leduc et al. [120]. Copyright 2007 Institute of Electrical and Electronics Engineers.)

[135], following the principle laid out in Sec. 2.1. However, for the complicated 3D connection, the placement of thermal TSV can be one of the design challenges. The area near the hot spot is a very "popular zone" to enhance SI/PI and thermal performance. To get the maximum performance of the nonhomogeneous 3D connection, the thermal TSV placement should be considered in SI/PI design as well.

When the stacked devices have different floorplans from each other, the signal/power TSVs are not located at the same position. In this case, thermal-aware floorplanning technologies, integrated with metamaterial elements and architectures can be used. Thermally aware floorplanning techniques can be categorized into TTSV insertion-based floor planning, force-directed technique-based floor planning, metaheuristic-based floor planning, and other floor planning methods [136]. From a package structure perspective, TTSV insertion-based floorplanning is a useful solution, as shown in Fig. 11. Many TTSV insertion-based floor planning studies had focused on an optimization method to reduce the number of TTSVs to keep peak temperature below the temperature criteria [34,36,37,39,40]. When the area and size of the 3D stacked devices are not the same, the smaller chip works as a heat path and the remaining area of the chip works as a thermal bottleneck. So, it is necessary to optimize the chip position or create an additional thermal channel, which may be achieved through a metamaterial with high contrast in the individual layer thermal conductivity as outlined in Sec. 2.3.

4 Thermal Metamaterials and Cooling Solutions for Packaging

Advanced electronic devices have been increasingly demanded to have integration of more functions into individual chips. This has resulted in high-density packaging of electronics. Moreover, device and interconnect scaling dramatically affect the design and

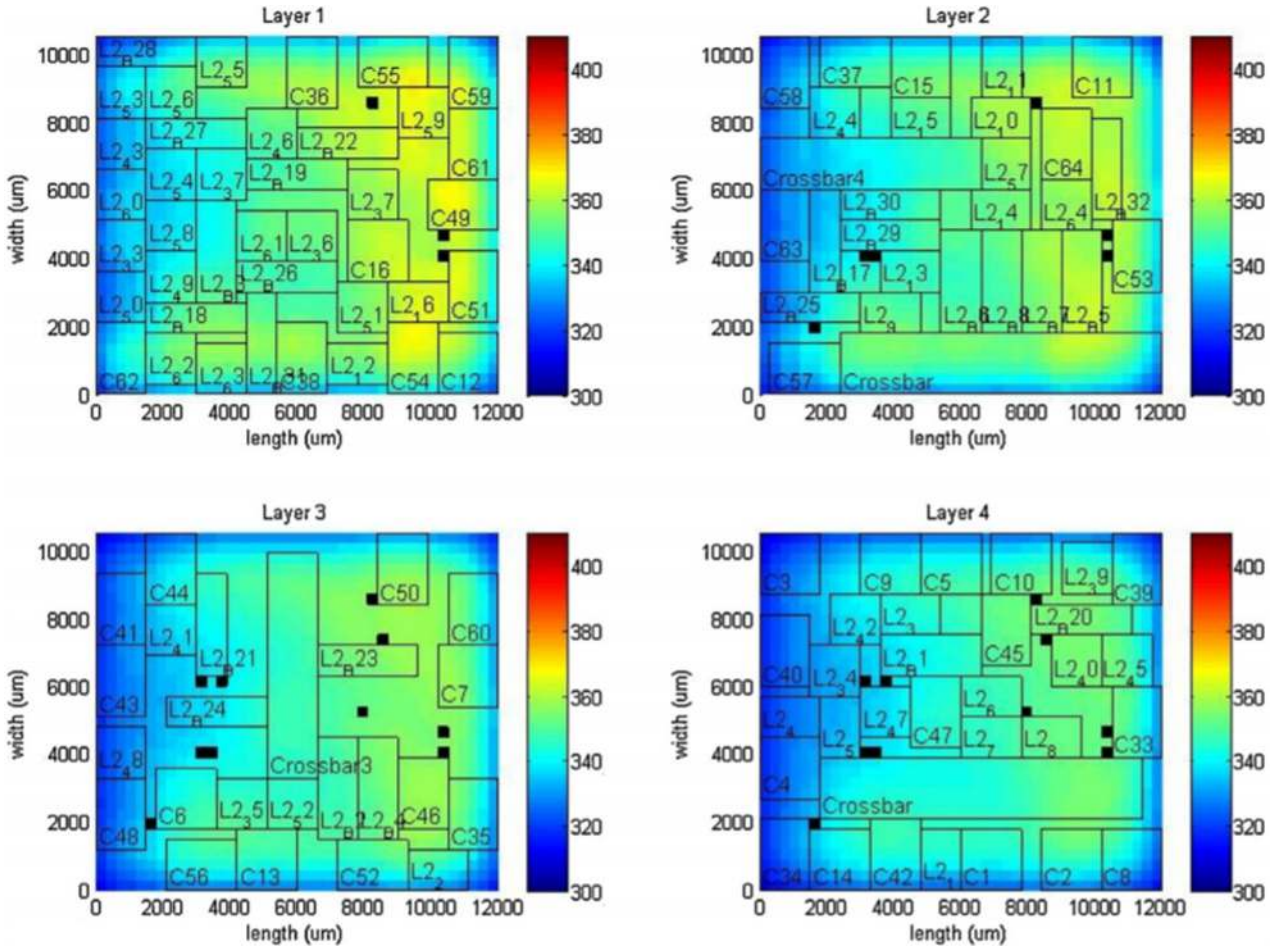

Fig. 11 TSV placement for 3D stacks. Thermal-aware TSV allocations can decrease temperature (Figure reprinted with permission from Cuesta et al. [132]. Copyright 2015 Elsevier B.V.).

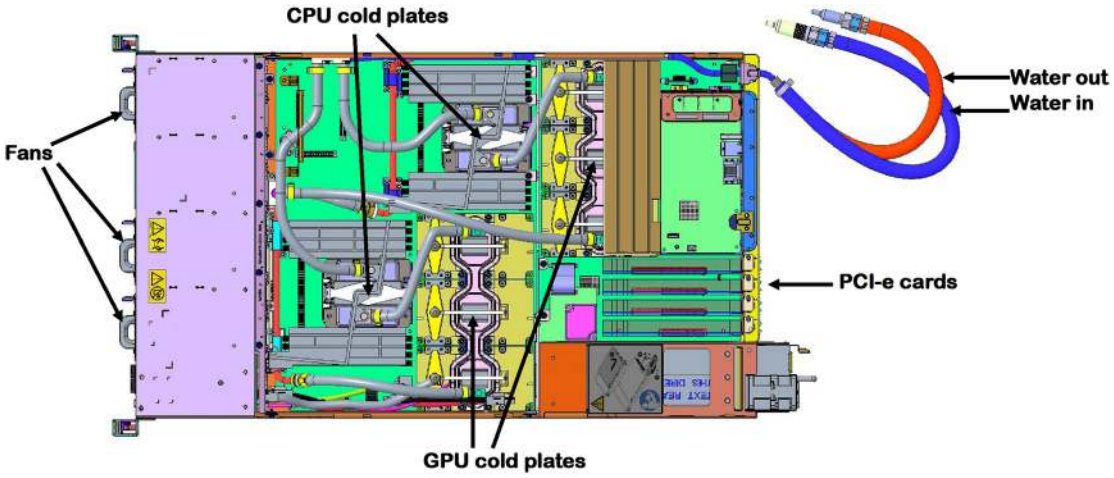

Fig. 12 Liquid cooled IBM power AC922

architecture of advanced assembly and packaging of electronics. Over the recent decade, power density associated with this scaling has been increasing because of increase in power dissipation and scaling down of the effective die area. It is also expected that power density will steadily increase for next-generation devices to beyond $1\,\mathrm{kW \cdot cm^{-2}}$ [137,138]. High heat fluxes on the components due to increase in power density create many challenges such as electromigration, material creep, thermal cycling, warpage; thus, thermal design and architecture considerations need to effectively keep the temperature under control to ensure reliable operation of electronics. Typical dies have different regions such as core, cache, so there are nonuniform power densities associated with these regions; thus, local heat fluxes can exceed $100\,\mathrm{W \cdot cm^{-2}}$. Cloaking and related thermal control applications, facilitated through metamaterial architectures (see Sec. 2.2), may be particularly useful in this regard for thermally sensitive device protection on the die.

4.1 Cooling Capacities of One Package to System Level. Traditional cooling techniques have limitations on removing these localized high-power densities $\sim 100\,\mathrm{W \cdot cm^{-2}}$. Air cooling which is either active or passive has been one of the most commonly used traditional cooling techniques due to availability, simplicity, and capability to cool less than $\sim$250 W power dissipation [139]. Heat spreaders, heat sinks with or without heat pipes are typical examples used in concert with air cooling. In passive air cooling, natural convection, conduction, and radiation heat transfer can cool the electronic components/devices via heat spreaders or heat sinks. Up to $\sim$10 W could be cooled by passive air cooling [140]. This type of cooling is useful for small electronic devices that have lower power. In active air cooling, external components such as a fan or blower circulate air over the electronics. In general, multiple fans or blowers with different configurations are designed to cool the high-density microelectronic packages. There are also some challenges mainly on the fans or blowers; for instance, higher rotational speeds result in higher noise which is also restricted by the acoustic limit of the system environment, and faster fatigue. Furthermore, heat sink design, TIM selection, and overall mechanical assembly of components create reliability concerns. Single-phase liquid cooling has long been applied when power dissipation within the electronic component exceeds $\sim$250 W and when traditional air-cooling thermal management is insufficient enough to cool below a thermal design point [41,141,142]. Two-phase liquid cooling, jet impingement, liquid–vapor phase change, immersion cooling, and direct liquid cooling are some of the other cooling techniques that have been continuously researched and developed for various electronic applications to cool up to $\sim 600\,\mathrm{W \cdot cm^{-2}}$ [42]. However, cost, leakage, and pressure drop within the system create concerns and limitations. Thus, the acceptance of liquid cooling varies for different industries.

System-level packaging and thermal cooling are also challenged by high power components within a limited space. For instance, IBM recently designed the fastest supercomputer in the world [143] that has six graphics processing units (GPUs) having 300 W thermal design power, and two central processing units (CPUs) having 250 W thermal design power, which is illustrated in Fig. 12. This system has two parallel paths where water is used as a liquid cooling to cool the high-power components (GPUs and CPUs) and forced air cooling is applied for the other low power components in the system. The evenly split flow cools CPU and 3 GPU modules that are connected via cold plate assembly in each path. The cold plate assembly is flexible and can accommodate the expected height range of GPUs. Energy efficient data center design was also considered and implemented.

The total power in the supercomputer is continuously increasing and exceeding $\sim$3 kW. Moreover, the typical server size installed into the racks is 2 U ($\sim$88.9 mm) high, 483 mm wide, and 711 mm deep, which makes the power density in the system high. Also, preheat is a main concern for the back section of the supercomputers in only forced air-cooled systems as there are some components such as I/O or OpenCapi cards that require high-thermal cooling. Due to the wiring and motherboard design constraints, design and architecture of these cards are not quite flexible which affects the cooling power of such cards. In today's market, each card dissipates $\sim$40 W with quad small form-factor pluggable optical transceivers. The high-power generation is very challenging for only forced air-cooled system especially with dramatically increasing field programable gate arrays powers due to the preheating [144]. Thus, with on-chip hot spot heat fluxes approaching $\sim 1\,\mathrm{kW \cdot cm^{-2}}$ and high-power servers exceeding $\sim$3 kW, next-generation thermal cooling techniques are crucial to address the challenges and current limitations [145].

Similar device-to-package-to-system thermal challenges arise for next-generation power electronics and sensors found in highly automated and electrified vehicles. From a power electronics perspective, single- or two-phase remote (i.e., power package separated from cold plate) cooling strategies have been extensively investigated at the package level [146], and new near-junction cooling solutions [43,44] are being actively explored for compact, highly integrated, and high-performance alternatives that may address power semiconductor heat fluxes approaching $\sim 1\,\mathrm{kW \cdot cm^{-2}}$. Here, TIM and thermal crosstalk issues may again be a concern as active gate drive components are eventually integrated into or placed close to the power package. Thermal routing

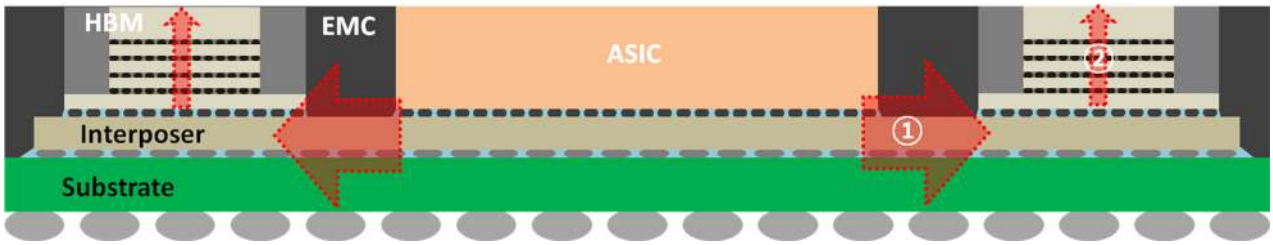

Fig. 13 Thermal metamaterial application example on 2.5D package platform. Cross-sectional schematic of a potential package platform where thermal metamaterials could be introduced in the area (1) to reduce thermal crosstalk between ASIC and HBM and in the area (2) to facilitate heat dissipation through 3D stacks.

for such gate drive components is already a challenge point [45], and higher levels of integration for future mobility solutions (e.g., in-wheel motors) will continue to require innovative heat flow control and anisotropic thermal routing in three-dimensions at multiple scales. Thermal metamaterial-related architectures may now be necessary to better regulate the path of heat transfer. In addition to microelectronics-related applications, advanced sensors, photonic components found in solid-state waveguide devices, such as ring resonators or thermal phase-shifters, may also benefit from the incorporation of effective thermal conduits facilitated through geometrically considered placement of meta-atom based materials (see Sec. 2.1) to reduce transient response time and required actuation power [147,148]. Furthermore, the integration of lasers on-chip for photonic sensing and processing solutions also presents a host of thermal challenges due to the proximity of the light source near other potentially thermally sensitive components [149]. Thus, highly local-scale application of thermal metamaterials as suggested by Loke et al. [150] is definite area for future exploration for a variety of device-to-package applications.

4.2 Thermal Metamaterials for Packaging and Future Research. While thermal metamaterials with extraordinary properties are expected to be useful for thermal management applications [25], most of the work is limited to materials investigations and fundamental studies. There have been recent developments in using thermal metamaterials and taking advantage of heat flow control for electronic systems at the PCB-level [23] and with microelectromechanical systems [151]. Further investigations on the implementation of thermal metamaterials could address chip-integrated and package-level thermal management challenges. For example, for 2.5D packages, thermal metamaterials based on anisotropic material layouts for thermally cloaking, or isolating designs could be used to engineer heat dissipation in a deterministic manner and minimize thermal crosstalk between ASIC and HBM (Fig. 13). Optimal patterning of interposers, as well as TTSVs, could not only minimize thermal crosstalk but also limit the temperature increase of the ASIC. For 3D packages, thermal metamaterials based on bending or shifting designs could be used to guide the heat efficiently toward heat sinks and facilitate heat dissipation through HBM stacks. Thermal management of 3D stacks could be further addressed by optimal arrangements of TSVs and potential use of silicon-based thermoelectric cooling elements [34,36,37,39,59,61,132,136]. Several studies discussed the potential use of thermal metamaterials for circuit designs [15,19,20,152]. Their work demonstrated an optimal separation of a hot spot region and a temperature-sensitive device region using the thermal metamaterial design functions in one PCB. We can infer that thermal metamaterial designs can be applied to heterogeneous packages where multiple chips are used and multiple hot spots are expected.

While the progress and development of thermal metamaterials are promising for electronic packaging applications, direct implementation of those thermal metamaterial designs in current packaging systems will be very challenging, due to disruption of used process flows, and further studies on their effectiveness, compatibility, and scalability are necessary. Dede et al. [152] provides an example design of a synchronous buck converter utilizing the various aspects of thermal metamaterials. It also talks about the lacking electrothermal design methodologies that are needed for incorporation of thermal metamaterial designs. Evans et al. [153] demonstrates-power packaging design tools, in which the tool could be adapted to incorporate thermal metamaterial design into power electronics. Thus, electronics computer-aided design (ECAD) or multi-objective optimization tools relevant to different applications (e.g., Ref. [153] for power packaging, [154,155] for light-emitting diode packaging, and [156] for microserver design) could be modified to foster further integration of anisotropic heat spreaders or thermal metamaterials.

From a material perspective, thermal metamaterial designs would also benefit from advances in materials science research that push the limits of high-thermal conductivity, k_{high}, and low-thermal conductivity, k_{low}, materials since the thermal-conductivity contrast ratio, k_{high}/k_{low}, is critical in the establishment of effective designs. This ratio crucially affects both heat flow control and the overall device maximum temperature profile. Hence, advances in robust, reliable, and cost effective anisotropic thermal composite substrates beyond traditional PCBs and ceramic substrates that allow for easy implementation of high-thermal-conductivity contrast ratios are needed.

Practical implementation of PCMs into new substrate or carrier configurations is then another logical and challenging next-step opportunity to address transient response. Nonsolid-state PCMs have challenges associated with encapsulation, voiding, and long-term reliability [157]. However, as discussed in Sec. 2.3, utilization of these materials introduces new ways to actively manipulate heat flow paths. Thus, to ensure packaging viability, compatibility, and scalability, the choices of materials for thermal metamaterial designs needs to be carefully reviewed. To avoid potential thermal expansion and long-term interface issues, thermal metamaterial designs based on a homogeneous material may be preferred. Materials, with well-defined geometric structures, that are easily fabricated or manufactured would be additionally useful.

Moving beyond thermal metamaterials that are passively designed to manipulate directions of heat flow, future research on active thermal metamaterial devices such as thermal diodes, switches, or regulators could lead to new pathways of temperature control and dynamic thermal management for electronic packaging. The aforementioned PCMs fall into this category, as well, and may be leveraged likewise in temperature adaptive response.

Finally, we expect future research could take on system-level studies that focus on implementation of thermal metamaterials in high-performance heterogeneous packages as related to frontier, 5G-related communications, or photonics applications.

5 Summary and Outlook

In this paper, we have reviewed the recent progress in conduction-based thermal metamaterials and considered their potential applications to electronic packaging. Such aspects indicate that basic research in thermal metamaterials can make a

positive impact not only on the fundamental understanding of heat transfer but also on designs of next-generation electronics and photonics. As notable examples, 2.5D and 3D packages can suffer from nontrivial thermal management challenges such as thermal crosstalk and local hot spots, and associated packaging designs may benefit from the new capabilities of controlling heat transfer paths in a deterministic manner, underlying the scope and aim of thermal metamaterial design. We have reviewed thermal metamaterial approaches including: (1) anisotropic heat spreaders and diffusers, (2) heat cloaking and isolating, and (3) heat guiding and bending and provided a comprehensive overview of the related studies from the recent literature. We have analyzed the thermal challenges of advanced heterogeneous packaging from two points of view involving: (1) high-performance chips that are laterally placed close to each other while their temperature-sensitivity and mechanical-reliability metrics are different (via the 2.5D package platform); and (2) high-performance chips that are vertically stacked while the thermal resistance increases with the number of stacked chips (via the 3D package platform).

While significant attention in the electronic packaging community has been given to various thermal management techniques, conventional approaches are usually confined to an individual design scale such as the device, package, or system. Many prior solution techniques operate in isolation and may ultimately conflict with each other. We have discussed the outlook on applying thermal metamaterials for electronic applications, and metamaterial solutions could be used for thermal management at all of these scales. While a thermal metamaterial design may be a good heat transfer solution in of itself, further research and development into associated and required multidisciplinary electronic packaging methodologies may hold the key to synergy between thermal management techniques at multiple levels. This observation and analysis encourage new ECAD design tools, base material systems, and active devices as critical future research directions. Thus, in the future, research on thermal management may logically combine efforts across technical fields by leveraging the metamaterial concept.

Acknowledgment

The authors would like to thank Dr. Tae Hwan Kim, Dr. Young Hoon Hyun, and Dr. Bangwon Lee at Samsung Electronics for helpful discussions.

Funding Data

- Samsung Electronics and the National Science Foundation (CMMI-1902685) (Funder IDs: 10.13039/100004358 and 10.13039/100000001).
- National Science Foundation (CBET-1606192) (Funder ID: 10.13039/100000001).

Nomenclature

I = applied current
ipop = interposer package on package
$k_{a\text{-}h}$ = thermal conductivity of region *a*-*h* of the perfect thermal diffuser
k_A = thermal conductivity of material A
k_B = thermal conductivity of material B
k_{Cu} = thermal conductivity of copper
k_{hb} = thermal conductivity of the host background material
k_{high} = high-thermal conductivity
k_{ij} = second-order thermal-conductivity tensor
k_{low} = low-thermal conductivity
k_{PDMS} = thermal conductivity of PDMS
k_x, k_y = in-plane thermal conductivity
k_z = cross-plane thermal conductivity
k_1 = thermal conductivity of material 1
k_2 = thermal conductivity of material 2
q'' = input heat flux to the perfect thermal diffuser
q_i = heat flux in the *i*th direction
sip = system in package
t = time
T_1 = temperature applied to the chip
T_2 = temperature applied to the spreader
θ = composite layer orientation
ϕ = heat flux bending angle
∇T_j = temperature gradient in the *j*th direction

References

[1] Schurig, D., Mock, J. J., Justice, B. J., Cummer, S. A., Pendry, J. B., Starr, A. F., and Smith, D. R., 2006, "Metamaterial Electromagnetic Cloak at Microwave Frequencies," Science, **314**(5801), pp. 977–980.
[2] Liu, R., Ji, C., Mock, J. J., Chin, J. Y., Cui, T. J., and Smith, D. R., 2009, "Broadband Ground-Plane Cloak," Science, **323**(5912), pp. 366–369.
[3] Cai, W., Chettiar, U. K., Kildishev, A. V., and Shalaev, V. M., 2007, "Optical Cloaking With Metamaterials," Nat. Photonics, **1**(4), pp. 224–227.
[4] Valentine, J., Li, J., Zentgraf, T., Bartal, G., and Zhang, X., 2009, "An Optical Cloak Made of Dielectrics," Nat. Mater., **8**(7), pp. 568–571.
[5] Gabrielli, L. H., Cardenas, J., Poitras, C. B., and Lipson, M., 2009, "Silicon Nanostructure Cloak Operating at Optical Frequencies," Nat. Photonics, **3**(8), pp. 461–463.
[6] Ergin, T., Stenger, N., Brenner, P., Pendry, J. B., and Wegener, M., 2010, "Three-Dimensional Invisibility Cloak at Optical Wavelengths," Science, **328**(5976), pp. 337–339.
[7] Zhang, B., Luo, Y., Liu, X., and Barbastathis, G., 2011, "Macroscopic Invisibility Cloak for Visible Light," Phys. Rev. Lett., **106**(3), p. 033901.
[8] Chen, X., Luo, Y., Zhang, J., Jiang, K., Pendry, J. B., and Zhang, S., 2011, "Macroscopic Invisibility Cloaking of Visible Light," Nat. Commun., **2**, p. 176.
[9] Li, J. Y., Gao, Y., and Huang, J. P., 2010, "A Bifunctional Cloak Using Transformation Media," J. Appl. Phys., **108**(7), p. 074504.
[10] Guenneau, S., Amra, C., and Veynante, D., 2012, "Transformation Thermodynamics: Cloaking and Concentrating Heat Flux," Opt. Express, **20**(7), pp. 8207–8218.
[11] Han, T., Yuan, T., Li, B., and Qiu, C. W., 2013, "Homogeneous Thermal Cloak With Constant Conductivity and Tunable Heat Localization," Sci. Rep., **3**, p. 1593.
[12] Narayana, S., and Sato, Y., 2012, "Heat Flux Manipulation With Engineered Thermal Materials," Phys. Rev. Lett., **108**(21), p. 214303.
[13] Schittny, R., Kadic, M., Guenneau, S., and Wegener, M., 2013, "Experiments on Transformation Thermodynamics: Molding the Flow of Heat," Phys. Rev. Lett., **110**(19), p. 195901.
[14] Ma, Y., Lan, L., Jiang, W., Sun, F., and He, S., 2013, "A Transient Thermal Cloak Experimentally Realized Through a Rescaled Diffusion Equation With Anisotropic Thermal Diffusivity," NPG Asia Mater., **5**(11), pp. e73–e73.
[15] Dede, E. M., Nomura, T., Schmalenberg, P., and Seung Lee, J., 2013, "Heat Flux Cloaking, Focusing, and Reversal in Ultra-Thin Composites Considering Conduction-Convection Effects," Appl. Phys. Lett., **103**(6), p. 063501.
[16] Ma, Y., Liu, Y., Raza, M., Wang, Y., and He, S., 2014, "Experimental Demonstration of a Multiphysics Cloak: Manipulating Heat Flux and Electric Current Simultaneously," Phys. Rev. Lett., **113**(20), p. 205501.
[17] Han, T., Bai, X., Gao, D., Thong, J. T. L., Li, B., and Qiu, C. W., 2014, "Experimental Demonstration of a Bilayer Thermal Cloak," Phys. Rev. Lett., **112**(5), p. 054302.
[18] Xu, H., Shi, X., Gao, F., Sun, H., and Zhang, B., 2014, "Ultrathin Three-Dimensional Thermal Cloak," Phys. Rev. Lett., **112**(5), p. 054301.
[19] Dede, E. M., 2010, "Simulation and Optimization of Heat Flow Via Anisotropic Material Thermal Conductivity," Comput. Mater. Sci., **50**(2), pp. 510–515.
[20] Dede, E. M., Nomura, T., and Lee, J., 2014, "Thermal-Composite Design Optimization for Heat Flux Shielding, Focusing, and Reversal," Struct. Multidiscip. Optim., **49**(1), pp. 59–68.
[21] Fujii, G., and Akimoto, Y., 2019, "Optimizing the Structural Topology of Bifunctional Invisible Cloak Manipulating Heat Flux and Direct Current," Appl. Phys. Lett., **115**(17), p. 174101.
[22] Han, T., and Qiu, C. W., 2016, "Transformation Laplacian Metamaterials: Recent Advances in Manipulating Thermal and Dc Fields," J. Opt. (United Kingdom), **18**(4), p. 044003.
[23] Dede, E. M., Zhou, F., Schmalenberg, P., and Nomura, T., 2018, "Thermal Metamaterials for Heat Flow Control in Electronics," ASME J. Electron. Packag., **140**(1), p. 010904.
[24] Li, Y., Bai, X., Yang, T., Luo, H., and Qiu, C. W., 2018, "Structured Thermal Surface for Radiative Camouflage," Nat. Commun., **9**(1), pp. 1–7.
[25] Jung, K. W., Zhang, C., Liu, T., Asheghi, M., and Goodson, K. E., 2018, "Thermal Management Research-From Power Electronics to Portables," Digest of Technical Papers—Symposium on VLSI Technology, Honolulu, HI, June 18–22, pp. 17–18.
[26] Moore, A. L., and Shi, L., 2014, "Emerging Challenges and Materials for Thermal Management of Electronics," Mater. Today, **17**(4), pp. 163–174.

[27] Ramalingam, S., 2016, "HBM Package Integration: Technology Trends, Challenges and Applications," IEEE Hot Chips 28 Symposium, HCS 2016, Cupertino, CA, Aug. 21–23, pp. 1–7.
[28] You, S. H., Jeon, S., Oh, D., Kim, K., Kim, J., Cha, S. Y., and Kim, G., 2018, "Advanced Fan-Out Package SI/PI/Thermal Performance Analysis of Novel RDL Packages," Proceedings—Electronic Components and Technology Conference, San Diego, CA, May 29–June 1, pp. 1295–1301.
[29] Zhu, Y., Wang, B., Li, D., and Zhao, J., 2016, "Integrated Thermal Analysis for Processing in Die-Stacking Memory," ACM International Conference Proceeding Series, Washington, DC, Oct. 3–6, pp. 402–414.
[30] Hsieh, C. C., Wu, C. H., and Yu, D., 2016, "Analysis and Comparison of Thermal Performance of Advanced Packaging Technologies for State-of-the-Art Mobile Applications," Proceedings—Electronic Components and Technology Conference, Las Vegas, NV, May 31–June 3, pp. 1430–1438.
[31] He, X., and Wu, L., 2013, "Design of Two-Dimensional Open Cloaks With Finite Material Parameters for Thermodynamics," Appl. Phys. Lett., **102**(21), p. 211912.
[32] Dede, E. M., Schmalenberg, P., Nomura, T., and Ishigaki, M., 2015, "Design of Anisotropic Thermal Conductivity in Multilayer Printed Circuit Boards," IEEE Trans. Compon., Packag. Manuf. Technol., **5**(12), pp. 1763–1774.
[33] Kang, S., Cha, J., Seo, K., Kim, S., Cha, Y., Lee, H., Park, J., and Choi, W., 2019, "Temperature-Responsive Thermal Metamaterials Enabled by Modular Design of Thermally Tunable Unit Cells," Int. J. Heat Mass Transfer, **130**, pp. 469–482.
[34] Cong, J., and Zhang, Y., 2005, "Thermal Via Planning for 3-D ICs," IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, ICCAD, San Jose, CA, Nov. 6–10, pp. 745–752.
[35] Wong, E., and Lim, S. K., 2006, "3D Floorplanning With Thermal Vias," Proceedings of the Design Automation and Test in Europe Conference, Munich, Germany, Mar. 6–10, pp. 1–6.
[36] Li, X., Ma, Y., Hong, X., Dong, S., and Cong, J., 2008, "LP Based White Space Redistribution for Thermal Via Planning and Performance Optimization in 3D ICs," Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC, Seoul, South Korea, Mar. 21–24, pp. 209–212.
[37] Wen, C. C., Chen, Y. J., and Ruan, S. J., 2013, "Cluster-Based Thermal-Aware 3D-Floorplanning Technique With Post-Floorplan TTSV Insertion at Via-Channels," Proceedings of the 5th Asia Symposium on Quality Electronic Design, ASQED 2013, Penang, Malaysia, Aug. 26–28, pp. 200–207.
[38] Shang, Y., Zhang, C., Yu, H., Tan, C. S., Zhao, X., and Lim, S. K., 2013, "Thermal-Reliable 3D Clock-Tree Synthesis Considering Nonlinear Electrical-Thermal-Coupled TSV Model," Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC, Yokohama, Japan, Jan. 22–25, pp. 693–698.
[39] Budhathoki, P., Henschel, A., and Elfadel, I. A. M., 2014, "Thermal-Driven 3D Floorplanning Using Localized TSV Placement," IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), Austin, TX, May 28–30, pp. 1–4.
[40] Ren, Z., Alqahtani, A., Bagherzadeh, N., and Lee, J., 2020, "Thermal TSV Optimization and Hierarchical Floorplanning for 3D Integrated Circuits," IEEE Trans. Compon., Packag. Manuf. Technol., **10**(4), pp. 599–610.
[41] Lee, P. S., Garimella, S. V., and Liu, D., 2005, "Investigation of Heat Transfer in Rectangular Microchannels," Int. J. Heat Mass Transfer, **48**(9), pp. 1688–1704.
[42] Das, S. K., Choi, S. U. S., Yu, W., and Pradeep, T., 2007, *Nanofluids: Science and Technology*, John Wiley & Sons, Hoboken, NJ.
[43] Jung, K. W., Kharangate, C. R., Lee, H., Palko, J., Zhou, F., Asheghi, M., Dede, E. M., and Goodson, K. E., 2019, "Embedded Cooling With 3D Manifold for Vehicle Power Electronics Application: Single-Phase Thermal-Fluid Performance," Int. J. Heat Mass Transfer, **130**, pp. 1108–1119.
[44] Zhou, F., Joshi, S. N., Liu, Y., and Dede, E. M., 2019, "Near-Junction Cooling for next-Generation Power Electronics," Int. Commun. Heat Mass Transfer, **108**, p. 104300.
[45] Dede, E. M., Liu, Y., Joshi, S. N., Zhou, F., Lohan, D. J., and Shin, J. W., 2019, "Optimal Design of Three- Dimensional Heat Flow Structures for Power Electronics Applications," ASME J. Therm. Sci. Eng. Appl., **11**(2), p. 021011.
[46] Hwang, T., Oh, D. K. S., Kim, J., Song, E., Kim, T., Kim, K., Lee, J., and Kim, T., 2019, "The Thermal Dissipation Characteristics of the Novel System-in-Package Technology (ICE-SiP) for Mobile and 3D High-End Packages," Proceedings—Electronic Components and Technology Conference, Las Vegas, NV, May 28–31, pp. 614–619.
[47] Shen, X., Li, Y., Jiang, C., and Huang, J., 2016, "Temperature Trapping: Energy-Free Maintenance of Constant Temperatures as Ambient Temperature Gradients Change," Phys. Rev. Lett., **117**(5), p. 055501.
[48] Han, T., Bai, X., Thong, J. T. L., Li, B., and Qiu, C. W., 2014, "Full Control and Manipulation of Heat Signatures: Cloaking, Camouflage and Thermal Metamaterials," Adv. Mater., **26**(11), pp. 1731–1734.
[49] Moccia, M., Castaldi, G., Savo, S., Sato, Y., and Galdi, V., 2014, "Independent Manipulation of Heat and Electrical Current Via Bifunctional Metamaterials," Phys. Rev. X, **4**(2), p. 021025.
[50] Li, Y., Shen, X., Wu, Z., Huang, J., Chen, Y., Ni, Y., and Huang, J., 2015, "Temperature-Dependent Transformation Thermotics: From Switchable Thermal Cloaks to Macroscopic Thermal Diodes," Phys. Rev. Lett., **115**(19), p. 195503.
[51] Nguyen, D. M., Xu, H., Zhang, Y., and Zhang, B., 2015, "Active Thermal Cloak," Appl. Phys. Lett., **107**(12), p. 121901.
[52] Maldovan, M., 2013, "Sound and Heat Revolutions in Phononics," Nature, **503**(7475), pp. 209–217.
[53] Chang, C. W., Okawa, D., Majumdar, A., and Zettl, A., 2006, "Solid-State Thermal Rectifier," Science, **314**(5802), pp. 1121–1124.
[54] Luo, Z., Maassen, J., Deng, Y., Du, Y., Garrelts, R. P., Lundstrom, M. S., Ye, P. D., and Xu, X., 2015, "Anisotropic in-Plane Thermal Conductivity Observed in Few-Layer Black Phosphorus," Nat. Commun., **6**(1), pp. 1–8.
[55] Smith, B., Vermeersch, B., Carrete, J., Ou, E., Kim, J., Mingo, N., Akinwande, D., and Shi, L., 2017, "Temperature and Thickness Dependences of the Anisotropic In-Plane Thermal Conductivity of Black Phosphorus," Adv. Mater., **29**(5), p. 1603756.
[56] Tang, J., Wang, H. T., Lee, D. H., Fardy, M., Huo, Z., Russell, T. P., and Yang, P., 2010, "Holey Silicon as an Efficient Thermoelectric Material," Nano Lett., **10**(10), pp. 4279–4283.
[57] Lee, J., Lim, J., and Yang, P., 2015, "Ballistic Phonon Transport in Holey Silicon," Nano Lett., **15**(5), pp. 3273–3279.
[58] Lim, J., Wang, H. T., Tang, J., Andrews, S. C., So, H., Lee, J., Lee, D. H., Russell, T. P., and Yang, P., 2016, "Simultaneous Thermoelectric Property Measurement and Incoherent Phonon Transport in Holey Silicon," ACS Nano, **10**(1), pp. 124–132.
[59] Ren, Z., and Lee, J., 2018, "Thermal Conductivity Anisotropy in Holey Silicon Nanostructures and Its Impact on Thermoelectric Cooling," Nanotechnology, **29**(4), p. 045404.
[60] Ren, Z., Yu, Z., Kim, J. C., and Lee, J., 2019, "TSV-Integrated Thermoelectric Cooling by Holey Silicon for Hot Spot Thermal Management," Nanotechnology, **30**(3), p. 035201.
[61] Wang, P., and Bar-Cohen, A., 2007, "On-Chip Hot Spot Cooling Using Silicon Thermoelectric Microcoolers," J. Appl. Phys., **102**(3), p. 034503.
[62] Vemuri, K. P., and Bandaru, P. R., 2016, "An Approach Towards a Perfect Thermal Diffuser," Sci. Rep., **6**, p. 29649.
[63] Hamed, A., and Ndao, S., 2018, "High Anisotropy Metamaterial Heat Spreader," Int. J. Heat Mass Transfer, **121**, pp. 10–14.
[64] Liu, Y., Jiang, W., He, S., and Ma, Y., 2014, "An Efficient Plate Heater With Uniform Surface Temperature Engineered With Effective Thermal Materials," Opt. Express, **22**(14), pp. 17006–17015.
[65] Han, T., Yang, P., Li, Y., Lei, D., Li, B., Hippalgaonkar, K., and Qiu, C. W., 2018, "Full-Parameter Omnidirectional Thermal Metadevices of Anisotropic Geometry," Adv. Mater., **30**(49), p. 1804019.
[66] Vemuri, K. P., Canbazoglu, F. M., and Bandaru, P. R., 2014, "Guiding Conductive Heat Flux Through Thermal Metamaterials," Appl. Phys. Lett., **105**(19), p. 193904.
[67] Raza, M., Liu, Y., Lee, E. H., and Ma, Y., 2016, "Transformation Thermodynamics and Heat Cloaking: A Review," J. Opt. (United Kingdom), **18**(4), p. 044002.
[68] Fan, C. Z., Gao, Y., and Huang, J. P., 2008, "Shaped Graded Materials With an Apparent Negative Thermal Conductivity," Appl. Phys. Lett., **92**(25), p. 251907.
[69] Chen, T., Weng, C. N., and Chen, J. S., 2008, "Cloak for Curvilinearly Anisotropic Media in Conduction," Appl. Phys. Lett., **93**(11), p. 114103.
[70] Alù, A., and Engheta, N., 2005, "Achieving Transparency With Plasmonic and Metamaterial Coatings," Phys. Rev. E—Stat. Nonlinear, Soft Matter Phys., **72**(1), p. 016623.
[71] Fachinotti, V. D., Ciarbonetti, Á. A., Peralta, I., and Rintoul, I., 2018, "Optimization-Based Design of Easy-to-Make Devices for Heat Flux Manipulation," Int. J. Therm. Sci., **128**, pp. 38–48.
[72] Shi, L., Dames, C., Lukes, J. R., Reddy, P., Duda, J., Cahill, D. G., Lee, J., Marconnet, A., Goodson, K. E., Bahk, J. H., Shakouri, A., Prasher, R. S., Felts, J., King, W. P., Han, B., and Bischof, J. C., 2015, "Evaluating Broader Impacts of Nanoscale Thermal Transport Research," Nanoscale Microscale Thermophys. Eng., **19**(2), pp. 127–165.
[73] Bergman, D. J., 1978, "The Dielectric Constant of a Composite Material-A Problem in Classical Physics," Phys. Rep., **43**(9), pp. 377–407.
[74] Li, Y., Zhu, K. J., Peng, Y. G., Li, W., Yang, T., Xu, H. X., Chen, H., Zhu, X. F., Fan, S., and Qiu, C. W., 2019, "Thermal Meta-Device in Analogue of Zero-Index Photonics," Nat. Mater., **18**(1), pp. 48–54.
[75] Park, G., Kang, S., Lee, H., and Choi, W., 2017, "Tunable Multifunctional Thermal Metamaterials: Manipulation of Local Heat Flux Via Assembly of Unit-Cell Thermal Shifters," Sci. Rep., **7**, p. 41000.
[76] Vemuri, K. P., and Bandaru, P. R., 2013, "Geometrical Considerations in the Control and Manipulation of Conductive Heat Flux in Multilayered Thermal Metamaterials," Appl. Phys. Lett., **103**(13), p. 133111.
[77] Liu, D. P., Chen, P. J., and Huang, H. H., 2018, "Realization of a Thermal Cloak-Concentrator Using a Metamaterial Transformer," Sci. Rep., **8**(1), pp. 1–11.
[78] Zhang, X., Lin, J. K., Wickramanayaka, S., Zhang, S., Weerasekera, R., Dutta, R., Chang, K. F., Chui, K. J., Li, H. Y., Wee Ho, D. S., Ding, L., Katti, G., Bhattacharya, S., and Kwong, D. L., 2015, "Heterogeneous 2.5D Integration on Through Silicon Interposer," Appl. Phys. Rev., **2**(2), p. 021308.
[79] Liu, D., and Park, S., 2014, "Three-Dimensional and 2.5 Dimensional Interconnection Technology: State of the Art," ASME J. Electron. Packag., **136**(1), p. 014001.
[80] Lau, J. H., 2019, "Recent Advances and Trends in Heterogeneous Integrations," J. Microelectron. Electron. Packag., **16**(2), pp. 45–77.
[81] Lau, J. H., 2019, "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging," ASME J. Electron. Packag., **141**(4), p. 040801.
[82] Hu, Y., Sarvey, T., Bakir, M., and Joshi, Y., 2018, "Design and Parametric Study of Microfluidic Cooling Manifold for 2.5D-SICs With Dielectric Coolant," Proceedings of the 17th InterSociety Conference on Thermal and

Thermomechanical Phenomena in Electronic Systems, ITherm 2018, San Diego, CA, May 29–June 1, pp. 379–383.
[83] Kelly, M., Fosnot, P., Wei, J., Min, M., and Galloway, J., 2018, "Multi-Die Packaging and Thermal Superposition Modeling," 34th Annual Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), **85284**(1), San Jose, CA, Mar. 19–23, pp. 21–25.
[84] Hwang, T., Oh, D., Song, E., Kim, K., Kim, J., and Lee, S., 2018, "Study of Advanced Fan-Out Packages for Mobile Applications," Proceedings—Electronic Components and Technology Conference, San Diego, CA, May 29–June 1, pp. 343–348.
[85] Hong, J., Choi, K., Oh, D., Park, S. B., Shao, S., Wang, H., Niu, Y., and Pham, V. L., 2018, "Design Guideline of 2.5D Package With Emphasis on Warpage Control and Thermal Management," Proceedings—Electronic Components and Technology Conference, San Diego, CA, May 29–June 1, pp. 682–692.
[86] Zhang, H., Sui, Y., Lin, T., and Liu, H., 2018, "Transient Thermal Characterization of Junction to Case Thermal Resistance for 2.5D Packages," Proceedings—19th International Conference on Electronic Packaging Technology (ICEPT), Shanghai, China, Aug. 8–11, pp. 115–120.
[87] Zhang, H. Y., 2014, "Thermal Analysis of 2.5-D Package Designs With Joule Heating Effect Along TSVs," Proceedings of the Electronic Packaging Technology Conference (EPTC), Chengdu, China, Aug. 12–15, pp. 711–717.
[88] Oprins, H., and Beyne, E., 2014, "Generic Thermal Modeling Study of the Impact of 3D—Interposer Material and Thickness Options on the Thermal Performance and Die-to-Die Thermal Coupling," Proceedings of Intersociety Conference on Thermomechanical Phenomena in Electronic Systems, Orlando, FL, May 27–30, pp. 72–78.
[89] Zhang, H. Y., Zhang, X. W., Lau, B. L., Lim, S., Ding, L., and Yu, M. B., 2014, "Thermal Characterization of Both Bare Die and Overmolded 2.5-D Packages on Through Silicon Interposers," IEEE Trans. Compon., Packag. Manuf. Technol., **4**(5), pp. 807–816.
[90] Zhang, H. Y., and Zhang, X. W., 2015, "Study of Thermally Enhanced 2.5D Packages With Multi-Chips Molded on Silicon Interposer," ASME J. Electron. Mater., **44**(7), pp. 2396–2405.
[91] Feng, Q., Tang, M., Fu, G., and Mao, J., 2016, "Fast Transient Thermal Simulation of 2.5-D Packages on Through Silicon Via Interposer," IEEE 20th Workshop on Signal and Power Integrity (SPI)—Proceedings, Turin, Itlay, May 8–11, pp. 1–4.
[92] Zhang, H. Y., Wang, Z. Q., and Lin, T. Y., 2016, "Thermal Evaluation of Partially Molded 2.5D Package With Pin Fin Heat Sink Cooling," 17th International Conference on Electronic Packaging Technology (ICEPT), Wuhan, China, Aug. 16–19, pp. 461–467.
[93] Usman, A., Shah, E., Satishprasad, N. B., Chen, J., Bohlemann, S. A., Shami, S. H., Eftekhar, A. A., and Adibi, A., 2017, "Interposer Technologies for High-Performance Applications," IEEE Trans. Compon., Packag. Manuf. Technol., **7**(6), pp. 819–828.
[94] Minz, J., Wong, E., and Lim, S. K., 2005, "Thermal and Crosstalk-Aware Physical Design for 3D System-on-Package," Proceedings—Electronic Components and Technology Conference, Lake Buena Vista, FL, May 31–June 3, pp. 824–831.
[95] Ravichandran, S., Yamada, S., Liu, F., Smet, V., Kathaperumal, M., and Tummala, R., 2019, "Low-Cost Non-TSV Based 3D Packaging Using Glass Panel Embedding (GPE) for Power-Efficient, High-Bandwidth Heterogeneous Integration," Proceedings—Electronic Components and Technology Conference, Las Vegas, NV, May 28–31, pp. 1796–1802.
[96] Minz, J., and Lim, S. K., 2006, "Block-Level 3-D Global Routing With an Application to 3-D Packaging," IEEE Trans. Comput. Des. Integr. Circuits Syst., **25**(10), pp. 2248–2257.
[97] Minz, J. R., Wong, E., Pathak, M., and Lim, S. K., 2006, "Placement and Routing for 3-D System-on-Package Designs," IEEE Trans. Compon. Packag. Technol., **29**(3), pp. 644–657.
[98] Scheuermann, M., Tian, S., Robertazzi, R., Wordeman, M., Bergeron, C., Jacobson, H., Restle, P., Silberman, J., and Tyberg, C., 2016, "Thermal Analysis of Multi-Layer Functional 3D Logic Stacks," IEEE International 3D Systems Integration Conference (3DIC), San Francisco, CA, Nov. 8–11, pp. 1–4.
[99] Ma, H., Yu, D., and Wang, J., 2012, "Thermal Analysis and Heat Dissipation Optimization of 3D Packaging With TSV Interposer," ICEPT-HDP Proceedings—13th International Conference on Electronic Packaging Technology and High Density Packaging, Guilin, China, Aug. 13–16, pp. 700–705.
[100] Rencz, M., 2005, "Thermal Issues in Stacked Die Packages," Annual IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, CA, Mar. 15–17, pp. 307–312.
[101] Kim, J., and Kim, Y., 2014, "HBM: Memory Solution for Bandwidth-Hungry Processors," IEEE Hot Chips 26 Symposium (HCS), Cupertino, CA, Aug. 10–12, pp. 1–24.
[102] Son, H. Y., Oh, T., Hong, J. W., Lee, B., Do, Shin, J. H., Kim, S. H., and Kim, N. S., 2016, "Mechanical and Thermal Characterization of TSV Multi-Chip Stacked Packages for Reliable 3D IC Applications," Proceedings—Electronic Components and Technology Conference, Las Vegas, NV, May 31–June 3, pp. 356–360.
[103] Jun, H., Cho, J., Lee, K., Son, H. Y., Kim, K., Jin, H., and Kim, K., 2017, "HBM (High Bandwidth Memory) DRAM Technology and Architecture," IEEE 9th International Memory Workshop (IMW), Monterey, CA, May 14–17, pp. 1–7.
[104] Emma, P. G., and Kursun, E., 2008, "Is 3D Chip Technology the Next Growth Engine for Performance Improvement?," IBM J. Res. Dev., **52**(6), pp. 541–552.
[105] Zhang, Y., Oh, H., and Bakir, M. S., 2013, "Within-Tier Cooling and Thermal Isolation Technologies for Heterogeneous 3D ICs," IEEE International 3D Systems Integration Conference (3DIC), San Francisco, CA, Oct. 2–4, pp. 1–6.
[106] Hoefflinger, B., 2011, "ITRS: The International Technology Roadmap for Semiconductors," Semiconductor Industry Association, Washington, DC, pp. 161–174.
[107] Hsu, F. C., Lin, J., Chen, S. M., Lin, P. Y., Fang, J., Wang, J. H., and Jeng, S. P., 2018, "3D Heterogeneous Integration With Multiple Stacking Fan-Out Package," Proceedings of Electronic Components and Technology Conference, San Diego, CA, May 29–June 1, pp. 337–342.
[108] Lee, C. C., Hung, C., Cheung, C., Yang, P. F., Kao, C. L., Chen, D. L., Shih, M. K., Chien, C. L. C., Hsiao, Y. H., Chen, L. C., Su, M., Alfano, M., Siegel, J., Din, J., and Black, B., 2016, "An Overview of the Development of a GPU With Integrated HBM on Silicon Interposer," Proceedings of Electronic Components and Technology Conference, Las Vegas, NV, May 31–June 3, pp. 1439–1444.
[109] Global Foundries, 2015, "Silicon, Interconnect, Packaging and Test Challenges From a Foundry Viewpoint," Semiconductor Wafer Test Workshop, San Diego, CA, June 7–10.
[110] Park, J. J., and Taya, M., 2006, "Design of Thermal Interface Material With High Thermal Conductivity and Measurement Apparatus," ASME J. Electron. Packag., **128**(1), pp. 46–52.
[111] Heng, H. C., Ben, V. S., Keok, K. H., and Jay, R., 2008, "Nondestructive Method of TIM Bondline Measurement in Flip Chips Package," Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium, Penang, Malaysia, Nov. 4–6, pp. 1–5.
[112] Lu, M. C., 2019, "Enhanced Sintered Silver for SiC Wide Bandgap Power Electronics Integrated Package Module," ASME J. Electron. Packag., **141**(3), p. 031002.
[113] Prasher, R., 2006, "Thermal Interface Materials: Historical Perspective, Status, and Future Directions," Proc. IEEE, **94**(8), pp. 1571–1586.
[114] Razeeb, K. M., Dalton, E., Cross, G. L. W., and Robinson, A. J., 2018, "Present and Future Thermal Interface Materials for Electronic Devices," Int. Mater. Rev., **63**(1), pp. 1–21.
[115] Zhang, Y., Heo, Y. J., Son, Y. R., In, I., An, K. H., Kim, B. J., and Park, S. J., 2019, "Recent Advanced Thermal Interfacial Materials: A Review of Conducting Mechanisms and Parameters of Carbon Materials," Carbon N. Y., **142**, pp. 445–460.
[116] Hou, S. Y., Chen, W. C., Hu, C., Chiu, C., Ting, K. C., Lin, T. S., Wei, W. H., Chiou, W. C., Lin, V. J. C., Chang, V. C. Y., Wang, C. T., Wu, C. H., and Yu, D., 2017, "Wafer-Level Integration of an Advanced Logic-Memory System Through the Second-Generation CoWoS Technology," IEEE Trans. Electron Devices, **64**(10), pp. 4071–4077.
[117] Oi, K., Otake, S., Shimizu, N., Watanabe, S., Kunimoto, Y., Kurihara, T., Koyama, T., Tanaka, M., Aryasomayajula, L., and Kutlu, Z., 2014, "Development of New 2.5D Package With Novel Integrated Organic Interposer Substrate With Ultra-Fine Wiring and High Density Bumps," Proceedings—Electronic Components and Technology Conference, Orlando, FL, May 27–30, pp. 348–353.
[118] Agrawal, A., Torrellas, J., and Idgunji, S., 2017, "Xylem: Enhancing Vertical Thermal Conduction in 3D Processor-Memory Stacks," Proceedings of the Annual International Symposium on Microarchitecture, MICRO, Boston, MA, Oct. 14-17, pp. 546–559.
[119] Chen, M. F., Chen, F. C., Chiou, W. C., and Yu, D. C. H., 2019, "System on Integrated Chips (SoIC(TM) for 3D Heterogeneous Integration," Proceedings 42nd Electronic Components and Technology Conference, Las Vegas, NV, May 28–31, pp. 594–599.
[120] Leduc, P., De Crécy, F., Fayolle, M., Charlet, B., Enot, T., Zussy, M., Jones, B., Barbé, J. C., Kernevez, N., Sillon, N., Maitrejean, S., Louis, D., and Passemard, G., 2007, "Challenges for 3D IC Integration: Bonding Quality and Thermal Management," Proceedings of the IEEE International Interconnect Technology Conference—Digest of Technical Papers, Burlingame, CA, June 4–6, pp. 210–212.
[121] Wakil, J., Colgan, E. G., and Chen, S., 2011, "Back-End-of-Line and Micro-C4 Thermal Resistance Contributions to 3-D Stack Packages," IEEE Trans. Compon., Packag. Manuf. Technol., **1**(7), pp. 1007–1014.
[122] Colgan, E. G., Polastre, R. J., Knickerbocker, J., Wakil, J., Gambino, J., and Tallman, K., 2013, "Measurement of Back End of Line Thermal Resistance for 3D Chip Stacks," Annual IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, CA, Mar. 17–21, pp. 23–28.
[123] Du, X., and Tang, Z., 2011, "Thermal Analysis of Four-Layer 3D IC With TSVs Based on Face-to-Back Bonding," IEEE Electrical Design of Advanced Packaging and Systems Symposium, EDAPS, Hanzhou, China, Dec. 12–14, pp. 1–4.
[124] Santos, C., Vivet, P., and Reis, R., 2014, "Thermal Impact of 3D Stacking and Die Thickness: Analysis and Characterization of a Memory-on-Logic 3D Circuit," 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marseille, France, Dec. 7–10, pp. 718–721.
[125] Koyanagi, M., Fukushima, T., and Tanaka, T., 2009, "High-Density Through Silicon Vias for 3-D LSIs," Proc. IEEE, **97**(1), pp. 49–59.
[126] Lee, M. J., Park, S. S., Ryu, D. S., Lee, M. J., Saiki, H., Mori, S., and Nagai, M., 2014, "Packaging Technology and Design Challenge for Fine Pitch Micro-Bump Cu-Pillar and BOT (Direct Bond on Substrate-Trace) Using TCNCP (Thermal Compression With Non-Conductive Paste Underfill) Method," IPC Apex Expo, Las Vegas, NV, Mar. 25–27.
[127] Zajac, P., Galicia, M., Maj, C., and Napieralski, A., 2016, "Impact of Floorplanning and Thermal Vias Placement on Temperature in 2D and 3D Processors," Microelectron. J., **52**, pp. 40–48.

[128] Pi, Y., Wang, W., and Jin, Y., 2016, "An Accurate Calculation Method on Thermal Effectiveness of TSV and Wire," Proceedings of the IEEE 18th Electronics Packaging Technology Conference, EPTC, Singapore, Nov. 30–Dec. 3, pp. 569–573.
[129] Clarke, H. A., and Murakami, K., 2011, "Thermal Effect of TSVs in 3D Die-Stacked Integrated Circuits," Proceedings 14th Euromicro Conference on Digital System Design: Architectures, Methods and Tools (DSD), Oulu, Finland, Aug. 31–Sept. 2, pp. 503–508.
[130] Ni, M., Su, Q., Tang, Z., and Kawa, J., 2011, "An Analytical Study on the Role of Thermal TSVs in a 3DIC Chip Stack," Date Workshop for 3D Integration, Grenoble, France, Mar. 14–18, pp. 137–141.
[131] Ayala, J. L., Sridhar, A., Atienza, D., and Leblebici, Y., 2012, "Through Silicon Via-Based Grid for Thermal Control in 3D Chips," *Design Technology for Heterogeneous Embedded Systems*, Springer, Dordrecht, The Netherlands, pp. 303–320.
[132] Cuesta, D., Risco-Martín, J. L., Ayala, J. L., and Hidalgo, J. I., 2015, "Thermal-Aware Floorplanner for 3D IC, Including TSVs, Liquid Microchannels and Thermal Domains Optimization," Appl. Soft Comput. J., **34**, pp. 167–177.
[133] Lim, S. K., 2011, "TSV-Aware 3D Physical Design Tool Needs for Faster Mainstream Acceptance of 3D ICs," Design Automation Conference, Anaheim, CA, pp. 321–326.
[134] Lau, J. H., and Yue, T. G., 2009, "Thermal Management of 3D IC Integration With TSV (Through Silicon Via)," Proceedings—Electronic Components and Technology Conference, San Diego, CA, May 26–29, pp. 635–640.
[135] Alqahtani, A., Ren, Z., Lee, J., and Bagherzadeh, N., 2018, "System-Level Analysis of 3D ICs With Thermal TSVs," ACM J. Emerg. Technol. Comput. Syst., **14**(3), pp. 1–16.
[136] Cao, K., Zhou, J., Wei, T., Chen, M., Hu, S., and Li, K., 2019, "A Survey of Optimization Techniques for Thermal-Aware 3D Processors," J. Syst. Archit., **97**, pp. 397–415.
[137] Yang, B., Wang, P., and Bar-Cohen, A., 2007, "Mini-Contact Enhanced Thermoelectric Cooling of Hot Spots in High Power Devices," IEEE Trans. Compon. Packag. Technol., **30**(3), pp. 432–438.
[138] Ohadi, M., and Qi, J., 2004, "Thermal Management of Harsh-Environment Electronics," Annual IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, CA, Mar. 11, pp. 231–240.
[139] Kandlikar, S. G., and Hayner, C. N., 2009, "Liquid Cooled Cold Plates for Industrial High-Power Electronic Devices Thermal Design and Manufacturing Considerations," Heat Transfer Eng., **30**(12), pp. 918–930.
[140] Tong, X. C., 2011, "Advanced Materials for Thermal Management of Electronic Packaging," Springer Science & Business Media, New York.
[141] Judy, J., Maynes, D., and Webb, B. W., 2002, "Characterization of Frictional Pressure Drop for Liquid Flows Through Microchannels," Int. J. Heat Mass Transfer, **45**(17), pp. 3477–3489.
[142] Morini, G. L., 2004, "Single-Phase Convective Heat Transfer in Microchannels: A Review of Experimental Results," Int. J. Therm. Sci., **43**(7), pp. 631–651.
[143] Yuksel, A., Mahaney, V., Marroquin, C., Tian, S., Hoffmeyer, M., Schultz, M., and Takken, T., 2019, "Thermal and Mechanical Design of the Fastest Supercomputer of the World in Cognitive Systems: IBM Power AC 922," ASME Paper No. IPACK2019-6444.
[144] Guelbenzu, G., Calabretta, N., and Raz, O., 2017, "Towards Standardization of Compact Data Center Switches," ICT Express, **3**(2), pp. 72–75.
[145] Bar-Cohen, A., Wang, P., and Rahim, E., 2007, "Thermal Management of High Heat Flux Nanoelectronic Chips," Microgravity Sci. Technol., **19**(3–4), pp. 48–52.
[146] Wang, P., Mccluskey, P., and Bar-Cohen, A., 2013, "Two-Phase Liquid Cooling for Thermal Management of Igbt Power Electronic Module," ASME J. Electron. Packag., **135**(2), p. 021001.
[147] Lei, S., Shen, A., and Enright, R., 2017, "Thermo-Optic Tuning Efficiency of Micro Ring Resonators on Low Thermal Resistance Silicon Photonics Substrates," ASME Paper No. IPACK2017-74181.
[148] Yoon, G. H., Dede, E. M., Nomura, T., and Schmalenberg, P., 2020, "Topology Optimization of Time-Transient Heat Conduction for Thermo-Optic Silicon Modulators," Int. J. Heat Mass Transfer, **157C**, p. 119862.
[149] Carroll, L., Lee, J. S., Scarcella, C., Gradkowski, K., Duperron, M., Lu, H., Zhao, Y., Eason, C., Morrissey, P., Rensing, M., Collins, S., Hwang, H. Y., and O'Brien, P., 2016, "Photonic Packaging: Transforming Silicon Photonic Integrated Circuits Into Photonic Devices," Appl. Sci., **6**(12), p. 426.
[150] Loke, D., Skelton, J. M., Chong, T. C., and Elliott, S. R., 2016, "Design of a Nanoscale, CMOS-Integrable, Thermal-Guiding Structure for Boolean-Logic and Neuromorphic Computation," ACS Appl. Mater. Interfaces, **8**(50), pp. 34530–34536.
[151] Roman, C. T., Coutu Jr, R. A., and Starman, L. A., 2010, "Thermal Management and Metamaterials," Proceedings of the Annual Conference on Experimental and Applied Mechanics, Indianapolis, IN, June 7–10, pp. 107–113.
[152] Dede, E. M., Wang, C. M., Liu, Y., Schmalenberg, P., Zhou, F., Shin, J. W., and Ishigaki, M., 2018, "Electrothermal Circuit Design With Heat Flow Control-Synchronous Buck Converter Case Study," IEEE Trans. Compon., Packag. Manuf. Technol., **8**(2), pp. 226–235.
[153] Evans, T. M., Le, Q., Mukherjee, S., Al Razi, I., Vrotsos, T., Peng, Y., and Mantooth, H. A., 2019, "PowerSynth: A Power Module Layout Generation Tool," IEEE Trans. Power Electron., **34**(6), pp. 5063–5078.
[154] Negrea, C., Gabor, L., and Svasta, P., 2012, "Optimization of LED Assembly for LCD Backlight Using Photo-Electro-Thermal Modeling and Simulation," IEEE 18th International Symposium for Design and Technology of Electronics Packages (SIITME)—Conference Proceedings, Alba Iulia, Romania, Oct. 25–28, pp. 247–252.
[155] Botau, A., and Negrea, C., 2013, "PCB Layout Optimization for LED Backlight Module Using FEM Simulation," IEEE 19th International Symposium for Design and Technology in Electronic Packaging (SIITME)—Conference Proceedings, Galati, Romania, Oct. 24–27, pp. 125–128.
[156] Cossale, M., Paredes, S., Luijten, R. P., and Michel, B., 2015, "Combined Power Delivery and Cooling for High Density, High Efficiency Microservers," THERMINIC—21st International Workshop on Thermal Investigations of ICs and Systems, Paris, France, Sept. 30–Oct. 2, pp. 1–6.
[157] Gonzalez-Nino, D., Boteler, L. M., Jankowski, N. R., Ibitayo, D., and Quintero, P. O., 2017, "Voiding Effects on the Thermal Response of Metallic Phase Change Materials Under Pulsed Power Loading," ASME Paper No. IPACK2017-74118.