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Recent Developments in p-type Oxide Semiconductor Materials and Devices

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The development of transparent p-type oxide semiconductors with good performance could be a true enabler for a variety of applications, where transparency, power efficiency and more circuit complexity are needed. Such applications include transparent electronics, displays, sensors, photovoltaics, memristors, and electrochromics. Hence, we review recent developments in materials and devices based on p-type oxide semiconductors, including ternary Cu-bearing oxides, binary copper oxides, tin monoxide, spinel oxides and nickel oxides. The crystal and electronic structures of these materials are reviewed, along with approaches to enhance valence band dispersion to reduce effective mass and increase mobility. Strategies to reduce the interfacial defects, off state current, and material instability are discussed. Furthermore, we show that promising progress has been made in the performance of various type of devices based on p-type oxides. For example, transparent oxide-based p-n junction diodes have experienced significantly improved performance, where rectification ratios $>10^7$ have been achieved. The performances of thin-film transistors and inverters have also been modestly improved. For example, thin-film transistors with field-effect mobilities exceeding 5 $cm^2\ V^{-1}\ s^{-1}$ have been reported. In addition, several innovative approaches were developed to fabricate transparent complementary metal oxide semiconductor (CMOS)

devices. These approaches include novel device fabrication schemes and utilization of surface chemistry effects, resulting in good inverter gains (as high as 120 has been demonstrated). Some progress has also been made in reducing the interfacial defects and off state currents using capping layers, high quality dielectrics and surface treatments. Resistive memory devices and hole transport layer in optoelectronic devices, mostly based on nickel oxide, have made decent progress. Transparent ferroelectric memory devices comprising p-type oxides have also been reported recently showing good hole mobilities (~3.3 cm^2 V^{-1} s^{-1}) and good retention characteristics. This even includes multistate memory devices that show good stability. Nanoscale (e.g. nanowire) devices have now been reported using p-type oxides and do show performance improvements at scaled device geometry. New process developments have been reported, and some p-type oxides can now be deposited using atomic layer deposition and chemical routes, with promising performances. However, despite these recent developments, p-type oxides still lag in performance behind the n-type counterparts, which have entered volume production in the display market. The recent successes along with the hurdles that stand in the way of commercial success of p-type oxide semiconductors are presented in this review.

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1. Introduction

Combining the visible range transparency and electrical conductivity, transparent conducting oxides (TCOs) and transparent semiconducting oxides (TSOs) in principle hold great potential in a variety of applications, including solar cells, solid-state sensors, flat panel displays, smart windows, electrochromics, transparent and flexible electronic devices. [1-5] For example, by employing high performance TSOs, transparent displays with higher pixel density (higher resolution) and higher refreshing frequency can be realized. [1, 6] In addition, using TSOs and TCOs, energy-efficient displays can be constructed which operate in standard lighting environments, where they may allow getting rid of the panel backlight which accounts for around 90% power consumption in current displays.[1, 6] Further, a variety of transparent electronic devices that may be deployed in security or entertainment applications will benefit greatly from developing better performing TSOs and TCOs (**Figure 1**).

However, many of the potential transparent electronic applications are limited by the lack of the availability of high performance p-type oxide semiconductors.[6-9] Hence, only applications which can be realized by using unipolar devices (based on n-type semiconductors) are currently able to capitalize on the promise of transparent semiconducting oxides. If equally well performing p-type TSOs were also available, more energy efficient and more complex transparent devices and circuits can be fabricated. For example, if a transparent CMOS device with good performance can be realized, similar types of circuits can be fabricated like in silicon technology. This would usher in an era of transparent gadgets that could affect many facets of our daily lives.[10] This is because CMOS circuit holds many advantages when compared to unipolar transistors, including: low power consumption, low waste heat generation, high noise margin, high logic swing output, high circuit integration density and architectural simplicity.[11-15]

The difficulty in achieving p-type TSOs with similar performance to the n-type ones comes from the unique electronic configuration of oxide materials. For n-type oxides, oxygen vacancies produce enough electrons and the electrons transport path in the conduction band minimum (CBM) is mainly composed of metal s orbitals. These s orbitals are spatially spread and could result in sufficient hybridization even in amorphous structure by employing heavy metal cations, where the highly dispersed and delocalized CBM facilitates a low electron effective mass and thus high mobility.[2, 16] In contrast, in p-type oxides, the creation of positive carriers (holes) is limited by (i) the high formation energy of native acceptors that produce holes, such as cation vacancies; (ii) the low formation energy of native donors that annihilate holes, such as anion vacancies.[17] Even when a certain concentration of holes is available, the transport path for holes, valence band maximum (VBM), consists mainly of anisotropic and localized oxygen 2p orbitals, resulting in a large hole effective mass and low mobility. All these effects render the realization of high performance p-type oxides more challenging.[15, 18] The chemical design concept for obtaining p-type TSOs was proposed by Kawazoe et al. in 1997.[15, 19, 20] According to this concept, promising p-type oxides should hold cationic species with (i) closed shell (i.e. $d^{10}s^{0}$) configuration to avoid coloration due to intra-atomic excitations and (ii) a comparable energy level to the oxygen 2p orbitals. The energy level of the d^{10} closed shell electrons is expected to overlap with that of the oxygen 2p electrons in order to form covalent bond, which could alleviate the localization of VB edge. The essence of this concept is to delocalize the VBM by forming the hybridization level between d levels of metal cations and 2p levels of oxygen anions. Also, tetrahedral coordination of oxide ions in some layered structures (e.g. delafossites) is believed to further reduce the localization of VB edge and avoid colorization from the d-d transition of adjacent Cu atoms. Following this principle, a series of novel p-type oxides with delafossite structure were discovered, namely $CuMO_2$ (M= Al, Ga and In, etc) and $SrCu_2O_2$ (non-delafossite structure). However, due to the presence of high VBM tail state, these Cu based oxides

suffered from either low hole mobility or unsuitable carrier concentrations.[15, 21-30] As a consequence, the chemical design concept was extended to the layered compounds with higher covalency of the Cu–chalcogen (Ch) interactions (LaCuOCh);[30-33] however, these materials still exhibited relatively high hole densities, which indicates that the p-channel cannot be effectively depleted and that these materials are not suitable for electrical switching applications like thin-film transistor (TFT). An alternative approach to attain high performance p-type oxides is to employ pseudo-closed ns^2 orbitals of metal cations that have similar energy levels close to the oxygen 2p orbitals and form strong hybridization. Such candidates include lead oxide (PbO), beryllium oxide (Bi_2O_3), and tin monoxide (SnO). While Bi_2O_3 exhibited low hole mobility and PbO was reported with n-type conductivity,[8, 9] SnO has shown a promising p-type performance and has attracted more attention. The relatively higher hole mobility in SnO is largely due to the low defect formation energy of Sn vacancies (V_{Sn}), which serve as acceptors, and to the creation of a suitable dispersed VBM by the hybridization of Sn 5s and oxygen 2p orbitals. At the very top of VBM, contribution from the spatially spread Sn 5s orbitals dominates, which results in a potentially promising p-type transparent oxide.[18, 34, 35] In fact, soon after the theoretical discovery of hole-transporting nature of SnO, p-type TFTs were successfully fabricated with relatively high hole field-effect and Hall mobility values.[6-9, 36, 37] Along with SnO, cuprous oxide (Cu_2O) has also been known as a promising p-type oxide for long time and still holds the best p-type Hall mobility value, which exceeds 100 $cm^2 V^{-1} s^{-1}$.[38] The p-type character of Cu_2O has been theoretically studied and is largely attributed to the formation of copper vacancies. Cu_2O holds a unique band structure, where the VB is composed of fully occupied hybridized levels from the Cu 3d and O 2p orbitals. The very top of VBM is mainly composed of the Cu d-states, which creates less localized hole transport pathway.[17, 39-42] Beyond the delafossites, Cu_2O, and SnO, Hautier et al. recently reported a new class of ternary oxides which they have predicted to be very good p-type oxide candidates, but few studies exist on these oxides.[43, 44]

2. Discovery and Synthesis of Hole-Transporting (p-type) Oxides

2.1. Ternary Cu-bearing oxides

As discussed in the introduction, the valence band (VB) in oxide materials is made of the deep and localized oxygen 2p orbitals, which are responsible for the poor hole transport in oxide materials. Introducing covalent bonds between metal cations and oxygen anions is believed to alleviate this localization at the VB edge in accordance with the chemical design concept (CDC) proposed by Kawazoe et al.[15, 20] From the point of forming considerable covalency, the energy level of the d shell electrons should be comparable with that of the oxygen 2p levels. For better transparent device applications, cations with closed shell levels ($d^{10}s^0$) are good candidates since this kind of electronic configuration can avoid the absorption in the visible range from the so-called d-d transitions.[20] Cu and Ag have the appropriate $d^{10}s^0$ states for the above mentioned requirements. The edge of VB becomes the antibonding level after the formation of considerable covalency, since both cation and anion hold closed shell electronic configurations (**Figure 2b**).[19] In this way, a more dispersed VB and a small hole effective mass can be achieved. Another factor that must be considered in the search for optimal p-type oxides is the crystal structure, which determines the coordination and the spatial stacking of the cations and anions. For one, the oxygen coordination is critical, since oxygen anion is the main contributor (O 2p) to the localization of holes. Tetrahedral coordination is preferred due to the fact that in this kind of system all eight electrons (including $2s^2$) of oxygen are participating in the four σ bonds, i.e. sp^3 hybridization.[15, 19, 20] In this manner, further delocalization at VB edge can be achieved. The second factor for crystal structure consideration is related to the transparency. The layered Cu-bearing delafossite oxides (with the general formula $CuMO_2$ and space group $R\bar{3}m$) consist of an alternating stack of Cu ion layers and MO_2 octahedral layers along the c axis (**Figure 2a**). This structural arrangement made them an interesting group of oxides to study due to the

significant decrease in crosslinking between the Cu^+ ions from three dimensions (as in Cu_2O) to two dimensions (as in delafossites). This made it possible to enlarge the bandgap in these oxides by reducing the interaction between d^{10} electrons in neighboring Cu^+ ions.[45] Based on these considerations, Cu^+ based delafossites were identified as potentially promising transparent p-type oxides (**Figure 2**).

Following this material selection criteria, the first batch of p-type transparent delafossite oxide thin films were successfully demonstrated by pulsed laser deposition (PLD), reactive frequency or direct current magnetron sputtering (RF/DCMS), chemical vapor deposition (CVD), thermal evaporation (TE) and hydrothermal methods. The general chemical formula for these oxides can be expressed as **$CuMO_2$** (M=Al[15, 19, 46-48], Ga[19, 22, 23, 49], In[25, 50, 51], Sr[49, 52], Y[49, 52, 53], Sc[49, 54-56] and Cr[49, 53]). The validity of CDC model was also confirmed experimentally in $CuAlO_2$ by mapping the valence band structure using spectroscopic methods, leading to the discovery that the resultant VBM is dominated by Cu 3d level.[19, 45] Among the above mentioned Cu^+ based delafossites, $CuInO_2$ was reported with both a large optical band gap (3.9 eV) and bipolar property, where p- or n-doping can be achieved by Ca or Sn substitutions, which paved the way to build transparent oxide based p-n homojunctions.[24, 25] The physics behind the bipolar property and the large band gap was explained by Nie et al., where a large disparity between the fundamental indirect band gap and apparent direct band gap contribute to the bipolar doping.[57] For the p-type character of $CuAlO_2$, Pellicer-Porres et al. and Tate et al. separately detected defect absorptions in the optical absorption spectra showing the copper vacancy (V_{Cu}) to be responsible for the p-type conductivity.[58, 59] Nolan calculated the defect formation energy in $CuAlO_2$ by density functional theory (DFT) and found the V_{Cu} with small formation energy was the most likely origin of the p-type character.[60] Scanlon et al. stated that the V_{Cu} or Cu on Al antisites defect was the dominant defect under Cu-poor or Al-poor conditions, respectively.[61] Fang et al. and Luo et al. reported that the oxygen interstitial (O_i) was a deep level defect and would not

contribute to the p-type conductivity.[62, 63] However, even after extensive efforts to search for Cu^+ based delafossite materials, the conductivity of the delafossite films remained low, only ~10^{-2} S cm^{-1}. This was attributed to the fact that doping was ineffective in increasing the hole concentration and thus the conductivity of the delafossite oxides.

Another ternary Cu-bearing oxide material, $CuSr_2O_2$, was subsequently proposed.[26, 64] The p-type nature of $CuSr_2O_2$ was studied by DFT, and the VBM was found to be formed by the hybridization between Cu 3d, 4s and 4p with O 2p levels.[64] It should be noted that $CuSr_2O_2$ did not possess the delafossite structure but it held similar dumbbell-like Cu-O bonding, with an even lower dimension of Cu^+ ions crosslinking (only single chain), which should improve the transparency in the visible range. Another structural feature of this compound is that the strontium (Sr) ion is located inside an octahedron of six oxygen atoms, which could be substituted by elements such as potassium (K) to enhance the conductivity.[20, 26] As expected, K was successfully doped into $CuSr_2O_2$ films, but the carrier concentration turned out to be lower than anticipated, and the conductivity of $CuSr_2O_2$ remained low, ~10^{-2} S cm^{-1}. An advantage for the $CuSr_2O_2$ is that the maximum processing temperature was only 300 ^oC, which could be extended to fabricate p-n junctions. Soon afterwards, $CuSr_2O_2$ was successfully used in the fabrication of transparent oxide based p-n junctions with rectifying effect.[65] UV electroluminescent effect was also detected in p-n junctions of heteroepitaxially grown p-$CuSr_2O_2$ on n-ZnO.[27-29]

However, these Cu^+-based ternary p-type transparent oxides still suffered from low hole concentration and low carrier mobility, although considerable efforts has been exerted into the optimization of their electrical properties.[30] As a consequence, the chemical design principle was extended by using chalcogen (Ch) element p orbitals to replace the oxygen ones, since a more dispersed VB edge was theoretically expected from the hybridization between Cu 3d orbitals and the Ch p orbitals, due to the increasing covalency between Cu and ch atoms in the sequence of O, S, Se and Te.[33] Following this approach, the first attempt was shown using

sulfur to replace oxygen to reduce the localization of VBM. A layered oxysulfide LaCuOS was demonstrated with p-type conductivity and a large band gap of 3.1 eV.[31, 32, 66-70] The controllable cation substitution of LaCuOCh was also reported, and degenerate p-type conduction in $LaCuOS_{1-x}Se_x$ (x=0 to 1) was shown with relatively high hole conductivity (σ) and the hole concentration was around 2.2×10^{20} cm^{-3}. Further, a conductivity of 140 S cm^{-1} was achieved by doping Mg^{2+} ions at the La^{3+} sites, while maintaining a Hall mobility of 4 cm^2 V^{-1} s^{-1}.[71-73] Details about the fabrication technique for LnCuOCh (Ln = La, Pr or Nd; Ch = $S_{1-x}Se_x$) epitaxial films and related optical or electrical properties were reported by Hiramatsu et al.[74] Although p-n junctions were demonstrated using p-type LnCuOCh semiconductors, the high carrier concentrations (>10^{18} cm^{-3}) impeded their further application in thin-film transistor (TFT) devices, in spite of the high carrier mobility.[23, 71]

Recently, a remarkable Hall mobility of 39.5 cm^2 V^{-1} s^{-1} for p-type delafossite $CuAlO_2$ was reported by Yao et al., where a new strategy of alloying non-isovalent Cu-O dimer inside $CuAlO_2$ host was demonstrated.[75] The $CuAlO_2$ thin films were deposited from radio frequency magnetron sputtering (RFMS) with a CuAl alloy target at substrate temperature of 940 ^oC under various oxygen partial pressures. The Cu^{2+}/Cu^+ ratio was tuned between 4.2 and 22.8% by controlling the RF power, while the optical band gap was also tuned from 3.36 to 3.87 eV. Hall mobility values from 8.6 to 39.5 cm^2 V^{-1} s^{-1} were obtained, with the mobility values being inversely related to the Cu^{2+}/Cu^+ ratio. The temperature-dependence resistivity measurement of all thin films showed similar behavior to pure $CuAlO_2$, and the authors concluded that CuO clusters were embedded into the $CuAlO_2$ host lattice as Cu-O dimmers. The high Hall mobility was thus attributed to the modulation of the electronic structure of the host $CuAlO_2$ by the hybridization of Cu-O dimers, i.e. the partial substitution of less-dispersive Cu^+ $3d^{10}$ (from $CuAlO_2$) with more dispersive Cu^{2+} $3d^9$ (from CuO) orbitals in the VBM. Such film was also used to build a p-type TFT exhibit a field-effect mobility of 0.97 cm^2 V^{-1} s^{-1}.

The electrical and optical properties of p-type ternary Cu-bearing oxide or chalcogenide thin films are summarized in **Table 1**. It should be noted that the table only covered reports with reliable Hall mobility data.

2.2. Binary copper oxides

Copper oxides have two well-known forms, cuprous oxide (Cu_2O) and cupric oxide (CuO). Cu_2O has a cubic crystal structure (space group $pn\bar{3}m$, a=4.27 Å), which consists of two interpenetrating diamond-like oxygen and copper networks, where Cu atoms are inserted between two consecutive body centered cubic (bcc) arrayed oxygen layers (**Figure 3a**). Each oxygen atom is surrounded by a tetrahedron of Cu atoms and each metal atom is two-fold coordinated.[39, 40, 78] For CuO, Cu^{2+} forms four coplanar bonds with oxygen in the tenorite structure (monoclinic space group C2/c) with the lattice parameters of a = 4.684 Å, b = 3.425 Å, c = 5.129 Å and $\beta = 99.28^{o}$.[79, 80] It is reported that the optical band gap is 2.1-2.6 eV for Cu_2O and 1.9-2.1 eV for CuO.[81] Both of them are reported to be p-type oxides, with several reports showing that Cu_2O holds Hall mobility exceeding 100 $cm^2\ V^{-1}\ s^{-1}$.[38, 82] The p-type character of the Cu_2O is attributed to the presence of Cu vacancy (V_{Cu}), which introduces an uncompensated acceptor level. Interstitial oxygen (O_i) atoms have also been pointed out as possible acceptor defects.[17, 40, 41, 78, 83] The high p-type mobility of Cu_2O is related to the band structure near the top of VB. In the majority of metal oxides, the valence band is mainly formed by the localized and anisotropic O 2p orbitals, which leads to a low hole mobility.[15, 17, 18] In contrast, the VB in Cu_2O is composed of fully occupied level which is formed by the hybridization of Cu 3d and O 2p orbitals (**Figure 3b**). The very top of VBM is mainly composed of the Cu d sates, which creates less localized hole transport pathway.[17, 39-42] The p-type behavior of CuO has also been studied theoretically and is attributed to the presence of V_{Cu}.[17, 40, 84-86] In the band structure of Cu_2O, it has been reported that the most significant

defect levels were one acceptor level at 0.3 eV and a deep donor level at 0.9 eV from the VB edge.[78, 87] Due to the high solar spectral absorption coefficient, special energy band configuration, abundance and nontoxicity, copper oxides have been used in photovoltaic devices[88-98], gas sensors[99, 100], high T_c superconductors[101, 102], memory devices[103, 104] and lithium ion batteries[105, 106]. Due to the high Hall mobility of Cu_2O[38], the applications in TFTs[107] were also extensively studied after Matsuzaki et al. successfully demonstrated the first high field-effect mobility Cu_2O p-type TFT by pulsed laser deposition (PLD).[82, 108]

The research on Cu_2O has a long history and the fabrication of Cu_2O thin films or nanostructures has been widely reported by various techniques, such as PLD[82, 108-115], magnetron sputtering[38, 87, 92, 116-138] and thermal oxidation[94, 139, 140]; and chemical routes, such as electrodeposition[96, 141], spin coating[142-146], atomic layer deposition[147-149], spray coating[150, 151], molecular beam epitaxy[152], microwave irradiation from Cu precursor[153], chemical vapor deposition[154, 155] and ink printing[156]. A summary of the most promising studies on binary copper oxide thin films is shown in **Table 2**.

In **Table 2**, some of the Cu_2O films grown by physical vapor deposition routes show pronounced Hall mobility (μ_{Hall}) values. Li et al.[38] reported a high μ_{Hall} of 256 $cm^2\ V^{-1}\ s^{-1}$ in their Cu_2O thin film deposited by magnetron sputtering at substrate temperature of 600 ^oC. Such a high mobility was achieved by introducing a low temperature buffer Cu_2O layer, which controlled the growing preference and enlarged the grain size. Matsuzaki et al.[82, 108] optimized the growth temperature and oxygen partial pressure using PLD route, achieved a μ_{Hall} of 90 $cm^2\ V^{-1}\ s^{-1}$ in epitaxial Cu_2O thin films on (110) MgO substrate. Zou et al.[112] studied the deposition temperature of Cu_2O by the PLD route, and a pure phase polycrystalline Cu_2O was achieved at 500 ^oC, with a μ_{Hall} of 107 $cm^2\ V^{-1}\ s^{-1}$. However, the above mentioned high quality films were all deposited at high substrate temperature, which could complicate the device fabrication process. An alternative strategy was demonstrated by Fortunato et al.[87], where the films were deposited at room temperature followed by a post

deposition annealing (PDA) process. The Cu_2O phase composition was adjusted by tuning the oxygen partial pressure and the PDA process was shown to increase the crystallinity and grain size. A Hall mobility of 18.5 cm^2 V^{-1} s^{-1} was achieved after annealing at 200 ^oC in air for 10 hrs. Chemical routes have also been demonstrated in fabricating Cu_2O thin films with promising electrical performances. Jeong et al.[154] reported a Cu_2O film with μ_{Hall} over 30 cm^2 V^{-1} s^{-1} by metal organic chemical vapor deposition (MOCVD) on ZnO coated glass at 400 ^oC. An increasing Hall mobility was found with larger grain sizes, indicating that the grain boundary scattering is a major contributor in limiting the electrical properties. Kim et al.[145] and Yu et al.[146] reported sol-gel methods to fabricate Cu_2O thin films followed by a two-step thermal treatment in oxygen and nitrogen, where a μ_{Hall} of 18.9 and 31.7 cm^2 V^{-1} s^{-1} were reported, respectively. Kwon et al.[132] successfully fabricated Cu_2O films in a plasma enhanced atomic layer deposition system, showing a Hall mobility of 37 cm^2 V^{-1} s^{-1}. The successful fabrication of high mobility thin films using chemical routes was an encouraging development for p-type oxides.

However, for all reported Cu_2O thin films, despite the encouraging Hall mobility values, a major concern is the low carrier concentration (~10^{14} cm^{-3}) and low optical band gap (~2.4 eV), which have limited the potential for Cu_2O thin films in fully transparent electronics. **Table 2** summarizes the performance of binary copper oxide thin films reported in the past fifteen years.

2.3. Tin monoxide

Two stoichiometric tin oxides with large optical band gaps and useful transparency have been identified for quite a long time (SnO and SnO_2). The stable phase of SnO has a tetragonal litharge structure (P4/nmm space group), four O atoms and one Sn atom form a pyramid structure. The Sn atoms and O atoms arranged alternatively with layered structure in a $Sn_{1/2}$–O–$Sn_{1/2}$ layer sequence, van der Waals gap (lone pair electrons) exist in the open

space between the Sn layers along the [001] crystallographic direction (**Figure 4a**).[9, 18, 34, 157, 158] Before the discovery of p-type charge transport in SnO, most research activities were focused on SnO_2, which held great potential in gas sensing, transparent passive and active electronic applications.[159-161] On the other hand, SnO was mainly targeted as anode material for Lithium batteries[162], catalyst in organic synthesis[163], and precursor for obtaining high quality SnO_2[164, 165]. However, this situation changed after the publication of theoretical studies that revealed the p-type nature of SnO, which is attributed to the low formation energy of V_{Sn} and a more dispersed VBM caused by the hybridization between oxygen 2p and spherical Sn 5s orbitals (**Figure 4b and 5**).[18, 34, 35] Soon afterwards, SnO was epitaxially grown on (001) yttria stabilized zirconia (YSZ) substrate by Ogo et al., showing a Hall mobility of 2.4 $cm^2 V^{-1} s^{-1}$ and field-effect mobility of 1.3 $cm^2 V^{-1} s^{-1}$ for the first time.[8, 9] Since then, SnO has been receiving increasing attention because of its relatively high Hall mobility and the abundance, non-toxic nature of tin.[166] However, it is known that SnO has a fundamental stability issue, and it is very challenging to deposite it as a pure phase thin film.[7, 8, 167-169] The physical properties were mainly reported from epitaxial SnO thin films deposited on (001) YSZ substrate by Ogo et al., including the optical band gap (E_g) of 2.7 eV by optical absorption measurement, and the fundamental (indirect) E_g of 0.7 eV by diffuse reflectance spectrum from SnO powder.[8] More detailed electronic properties were also studied by Ogo et al., including the ionization potential (5.8 eV), hole effective mass ($2.05m_e$), and the thermal activation energy (45 meV).[9] Fortunato et al. reported p-type oxide TFTs using SnO deposited by room-temperature radio frequency magnetron sputtering (RFMS) process followed by an air ambient annealing. The annealed thin film and device exhibited a high Hall (4.8 $cm^2 V^{-1} s^{-1}$) and field-effect (1 $cm^2 V^{-1} s^{-1}$) mobilities, suggesting that there was room to improve in the performance of SnO based device.[6, 7] This was followed by Guo et al. and Liang et al., who performed very detailed structural, optical and electrical studies on SnO thin films grown by e-beam evaporation (EBE).[36, 170-172]

Although there have been several materials demonstrating ambipolar behavior, i.e. conducting both electrons and holes in the same channel, SnO is the only one that has been successfully used as a channel conducting both electron and hole currents in thin-film transistors.[173-176] Due to the co-contribution of spherically spread Sn 5s orbitals to the valence band maximum (VBM); Sn 5p orbitals to the conduction band minimum (CBM), and the suitable electronic structure, SnO is endowed with ambipolar property even without doping.[18, 173, 177, 178] There are two factors that contribute to the ambipolar behavior of SnO: valence/conduction band structure and energy band configuration. As mentioned before, the VBM of SnO is composed by hybridized Sn 5s and O 2p, the spherically spread Sn 5s orbital endows SnO with a relatively high hole mobility. At the same time, the CBM of SnO comes mainly from Sn 5p orbitals and the partial density of state (PDOS) curve shows a free-electron-like band which indicates that electrons can also be conducted in SnO if enough electrons exist.[18, 179] Furthermore, in SnO, a small fundamental (indirect) band gap of ~0.7 eV and an optical (direct) band gap of 2.7 eV have been confirmed. Due to the presence of these two band gaps, both the large electron affinity and small ionization potential are attained, which are the desired criteria for n- and p-doping. [173, 177-179]

Fabrication of SnO thin films has been extensively evaluated using a series of methods, including physical vapor deposition (PVD) routes, such as PLD[8, 9, 21, 173, 177, 178, 180, 181], EBE[36, 170, 171, 176], RFMS[6, 7, 37, 168, 182-194] and DCMS[167, 195-200] using Sn[6, 7, 14, 167, 168, 180, 183, 185, 187-189, 191, 193, 197, 201-213], SnO[8, 9, 21, 37, 173, 177, 178, 181, 182, 186, 192, 214-216], SnO_2[36, 165, 169-171, 175, 179, 190, 217] targets on both rigid and flexible substrates. The Hall mobility, carrier (hole) concentrations, along with deposition conditions are listed in **Table 3** for relatively recent studies. It should be noted that only reports with reliable Hall mobility values are summarized in this table. Meanwhile, among the contents of **Table 3**, atomic layer deposition (ALD) method has been demonstrated by Han et al. for growing p-type SnO thin films, showing a polycrystalline structure and Hall mobility of 2.9 $cm^2 V^{-1} s^{-1}$.[218] Besides ALD, chemical routes like chemical vapor deposition

(CVD) and aerosol-assisted CVD were also successfully employed in the fabrication of the SnO thin films, however, no Hall measurement results were shown.[219, 220]

From **Table 3**, it is obvious that there are quite limited reports about the fundamental (indirect) E_g of SnO, although it is one of the most important parameters for a semiconductor. The weak optical absorption from the indirect transition is behind the difficulty in evaluating the indirect E_g, since not only a photon but also a phonon are needed to complete this transition. As already mentioned above, Ogo et al. firstly measured the indirect E_g to be 0.7 eV from powder SnO sample by diffuse reflectance spectroscopy.[8] After this, more efforts had been exerted to measure the indirect E_g values from thin film samples. Liang et al. measured a small indirect E_g of 0.5 eV by optical absorption from a polycrystalline SnO thin film capped by Al_2O_3.[172] Toyama et al. successfully demonstrated the measurement of indirect E_g of SnO by photoacoustic spectrum and photothermal deflection spectroscopy, with the result of 0.7 and 0.6 eV, respectively.[182, 215] Quackenbush et al. also studied this indirect E_g on SnO thin films using hard X-ray photoelectron spectroscopy (HAXPES) and the O K-edge X-ray emission/absorption spectroscopy (XES/XAS), where the occupied states (by HAXPES and XES) and unoccupied states (by XAS) could be measured separately. An indirect E_g of 0.7 eV was confirmed.[178] The optical properties of SnO are also presented in **Table 3**, including both the average transmittance in the visible range and E_g information (direct and indirect). The Seebeck measurement was also used to detect the majority charge carrier type in SnO thin films. Rather large Seebeck coefficients (S) were reported: +1.99 mV K^{-1} (by Ogo et al.[9]), +479 uV K^{-1} (by Hosono et al.[177]), +763 uV K^{-1} (by Hayashi et al.[180]), and +1.69 mV K^{-1} (by Jiang et al.[193]). This variation is likely due to the differences in carrier concentration and the variation in band structure originates from different deposition methods, film crystalline quality and orientations.

2.4. Spinel type oxides

As previously discussed, the chemical design concept is based on combining closed shell metal d^{10} orbitals with the oxygen p orbitals to achieve significantly delocalized VBM. Using closed shell metal cations can effectively avoid colorization from metal d-d or oxygen 2p-metal d transitions.[15] Considering the fact that transition metal ions (Co^{3+}, Rh^{3+}, Ir^{3+}) with d^6 configuration in an octahedral crystal field will behave in low-spin configuration (ground state), i.e. the so-called "quasi-closed shell", these ions are expected to behave similarly to Cu^+ (d^{10} closed shell) when bonding with oxygen.[30, 221-223] Due to the hybridization between oxygen 2p levels and metal d states, the latter will split into sixfold degenerate t_{2g} and fourfold degenerate e_g states, and a band gap between the above mentioned levels will emerge.[222, 224] Following this idea, a new class of p-type oxides named spinel oxides (**ZnM_2O_4**, M= Co, Rh and Ir) was discovered. The crystal structure of ZnM_2O_4 spinel oxides (space group: cubic Fd3m) is shown in **Figure 6a**, where Zn and M atoms are tetrahedrally and octahedrally bonded with oxygen atoms, respectively. The band configuration is shown in **Figure 6b**.[225] Mizoguchi et al. reported a magnetron sputtered $ZnRh_2O_4$ thin film of p-type conducting character with band gap of 2 eV and conductivity of 0.7 S cm^{-1}.[222] The temperature dependent magnetic susceptibility showed that the electronic configuration of Rh $4d^6$ was in the low spin state ($t_{2g}^6e_g^0$). The spectroscopic measurements revealed that the band gap was defined by the empty e_g^0 (CB) and the fully filled t_{2g}^6 (VB) subshell, the latter hybridizing with O 2p. Soon afterwards, Narushima et al. and Ohta et al. demonstrated high performance p-n junction diodes based on amorphous and epitaxial p-type $ZnRh_2O_4$, respectively, which attracted a wide attention to this new class p-type oxides.[226, 227] Kamiya et al. studies amorphous $ZnRh_2O_4$ and proposed that the p-type conduction in the amorphous structure originated from the isotropic nature of spinel structure and the edge-sharing RhO_6 networks, which were less affected by the structural disorder and even stable in amorphous network.[228] In 2004, Kim et al. reported spinel oxide $ZnCo_2O_4$ thin films prepared by magnetron sputtering with p-type conductivity.[229] In 2007, Dekkers et al. demonstrated the p-type nature

of spinel ZnM_2O_4 (M= Co, Rh and Ir) thin films prepared by pulsed laser deposition (PLD), where an increase in both band gap and conductivity was reported with increasing quantum numbers (Co, Rh, Ir), with maximums of 2.97 eV and 3.39 S cm^{-1} for $ZnIr_2O_4$.[230] In 2010, Kim et al. fabricated p-type $ZnCo_2O_4$ thin film and related p-n junction diode by PLD with controllable electrical performance, showing band gap of 2.3 eV and conductivity of 21 S cm^{-1}, while the carrier density could be tuned from 10^{16} to 10^{20} cm^{-3} by controlling the oxygen pressure.[231] Recently, Grundmann and coworkers demonstrated high performance amorphous p-n junction diodes and junction field-effect transistors using p-type spinel oxide $ZnCo_2O_4$ deposited at room temperature, indicating great potential for this material, despite its low hole mobility (< 0.1 cm^2 V^{-1} s^{-1}).[232-236]

Along with these experimental results, theoretical studies of ZnM_2O_4 (M = Co, Rh, Ir) spinel oxides were also reported. The theoretical studies of electronic structure in these material were consistent with the experimental results, showing that, for example, the band gap was created from the crystal field splitting M d^6 orbitals.[224, 237-242] However, the theoretical band gap studies also showed discrepancies with experiments in both the magnitude and trend of band gap values. Specifically, Dekkers et al.[230] reported an experimental result of increasing band gap with the quantum number, while Scanlon et al.[241], Amini et al.[243] and Samanta[242] found different trend in their theoretical works. The p-type character of ZnM_2O_4 spinel oxides was found to originate from the acceptor-like antisite defect Zn_M (Zn replacing M, M = Co, Rh, Ir) and cation vacancy V_{Zn}.[225, 240, 243-245] However, no significant dispersion in VBM was found in theoretical studies, which indicated the presence of large effective mass or polaron conduction, limiting the p-type conductivity of spinel oxides.[224, 225, 238, 241, 243] A large hole effective mass of $7m_e$ was reported by Nagaraja et al.[225] Perkins et al. studied the hole doping in $ZnCo_2O_4$ by both minimizing the formation of intrinsic hole-killers and increasing concentration of hole producers, thus increasing the conductivity of resultant thin films by 20 times.[246] Singh et al. found S doping in $ZnIr_2O_4$

decreases the band gap, making the material an efficient photocatalyst in the visible range by enhancing the optical absorption.[239] Ramo et al. demonstrated that amorphization in $ZnIr_2O_4$ would lead to a large decrease of the band gap and localized states at the VB edges which limit the p-type conduction.[240]

2.5. Nickel oxide

Nickel oxide (NiO) has been known as p-type TCO for long time, with reporting large work function of 5.4 eV and optical E_g from 3.6 to 4.0 eV.[247] However, the visible range transparency had been hindered by the minor absorption due to low oscillator strength d-d transitions[248]. NiO has a cubic structure (space group: Fm3m), similar as NaCl (rock salt structure) with octahedral Ni^{2+} and O^{2-} occupations. From the proposed band structure model[249-251], the VB of NiO is hybridized by O 2p and partially filled metal d orbitals, thus a metallic conduction is expected. However, giving the fact that stoichiometric NiO is an electrical insulator, some models are used to describe the conducting behavior, namely, Mott-Hubbard insulator[252-255] and charge-transfer insulator model[251, 256]. In the former, the E_g is formed by the splitting d bands by strong electron correlation; in the latter, the E_g is defined between higher metal site and ligand site (O 2p). The p-type character for NiO is attributed to the spontaneously formed Ni vacancies (V_{Ni}) and this p-type character is stable.[257] Theoretically, this acceptor level was shown insufficiently close to the VBM, which limits the free hole density and thus the conductivity in stoichiometric NiO (~10^{-13} S cm^{-1}).[257] However, the conductivity can be effectively enhanced by intentionally doped extrinsic monovalent atoms like Li or increasing the concentration of Ni^{3+} ions.[257-259] NiO is also showing electrochromic properties and mainly used as anode electrochromic materials along with WO_3 at the cathode.[260] After connected to the anode, the NiO (bleached state) is oxidized to $NiO(OH)_x$ (colored state) along with the insertion of OH^- and extraction of e^-.[261] To date, NiO thin films can be fabricated by both physical methods like magnetron sputtering[262],

pulsed laser deposition[263], electron beam evaporation[264, 265], and chemical methods like sol-gel processing[266], spray pyrolysis[267] and atomic layer deposition[268]. High p-type Hall mobility had been achieved by both RF sputtering[262] (28.56 $cm^2 V^{-1} s^{-1}$) and spray pyrolysis method[267] (11.96 $cm^2 V^{-1} s^{-1}$), with typical carrier concentrations of 10^{17} ~ 10^{18} cm^{-3}. Similar as previously discussed p-type oxides, NiO had also been used in conventional electronic devices, such as TFTs[269-273], p-n diodes[274-277]. Apart from these, NiO also shows promise in electrochromic[260, 261], resistive switching memory[278-280] and optoelectronic[272, 281-283] or photovoltaic (PV)[263, 282, 284, 285] applications.

3. Device Basics for p-Type Oxides

3.1. Thin-film transistors

Thin-film transistors (TFTs) are widely studied semiconductor devices, primarily due to their simple structure and dominant application in the display industry, where TFTs serve as the basic units that control pixels in flat panel displays including liquid crystal displays (LCD) and active matrix organic light-emitting diode (AMOLED) screens.[286-288] Even though high performance n-type oxide TFTs have already been used in commercial display applications[1, 10, 289, 290], the search for equally good p-type oxides and TFTs has lagged behind. On the one hand, p-type oxide TFTs hold several potential benefits to the related sensing or memory applications, if reasonable performance can be achieved. On the other hand, achieving high performance p-type oxides holds the promise for the implementation of the oxide based complementary metal oxide semiconductor (CMOS) devices, which are known for their power efficiency.[6]

Thin-film transistors are three-terminal field-effect devices comprised of three components, namely, semiconductor, dielectric and electrodes (source, drain and gate). The source and drain electrodes (S&D) are spatially separated with the gate electrode (G) by the dielectric layer. The structures of TFTs can be divided into coplanar (C) and staggered (S)

type, depending on the relative locations of the three electrodes to the semiconductor layer. Within each TFT type, two further classifications can be defined depending on the position of the gate electrode (on the top or bottom of the whole TFT stack), namely, top-gate (-TG) or bottom gate (-BG). These typical structures of TFTs are illustrated in **Figure 7**, classified as mentioned above.[1] The current flow directions differ from structure to structure. For example, in the C-TG or C-BG TFT structures, the semiconductor/dielectric interface directly contacts the S&D, meaning that the current flows horizontally in a single plane. In contrast, in the staggered configurations (S-TG and S-BG), the S&D contact the opposite side of the semiconductor/dielectric interface, meaning that the current flows in two planes: first vertically to the channel then horizontally from S to D.[288]

The structure selected to build TFTs mainly depends on the materials involved in the fabrication and the working conditions of the TFT devices.[1] The TG structures are normally preferred when a given material (e.g. semiconductor) requires high processing temperatures that may damage the previously deposited layers (e.g. dielectric and/or source and drain electrodes). The TG configuration is also preferred when semiconductor with high-quality crystal structure (epitaxial) is desired, which benefits from a small lattice mismatch between semiconductor and the single crystal substrate. The BG structures are more popular in TFT fabrications, mostly due to the simple fabrication process and the fact that most researchers use commercial high quality indium tin oxide (ITO)/glass substrates (where the gate electrodes are already grown on the substrates). Another point for using BG structure is the TFT working conditions, such as instability caused by the back light in the case of hydrogenated amorphous silicon (a-Si:H) TFTs, which are widely used in LCD displays.[1, 291] Consequently, the S-BG structure TFT configuration was chosen for both simplifying the fabrication process and blocking the backlight by the metal gate electrodes on TFTs. It is noted that the semiconductor surfaces are exposed to air in the BG structured TFTs, which can be either advantageous or disadvantageous, depending on the material itself. In some

cases, this structure is preferred when the as-deposited oxides need further processing to attain the desirable stoichiometry and crystal structure, for instance, a post-deposition annealing process in a controlled atmosphere or a surface treatment under plasma exposure.[288, 292]

The basic principle of a field-effect device is to control the flow of electrons (or holes) between the source and drain by the modulation of a semi-conducting channel. This modulation is achieved by the injection of carriers near the semiconductor/dielectric interface[293], through the voltage applied on the gate electrode, which forms a parallel plate capacitor structure along with the gate dielectric and semiconductor. The modulation of channel conductance in p-type TFTs is achieved by the formation of an accumulation layer, i.e. holes accumulated at the p-type semiconductor/dielectric interface. The static characteristics of p-type thin-film transistors can be evaluated by their output and transfer characteristics as shown in **Figure 8**. The output characteristics are obtained by measuring the drain to source current (I_{DS}) as a function of drain-source voltage (V_{DS}) for various gate-source voltages (V_{GS}), as shown in **Figure 8a**, where both the linear and saturation regions are illustrated. Transfer characteristics are obtained by sweeping V_{GS} at a constant V_{DS}, as shown in the logarithmic plot in **Figure 8b**.

The output characteristic (**Figure 8a**) of p-type TFT can be described in two regimes according to the value of the drain-source voltage (V_{DS}): [3, 288, 292, 294-297]

1. Linear region. A conductive channel is formed and current flows between the source and drain. In this regime (which is also known as the pre-pinch-off regime), the accumulated charges are uniformly distributed throughout the channel. The TFT behaves as a resistor, with a linear increment in the current with respect to V_{DS}.

This regime occurs when $|V_{DS}| << |V_{GS} - V_{TH}|$ and the drain to source current (I_{DS}) is modeled as:

$$I_{DS} = -\mu_{FE} C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \qquad (1)$$

where μ_{FE} is the field-effect mobility, C_{ox} is the gate dielectric capacitance per unit area, W and L is the channel width and length.

2. Saturation region. In this regime, the drain voltage is higher than the gate voltage causing the carriers to spread out from the narrow channel created during the linear regime. Current flows in a broader region than just the semiconductor/dielectric interface. Near the drain electrode a lack of channel region results from the depletion of the charges in the accumulation layer near this electrode, and is defined as pinch-off.

This regime occurs when $|V_{DS}| > |V_{GS} - V_{TH}|$. I_{DS} saturates (also defined as the post-pinch-off regime) and is primarily controlled by the V_{GS}, and described approximately by:

$$I_{DS} = -\mu_{Sat} C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2 \qquad (2)$$

where μ_{sat} is the saturation mobility.

TFTs can operate as enhancement-mode or depletion-mode devices. The former is defined as *normally off* device, that is, negligible I_{DS} flows at $V_{GS} = 0$ V; while the latter is defined as *normally on* device, where some I_{DS} flows at $V_{GS} = 0$ V. Turning off a depletion-mode device can be done by applying a V_{GS} of the opposite polarity (i.e. positive V_{GS} for p-type TFTs). Although both operation modes are useful for certain applications, the enhancement-mode is preferred, since it requires no extra power to turn off, facilitating circuit design and dissipating less power in the standby mode.

Typical transfer characteristic of p-type TFT is shown in **Figure 8b**. Depending on the value of applied V_{DS}, the transfer curve will show the performance at the linear or saturation region. The transfer characteristics permit *quantitative assessment* of a large number of important TFT operating parameters[1], including: On-to-off current ratio (I_{on}/I_{off}), threshold voltage (V_{th}), turn-on voltage (V_{on}), subthreshold swing (SS), interface trap density (D_{it}) and mobility (μ). The definition and evaluation for these important parameters are introduced below.

I_{on}/I_{off}, defined as the ratio of drain current in the on state (I_{on}) to current in the off state (I_{off}). V_{th}, defined as the value of V_{GS} when the conductive channel (or an accumulation layer near the dielectric/semiconductor interface) just begins to connect the source and drain electrodes. In ideal case, the channel readily forms on the presence of a very small V_{GS}. In the real case, V_{th} will deviate from the ideal value (close to 0 V). V_{th} can be estimated by different methodologies, linear extrapolation being the most widely used. In this method, the V_{th} can be estimated from the intercept of a straight-line fit of the I_{DS}-V_{GS} transfer curve (linear operation region). V_{th} can also be estimated from a $(I_{DS})^{1/2}$-V_{GS} plot for high V_{DS} (saturation region). The V_{th} estimation in the linear region (obtained at low V_{DS}) is preferred, as series resistance is usually negligible at low drain currents[298]. V_{on} is simply defined as the V_{GS} for the onset of drain current conduction, i.e. the V_{GS} at which the drain current rises. SS is defined as the gate voltage required to increase the drain current by one decade. SS is obtained by the inverse of the maximum slope of the transfer characteristics in the subthreshold region ($|V_{GS}|<|V_{th}|$). Low values of SS result in high operating speed and low power consumption[1, 299].

$$SS = \left(\frac{\partial \log I_{DS}}{\partial V_{GS}} \bigg|_{\max} \right)^{-1} \tag{3}$$

D_{it} can be obtained from the SS and is given by

$$D_{it} = \frac{1}{q}\left(\frac{qSS}{2.3kT} - 1 \right) C_{ox} \tag{4}$$

where q is the magnitude of electron charge, k is the Boltzmann constant and T is temperature in kelvin scale.

Mobility (μ), defined as the efficiency of the majority carrier transport in a semiconducting material, it is obtained from a field-effect measurement. In an ideal TFT, mobility is assumed to be constant and shows no change with V_{GS}. In a real TFT, the channel mobility may not be constant and can vary with V_{DS} and V_{GS}.[1, 298] Several scattering mechanisms (lattice vibrations, ionized impurities, grain boundaries, interface surface

roughness, lattice strain and other structural defects[298]), velocity saturation, and electron trapping can affect the mobility of field-effect devices. In a real TFT, an increment of mobility is observed above threshold voltage, reaching a maximum value at a saturation peak, and finally decreasing as the gate-source voltage increases. The voltage dependence of mobility requires the definition of several types of mobilities to evaluate. The most common ones used in the TFT community are effective mobility (μ_{eff}), field-effect mobility (μ_{FE}) and saturation mobility (μ_{sat}).

The μ_{eff} can be obtained in the linear operation region, as shown in **Equation 5**; μ_{eff} may be found using the measured linear region output conductance. Effective mobility is normally considered the most accurate estimation of mobility as it includes the effect of V_{GS}[298]. Nevertheless, errors in the threshold voltage determination can lead to inaccuracies in the effective mobility evaluation.

$$\mu_{eff} = \frac{g_d L}{W C_{ox} \left(V_{GS} - V_{TH} \right)} \tag{5}$$

where g_d is the output conductance,

$$g_d = \left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{V_{GS}=cons.} \tag{6}$$

The μ_{FE} is the most commonly used mobility to describe the performance of TFTs. It is obtained at a low V_{DS}, but it does not depend on V_{th} determination,

$$\mu_{FE} = \frac{g_m L}{W C_{ox} V_{DS}} \tag{7}$$

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS}=cons.} \tag{8}$$

where g_m is the transconductance and defined as the change in I_{DS} for a unit change in V_{GS} at a constant V_{DS}.

The μ_{sat} can be obtained using the measured saturation region transconductance (at high V_{DS}) according to **Equation 9**.

$$\mu_{Sat} = \frac{2L}{WC_{ox}}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2 \quad (9)$$

Other definitions of mobility include the ones proposed by Hoffman[300], defined as average and incremental mobility, μ_{avg} and μ_{inc}, respectively. μ_{avg} indicates the average mobility of the total carriers in the channel, while μ_{inc} reflects the mobility of the carriers added to the channel as $|V_{GS}|$ increases. The fact is that most of the reported p-type oxide TFTs operate in the depletion mode, i.e. significant I_{DS} exists when V_{GS}=0 V, hence care must be taken to make sure channel mobility is not overestimated due to the inevitable contribution from the bulk mobility (μ_{bulk}). Recently, a comprehensive depletion-mode model was proposed by Zhou et al.,[301] which could help better evaluate the actual interface mobility ($\mu_{interface}$) from a depletion-mode operating TFT by subtracting the contributions from the μ_{bulk}.

3.2. CMOS inverters

As transistors are the elementary building block for circuit design, the ultimate objective of developing high performance p-type transistors is to create circuits with more complex functionality and low power consumption for the emerging transparent electronics industry. This is done by developing a robust complementary metal oxide semiconductor (CMOS) device. The reasons behind the significant importance of the CMOS devices include low power consumption, low waste heat generation, high noise margin, high logic swing output, high circuit integration density and architectural simplicity.[11-14]

As its name suggests, an inverter is used to reverse the high and low voltages corresponding to binary signal of 1 and 0 in digital electronics, where a binary 0 input becomes a binary 1 output and vice versa. Although the inverting function can be realized using NMOS devices, the high power dissipation, lower logic switching performance and

high waste heat generation make them less attractive.[11, 13] The low power consumption in CMOS inverter can be understood from basic device operation.

A CMOS inverter (the NOT gate) is the basic building block of a CMOS circuit, it contains two serially connected n- and p-type transistors drain to drain. Typical structure and schematic circuit diagram of a CMOS inverter are presented in **Figure 9**. The input signal is applied simultaneously to the gate electrodes of both transistors, while the output signal is taken from the common drain electrode.[11] A typical voltage transfer curve (VTC) of CMOS inverter is shown in **Figure 10a**, which is acquired by measuring the voltage from the output electrode (V_{out}) when sweeping the applied voltage in the input terminal (V_{in}). Important parameters of CMOS inverters include I_{dd}, gain, and noise margins, which will be briefly introduced below.

I_{dd} is defined as the static current from the supply rail to the ground, which is related to the power consumption of a CMOS inverter. The functional quality of a CMOS inverter is evaluated by the gain value, which is defined as negative slope in the VTC curve,

$$Gain = -\frac{\partial V_{out}}{\partial V_{in}} \tag{10}$$

The noise margin (NM) is an important parameter for logic circuits, representing the threshold value for a circuit to distinguish the proper signal between '0' or '1', i.e. the amount of noise that a circuit can withstand. The NM of CMOS inverter can be extracted from the unity gain positions ($\partial V_{out} / \partial V_{in} = -1$) from the VTC curve (**Figure 10b**), where the corresponding coordinates of these positions are defined as V_{OH}, V_{OL} in V_{out} axis; V_{IH}, V_{IL} in V_{in} axis. The high NM (NM_H) and low NM (NM_L) can be calculated as follows,

$$NM_H = \left| V_{OH} - V_{IH} \right| \tag{11}$$

$$NM_L = \left| V_{IL} - V_{OL} \right| \tag{12}$$

A basic CMOS operation can be understood from five different regimes presented in the VTC curve, as shown on the top of **Figure 10b**.[302, 303] When a small V_{in} is applied [regime (a) in **Figure 10b**], the p-channel operates in the linear mode while n-channel is turned off. In this regime, the V_{out} can be expressed as

$$V_{out} = V_{SD,n} = V_{DD} - V_{SD,p} \tag{13}$$

Further increase in the input voltage (V_{in}) would forward the operation into regime b, where the n-channel is in saturation mode and p-channel remains in the linear operation mode. Since the current through both TFTs is the same, the turning on of the n-channel TFT (decreasing resistance of n-channel) leads to a drop in V_{out}, the operation in this regime can be described as

$$V_{out} = \left(V_{in} - V_{th,p}\right) + \left[\left(V_{in} - V_{DD} - V_{th,p}\right)^2 - \frac{g_{m,n}}{g_{m,p}}\left(V_{in} - V_{th,n}\right)^2\right]^{1/2} \tag{14}$$

where, $V_{th,n}$ and $V_{th,p}$ are the threshold voltages of the n- and p-channel TFTs, respectively, and $g_{m,n}$ and $g_{m,p}$ are the transconductances of n- and p-channels, as we previously discussed in the TFT operation part.

The conduction in the n-channel TFT leads to a current path from the V_{dd} to V_{ss} through the n- and p-TFT channels. As V_{in} further increased, this current increases, leading to a higher voltage drop across the p-channel TFT, which will eventually be turned on (saturation mode). This is indicated as regime c in **Figure 10b**, where the static current (I_{dd}) across the V_{dd} and V_{ss} terminals is very large, since both TFTs are in saturation mode. Consequently, the I_{dd} climbs to its maximum (**Figure 10a**) and the gain value reaches its peak. Further increase in the V_{in} leads to the n-channel TFT moving into the linear region (regime d). The analysis of this regime is similar to that of regime b, except that the operation regions of the n- and p-channel TFTs are reversed. Eventually when V_{in} is raised beyond the $V_{th,p}$, the inverter enters regime e, where the p-channel is turned off and n-channel device operates in the linear region.

At this point, the ideal V_{out} should be zero.

In summary, the low power consumption of CMOS inverter can be understood as follows, under a high input voltage (1 signal), p-channel is switched off while n-channel is on, and only a negligible I_{dd} (defined by the off current of p-channel) flows from V_{ss} to V_{dd}. This situation is reversed when a low input (0 signal) is applied, where the negligible I_{dd} is defined by the off current of n-channel transistor. In both of the above-mentioned cases, power consumption of CMOS inverters is almost negligible, except for the on/off switching period, which corresponds the peak I_{dd} in **Figure 10a**.[11, 14] Thus, a small overall power consumption can be achieved using CMOS inverters. The low power dissipation results in lower heat generation, which avoids the damage of circuits from overheated devices, cuts down the budget for cooling systems and makes it possible to fabricate more complex circuits at high building density.[11]

3.3. p-n Junction diodes

The p-n junction is a simple yet powerful device that consists of two oppositely doped semiconductor films (p- and n-type). It has been used in many applications including rectification, surge protection, light emission, and receiving or generating radio frequency signals. Apart from the rectifying effect, p-n junction devices have also been widely used in sensor applications, such as thermometers, photodetectors and radiometers. [302, 303]

The rectifying operation of p-n junctions can be understood from the formation of the depletion region, where free electrons in the n-layer diffuse across the junction and recombine with the holes in p-layer, leaving the charged ions in both sides. A built-in voltage is formed due to the difference in work function of p- and n-semiconductors, which impedes further free carrier diffusion across the junction. A reverse bias (i.e. high voltage on n-side, the same direction as the built-in voltage) increases the barrier for electron flow across the junction and reduces diode current. However, a forward bias (i.e. high voltage at the p-type, against the

built-in voltage) assists the electrons in overcoming the Coulomb barrier of the space charge in depletion region. Electrons thus flow with very small resistance in the forward direction.

The schematic structure for typical p-n junction is shown in **Figure 11**. Typical voltage-current characteristic curve of diode operation is shown in **Figure 12a**, which clearly indicates the forward bias, reverse bias and breakdown regions. The characteristic curve in log scale is shown in **Figure 12b**, from which important parameters in diode operation can be extracted, including knee voltage (or cutting voltage, turn on voltage), breakdown voltage, reverse saturation current, forward/reverse rectifying ratio and ideality factor.

The knee voltage (V_{knee}) is the applied voltage which can overcome the potential barrier from the depletion region and allow the flow of charged carriers across the junction. From device point of view, V_{knee} is the voltage at which the forward current starts to increase sharply from its leakage (almost zero) value. The V_{knee} can be extracted by taking the voltage axis intercept from extrapolating the linear part of the current-voltage curve in forward operation, as indicated in **Figure 12a**. Breakdown voltage (V_b) is defined by the largest reverse voltage that can be applied to a diode without causing an exponential increase in the current. Reverse saturation current (I_s) is the current formed by the drifting of minority carriers from the neutral regions to the depletion region. This current is almost independent of the reverse voltage, as shown in **Figure 12a**. Forward/reverse rectifying ratio (I_f/I_r) is the maximum ratio of the forward current to the reverse saturation current in the diode operation, as shown in **Figure 12b**. Ideality factor (n) is the most important parameter of diode operation, it can be used to evaluate how closely the diode behavior matches the ideal diode equation. An acceptable ideality factor for diode device is between 1 and 2. The n can be extracted from the slope of the lnI-V curve,

$$n = \frac{q}{kT}\left(\frac{\partial \ln I}{\partial V}\right)^{-1} \qquad (15)$$

where q is the electron charge, k is the Boltzmann constant and T is the device operating temperature in Kelvin scale.

4. Performance of p-Type Oxide Thin-Film Transistors

4.1. Ternary Cu-bearing oxide thin-film transistors

In 2012, Yao et al. successfully fabricated a coplanar top-gate structured TFT based on $CuAlO_2$ delafossite[75]. This was the first demonstration of TFT application for $CuAlO_2$ delafossite, even though this material had been extensively studied since 1997[15]. (**Figure 13**) Here, the active layer was a mixed phase of Cu-O dimmer inside $CuAlO_2$ host lattice rather than a pure phase. The mixed phase thin film showed an encouraging peak Hall mobility of 39.5 $cm^2\ V^{-1}\ s^{-1}$, which was attributed to the synergistic effects of energy band offset and hybridization of less-dispersive $Cu^+\ 3d^{10}$ with the $Cu^{2+}\ 3d^9$ level at the VBM. The active layer (μ_{Hall} = 8.4 $cm^2\ V^{-1}\ s^{-1}$) was deposited using RFMS at a substrate temperature of 940 ^oC. The TFT showed a typical p-type behavior with a μ_{FE} of 0.97 $cm^2\ V^{-1}\ s^{-1}$, V_{on} of 5 V and I_{on}/I_{off} modulation of 8×10^2. The high μ_{FE} and large optical E_g (>3.46 eV) revived interest in Cu based delafossite oxides.

4.2. Binary copper oxide thin-film transistors

In 2008, Matsuzaki et al. reported a high Hall mobility of ~90 $cm^2\ V^{-1}\ s^{-1}$ in p-type Cu_2O thin films, which was grown by PLD and successfully used in a p-type Cu_2O TFT.[82] By varying the oxygen partial pressure (P_{O2}) and substrate temperature during deposition, a narrow process window for high mobility Cu_2O was found, which was centered about 0.5 Pa and 700 ^oC. The narrow process window indicated that the nonstoichiometric nature of the metastable Cu_2O greatly influenced the electrical properties. According to atomic force microscope (AFM) surface morphology measurement, the growth mechanism of Cu_2O thin films was shown to be strongly dependent on P_{O2}, which affected the grain size. Specifically,

at small P_{O2} (< 0.5 Pa), small crystallite size was observed; when P_{O2}=0.50-0.65 Pa, the film growth was dominated by two-dimensional growth mechanism; at P_{O2}=0.80 Pa, a three-dimensional granular growth mechanism dominated. The low Hall mobility at low P_{O2} or high P_{O2} range was attributed to grain boundary scattering. Eventually, a high Hall mobility of 90 $cm^2\ V^{-1}\ s^{-1}$ was achieved using a 650 nm Cu_2O thin film which was grown at 700 ^oC under P_{O2} of 0.65 Pa. It should be noted that this high Hall mobility was in large part due to the large grain size (two-dimensional growth region) since the 100 nm Cu_2O thin film from the same condition only showed a lower Hall mobility of 70 $cm^2\ V^{-1}\ s^{-1}$. Finally, a coplanar top gate structured TFT was fabricated by depositing the AlO_x by PLD and Au source and drain electrodes by e-beam evaporation (**Figure 14**). The TFT exhibited a μ_{FE} of 0.26 $cm^2\ V^{-1}\ s^{-1}$and I_{on}/I_{off} ratio of 6. A further detailed research[108] on post deposition thermal treatments revealed that the origin of low μ_{FE} was mainly from the subgap traps formed by extra defects (V_O or secondary CuO phase), where the density of subgap states was increased by the thermal treatment. The subgap states even existed in the films grown at the optimum conditions, and showed a rather high density of $10^{18}\ cm^{-3}$.

In 2009, Liao et al. presented a Cu_2O nanowire (NW) FET with encouraging μ_{FE} and large drain current swing ratio.[304] The polycrystalline Cu_2O NWs were fabricated by an Ar/H_2 atmosphere reduction from the CuO nanowires, which were made by annealing a Cu foil in air at 400 ^oC for 24 hrs.[305] An optical band gap of 2.17 eV was acquired from photoluminescence (PL) spectrum. After transferring the Cu_2O NWs onto SiO_2/Si substrate, 100 nm Au electrodes were deposited and patterned by e-beam lithography. The staggered bottom-gate structured NW FETs exhibited encouraging μ_{FE} of 95 $cm^2\ V^{-1}\ s^{-1}$ and large I_{on}/I_{off} ratio of 10^6, with V_{th} and V_{on} of 15 and 32 V, respectively.

Fortunato et al. reported the first fabrication of p-type Cu_2O TFT by RF magnetron sputtering, where the substrate was kept at room temperature, followed by an ambient annealing at 200 ^oC.[87, 306] This study was important due to the successful fabrication of p-

type oxide TFTs using an industry-compatible method and abundant, non-toxic source (Cu). The process window was narrow and films deposited at oxygen partial pressure [Opp, $P_{O2}/(P_{O2}+P_{Ar})$] of 9% were found to show good crystalline quality with relatively high Hall mobility. Interestingly, the XRD results showed no difference in peak position after post-deposition annealing for 10 hours. At the same time, the full width half maximum (FWHM) decreased, resulting in an enlargement of the average grain size from 8.3 nm for the as-deposited films to 15.7 nm for annealed Cu_2O films. The Hall mobility of thin film also increased (to 18.5 $cm^2 V^{-1} s^{-1}$) after post deposition annealing, which indicated that the carrier transport was limited by the grain boundary scattering.[87, 306] The same trend was also reported by Jeong et al.[130] and Matsuzaki et al.[108] A staggered bottom-gate structured TFT was built on commercial ATO (Al_2O_3 and TiO_2 superlattice)/ ITO (tin doped indium oxide)/glass substrate using a 40 nm Cu_2O film as active layer, while the IZO (indium zinc oxide) top gate was grown by RF magnetron sputtering and patterned by the lift-off technique. After annealing at 200 ^oC in air, the TFT showed a μ_{FE}, V_{th}, and I_{on}/I_{off} ratio of 1.2×10^{-3} $cm^2 V^{-1} s^{-1}$, -12 V and 2×10^2, respectively. A further report from Figueiredo et al. showed a μ_{FE} of 7×10^{-3} $cm^2 V^{-1} s^{-1}$, V_{on} of 7 V and I_{on}/I_{off} ratio of 10^3.[125]

Sung et al. reported a p-type CuO TFT by oxidizing the as-deposited Cu_2O film.[121] The active layer was deposited by RF magnetron sputtering using a Cu_2O target, and the as-deposited Cu_2O film was oxidized to CuO at 300 ^oC in air. The measured optical band gaps were 2.44 and 1.41 eV for Cu_2O and CuO, respectively. The staggered bottom-gate TFT was finished by e-beam evaporated Au/Ni source and drain electrodes. The TFT exhibited a μ_{FE} of 0.4 $cm^2 V^{-1} s^{-1}$, V_{on} of 12 V and I_{on}/I_{off} ratio of 10^4.

Another significant achievement in p-type Cu_2O TFTs was presented by Zou et al. in 2010.[112] The Cu_2O films were deposited by PLD at various substrate temperatures ranging from 400 to 700 ^oC. The XRD results showed a clear increase of average valence state of Cu with increasing substrate temperature (T_{subs}). Specifically, the Cu^0 state dominates at

T_{subs}=400 ^{o}C, pure phase polycrystalline Cu_2O at T_{subs}=500 ^{o}C, a Cu_2O+CuO mixed phase with nearly equal contents at T_{subs}=600 ^{o}C, and CuO dominant at T_{subs}=700 ^{o}C. A decrease in grain size was also revealed. The relative composition of Cu_xO films was measured by XPS, and the result was consistent with the XRD analysis, showing that the film grown at 500 ^{o}C is made of single phase polycrystalline Cu_2O. Thus, scattering from both the nonstoichiometric impurities and the grain boundaries was suppressed by optimizing the deposition temperature. The Hall measurement showed an encouraging μ_{Hall} value of 107 cm^2 V^{-1} s^{-1} for the 500 ^{o}C deposited film and this value decreased with the increasing deposition temperature. Finally, TFTs with coplanar top-gate structure were fabricated by employing a high k dielectric HfON and Pt gate/source/drain electrodes. The resulting TFTs showed good performance: saturation mobility of 4.3 cm^2 V^{-1} s^{-1}, V_{th} and V_{on} of -0.8 and 0.5 V, I_{on}/I_{off} ratio of 3×10^6 and a small subthreshold swing of 0.18 V dec^{-1}. Such performance indicated that a better interface exists between HfON and Cu_2O, which inhibited the formation of subgap trap states. As reported in their previous studies[307, 308], a decrease in interface state density (D_{it}) was found by annealing the as-deposited Cu_xO/HfO_2 films in N_2 atmosphere, which was attributed to the suppression of impurity penetration and improvement of interface quality by incorporation of nitrogen into the HfO_2, as also reported by Kang et al.[309] The reported good Hall and TFT performance brought much attention to this promising p-type oxide, Cu_2O.

In 2011, Zou at al. reported another p-type Cu_2O TFT using a bilayer stack of SiO_2 and HfO_2 for gate dielectric, manifesting an improved interface properties and decreased gate-leakage current (**Figure 15**).[113] A 100 nm HfO_2 layer was room-temperature deposited on SiO_2(10 nm)/Si substrate by PLD before the deposition of Cu_2O layer at 500 ^{o}C. The staggered bottom gate structured TFT was completed by deposition of Pt electrodes. No post annealing was applied. Another TFT (reference sample) was fabricated with the same structure, but replacing the bilayer dielectric with 110 nm of SiO_2. The TFT with bilayer dielectric (HfO_2/SiO_2) showed a high saturation mobility of 2.7 cm^2 V^{-1} s^{-1}, V_{th} of 0.3 V,

I_{on}/I_{off} of 1.5×10^6 with a small subthreshold swing of 0.137 V dec^{-1}, which is better than the reference sample as shown in **Figure 15**. The better TFT performance obtained with the bilayer dielectric was attributed to the improved interface properties, including a large accumulation capacitance and low interface-state density, which resulted in less charge trapping at bilayer/Cu_2O interface and a small gate leakage current. This study revealed an effective way of improving the interface quality between dielectric and Cu_2O semiconductor layer, which contributed to better overall TFT performance.

A Cu_2O nanowire FET was reported by Han et al., where the Cu/Cu_2O core-shell structure was formed by thermal oxidation and the core/shell were used as gate and channel, respectively.[310] A Pt Ohmic contacting layer was deposited on the outer surface of the Cu/Cu_2O nanowires, while another Cu-wire layer was perpendicularly aligned on top of the Pt layer and connected at each intersection via metallic paste (**Figure 16**). The nanowire FET showed a saturation mobility of 26.3 cm^2 V^{-1} s^{-1}, V_{th} of 0.7 V, and I_{on}/I_{off} of 10^4. It is noted that the current was induced by applying a positive gate voltage. The drain current in nanowire FET showed a positive response (increase) with the increase of the humidity, and this change was reversible, although the detachment of water molecules took longer than the attachment process. A polycrystalline structure with crevices between grain boundaries was observed by SEM. The embedding of H_2O vapor into these crevices was responsible for the increase of the drain current when this NW FET was employed as sensor. As the Cu_2O was formed in-situ by thermal oxidation of the core Cu metal, it is possible that this Schottky junction was not perfectly flat due to some non-uniform oxidation along the Cu NW surface. This implies that some metallic Cu might exist in the oxide channel layer, which may have affected the device mobility. Finally, the easy fabrication and response to humidity of this Cu_2O NW FET indicated its potential usage in future e-textile fields.

Nam et al. studied the effect of active layer thickness on p-type Cu_2O TFTs.[126] Staggered bottom-gate TFTs were built on Si substrate with a 100 nm thermally grown SiO_2

as dielectric layer, while Ni was evaporated as top contacts. The Cu_2O active layers were deposited by RF magnetron sputtering at room temperature, and the thickness of Cu_2O was controlled by varying the deposition time, between 15 and 155 nm. This was followed by a vacuum annealing at 500 ^oC for 7 minutes. The AFM and SEM images showed an increased surface roughness and grain size with increasing film thickness, which was also confirmed by the XRD analysis. It showed that a small amount of metallic Cu existed in the 15 nm Cu_2O polycrystalline thin film, while CuO existed in the 155 nm thin film, although in both cases the Cu_2O was the dominant phase. The optical transmittance spectrum for 45 nm Cu_2O film showed an average transmittance of 59.3 % and optical band gap of 2.7 eV. For the TFT devices, positive shift in turn on voltages and noticeable humps in thick-channel TFTs were observed, which was attributed to the formation of multiple channels by the conductive back surfaces. Finally, the optimized performance was found in TFT with 45 nm Cu_2O, where μ_{FE} of 0.06 $cm^2\ V^{-1}\ s^{-1}$, V_{th} and V_{on} of -6.7 and 3 V, I_{on}/I_{off} of 1.8×10^4 and SS value of 1.6 V dec^{-1} were exhibited.

In 2012, Yao et al. successfully fabricated p-type Cu_2O TFT at room temperature on a flexible PET substrate without any post annealing process.[127] The Cu_2O film was deposited by magnetron sputtering from a Cu target, while the film showed a nano-crystalline structure with strong (200)-preferred orientation, which was attributed to the limited growth kinetics at low temperature. Uniform nano-crystalline grains (with diameter from 10 to 20 nm) that tightly embedded in the Cu_2O films matrix could be observed from the plane-view TEM micrograph. Each grain was a high-quality single crystal without appearance of amorphous or void structure as confirmed by the HRTEM image. The single phase of Cu_2O was further confirmed by XPS spectra. The Hall mobility and hole carrier concentration were 20.2 $cm^2\ V^{-1}\ s^{-1}$ and 1.5×10^{16} cm^{-3} which is much higher than other reports using the same room-temperature deposition without any annealing. Finally, a staggered bottom-gate structured TFT was built on PET substrate employing ITO as gate electrode, magnetron sputtered

aluminum nitride (AlN) as gate dielectric, and evaporated Au for top contacts. The TFT showed a μ_{FE} mobility of 2.4 cm^2 V^{-1} s^{-1}, V_{th} and V_{on} of -4 and 4 V and I_{on}/I_{off} of 3.96×10^4. The encouraging TFT performance using near room-temperature process on a flexible substrate suggested a great potential for Cu_2O TFTs in low-cost, flexible, large area electronic applications.

In 2012, Sohn et al. presented a p-type Cu_2O TFT by reducing the as-deposited CuO channel at high temperature.[131] The CuO film was deposited at room temperature by RF sputtering using a Cu target, followed by subjecting the as-deposited film at various annealing temperature in vacuum for 7 minutes. The film showed an increased grain size and crystallinity with increasing the annealing temperature, while the XRD revealed a deoxidization in as-deposited CuO film. The films were fully reduced to Cu_2O phase at around 500 ^oC along with an increase in optical band gap from 2.0 to 2.6 eV, corresponding to the reduction reaction. The Hall mobility of films annealed at 500 ^oC was 47.5 cm^2 V^{-1} s^{-1} with a hole concentration of 2.95×10^{14} cm^{-3}. The TFT also showed improving performance with the increase of anneal temperature. Specifically, no field-effect was observed below 350 ^oC, while p-type operation was observed beyond 350 ^oC; the optimal anneal temperature was estimated to be 500 ^oC. The TFT exhibited a μ_{FE} of 0.07 cm^2 V^{-1} s^{-1}, V_{th} of -7.5 V, I_{on}/I_{off} of 1.1×10^4 and SS value of 2.7 V dec^{-1}.

In 2013, Jeong et al. reported a detailed study of the charge transport mechanism in Cu_2O TFTs.[130] A staggered bottom-gate structured Cu_2O TFT was fabricated on a Si substrate where 100 nm thermally grown SiO_2 was used as gate dielectric layer. The Cu_2O channel was deposited by RF sputtering at room temperature and annealed in vacuum at 800 ^oC for 20s using a rapid thermal annealing (RTA) technique, followed by e-beam evaporated Ni electrodes. The TFT exhibited a μ_{FE} of 0.06 cm^2 V^{-1} s^{-1}, V_{th} of -6 V, I_{on}/I_{off} of 10^4 and SS value of 3 V dec^{-1}. Transfer characteristics were measured at various stage temperatures (from 25 to 75 ^oC, 10 ^oC per step) and these curves were used to evaluate the current conduction

mechanism in TFTs operation. The study concluded that multiple trapping and release model was the dominant current conduction mechanism, since the thermally activated drain current obeyed the Meyer-Neldel rule, which mostly originates from the multiple trapping-dominated transport behavior.[311, 312] Therefore, the poor operation of Cu_2O TFT was attributed to the high concentration of trap states located at grain boundaries or the channel/dielectric interface, which was estimated to be ~10^{22} eV^{-1} cm^{-2} near valence band level.

Kim et al. presented the first solution processed p-type Cu_2O TFT.[145] (**Figure 17**) Cu (II) acetate hydrate [$Cu(COOCH_3)_2 \cdot xH_2O$] was used as the precursor, and dissolved in 2-methoxyethanol ($CH_3OCH_2CH_2OH$). A 1.4 M of monoethanolamine (C_2H_7NO) solution was employed as stabilizer. The spin-coated films were subjected to a two-step annealing process, with the first anneal at 400 ^oC in N_2 atmosphere for 30 min, followed by 700 ^oC annealing in O_2 atmosphere for another 30 min. The XRD showed that metallic Cu was the dominant phase after the first annealing step, and it was oxidized to Cu_2O during the second annealing step at low oxygen partial pressure. It was proved that the two-step annealing process helped the formation of a Cu_2O film with one uniform and continuous surface along with a high-quality semiconductor/dielectric interface. The Hall mobility of the spin-coated Cu_2O was 18.9 cm^2 V^{-1} s^{-1} with hole concentration of 1×10^{15} cm^{-3}, after the second step annealing at oxygen partial pressure of 0.04 Torr. Finally, the staggered bottom-gate structured TFT was fabricated by spin-coating such Cu_2O films on top of the SiO_2/Si substrate, while Ni/Au electrodes were e-beam evaporated on the Cu_2O thin film and patterned by shadow masks. The solution processed TFT exhibited a μ_{FE} of 0.16 cm^2 V^{-1} s^{-1} and I_{on}/I_{off} ratio of 10^2. Achieving p-type Cu_2O TFT from solution process was an important development in this field even though the mobility remained low.

Pattanasattayavong et al. reported another solution processed Cu_2O TFT.[151] (**Figure 18**) The Cu_2O film was fabricated by solution-based spray pyrolysis from a precursor solution consisted of 0.04 M Cu(II) acetate monohydrate [$Cu(CH_3COO)_2 \cdot H_2O$], 0.04 M glucose, and

40 vol% isopropyl alcohol (IPA). The substrate was kept at 275 ^{o}C and the film was annealed at 200 ^{o}C for 12 hrs after sprayed. The as-sprayed and annealed Cu_2O films showed similar diffraction patterns, surface roughnesses and transmittances, while the optical band gap was about 2.57 eV. The coplanar bottom-gate TFT was fabricated on Si substrate with 200 nm SiO_2 as dielectric layer, the ITO/Au was chosen as source and drain electrodes. The TFTs exhibited an average μ_{FE} of 3×10^{-4} cm^2 V^{-1} s^{-1}, V_{th} of -70 V, I_{on}/I_{off} ratio of 4×10^3 and SS slope of 30 V dec^{-1}.

Vaseem et al. reported a high performance CuO based TFT by inkjet printing technique.[156] Copper acetate dihydrate [$Cu(CH_3COO)_2\cdot2H_2O$] was used as precursor. The CuO nanoparticles (NPs) were formed by adding 0.5 g NaOH into a mixed solution composed of 100 mL 0.02 M copper acetate and 0.5 mL acetic acid at 90 ^{o}C. Then, the NPs were added into a mixture solution and used as the printing ink, which consisted of NPs, water, ethanol, isopropyl alcohol and ethylene glycol. The ink was printed between Ag electrodes on top of a SiO_2/Si substrate, forming a coplanar bottom-gate structured TFTs. The CuO NPs were printed in line and dot shape patterns, while the channel sizes (W and L) were determined by the actual overlapping of NPs stack between Ag electrodes, which were 40 and 18.8 μm for line shape patterned channel, 70 and 10 μm for dot shape patterned channel. The devices were subjected to a microwave-assisted annealing for 120 s, and the resultant TFTs exhibited large μ_{FE} of 28.7 and 31.2 cm^2 V^{-1} s^{-1}, for the line and dot shape patterned channels, respectively. The latter device also exhibited an I_{on}/I_{off} ratio of 7×10^3 and V_{th} of 0.8 V. The high mobility of ink-printed TFT was indeed a promising development for solution based synthesis of copper oxide. The summary of the literature reports on p-type binary copper oxide TFTs is summarized in **Table 4**.

4.3. Tin monoxide thin-film transistors

In 2008, Ogo et al. demonstrated the first high performance SnO based p-type TFT.[8] (**Figure 19**) An epitaxial SnO film was grown on (001) yttria-stabilized zirconia (YSZ) substrates by PLD at substrate temperature of 575 ^{o}C, resulting in highly (*00l*) orientated SnO films. It should be noted that the reported process window for obtaining high performance SnO phase was extremely narrow, and considerable efforts have been made to optimize the growth conditions. As SnO is a metastable phase, it is likely to either reduced to zero valence state (metal Sn) or oxidized to the higher valence state (SnO_2), even in absence of external oxygen.[165] In addition, the high vapor pressure of SnO and Sn also limits the process temperature. The coplanar top-gate structure TFT was completed by PLD deposited Al_2O_3 dielectric and e-beam evaporated Au/Ni top contacts. Typical p-type behavior was observed, where a negative (positive) gate voltage enhanced (depleted) the channel. The V_{th}, μ_{FE}, μ_{sat} and I_{on}/I_{off} ratio were determined to be 4.8 V, 1.3 $cm^2\ V^{-1}\ s^{-1}$, 0.7 $cm^2\ V^{-1}\ s^{-1}$ and ~10^2. The depletion operation mode and the small I_{on}/I_{off} ratio was attributed to the large hole density in the channel. Hall measurement of SnO thin films showed a large μ_{Hall} value of 2.4 $cm^2\ V^{-1}\ s^{-1}$ and hole concentration of 2.5×10^{17} cm^{-3}. In addition, for the first time, the fundamental (indirect) band gap of SnO was determined to be ~ 0.7 eV by diffuse reflectance spectra from SnO powder sample.

Ogo et al. carried out extensive studies on SnO thin films involving both theoretical and experimental device fabrication.[9] They confirmed that the hybridization of Sn 5s and O 2p orbitals does occur by observing the valence band (VB) structure of the SnO thin films. This hybridized VB theory was reported by Watson et al. and Togo et al.,[18, 34, 35] which was considered to be the main mechanism responsible for the large hole mobility in SnO, although no experimental evidence had been demonstrated. Soft X-ray photoelectron spectra (SX-PES) and hard X-ray PES (HX-PES) were used to study the VB of SnO. Here, SnO_2 thin films were used as reference since the VB of SnO_2 is mainly formed by O 2p orbitals. The ratio of the photoionization cross-section between Sn 5s and O 2p was enhanced 30 times under HX-PES

measurement (high energy excitation), which successfully confirmed the hybridization of Sn 5s and O 2p orbitals in the VB of SnO, since the photoionization cross-section of the large spatially distributed Sn 5s orbitals was more sensitive to the excitation energy. In addition, the measurements were used to estimate the hole effective mass and work function of the SnO for the first time. The hole effective mass was estimated by taking the curvature of VB density of states (DOS) from SnO total density of states (TDOS) calculation by density-functional theory (DFT). The value was determined to be 2.05 m_e (m_e denotes the rest mass of electron), which is small among p-type semiconductors.[43] The work function was estimated (~5.8 eV) by ultraviolet PES (UPS) measurements, taking a SnO_2 sample as reference. Finally, the simulation of p-type SnO TFT characteristics revealed a large subgap hole trap density of ~ 10^{19} cm^{-3} (much higher than that in a-GIZO channel[313]), which limited the mobility and subthreshold swing of the SnO TFTs. The large subthreshold swing value is still an open issue since even the most recent reports on SnO based TFTs still suffered from a large SS value.

Ou et al. and Dhananjay et al. reported the tin oxide (SnO_x) based p-channel TFT in the same year.[211, 212] The p-type SnO_x films were deposited by thermal reactive evaporation under a controlled oxygen environment, and the latter report mentioned that a substrate temperature of 100 ^oC was applied. It should be noted that the as-deposited thin films were n-type in nature with small resistivity of 1.2 Ω·cm, indicating a high background carrier concentration. Thin films with such small resistivity values cannot directly be used as TFT channels. However, a post deposition annealing process at 100 ^oC for 1 hr was found to modulate the electrical properties of as-deposited films and the resultant samples showed p-type conductivity. The XRD analysis indicated an amorphous structure of the SnO_x thin film even after annealing. The obtained XPS spectra of the nonstoichiometric tin oxide thin film suggested the existence of Sn^0 state in the as-deposited films, which disappeared after annealing. The p-type conductivity was attributed to the oxygen rich composition, mixed valence states of tin and grain boundary densities. Such films were deposited on top of the

SiO_2/Si surface and the same annealing treatment was applied. The staggered bottom-gate TFT structure was completed by thermally evaporated Ag as source and drain electrodes and patterned by shadow masks. The TFT exhibited typical p-type characteristics with a negative current when a positive gate voltage was applied. The threshold voltage, saturation mobility, and I_{on}/I_{off} ratio were determined to be 30.4 V, 0.011 $cm^2\ V^{-1}\ s^{-1}$ and 10^3, respectively. An undesirable high interface trap density of ~8.1×10^{11} cm^{-2} was measured from the subthreshold swing value of 2 V dec^{-1}. In addition, an increased post annealing temperature was found to negatively shift the V_{th}. On basis of this, a bottom contact inverter structure was built by combining two p-type TFTs with different V_{th}, and a gain of 2.8 was obtained using supply voltage (V_{DD}) of 80 V.[212] The p-SnO_x TFT was also applied in a CMOS inverter incorporating n-type In_2O_3 TFT, resulting in a gain value of 11.[211]

In 2010, Lee et al. reported p-type SnO TFT fabricated using SnO films deposited by vacuum thermal evaporation from SnO powder source.[214] The deposition was performed at room temperature and the as-deposited thin films showed an amorphous structure. The study showed that post deposition annealing at 300 ^oC for 1 hr in Ar atmosphere will improve both the transparency and the crystalline quality of the SnO thin films. The Hall measurement showed a μ_{Hall} value of 2.83 $cm^2\ V^{-1}\ s^{-1}$ and carrier concentration of 5.03×10^{17} cm^{-3}. For building a coplanar bottom-gate TFT, 200 nm ITO contacts were firstly deposited by RF sputtering on the surface of SiO_2/Si substrate, patterning by a shadow mask. The channel layer (100 nm SnO) was then evaporated on top of ITO contacts, and patterned by another shadow mask. Finally, after annealing at 310 ^oC for 1h in Ar atmosphere, the device exhibited a μ_{FE} of 4×10^{-5} $cm^2\ V^{-1}\ s^{-1}$, $I_{on}/I_{off} > 10^2$ and a negative V_{th}.

Liang et al. presented a p-type SnO TFT by e-beam evaporation. [36] A high purity SnO_2 source was used to deposit SnO at room temperature. The as-deposited 100 nm SnO thin film on SiO_2/Si was amorphous, but polycrystalline films could be obtained after a rapid thermal anneal process in Ar for 10 min. The measured μ_{Hall} was 1.6 $cm^2\ V^{-1}\ s^{-1}$. The TFT structure

was completed by e-beam evaporating Au/Ni source and drain electrodes. The TFT was treated with RTA process at 400 ^{o}C in Ar for 10 min resulting in V_{th}, V_{on}, μ_{FE}, μ_{Sat}, SS and I_{on}/I_{off} values of -3.5 V, 1 V, 0.87 cm^2 V^{-1} s^{-1}, 0.46 cm^2 V^{-1} s^{-1}, 11 V dec^{-1} and ~ 2×10^2, respectively. The authors attributed the high I_{off} to the extra trap states at deep energy levels (> 0.2 eV above VB) which pin the Fermi level, consistent with prior reports by Ogo et al.[9] In addition, a decrease of the refractive index during phase transformation from SnO to SnO_2 was observed.

In 2010, another milestone in this field was achieved when Fortunato et al. published their research on fabricating high performance p-type SnO TFT by magnetron sputtering at room temperature, followed by a thermal annealing at 200 ^{o}C in air.[7] (**Figure 20**) This was an important result since magnetron sputtering is a commercially viable technique and is fully compatible with the existing TFT fabrication technologies. Fortunato et al. reported that the process windows for acquiring high performance p-type SnO was quite narrow, but compared with the PLD at high temperature, sputtering actually gave a wider one since the films could be deposited at room temperature. The as-deposited films were amorphous in nature and a simple post deposition annealing could turn them to polycrystalline structure. All thin films showed carrier concentrations between ~10^{16} and 10^{18} cm^{-3} and a maximum μ_{Hall} of 4.8 cm^2 V^{-1} s^{-1}. This mobility is higher than that of well crystallized films grown by PLD at 575 ^{o}C, indicating the enormous potential of the sputtering technique. Interestingly, according to the XRD patterns, the high mobility thin films were actually a mixture of α-SnO (dominant) and metallic tin (β-Sn) phases. A 220 nm ATO and 200 nm ITO were used as dielectric and bottom electrode, respectively. The staggered bottom-gate TFT with 30 nm SnO and Au/Ti contacts exhibited a V_{th}, μ_{FE} and I_{on}/I_{off} values of -5 V, 1.2 cm^2 V^{-1} s^{-1} and ~ 10^3, respectively. Even better performance was reported with Ni/Au source and drain contacts: μ_{Sat} and I_{on}/I_{off} of 4.6 cm^2 V^{-1} s^{-1} and 7×10^4.[6] (**Figure 21**).

In 2011, Yabuta et al. reported a staggered bottom-gate TFT using 20 nm SnO channel layer by magnetron sputtering, followed by a post deposition annealing at 300 ^{o}C in N_2 for 2 hr.[37] The TFT exhibited a V_{th}, μ_{FE} and I_{on}/I_{off} values of 30 V, 0.24 cm^2 V^{-1} s^{-1} and ~ 10^2. In addition, an ambipolar behavior was observed by annealing the device at a higher temperature (400 ^{o}C). In the same year, Nomura et al. demonstrated the first SnO based ambipolar TFT, where both holes and electrons could be effectively transported by the same channel depending on the applied gate bias (**Figure 22**).[173] The ambipolar TFT showed great advantage since it could simplify the fabrication process of complementary circuits by combining the deposition processes for both p- and n-type semiconductors. The 15.4 nm SnO channel was deposited by PLD at room temperature, and the amorphous as-deposited SnO film was transformed to polycrystalline by post deposition annealing at 250 ^{o}C in air for 30 min. SiO_2(15 nm)/Si and ITO were used as gate/dielectric and top contacts in a staggered bottom-gate TFT. In addition, about 330 nm Y_2O_3 layer and a top gate were deposited to make a dual-gate TFT. Mobility (μ_{Sat}) values of 0.81 cm^2 V^{-1} s^{-1} for p-channel operation and 5×10^{-4} cm^2 V^{-1} s^{-1} for n-channel operation were obtained. A CMOS-like inverter was built by combining two ambipolar SnO TFTs, showing gain value of 2.5. They attributed the ambipolar operation to the small trap states in thinner channel. This was the first demonstration of CMOS-like inverter using a single channel oxide semiconductor.

In 2012, Liang et al. showed a high performance CMOS-like inverter based on the ambipolar operation of SnO channels, which possessed balanced electron and hole field-effect mobilities.[179] (**Figure 23**) The SnO film was deposited on SiO_2(106 nm)/Si substrate by e-beam evaporation at room temperature from a SnO_2 source, followed by a RTA at 400 ^{o}C in Ar atmosphere for 10 min to achieve polycrystalline structure. It should be noted that the Sn/O atomic ratio detected by XPS was ~ 52.4/47.6; this small oxygen deficiency was believed to favor both the dual carrier transport and long-term air stability. Au/Ni electrodes were e-beam evaporated to complete the staggered bottom-gate TFT stack. The ambipolar

TFT showed an improved electrical performance in both p- and n-type operation regime, namely, μ_{FE} and μ_{Sat} of 0.32 and 0.16 $cm^2\ V^{-1}\ s^{-1}$ for the p-type operation, and μ_{FE} and μ_{Sat} of 1.02 and 0.63 $cm^2\ V^{-1}\ s^{-1}$ for the n-type operation. Such a balanced performance assured the high performance of CMOS-like inverter when two such identical devices were connected, showing maximum gain over 30 in both first and third quadrants under supply voltage (V_{DD}) of |40 V|. The device showed a long-term stable gain value in air which illustrated the promise for oxide material of SnO.

An interesting application of p-type oxide SnO was the fabrication of tin oxide CMOS on paper by Martins et al.[13, 14, 203, 314] (**Figure 24**) Building oxide TFTs on flexible, low-cost and fully recyclable paper substrates demonstrated the potential of this technology. The track paper showed a high capacitance of 40 nF cm^{-2} at low sweep frequency. About 8 nm SnO was deposited by RF sputtering on paper substrate, patterned by shadow mask, and followed by annealing process to crystallize the as-deposited SnO. IZO and Au/Ni were used as gate and top contacts, while the paper was used as both substrate and dielectric of the staggered bottom-gate TFT device. The electrical performance of SnO TFT was as follows: V_{th} of 1.4 V, μ_{Sat} of 1.3 $cm^2\ V^{-1}\ s^{-1}$, SS of 3.1 V dec^{-1} and $I_{on}/I_{off} \sim 10^4$. The n-type counterpart GIZO TFT showed V_{th} of 2.1 V, μ_{Sat} of 23 $cm^2\ V^{-1}\ s^{-1}$, SS of 6.9 V dec^{-1} and $I_{on}/I_{off} > 10^2$. The CMOS inverter exhibited a gain value of ~ 4.5 and a static power dissipation of 32 pW per inverter.[14]

In 2012, Okamura et al. demonstrated the first p-type SnO TFT by solution process.[315] (**Figure 25**) Precursor of $SnCl_2 \cdot 2H_2O$ was dissolved in methanol and spin-coated on 200 nm SiO_2/Si substrates in a nitrogen-filled glove box, followed by NH_4OH exposure for 1 hr and annealing at 450 ^oC for 2 hr in a mixture gas of N_2 and H_2. After annealing, the SnO thin film tuned to polycrystalline litharge structure. The staggered bottom-gate TFT showed a V_{th} of -1.9 V, μ_{Sat} of 0.13 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} of 85. The successful fabrication of solution

processed p-type SnO and functional devices was another promising development for this oxide.

In 2013, Caraveo-Frescas et al. reported a detailed study on high performance SnO TFT by dc reactive magnetron sputtering.[167] (**Figure 26 and 27**) The main sputtering parameters, i.e., the Opp and the whole deposition pressure, were carefully controlled, and varied from 3 to 25% for the former and from 1.2 to 2.2 mTorr for the latter. The as-deposited films were annealed at 180 ^{o}C in air for 30 min. The XRD patterns indicated that the phase formation strongly depended on the Opp and whole sputtering pressure. The p-type SnO polycrystalline (α-SnO) with or without metallic tin was only obtained in a narrow window between Opp of 7% and 15%, and pressure of 1.5 and 2 mTorr. Considerable efforts involving hundreds of experiments were used to generate a deposition phase map for the vapor-phase deposition of SnO.[165] (**Figure 26a**) For each process pressure between 1.5 and 2.0 mTorr, the deposited film composition showed a specific trend as indicated in the map shown in **Figure 26a**. The lattice strain analysis using XRD pattern showed higher strain value in mixed phase (mp-) SnO, indicating the presence of more lattice defects which might cause additional carrier scatterings. Hall measurements showed that mp-SnO composition exhibited better Hall mobility compared to pure phase SnO, reaching a peak hole mobility (μ_{Hall}) of 18.7 $cm^2 V^{-1} s^{-1}$ for films consisting of mp-SnO with ~3 at% β-Sn second phase (**Figure 26b**). Density functional theory simulations suggested that defects (Sn interstitial and oxygen vacancy) generated under Sn-rich growth conditions gave a more metallic character to the valence band of the SnO, which contributed to higher mobility.[316] The high hole mobility obtained was attributed to the balance between the valence band modulation at low concentrations of β-Sn second phase (< 3 at%), and the charge carrier scattering that increases at higher concentrations of β-Sn second phase. Finally, a staggered bottom-gate TFT was built on both rigid (glass) and flexible (polyimide) substrates using the highest mobility mp-SnO films. In both cases, ITO and ITO/Ti were used as gate and top contacts, while atomic layer deposition

(ALD) grown HfO_2 was used as gate dielectric. The device was annealed at 180 ^oC in air for 30 min. The device showed a V_{th} of -1 V, μ_{FE} of 6.75 $cm^2 V^{-1} s^{-1}$, I_{on}/I_{off} ratio of 6×10^3, and SS value of 7.63 V dec^{-1} for device on transparent glass substrate. In comparison, -1.2 V, 5.87 $cm^2 V^{-1} s^{-1}$, ~ 6×10^3 and 7.63 V dec^{-1} were obtained for the same parameters, respectively, on flexible substrate. The μ_{FE} value was stable under various channel W/L ratios and the transfer curve remained stable after repeated testing. The reported Hall mobility and field-effect mobility was a new record in SnO p-type oxides.

In the same year of 2013, Caraveo-Frescas et al. demonstrated the first p-type SnO nanowire field-effect transistor (NW-FET), in which a high μ_{FE} of 10.83 $cm^2 V^{-1} s^{-1}$ was achieved at low processing temperature.[195] (**Figure 28**) The reported high performance nanowire FET adopted a staggered bottom-gate structure, in which ITO and HfO_2 were used as gate electrode and dielectric, while Au/Ti was used as source and drain contacts. The 15 nm SnO film was deposited by magnetron sputtering in a mixture of oxygen and argon gases (13% Opp). E-beam lithography and the lift-off technique were used to define and pattern the nanowires. The nanowire FET had a channel length of 5 μm with a variable width, ranging from 100 to 500 nm. The 160 ^oC ambient annealing process was enough to turn the amorphous as-deposited film into a polycrystalline one with grain size between 10 to 15 nm. The NW-FET exhibited excellent performance with turn-on voltage and SS value of ~ 2.03 V and ~ 0.68 V dec^{-1}, respectively. The μ_{FE} was 10.83, 10.58 and 10.30 $cm^2 V^{-1} s^{-1}$ for nanowire widths of 100, 200 and 500 nm devices, respectively. Obviously the nanowires were too large for confinement effects to explain the enhanced mobility. Instead, the authors attributed this good result to the small density of trap states in the SnO channel layer and at the SnO/HfO_2 interface (with D_{IT} of 3.96×10^{12} eV^{-1} cm^{-2} and effective hysteresis density, N_{HYS} of 7.57×10^{11} cm^{-2}), indicating a more stoichiometric tin oxide phase in the nanowire case. The authors argued that since the nanowire has a larger specific surface area and smaller dimensions, smaller diffusion distances (e.g., for oxygen) were needed during the crystallization anneal to

form the required SnO stoichiometry. This explanation was also supported by the fact that lower temperatures were needed in the case of nanowires (as opposed to SnO films) to crystallize the as-deposited amorphous films to polycrystalline SnO. In fact, a temperature as low as 160 ^{o}C was enough to crystallize the nanowires, while temperatures above 180^{o}C were needed to crystallize the thin films. Although metallic Sn was not detected in the XRD pattern, it is still possible that nano-crystalline metallic Sn may be present but in amounts well below the detection limit of XRD; small amounts of metallic tin have been shown to improve SnO hole mobility.[167, 317]

In 2014, Chiu et al. reported stability evaluations for SnO channel TFTs under gate bias stress.[206] A 100 nm thick patterned Cr gate electrode was used along with 50 nm HfO_2 dielectric layer deposited by ALD. The 30 nm SnO channel layer was deposited by magnetron sputtering at room temperature under a mixture of O_2 and Ar gases, with Opp of 2.34%. Top source/drain contacts were made of ITO, and the TFT was subsequently annealed in ambient at 250 ^{o}C for 60 min. The TFT exhibit a moderate performance with a μ_{FE} of 0.24 $cm^2\ V^{-1}\ s^{-1}$, I_{on}/I_{off} of 1×10^3, V_{th} of 2.5 V, and SS value of 2 V dec^{-1}. The authors evaluated the operational stability of SnO TFT under both positive and negative-gate bias stress at multiple stress levels. The shift of the V_{th} under positive gate-bias stress was larger than that under a negative gate-bias stress, which is different from the behavior of common n-TFTs with channel material such as GIZO. In the same year, this group reported another SnO TFT using the same device structure[210], while the channel thickness was decreased to 15 nm, and SnO was deposited at Opp of 4.1%. The post-deposition annealing temperature was also optimized to be 225 ^{o}C in air for 30 min. The device exhibited a μ_{FE} of 0.33 $cm^2\ V^{-1}\ s^{-1}$, threshold voltage of -1 V, I_{on}/I_{off} of 10^3 and SS value of 2.5 V dec^{-1}. The slight increase of SS value indicated that SnO contained more defects due to the lower annealing temperature and shorter duration. A hybrid oxide based CMOS inverter and a five-stage ring oscillator using SnO and ZnO as

semiconductors were demonstrated, showing a maximum gain of 17 at V_{dd} of 10 V for the inverter and the oscillation frequency was 2 kHz at V_{dd} of 14V for the ring oscillator.

Also in 2014, U et al.[208] reported a study on the effects of semiconductor deposition temperature on the properties of both SnO thin-films and TFT devices. About 10 nm SnO layers were deposited at substrate temperatures ranging from 60 to 220 ^{o}C, while SiO_2 (17 nm)/Si was used as the dielectric/gate electrode in a staggered bottom-gate TFT. About 50 nm Ni was deposited by e-beam evaporation to form the source and drain contacts. No post annealing treatment was used. For the TFT deposited at 60 and 220 ^{o}C, no field-effect operation was observed. The TFTs deposited between 100 and 180 ^{o}C demonstrated pronounced p-type field-effect operation with well-defined turn on voltages and a modulated drain current by sweeping the gate bias. With increasing deposition temperature, the μ_{FE} decreased and the threshold voltage shifted to more negative value. Specifically, the mobility decreased from 1.2 to 0.1 $cm^2 V^{-1} s^{-1}$, and the threshold voltage from -1.1 to -4 V at 100 and 180 ^{o}C, respectively. The authors reported that the same trend was observed in Hall mobility. The grain size analysis indicated that the average grain size decreased with increasing deposition temperature. To understand the connection between the change of electrical properties and grain size in SnO thin film, the authors invoked a grain-boundary charge-trapping model proposed by Seto[318]. In this model, the grain boundaries not only trap the free carriers but also scatter them. The smaller grain size implies a higher grain boundary density, thus resulting in lower hole mobility and more negative threshold voltage, which was consistent with the experimental facts.

In the same year, this team reported further optimization of the p-type SnO TFT by varying the dielectric layer.[205] The same structured devices were fabricated on various surfaces, including thermally grown SiO_2, plasma-enhanced chemical vapor deposition (PECVD) SiN_x (at 250 ^{o}C) and SiO_x (at 150 and 300 ^{o}C). The same SnO thin film (10 nm) was deposited on the dielectrics by magnetron sputtering. A substrate temperature of 90 ^{o}C,

Opp of 6.25%, and no post deposition annealing was applied. The TFT using PECVD SiO_x deposited at 150 ^oC exhibited excellent performance, with a high μ_{FE} of 4.86 $cm^2\ V^{-1}\ s^{-1}$, V_{th} of -2.3 V, V_{on} of -0.1 V, $I_{on}/_{off}$ ratio of 3×10^4 and SS value of 0.7 V dec^{-1}. The XRD analysis indicated a much smaller grain size and lower crystallinity for SnO film deposited on the 150 ^oC PECVD SiO_x dielectric. The smaller grain size of the SnO films was attributed to the rougher surface of the SiO_x dielectric deposited at 150 ^oC, which resulted in enhanced nucleation rate, and hence a smaller grain size. Again, the Seto's localized-trap-states model[318] was used to explain these results, where the partially filled grain boundaries exhibit low potential barrier height, which increased mobility when carriers transport across them. However, when optimizing the device performance by downsizing grains, a trade-off should be noted between lowering the free carrier concentration and enhancing mobility from partially filled grain boundaries, since the operation of TFT needs both a moderate carrier concentration and a high carrier mobility.

Han et al. reported an SnO based p-type TFT with staggered bottom-gate structure, where Su-8 passivation layer was shown to enhance both the long-term durability and gate-bias stress stability.[204] Si and thermally grown SiO_2 (35 nm) were used as gate and dielectric, while e-beam evaporated Ni was used for source and drain contacts. The 10 nm SnO channel layer was deposited by magnetron sputtering at room temperature with an Opp of 5.4 %, followed by a rapid thermal annealing at 200 °C for 100 seconds. The device showed a μ_{FE} and μ_{sat} of 1.2 and 1.1 $cm^2\ V^{-1}\ s^{-1}$, SS value of 1.1 V dec^{-1}, V_{th} of 4.1 V, and I_{on}/I_{off} ratio of $\sim 2.5 \times 10^4$. In addition, compared with the un-passivated TFT, the SU-8 passivated device exhibited superior stability and durability under both gate-bias stress and long-term air exposure.

In 2015, Han et al. reported important results on the stability of p-type SnO TFTs in moist and ambient environments.[207] (**Figure 29**) Si and thermally grown SiO_2 (35 nm) were used as gate and dielectric, while e-beam evaporated Ni was again used for the top source and

drain contacts. Magnetron sputtering was employed to grow a 10-nm-thick SnO thin film at room temperature under an Opp of 5.4%, followed by a rapid thermal annealing treatment at 250 ^{o}C for 100 s. The device exhibited a μ_{FE} of 1.8 cm^2 V^{-1} s^{-1} and V_{th} of 0.24 V. An I_{on}/I_{off} ratio of approximately 1.0×10^5 and small subthreshold swing value of 0.55 V dec^{-1} were reported, both of which are record values for this material. The small SS value and high I_{on}/I_{off} ratio indicated that significantly improved defect levels and reduced trap density at semiconductor/dielectric interface can be achieved using p-type SnO. A summary of the studies reported for p-type SnO TFTs is given in **Table 5**, which includes the key performance metrics of this oxide.

4.4. Nickel oxide thin-film transistors

NiO based TFTs were firstly demonstrated by physical routes. In 2008, Shimotani et al. demonstrated the first p-type FET using NiO single crystal as channel employing an electric double-layer gating technique, the μ_{FE} and I_{on}/I_{off} ratio were 1.6×10^{-4} cm^2 V^{-1} s^{-1} and 130.[269] In 2013, Jiang et al. reported a NiO based p-type TFT with μ_{FE} and I_{on}/I_{off} ratio of 5.2 cm^2 V^{-1} s^{-1} and 2.2×10^3.[271] The NiO layer was formed by thermally oxidizing the e-beam evaporated Ni thin film. By controlling the annealing time, partial oxidization was achieved on the NiO layer and a quasi-discontinuous Ni layer remained at the semiconductor/dielectric interface, which contributed to the high mobility of this TFT. NiO based p-type FETs have also been successfully fabricated by chemical routes. Takami et al. reported synthesis of NiO nanoplate by hydrothermal method and a FET was built by drop-cast the solution on top of the substrate.[270] However, this FET showed high operation voltage (~100 V) and low drain current (on the order of nanoamperes). In 2014, Liu et al. reported a solution processed p-type NiO TFT, the device exhibited a μ_{sat} of 0.141 cm^2 V^{-1} s^{-1}.[272] Matsubara et al. fabricated a NiO:Li NW FET on SiO_2 dielectric using Pt as S&D electrodes, the NW was synthesized by solution process.[273] The NW FET exhibited a μ_{FE} of 3.4×10^{-4} cm^2 V^{-1} s^{-1}.

In order to summarize the large number of studies we have presented so far on the various classes of p-type oxides, **Figure 30a** gives a graphical summary of their key performance indicators. The horizontal axis shows the number of studies we reviewed, and the vertical axis shows the relevant thin film or TFT properties. It is clear that the binary copper oxides (mainly Cu_2O) give the best Hall mobility values, despite their limited optical band gap (E_{opt} < 2.4 eV) and low carrier concentration (~ 10^{14} cm^{-3}). The Cu-bearing semiconductors (E_{opt} > 3 eV) and SnO (E_{opt} ≈ 2.7 eV) show moderate Hall mobility values, clearly suggesting that there is further room to optimize their mobilities. Considering all p-type semiconductors analyzed in this review, the maximum and minimum reported Hall mobility values are 256 and 0.2 cm^2 V^{-1} s^{-1}, respectively. (see details in **Table 1, 2 and 3**) The average Hall mobility (below 10 cm^2 V^{-1} s^{-1}) of p-type oxide is lower than the n-type a-GIZO (>10 cm^2 V^{-1} s^{-1})[2]. This means that additional materials design strategies are needed to further disperse the valence band, and better deposition processes are needed to suppress the inner layer defects to improve the mobility of p-type oxide semiconductors. Perhaps techniques like ALD and ultralow-damage sputtering methods should be evaluated. **Figure 30b, c and d** show a summary of the main TFT parameters (μ_{FE}, SS and I_{on}/I_{off} ratio) reported using the different classes of p-type oxides. It is noted that although binary copper oxides exhibit higher average Hall mobility values, their TFT field-effect mobility is lower than expected (< 1 cm^2 V^{-1} s^{-1}). This indicates that a large density of interface traps exist at the semiconductor/dielectric interfaces, or the presence of significant amount of defect inside the thin films (e.g., metal interstitials or clusters, grain boundaries, or higher valence state impurities). In contrast, although SnO thin film shows a moderate Hall mobility, the average device field-effect mobility is higher than those of binary copper oxides or Cu-bearing oxides. Giving the fact that more than 20 reports have presented p-type SnO TFTs with μ_{FE} more than 1 cm^2 V^{-1} s^{-1}, this oxide seems to be the most promising one at this stage. However, the SS

value and I_{on}/I_{off} ratio are less than expected, and further efforts are needed to reduce the trap density at the semiconductor/dielectric interface. This can be accomplished by using higher quality dielectrics, low energy processes, and capping layers.

4.5. Stability of p-type oxide thin-film transistors

The TFT stability evaluation under given gate bias stress is of great importance, since the TFTs are among the most frequently used units in display circuits. Any gate-bias-induced degradation in device performance or shift in threshold voltage would seriously affect the overall performance of the corresponding circuits.[319-322] The stretch-exponential model can be used to describe the threshold voltage shift under gate-bias at given temperature, which was first proposed by Jackson et al. to explain the gate-bias induced threshold voltage shift in hydrogenated amorphous silicon (a-Si:H).[323] The observed threshold voltage shift was attributed to the creation of dangling bond defects in the a-Si:H channel. However, Gelatos et al. observed a parallel threshold voltage shift with the bias and a similar thermal activation energy value in both positive and negative gate bias stress tests. Thus, they claimed that the threshold voltage shift was due to the generation of bias stress induced defects (interface trap creation) at the a-SiN_x:H/a-Si:H interface instead of inside a-Si:H body.[324, 325] In their view, the parallel shift of threshold voltage could be attributed to the trapping of carriers in the interface or bulk dielectric layers, while the creation of trap states is always accompanied by subthreshold slope or mobility degradation.

The gate bias stability test has been extensively reported using the stretch-exponential model for n-type TFTs employing a-Si, ZnO, IZO and a-IGZO as channel layers.[320, 324-330] Similarly, this model was also successfully used to describe the threshold voltage shift behavior for p-type Cu_2O TFTs[331] and organic TFTs[332], where the stretch-exponential equation can be expressed as[325]

$$|\Delta V_{th}| = |\Delta V_{th0}| \left\{ 1 - \exp\left[-(t/\tau)^{\beta} \right] \right\} \quad (16)$$

where the $|\Delta V_{th0}|$ is $|\Delta V_{th}|$ at infinite time; β is the stretch exponential exponent; and τ is the characteristic time constant, $\tau = \tau_0 \exp(E_\tau / kT)$, represents the characteristic trapping time of carriers, where τ_0 is the thermal prefactor for emission over the barrier. The thermal activation energy can be expressed by $E_a = E_\tau \beta$, in which E_τ is the average effective energy barrier for carriers to enter the dielectric.[325]

4.5.1. Binary copper oxide TFT stability

Zou et al. studied the stability of p-type Cu_2O TFTs by applying a positive gate bias of 10 V for 3600 s.[113] (**Figure 31**) Two TFTs were subjected to the gate bias stress, one with SiO_2 dielectric and another with a bilayer stack of HfO_2/SiO_2 dielectric, maintaining the same overall thickness. Both devices showed negative shift in transfer curves after stress, with negligible change in subthreshold slope. This result indicated that charge trapping at the semiconductor/dielectric interface was dominant and the creation of trap states could be neglected. The value of the threshold voltage shift was also monitored and a relatively small shift (ΔV_{th} = 1.4 V) was observed for the TFTs with HfO_2/SiO_2 bilayer dielectric. The authors attributed the more stable performance of bilayer dielectric device to the high quality interface between channel and bilayer dielectric. The high quality interface also improved the device performance, including higher mobility, near zero volt threshold voltage, small subthreshold swing value, and a small leakage current.

Nam et al. observed a slight increase in the on current of Cu_2O TFTs during operation after exposing the device in air for 4 weeks.[126] The TFT had a staggered bottom-gate structure and the channel thickness was 45 nm. It should be noted that no obvious change in subthreshold swing was observed, which indicated that the creation of trap states between channel and dielectric was negligible. In addition, a counterclockwise hysteresis was observed

in a dual sweep transfer curve measurement and was attributed to hole trapping at interface and/or bulk trap states within the semiconductor.

Park et al. studied the stability of Cu_2O TFT under gate bias stress in oxygen and vacuum environments.[132] (**Figure 32**) A negative gate bias of -30 V was applied on the gate electrode for 1.5×10^4 s in air and vacuum environment, resulting in a negative shift in the transfer curve in both cases. It was noted that the shift in threshold voltage in air and vacuum was identical, indicating that the stability of Cu_2O TFT was insensitive to oxygen partial pressure, which was attributed to the high electronegativity of oxygen and the negligible electron concentration in the conduction band of Cu_2O (oxygen was expected to take electrons from the channel and form O^- species that chemically attached on the channel surface). The TFT was then subjected to a negative bias stressing (-25 V) in air for different durations. This test showed a gradual negative shift in the transfer curve with increasing stress time, while the slope and subthreshold slope showed no obvious change, indicating that the trapping of holes at the channel/dielectric interface or inside the dielectric layers was responsible for the shift of the transfer curve, and that the creation of interface trap states could be neglected. The recovery behavior was also studied, and it was found that both the stressing and recovery behavior could be explained well by the stretched-exponential model, with a time constant τ and stretched-exponential exponent β of 1.1×10^5 s and 0.245 in stressing section; 4.5×10^3 s and 0.26 in the recovery section, respectively.[132] However, the positive gate bias stress showed a small V_{th} shift and a significant change in subthreshold slope, which indicated that the interface trap states were created by the positive bias stress, while the small concentration of free electrons in the channel was responsible for the V_{th} shift. The device simply recovered to the initial state after removing the positive gate bias.

4.5.2. Tin monoxide TFT stability

In 2014, Chiu et al. reported the threshold shift of p-type SnO TFT under constant gate bias stressing.[206] (**Figure 33**) The TFT was subjected to gate-bias stress measurements for various stress durations with stress levels ranging from 5 to 12.5 V, while the source and drain electrodes were grounded during the test. They observed that the transfer curves parallel shifted with the applied gate bias stress polarity. They also observed that the magnitude of the shift gradually increased with stress time and level. The interface trap state density was about 5.7×10^{13} cm^{-2} before stressing the device, and no obvious degradations of the subthreshold slope or the field-effect mobility were observed during the whole stress measurement. This result indicated that the creation of trap states induced by the gate bias was negligible, and that the dominant mechanism for the threshold voltage shift was charge trapping at the semiconductor/dielectric interface or inside the gate dielectric. The threshold voltage shift under various gate-bias stress voltages could be fitted well by the stretch exponential relation, suggesting that charge trapping is the dominant mechanism for the instability of SnO TFT in the gate voltage stressing tests. The stretch exponential exponent β was extracted and was found to be 0.35 and 0.42 for positive and negative-bias stress, respectively, which is similar to most of the bias stress test on n-type oxides.[327] The trapping time of carriers, τ, was estimated to be between 1.2×10^4 and 6.8×10^5 s for negative gate bias stress, while for positive gate bias stress this value was calculated to be 1.3×10^3 to 4.7×10^4 s, which is smaller compared with most oxide semiconductors. A similar decrease in carrier trapping time was also reported by Chen et al., where the zinc tin oxide TFT was exposed to an increased oxygen partial pressures.[330] The smaller τ obtained in the positive gate-bias stress was attributed to the bias-induced adsorption of oxygen during the stability test.

The long term durability test of SnO based p-type TFT was studied by Han et al. in 2014.[204] (**Figure 34**) A significant degradation in mobility (from 1.2 to 0.14 cm^2 V^{-1} s^{-1}) and a negative shift in threshold voltage were observed after dipping the TFT into de-ionized (DI) water for 3 hrs. This result indicated that the humidity or water molecules in air would be a

major concern for the long term operation in ambient conditions. Although the exact mechanism for the humidity effects on the electrical performance is still unclear, the degradation of p-type performance by water exposure was attributed to two possible causes: the interaction between the hole charges and polar water molecules at the grain boundaries, or the increased energy barrier for hole inter-grain transport due to the polar water molecules residing at the grain boundaries. In contrast, oxygen exposure showed negligible effect on the operation of SnO TFT, which was attributed to the high electronegativity of oxygen and negligibly small free electron concentration in p-type oxide semiconductors, as reported by Park et al. for Cu_2O TFTs.[331] The SU-8 passivation layer was used to protect the device from ambient conditions and the devices were exposed to air for 100 days. The results showed a noticeable degradation in mobility and a large negative shift in threshold voltage for the unpassivated devices, while the SU-8 passivated devices showed a negligible change in device operation. In addition, the SU-8 passivated sample exhibited high stability after cyclic transfer curve measurements, manifesting the importance of encapsulation for stabilizing the operation of SnO based device. Actually, the SU-8 passivation layer was also studied using n-type GIZO TFTs by Olziersky et al., and a similar increase in long-term stability under gate-bias stressing was reported; interestingly, the passivated GIZO devices showed about 2 orders of magnitude decrease in the off current.[322]

In a subsequent work, Han et al. studied the mechanism of instability of SnO TFTs under negative gate-bias stress and water exposure.[207] A noticeable degradation in both subthreshold slope and mobility was observed after dipping the SnO TFT in DI water for 3 hrs, indicating the creation of hole trap states from the residual water molecules. The larger negative shift of threshold voltage after the DI water exposure was attributed to the partially depleted channel from the residual-water-related hole traps near valence band edge. The existence of hole trapping sites was further confirmed by observing a significantly larger frequency dispersion in the capacitance-voltage curves for the DI water-exposed SnO TFTs.

In contrast, in the positive gate-bias stress test, no significant threshold voltage shift was observed in water-exposed TFTs, implying that the concentration of electron traps near the conduction band was negligible. The gate-bias stress tests under vacuum and oxygen atmosphere were also performed. The results showed that the oxygen partial pressure did not significantly affect the electrical stability, consistent with previous reports.[204]

5. Performance of Oxide Based CMOS Inverters

Transistors are the fundamental building block of electronic circuits for many applications. Single channel type transistors (mainly n-type) have been remarkably successful in display applications. Yet, many emerging electronic applications (both digital and analogue), beyond displays, would be benefit greatly, if high performance oxide-based CMOS devices were available today. The reasons behind this are the well-known low-power consumption, low waste heat generation, high noise margins, high logic swing output, and high circuit integration density and architectural simplicity of CMOS devices.[11-14] The realization of such device has of course been hampered by the difficulty encountered in developing a robust p-type oxide material. Nonetheless, commendable efforts have been exerted in developing such a device by the research community and hence we review those activities next.

5.1. Binary copper oxide CMOS inverters

In 2011, Dindar et al. presented a novel vertical geometric complementary inverter fabricated on flexible polyethersulfone (PES) substrate.[122] (**Figure 35**) The CMOS inverter was composed of two stacked TFTs with a common gate electrode, i.e. a coplanar top-gate TFT at the bottom, and a staggered bottom-gate TFT at the top. Amorphous (a-) GIZO was used as n-channel layer in the bottom TFT, while Cu_2O was used as p-type counterpart in the top TFT. Both a-GIZO and Cu_2O were deposited by magnetron sputtering at room

temperature, with a deposition of Al_2O_3 dielectric layer by ALD at low temperature. A common gate of Ni/Au/Ni was e-beam evaporated between two Al_2O_3 dielectric layers. The whole device was annealed at low temperature of 150 ^oC in oxygen for 30 min, which is compatible with flexible PES substrate. The device exhibited saturation mobility, V_{th} and I_{on}/I_{off} ratio of 2.2×10^{-3} cm^2 V^{-1} s^{-1}, -4.75 V and 3.9×10^2 for the p-type TFT; 1.58 cm^2 V^{-1} s^{-1}, 5.77 V and ~10^5 for the n-type TFT, respectively. The final oxide based vertical CMOS inverter showed a large gain value of 120 at V_{dd} = 20 V, with a NM_H and NM_L of 11.68 and 6.01 V, respectively. The achievement of this encouraging logic swing performance at low processing temperature was actually a good milestone for this field.

5.2. Tin monoxide CMOS inverters

A few reports on p-type SnO TFTs have shown an initial exploration of oxide based CMOS inverters. Ou et al. firstly fabricated an inverter composed of two SnO_x based p-type TFTs with different threshold voltages, the inverter showed a maximum gain of 2.8 at a V_{dd} of -80 V.[212] Another demonstration of oxide CMOS inverter based on p-type SnO_x was then reported by Dhananjay et al.[211] (**Figure 36**) By serially connecting p-type SnO_x TFT with n-type In_2O_3 TFT, a CMOS inverter was successfully fabricated, with a maximum gain of 11 at V_{dd} =100 V. Chiu et al. reported another oxide based CMOS inverter composed by p-type SnO and n-type ZnO TFTs, both the SnO and ZnO channel layer were deposited from magnetron sputtering.[210] (**Figure 37**) Geometric aspect ratio $(W/L)_p/(W/L)_n$ of 5 was chosen in circuit design in order to compensate the unbalanced channel mobilities, which were 0.33 and 3.5 cm^2 V^{-1} s^{-1} for p- and n-channel, respectively. The CMOS inverter exhibited a maximum gain of 17, NM_H of 4.29 V and NM_L of 4.35 V at V_{dd} = 10V. The noise margin values were close to the ideal value of $V_{dd}/2$. The authors also fabricated an oxide based five-stage ring oscillator for the first time. The oscillation frequency was ~2 kHz, indicating a propagation delay per stage of 50 μs, at V_{dd} of 14 V. The author attributed the large

propagation delay to the parasitic capacitance from the large overlap between the gate and the source/drain electrodes.

Martins et al. demonstrated a flexible CMOS inverter with SnO p-type transistors on paper, the paper was used as both substrate and dielectric.[13, 14, 203, 333] (**Figure 38**). The n-type transistors were made of GIZO. Both n-TFT and p-TFT exhibited acceptable performance on the paper substrate, with μ_{FE} of 21 and 0.8 cm^2 V^{-1} s^{-1}. The geometric aspect ratios $[(W/L)_p/(W/L)_n]$ were designed to be 1.83 and 2 to balance the device current and performance in p- and n-TFTs. The CMOS inverter showed an average gain of 4.5 for devices operated under V_{dd} = 15 or 17 V. (**Figure 39**) The absence of hard saturation in the p-type TFT is a possible reason for the lower than expected CMOS inverter logic swing quality, which was possibly related to the damage of the dielectric (paper) surface during the sputtering deposition. The NM_H and NM_L for paper based CMOS inverter were 9.8 and 1.0 V at V_{DD} = 15 or 17 V. The maximum static power dissipation was estimated to be 32 pW per inverter at the high or low states, although this value could be further decreased by downsizing the devices. The authors stated the device performance could recover from bending without creating fold lines, while the creation of fold lines led to electrical breakdown. Besides the CMOS inverter, analog and digital circuits such as transmission gate, common source CMOS amplifier, differential CMOS amplifier, NOR gate and NAND gate were also successfully built on the paper substrate.[14] This was the first demonstration of paper based oxide CMOS, and it indicated that oxide semiconductors can be made at low processing temperature on recyclable substrates.

In 2011, Nomura et al. presented a CMOS-like inverter based on ambipolar SnO TFTs, where two identical SnO layers served as both n- and p-channel.[173] (**Figure 40**) Clear inverter behavior was observed in both first and third quadrants, which is characteristic behavior of ambipolar TFTs based CMOS inverter. The gain values are 2.4 and 2.5 for the first and third quadrant, respectively, at $|V_{dd}|$ = 5 V. The low gain value was attributed to the

unbalanced performance for n- and p-channel, specifically, the low mobility of n-TFT. Although the CMOS performance was ordinary, the achievement in simplifying the process of fabricating CMOS inverter based on oxides was clever, and could in principle simplify the fabrication process of CMOS devices.

In 2012, Liang et al. presented the high performance CMOS-like inverter based on ambipolar SnO TFTs.[175, 179] (**Figure 41**) Significant efforts were exerted in balancing both the transport and injection of holes and electrons. The balancing of electron and hole transport, i.e. the ambipolar performance, was achieved by thinning the SnO film and the optimal thickness was found between 26 and 40 nm. The enhancement for n-type mobility was attributed to oxygen deficiency, as excess oxygen would significantly reduce electron concentration. This was supported by the experimental fact that a 15 nm SnO transistor showed only p-type unipolar operation, since the thinner channel would attain a higher oxygen concentration when exposed to the same annealing treatment. The balancing of electron and hole injection was achieved by aligning the band structure between SnO and electrodes. The onset voltage (voltage with minimum current in the transfer curve) showed positive shift with increase of metal work function and a near zero onset voltage was achieved by using Ni/Au electrode (work function 5.1-5.2 eV). Finally, a CMOS-like inverter comprising two identical ambipolar SnO TFTs was fabricated and exhibited good electrical performance: maximum gain of 30.6 and 31.3 in first and third quadrant at $|V_{dd}|$ =40 V, a good logic voltage swings (> 82% of V_{OH}) and wide noise margins (~20%) at $|V_{dd}|$ =40 V. Moreover, the CMOS-like inverter showed a great long term stability while exposing the device to relative humidity of 20-30%. In addition, by employing only one oxide semiconductor, the process for semiconductor layer fabricating and patterning was simplified. The excellent performance and simple fabrication technique demonstrated that ambipolar CMOS-like inverters based on ambipolar SnO TFTs could be a useful building block in transparent electronic circuits.

Yabuta et al. reported formation of both n- and p-type SnO TFTs using the same deposition process.[37] By selectively employing a SiO_2 passivation layer on top of SnO, the as-deposited SnO film was transformed to either p-type SnO (passivated) or n-type SnO_2 phase (unpassivated). The SiO_2 passivation layer effectively protected the underlying SnO layer from being over oxidized even at a high annealing temperature of 400 ^oC; in contrast, the un-passivated one was oxidized to SnO_2. **Figure 42** shows the conceptual design of the SnO-based complimentary circuit, where n-type SnO_2 phase was selectively formed from the same starting thin films of SnO_x. Following this conceptual design, novel concepts for fabricating complementary devices were reported by Nayak et al.[198] and Wang et al.[199]

In 2014, Nayak et al. reported fabrication of CMOS inverter from a single step deposition of SnO active layer.[198] (**Figure 43**) Selective oxidation was achieved by using two different Al_2O_3 dielectric layers: one prepared by solution process (SD-Al_2O_3), and the other by atomic layer deposition on the same substrate (ALD-Al_2O_3). The SnO channel layer was deposited on both dielectrics at the same time by magnetron sputtering. After annealing the as-deposited SnO film, the SnO region on top of the ALD-Al_2O_3 dielectric showed p-type behavior, as expected[167, 195]. In contrast, the SnO region on top of SD-Al_2O_3, surprisingly, showed n-type behavior. A detailed materials analysis was performed to understand this phenomena. Fourier transform infrared (FT-IR) spectroscopy of SD-Al_2O_3 films (**Figure 44a**) showed an intense and broad peak centered at 3368 cm^{-1} corresponding to the stretching vibration of the hydroxyl (OH-) group, indicating the presence of a large number of OH-groups. From the x-ray photoelectron spectroscopy (XPS) spectra, an Al2p peak at lower binding energy in the solution derived film was observed and attributed to the incomplete oxidation of the SD-Al_2O_3 film, consistent with the FT-IR results. (**Figure 44b**) The deconvolutions of O1s peaks also revealed a significantly higher content of OH-group in the SD-Al_2O_3 film (**Figure 44c and d**). As the SnO film was deposited and annealed simultaneously on both dielectrics, the phase transformation from p- to n-type on top of the

SD-Al_2O_3 dielectric was attributed to the presence of a large number of OH-groups in this dielectric, which acted as additional oxygen source during annealing. This helped to convert the metastable SnO phase to an n-type SnO_2 phase. A CMOS inverter was demonstrated by serially connecting the p- and n-type TFTs, showing a maximum gain of 3 at V_{dd} = 10 V. Although this gain value is low, the fabricated devices clearly demonstrated the validity of this novel surface approach for simultaneous formation of n- and p-type tin oxide thin film channel layers.

In 2015, Wang et al. reported a tin oxides based CMOS inverter by local oxidation process.[199] (**Figure 45**) The n-type polarity was realized by employing a dual-active-layer structure, i.e. stacking a Cu_2O passivation layer on top of SnO channel. A single tin oxide channel layer was deposited, this followed by the deposition of a Cu_2O passivation layer on top of SnO channel in selected regions on the substrate, forming bilayer structures. The devices were exposed to the same post deposition annealing process at 190 ^oC in air for 30 min. The single layer TFTs showed typical p-type behavior with μ_{FE} of 2.39 $cm^2\ V^{-1}\ s^{-1}$. In contrast, the bilayer TFTs exhibited an n-type behavior with μ_{FE} of 0.23 $cm^2\ V^{-1}\ s^{-1}$. The n-type conductivity of the latter was attributed to the presence of a dominant SnO_2 phase in the bilayer system, which is actually predicted under thermodynamic considerations, as illustrated by the Ellingham diagram (**Figure 46a**). The XPS analysis was performed to confirm this phase transformation process (**Figure 46b, c & d**). The quantitative XPS analysis of Sn^{4+} in the bilayer sample showed an increased Sn^{4+} content (from 28 to 78 at%) after annealing, which was responsible for the n-type polarity. It should be noted that the annealing temperature for achieving SnO_2 phase (190 ^oC) was much lower than the normally needed to from SnO_2 (300 ^oC)[164] and this was attributed to a local oxidation process in the bilayer system. The copper oxide layer was located directly above tin oxide layer and thus acted as an oxygen source.[199] Finally, a CMOS inverter was fabricated by connecting p- and n- type tin oxide TFTs with a small geometric aspect ratio to balance the current in each channel. The

CMOS inverter exhibited a maximum gain of 4 at V_{dd} =10V. Although the performance for CMOS inverter was ordinary, it showed yet another approach for the realization of tin oxide based CMOS devices with simple process flow at low temperature. The summary of the literature reports on tin monoxide based CMOS inverters is given in chronological order in **Table 6**.

6. Performance of Oxide Based p-n Junctions

The p-n junction is a simple yet powerful device that composed of serially connected p- and n-type semiconducting films.[302, 303] The p-n junction devices have also been widely used in sensor applications, such as thermometer, photodetector and radiometer. Most of the existing diodes are based on silicon with narrow band gap, thus not transparent. Hence the development of high performance transparent diodes is a critical activity for large-area transparent electronics to be deployed. Since the first all-oxide junction diode demonstrated by Kudo et al.,[65] an increasing number of studies have been reported, with very good results.[226, 234] In spite of the short research history on oxide based p-n junctions, excellent performance devices were reported on p-type amorphous $ZnO{\cdot}Rh_2O_3$ and $ZnCo_2O_4$ (ZCO).[226, 231, 234-236] For the ZCO based diode, a recent report showed a large forward current to reverse current (I_f/I_r) ratio of ~ 2×10^{10} at ± 2V, an ideality factor of 2.04 and long term stability, where the p-ZCO layer was deposited at room temperature by PLD. This junction diode is the best among oxide based p-n junction diodes that we could find in the open literature reports.[234]

6.1. Ternary copper bearing oxide p-n junctions

The research on transparent oxide p-n junctions using p-type Cu-bearing semiconductors has been an active field with a variety of transparent p-n junction devices reported, including traditional rectifying and light emitting diodes. The first Cu-bearing oxide p-n junction was

achieved using $SrCu_2O_2$ (SCO) by Kudo et al.[65] The p-type SCO film was deposited at the relatively low temperature of 350 ^oC by reactive evaporation, while the n-type ZnO was deposited on top of SCO by sputtering at 250 ^oC. Transparent n^+-ZnO and ITO were used as n-and p-contacts, and the whole junction showed a transparency over 60% in the visible range. For electrical performance, a turn on voltage of 0.6 V, ideality factor of 1.62, and I_f/I_r ratio of 80 was reported. P-n junctions based on the p-SCO and n-ZnO oxides were also reported by others[27-29, 334, 335], among which UV light emitting diode performances were demonstrated by heteroepitaxial interfaces of the p- and n-type oxides.[27-29] The lattice mismatch between (112) SCO and (0001) ZnO was ~0.1%. A sharp emission band centered at 382 nm was detected in the electroluminescence (EL) spectra, which was attributed to the transition associated with electron–hole plasma in ZnO[27]. In addition to the above mentioned heterojunctions, transparent oxide p-n diodes were also fabricated using homojunction scheme. In one study, n- and p-doped delafossite $CuInO_2$, with Sn and Ca as n- and p-dopants, respectively, was used to fabricate a transparent homojunction diode.[24, 25] The polycrystalline $CuInO_2$ films were deposited by PLD with n- and p-dopants at around 450 ^oC, while ITO contacts were applied to both layers. The p-n junction diode showed a turn-on voltage of 1.8 V and a visible range transparency of 60 to 80%. Furthermore, a p-n junction diode based on epitaxial LaCuOSe and amorphous (a-) GIZO n-layer was reported.[336] The LaCuOSe was epitaxially grown on (001) MgO substrate by reactive solid-phase epitaxy (R-SPE) technique[74] which involved an annealing step over 1000 ^oC. The a-GIZO was grown by PLD at room temperature and patterned by shadow mask. This diode showed a turn-on voltage of 6 V and I_f/I_r ratio of 10. It also exhibited a sharp blue EL peak at 430 nm at room temperature, which was attributed to intrinsic excitons in LaCuOSe.[336] A summary of the key studies on transparent oxide p-n junctions comprising ternary Cu-bearing oxide or chalcogenide thin films is shown in **Table 7**.

6.2. Binary copper oxide p-n junctions

Binary copper oxides have also been evaluated in p-n junction devices, especially for rectifying[91, 92, 132, 138, 338-341] and photovoltaic (PV) applications[90-94, 96, 98]. The interest in CuO for PV applications is mainly due to its nearly ideal band gap of 1.4 eV, which theoretically can give a solar conversion efficiency of 33%.[137, 342-345]

Recently, Chen et al. demonstrated a p-Cu_2O/n-GIZO oxide based diode on flexible PEN substrate with excellent performance in both static and dynamic measurements.[138] (**Figure 47**) Both the p-type Cu_2O and n-type GIZO were deposited by magnetron sputtering at room temperature on ITO coated glass or PEN substrates, without any post deposition thermal treatments. The XRD revealed a polycrystalline structure of p-Cu_2O and amorphous nature in n-GIZO films. The major carrier type was confirmed by Hall measurement, which showed satisfactory mobility values for both layers: 2.11 and 15.06 $cm^2\ V^{-1}\ s^{-1}$ for Cu_2O and a-GIZO, respectively. The fabricated p-n junction diodes showed excellent performance with knee voltage of 0.44 V, ideality factor of 1.4, forward current density of 1 A cm^{-2} and high rectification ratio up to 3.4×10^4 at ±1.2V on both glass and PEN substrates. No obvious degradation in device performance was detected on the flexible substrate, even during the bending tests. The flexible p-n diode was subjected to a high frequency rectifying test, under an alternating current (ac) input signal with an amplitude of |4 V|. The diode showed a high output direct current (dc) voltage of no less than 3 V at a frequency of 13.56 MHz; this value decreased to 2.5 V when the input ac frequency was increased to 27 MHz. This experiment demonstrated that excellent all-oxide (p-Cu_2O/n-GIZO) diodes can be fabricated. A summary of the recent reports on binary copper oxides p-n junction diodes is shown in **Table 8**.

6.3. Tin monoxide p-n junctions

Several reports exist on p-n junction diodes employing SnO as p-type layer. In 2011, Hosono et al.[177] demonstrated the bipolar (ambipolar) nature of SnO for the first time, where

both the conduction band and valence band energy levels can be doped, while retaining the large direct band gap and transparency in the visible range. (**Figure 48**) Moreover, the density function theory calculations indicated sufficient dispersions in both CBM and VBM, which meant that large mobilities for both electron and hole were possible in this material.[9, 178, 179] By doping Sb into SnO lattice, similar donor and acceptor levels were found, between 92-96 meV. A symmetry in hole and electron mobility values (confirmed by Hall measurements) was also obtained, showing the potential of employing ambipolar SnO in complementary metal oxide devices, where a balanced n- and p-channel performance is desired.[173, 179] Subsequently, a p-n homojunction diode was fabricated using SnO and SnO:Sb layers, and a clear rectifying effect was shown with a knee voltage of 0.7 V, which approached the theoretical built-in potential value.

In 2014, Sathyamoorthy et al. showed a tin oxide based diode using p-SnO/n-SnO_2 on glass substrate.[346] Both SnO and SnO_2 were grown by reactive thermal evaporation, while a thermal annealing at 600 ^oC for 2 hrs was applied to fully oxidize the as-deposited SnO_2 before depositing the top SnO layer. This diode showed a knee voltage of 3.5 V with a large ideality factor of 21.5. About 80 nm of interfacial layer was found by TEM, which was claimed to be responsible for the non-ideal operation of this p-n diode. Um et al.[189] also reported a p-SnO/n-SnO_2 diode by reactive magnetron sputtering where both n- and p-type films were prepared in the same deposition by varying the deposition parameters, followed by thermal annealing at 300 ^oC for 2 hrs. XPS measurement confirmed the dominance of Sn^{2+} and Sn^{4+} oxidation states in p- and n-type layer, respectively. The diode had a knee voltage of 2.3 V, but no further information on the device operation was reported. Wang et al. recently demonstrated another all tin oxide (p-SnO/n-SnO_2) diode, deposited by DCMS, with an ideality factor of 3.39 and rectification ratio of 10^3.[347] The better device performance than previous reports was attributed to the improvement in the quality of the interface between p-SnO and n-SnO_2. The p-n diode also exhibits a large temperature induced knee voltage shift

of -20 mV $^{o}C^{-1}$, which is attributed to the large band gap of tin oxides and shallow states from the small activation energy in p-SnO layer. The authors suggested this p-n junction could also be used as transparent temperature sensor.

Yang et al. reported a p-n diode based on p-SnO and n-SnO_2:Sb.[192] The p-type SnO film was prepared by magnetron sputtering at substrate temperature of 200 ^{o}C, and the film showed polycrystalline structure and high hole mobility of 3.34 $cm^2 V^{-1} s^{-1}$. The p-n junction diode showed a knee voltage of 2.88 V, with rectifying ratio of 510, ideality factor of 6.4 and the reverse saturation current of 2.79 μA. In 2015, Li et al. reported a detailed study on a p-n junction diode based on p-SnO/n-Si.[217] The SnO film was deposited by e-beam evaporation at room temperature followed by a RTA treatment at 350 ^{o}C for 10 min in Ar atmosphere. The work function and relative permittivity of SnO were determined to be 4.3 eV and 18.8±1.7 by ultraviolet photoelectron spectroscopy and capacitance-voltage measurement, which is in agreement with previous measured values by Ogo et al. and Quackenbush et al.[9, 178] The diode exhibited a rectifying ratio of 58 at ± 2 V, an ideality factor of 5.5 and small serial resistance of 7.3 Ω. In addition, the measured I-V behavior of diode was explained by the band structure model of SnO and Si based on the measured and reported data. Three regions were identified in the diode I-V curves: (1) blind zone (V_D < 0.69 V), where the injections of both electron and hole are inhibited with negligible current flowing through the device, (2) electron-injection-only zone (0.69 V < V_D < 1.12 V), where only electrons can be injected into depletion region, and (3) dual-carrier-injection zone (V_D > 1.12 V), where both electrons and holes can be injected, i.e. the diode was turned on. This detailed analysis of the I-V behavior verified the existing electronic structure reports and helped understand the fundamental physical properties of SnO. A summary of recent studies of tin monoxide p-n junction diodes is shown in **Table 9**.

6.4. Spinel oxide p-n junctions

In 2003, Narushima el al.[226] reported the first amorphous p-type oxides of $ZnRh_2O_4$ (or a-$ZnO{\cdot}Rh_2O_3$), with optical band gap around 2.1 eV and conductivity around 2 S cm^{-1}. (**Figure 49**) Such films were used to build oxide-based all amorphous flexible p-n junction diodes with n-type a-GIZO layer. The diode exhibited a knee voltage of 2.1 V, ideality factor of 2.3, and an I_f/I_r ratio of 10^3 at ±5 V. The knee voltage value was in agreement with the band gap of $ZnRh_2O_4$. A further research by Kamiya et al.[228] explained the diode behavior using a parallel diode model, in which the nature of p-type conductivity in the amorphous structure was also elucidated. In 2003, Ohta et al.[227] fabricated a heteroepitaxial p-n junction diode using p-$ZnRh_2O_4$/n-ZnO by reactive solid-phase epitaxy technique. The polycrystalline p-$ZnRh_2O_4$ was deposited at room temperature followed by a high temperature ambient annealing (950 ^oC). The diode exhibited a knee voltage of 2 V and rectifying behavior, in addition, photovoltage was observed when the diode was exposed to UV-light illumination.

Recently, a high performance p-$ZnCo_2O_4$ (ZCO)/n-ZnO based diode was reported by Schein et al.[234] (**Figure 50**) The p-type ZCO was deposited by PLD at room temperature, showing amorphous structure. The diode presented a solid performance with ideality factor of 2.04, I_f/I_r ratio of 2×10^{10} at ±2 V, and acceptable long-term stability in air. In 2015, Schlupp et al.[235] demonstrated all amorphous p- ZCO and n-ZTO based p-n junction diodes, with ideality factors between 1.2 and 2.0 and high rectifying ratios of 4×10^6 at ±1.6 V, when a thin insulator was inserted between p- and n-layer. The p-i-n diode also showed stable performance when subjected to high temperature stability testing. Amorphous p-type ZCO was also applied to fabricate a gate oxide-based junction field-effect transistors (channel: n-ZnO), where p-n junction based gate was used to induce the channel transconductance, showing satisfactory performance.[232, 233]

The summary of p-type spinel oxide p-n junction diodes is shown in **Table 10**. It should be noted that this class of p-type materials shows great application potential in the p-n junction diodes field, with several reports demonstrating excellent diode performance.[226, 234]

6.5. Nickel oxide p-n junctions

P-n diodes using NiO as p-layer were demonstrated using both physical and chemical routes. In 2003, Ohta et al. reported an all oxide (p-NiO/n-ZnO) diode with strong rectifying effect and response to UV illumination.[275, 283] The ideality factor of this p-n diode was ~2, owing to a smooth interface between the PLD deposited NiO and ZnO layers. In 2013, Münzenrieder et al. reported a p-NiO/n-GIZO p-n diode on a flexible polyimide substrate, where the whole device was fabricated at room temperature.[276] The NiO layer was deposited by DC reactive sputtering from a metallic Ni target and a mixture gas of Ar and O_2. The ideality factor and rectification ratio was 3.2 and 10^4, respectively. The flexible p-n diode was successfully used for rectifying a 50 Hz AC input in both flat and bent mode.

A graphical summary of the literature reports on oxide p–n junctions that have been analyzed in this review is shown in **Figure 51**. As depicted, significant improvement has been achieved in oxide p-n junction diodes using spinel oxide as p-layer. Specifically, I_f/I_r ratio over 10^{10} and ideality factor near 2 have been achieved. In contrast, the other p-type oxide based p-n junction diodes shows moderate performance, with most of the I_f/I_r ratios being less than 10^3, and the ideality factors far from 2. A possible reason is that both high performance p-type SnO and Cu_2O are metastable phases, and are quite sensitive to device processing conditions, including both atmospheric exposure and the processing temperature. Defect reduction by using low energy deposition processes, and using better quality interfaces can be expected to achieve higher performance diodes with these two binary oxides. In addition, as the operating quality of p-n junction diode is highly dependent on the interface between n-/p-layer, the surface roughness and impurity phase should be carefully controlled, suggesting that the amorphous or epitaxial bilayer thin films are preferred.

7. Memory Devices using p-Type Oxides

7.1. Resistive switching memory

Various types of memories have been demonstrated using p-type oxides. Two common types are resistive switching (RS) memory and ferroelectric field-effect memory. The first type of memory has been commonly reported using p-type oxides.[278-280, 348-353] The device works by changing the state of the material from low resistance to high resistance state using a large writing (forming) voltage. Then the memory is read non-destructively using a small read voltage. RS property of oxide materials was firstly discovered in NiO and has been studied for 50 years, since Gibbons et al. studied the cyclic repetitive RS effect in crystalline NiO.[348] The bi-stable resistive memory switching property has potential application in resistive random access memory (RRAM), which has several advantages including high-speed switching, structural simplicity, nonvolatile and nondestructive readout.[354-358] Reproducible bi-stable memory switching has been achieved by adjusting the oxygen content in non-stoichiometric NiO_x thin films.[278, 279, 349] The operation of the bi-stable memory switching process is characterized by an abrupt increase (or drop) in leakage current after the applied voltage exceeds the SET (or RESET) voltage. The high and low current states are defined as ON (or OFF) state, corresponding to the '1' or '0' binary code. Both states are nonvolatile, and stably reversible and reproducible. Typical current ratio between ON and OFF states is $10^2 \sim 10^3$.[278, 279, 349] The switching mechanism between ON and OFF state has been studied for long time and is still controversial. The filament model was proposed by Gibbons et al., where they attributed the resistance switching to the formation and rupture of metallic filaments.[348] Other models were also proposed for the filament formation, including immobile neutral impurities and injected anodic metal ions.[359, 360] Lee et al. studied the memory switching of NiO by density functional theory and attributed the formation and rupture of the filament to the migration of oxygen ions during the oxidation/reduction process.[280] A charge-trapping model was proposed by Austin, where the trapping and release of charge near the electrodes switched the resistance of the whole structure.[350] Seo et al.

studied the resistance switching performance of various stoichiometric NiO_x thin film and attributed the RS effect to the existence of deep-level metallic nickel defect states in non-stoichiometric NiO_x thin films.[278] In 2012, Yoon et al. showed a solution processed NiO memory device with improved RS performance, where a solution processed NiO thin film with embedded Ni nanoparticles were used.[351] The reported memory device showed improved operating voltage, including both SET, RESET and forming voltage, while the ON state to OFF state switching ratio was increased to ~10^5 at 0.2 V.

In 2014, Hota et al. presented an electroforming-free RS memory device based on p-type oxide SnO with a simple Al/SnO/ITO metal-insulator-metal structure.[352] (**Figure 52**) The device was fabricated at room temperature without any post-deposition thermal treatment. A reasonable memory performance was observed for this p-type semiconductor memory device with HRS/LRS ratio of over10^2, retention times more than 10^3 s and dc cycling switch stability. The Al electrode/SnO interface was found to play a critical role in the operation of the RS memory device. Specifically, the high resistance state (HRS) and low resistance state (LRS) were attributed to the formation and reduction of a very thin AlO_x interfacial barrier layer between p-type SnO and Al contacts. Ohmic conduction was observed in the LRS over the entire voltage range, while the HRS showed a transition from Ohmic to Poole-Frenkel conduction at high voltage. This RS effect in SnO was explained by the formation/rupture of conducting filaments involving the exchange and migration of oxygen vacancies and Sn interstitials along with the interfacial effect. The low DC voltage and the electroforming-free operation were encouraging attributes, but warrant additional study, particularly on the stability of the devices.

In 2015, the same team reported another resistive switching device based on a bilayer p-type SnO thin film in a nanoscale cross point (300 × 300 nm^2) device configuration.[353] (**Figure 53**) By using an SnO (oxygen rich)/SnO (oxygen deficient) bilayer film in between the Au/Ti and Al electrodes, an improved memory performance was observed compared with

the single layer SnO. Specifically, HRS/LRS ratio of 10^3, retention time more than 6×10^3 s, stable DC switching and low voltage operation. It was also observed that multiple charge transport mechanisms exist in both LRS and HRS states of the device, depending on the bias condition, including Ohmic conduction and space charge limited conduction. The elemental mapping by electron energy loss spectroscopy (EELS), energy-dispersive X-ray spectroscopy (EDS) and HRTEM confirmed the existence of interfacial TiO_x and AlO_x layers, which were deemed responsible for the LRS and HRS state, respectively.

7.2. Ferroelectric field-effect memory devices

Electronic information can also be stored in a ferroelectric material due to the existence of two stable polarization states. Two common ferroelectric memory devices are known: capacitors and ferroelectric field-effect transistors (FeFET).[361, 362] A major concern of ferroelectric capacitor devices is the destructive data read-out, as the voltage applied to read the memory state of the device reverses the polarization state of the ferroelectric element. Thus, every time after a bit is read, it needs to be written again. In contrast, FeFET memories can be read out non-destructively. During the read operation, a small drain voltage is applied to measure channel conductance without the need to switch polarization state in the active ferroelectric material.[363] FeFET is a promising candidate for non-volatile random access memory due to its high speed, high packing density, low power consumption, and non-destructive read-out operation. However, the FeFET memory devices suffer from the short retention time, which has been attributed to a) the depolarization effect and b) gate leakage current and trapping in the gate stack.[364]

The vast majority of FeFET devices have used n-type semiconductor channels. In contrast, there have been limited reports on FeFETs with p-type semiconductor channel, all of which have used p-type organic small molecules or polymers resulting in low hole mobility

(<1 cm^2 V^{-1} s^{-1}).[362, 365-368] Recently, few reports have emerged on p-type FeFET devices using p-type oxide semiconductors with more promising performance.[200, 363]

In 2014, Caraveo-Frescas et al. demonstrated the first p-type SnO based ferroelectric polymer FET memory device on both rigid and flexible substrates with record mobility.[198] (**Figure 54**) The ferroelectric polymer poly[vinylidenefluoride-co-trifluoroethylene] [P(VDF-TrFE)] was used as the gate dielectric and transparent p-type oxide (SnO) as the active channel layer. The maximum device fabrication temperature was 200 ^oC on both rigid glass and flexible polyimide substrates. The top-gated devices exhibit a μ_{FE} of 3.3 and 2.5 $cm^2 V^{-1} s^{-1}$ on the rigid and flexible substrates, respectively. The mobilities achieved in these devices were over 10 times higher than previously reported p-channel FeFET memory devices. For memory performance, large memory window (16 V), low read voltage (-1 V), and excellent retention characteristic up to 5000 s had been achieved. This demonstration meant both n- and p-type transparent non-volatile memory devices can be fabricated, giving the possibility to fabricate more complex devices and circuits on transparent and flexible substrates with low-power consumption.

In 2014, Khan et al. reported a hybrid organic/inorganic ferroelectric memory device with multilevel information storage using transparent p-type SnO semiconductor and ferroelectric P(VDF-TrFE) polymer.[200] (**Figure 55**) The dual-gated memory device was comprised of a top FeFET and a bottom thin-film transistor (TFT). The devices were fabricated at low temperatures (200 ^oC), demonstrating excellent performance with high μ_{FE} of 2.7 cm^2 V^{-1} s^{-1} and low SS value of 4 V dec^{-1}. The channel conductance of the bottom-TFT and the top-FeFET could be controlled independently by the bottom and top gates, respectively. The hybrid ferroelectric memory device demonstrated multilevel nonvolatile information storage with good retention characteristics. Specifically, a large memory window of 18 V and two bit (four levels) information storage from a single FeFET with good retention characteristics up to 3600 s was obtained.

8. Miscellaneous applications of p-type oxides

8.1. Hole-transporting layer

Another important application for NiO is the hole-transporting layer (HTL) in organic optoelectronic[272, 281-283, 369] or PV[263, 282, 284, 285] devices. Irwin et al. had performed excellent study on the usage of NiO for HTL in organic PV devices.[248, 285] In solar cell applications, a major issue is the formation of Ohmic contact between the bulk-heterojunction (BHJ) and anode or cathode, which can in principle facilitate the collection of the generated charges (electrons or holes). For this purpose, an interfacial layer (or HTL) is often inserted between the ITO anode and the p-layers, to collect the generated holes and block the injection of the minority carriers (electrons). For the former, a HTL with a large enough work function is needed to match the VB or highest occupied molecular orbital (HOMO) of the selected p-type materials; for the latter, a HTL with a large band gap is needed to provide sufficient barrier for electrons. This HTL layer should also have enough transparency in the PV device spectral working range. Finally, the HTL itself should have enough hole mobility for fast collection of charges. Based on these requirements, NiO is believed to be an excellent candidate for HTL in PV devices. For example, NiO has a large work function of 5.4 eV, which matches the HOMO level (5.2 ~ 5.5 eV) of the state of the art organic p-type semiconductors.[285, 370] Taking the E_g value of 3.7 eV, the CB of NiO is located at 1.7 eV below the vacuum level, while the typical lowest unoccupied molecular orbital (LUMO) level for organic p-layer is 4.0 eV below the vacuum level. Thus, a ~2.3 eV barrier exists to block electrons. The conductivity and transparency of NiO can actually be tuned by changing the stoichiometry. Furthermore, compared with the bare ITO surface, a homogeneous distribution of the conductivity in NiO coated ITO surface was achieved, which enhanced the power conversion efficiency of organic PV devices.[285] The same mechanism works for the light-emitting diode (LED) or organic LED devices, compared with ITO, a better band alignment between NiO

and p-layers can be achieved. It was shown that, the NiO HTL increases both the LED drain current and the luminance, and enhances the power conversion efficiency.[272, 281, 282, 369]

8.2. Electrochromics

Electrochromism is a phenomenon where the material optical properties can be changed reversibly by an applied voltage, along with injection and extraction of ions within the crystal structure of the material.[371-374] Electrochromic (EC) devices have attracted increasing attention due the low switching voltage, high coloration efficiency, and memory effect under open circuit condition.[372, 373, 375] Generally, EC devices consist of two electrochromic materials with opposite coloring polarities (anodical and cathodical), located on TCO substrates (e.g., FTO or ITO), and separated by an electrolyte layer.[372] The EC devices are often used in "smart window" applications. When a voltage is applied, the optical transparency and reflectivity of the EC materials change simultaneously, maintaining the brightness and warmness in corresponding area.[376] Due to the high EC efficiency, durability and cyclic reversibility, NiO is one of the most widely used anodic EC oxide, especially along with tungsten oxide (WO_3) on the cathode side[376, 377]. After an external voltage is applied, NiO (bleached state) is oxidized to $NiO(OH)_x$ (colored state) along with the insertion of OH^- and extraction of e^-, and vice versa.[261]

Up to now, EC NiO film with stable colored and bleached performance has been fabricated by DCMS[378], EBE[265], PLD[379] and other conventional PVD methods. Pereira et al. studied the thickness effect of e-beam evaporated NiO film on their EC performance.[265] The thicker film showed better EC performance, including higher color efficiency, better color modulation and cyclic stability. No post-deposition annealing was performed on these films, indicating the compatibility of this method with low cost and flexible substrates. Penin et al. reported pulsed laser deposited NiO film with increased cyclic stability by doping WO_3 (5% in target) inside NiO host matrix.[379] Recently, high EC performance NiO films with fast

response and high coloration efficiency were reported from atmospheric chemical routes, including sol-gel[380], chemical bath deposition (CBD)[381] and ultrasonic spray deposition[382]. Jiao et al. reported a durable EC NiO film by sol-gel process.[380] Xia et al. reported a porous NiO film with noticeable coloration efficiency (42 $cm^2 C^{-1}$ at 550 nm) and good memory effect by CBD.[381] Owing to the porous structure, a fast switching speed was also observed. Tenent et al. studied the EC performance of NiO and NiO: Li by ultrasonic spray deposition, where NiO crystallites were embedded in amorphous LiNiO matrix.[382] Higher transmission modulation, faster coloration, longer durability was achieved in the NiO: Li system.

8.3. Gas sensors

Oxide semiconductor gas sensors have been attracting significant attention due to their low cost, high sensitivity, reliability, and compatibility with existing solid-state device fabrication processes. The majority of the commercial gas sensors employ n-type oxides as sensing materials, for instance, SnO_2 and ZnO.[383] However, p-type oxides are receiving increasing attention for gas sensor applications. Recently, Kim and Lee systematically reviewed the use of p-type oxide semiconductors in gas sensing applications.[384] In contrast to n-type oxides, the gas sensing mechanism for p-type oxide is related to the modulation of the carrier (hole) concentration in the shell hole accumulation layer (HAL), which is formed by the electrostatic interaction between the oppositely charge species (O_2^-, O^-, and O^{2-}).[385] When exposed to the reducing gases, the electrons are injected into the material surface and decrease the hole concentration in the HAL, thus increase the channel resistance. When exposed to oxidizing gases, the resistance of p-type oxide semiconductors decreases due to the increase of hole concentration in the HAL by ionosorption of the oxidizing gas.[384] It is noted that the gas response of p-type oxide based gas sensors (pGS) is shown to be lower than that of n-type oxide sensors, even when these two oxides have identical morphology, which indicates that the achievement of high performance pGS is challenging.[386]

So far, several methods have been proved to boost the response of pGS, including electronic sensitization (by aliovalent doping)[387-389], chemical sensitization (by loading catalyst)[390] and minimizing the particle size[391]. Kim et al. and Yoon et al. reported that, by doping Fe, the gas response (R_{gas}/R_{air}) of p-type NiO to 100 ppm C_2H_5OH could be increased to 172.5 and 245, where the pristine sensor only showed a small gas response of ~ 5.[387, 389] The authors attributed the improved gas response to the decrease of the carrier concentration in HALs. The gas selectivity can also be modulated by doping specific elements or loading catalysts.[388, 390] Cho et al. reported that the response of p-type NiO nanotubes gas sensor to C_2H_5OH can be increased to 11.7 (from 1.69), after loading Pt nanoparticles (NPs) onto the surface of the nanotubes.[390] Good quality p-type oxides can enable the fabrication of p-n junctions as gas sensors, which offers additional ways to monitor the targeted gas concentration, including monitoring the I-V characteristics of the p-n junction diodes,[392-394] and measuring AC resistance [395, 396]. Ushio et al. reported an increase in forward current when their patterned CuO/ZnO p-n junctions were exposed to high humidity.[392] Hikita et al. successfully detected and distinguished CO and H_2 by applying AC resistance measurement across their CuO/ZnO heterocontacts.[395, 396] The gas response can be enhanced by simply using the p-n nanocomposite as the sensing material.[397, 398] Tamaki et al. reported a CuO/SnO_2 p-n nano-junctions based gas sensor, which showed high response and selectivity to the H_2S gas. When the nano-composites were exposed to H_2S, the surface of CuO was converted into CuS, followed by the change in the junction built-in potential, and the resistance of the whole sensor.[398] Another merit for p-type oxides in gas sensing application is the enhancement in the sensing performance of the n-type oxide based sensors, when the p-type NPs are loaded on n-type oxide structure.[399-401] It has been shown that the sensors can recover faster by embedding p-type oxide NPs in the host n-type oxide structure.[399] It was also reported that humidity-independent gas sensors can be built in this way, where the host n-type oxide surface would stay dry due to the higher affinity between p-type oxide (NiO) and

water molecules.[400, 401] Therefore, p-type oxide semiconductors show promising potential in gas sensing applications, where not only can they be independently used as gas sensing materials, but also enhance the performance of n-type oxide gas sensors.

9. Conclusion and Perspective

A detailed review of hole-transporting (p-type) transparent oxide semiconductor materials and devices has been presented. Material physics, various device architectures, and potential applications of these interesting materials have been discussed, along with their promising attributes and remaining challenges. These oxides, in principle, have significant potential in many applications that were discussed including low-power electronics, transparent electronics, display applications, memories, gas sensors, electrochromics, and photovoltaics.

In our view, the current state of affairs in p-type oxide development reveals a mixture of promising developments and persistent challenges that continue to hamper commercial adoption of these materials. On the one hand, p-type oxides have made good progress in the development of resistive memories, oxide p-n junction diodes, and electrochromics. Resistive memories based on p-type NiO are a good example of this progress. In addition, transparent p-n junctions with excellent characteristics have been achieved using p-type oxides. NiO has been used as hole transporting layer in photovoltaic and optoelectronic devices. Some commercial electrochromics may actually employ transition metal oxides including p-type NiO. On the other hand, p-type oxide development for transparent electronics has been challenging. Several innovative studies to improve the performance of thin-film transistors and inverters comprising p-type oxides have been reported. These rely on both device fabrication as well as surface chemistry approaches and have achieved some good inverter gains. In addition, progress has been made in reducing the off state currents of some p-type oxide thin-film transistors using approaches such as capping layers, better quality dielectrics,

and surface treatments. Nanoscale (e.g. nanowire) devices have now been reported and do show that significant performance improvements can be made at small device geometries. Transparent ferroelectric memory devices comprising p-type oxides have been reported for the first time showing good mobilities and retention characteristics. This even includes multistate memory devices that show good stability. Process developments have been reported and some p-type oxides can now be made using atomic layer deposition and chemical synthesis, with encouraging performance.

In terms of future research directions, several key areas need to be addressed. For example, the off state current in p-type oxide TFTs is still very high compared to n-type semiconductors and must be reduced. While the I_{on}/I_{off} ratio requirements for some devices (e.g., CMOS) may not be as high as those for display applications, the off currents still need to be significantly decreased for p-type oxides to find widespread adoption. This can come about by adopting strategies that improve the semiconductor growth process and reduce interfacial defects. The fact remains that interfacial defect/states are much higher in p-type oxides than in the n-type ones. This is also reflected in the subthreshold slope value in p-type oxide TFTs, which can be several volts in some cases. Capping layers, better process technologies (e.g., ALD), and high quality dielectrics can all help in that regard and should be more thoroughly investigated. Further, the mobilities of these oxides remain relatively low, despite some encouraging field-effect mobilities that have been recently reported. This can complicate CMOS circuit design. Improving mobilities will require fundamental material design strategies to induce further orbital overlap and band dispersion such as dopant incorporation, strain engineering, or microstructure control. It will also require technological developments involving new and more precise processing technologies, such as atomic layer deposition or low-energy sputtering.

In addition, more studies are needed to improve our understanding of the electrical and environmental stability of these p-type oxides in various device configurations. The effect of

passivation layers on stability should also be more thoroughly evaluated. Recent studies have shown that multilayer channels (involving semiconductor/dielectric superlattices) have improved stability of n-type devices. The same should be evaluated for p-type materials. Another area that seems to have received less attention is nanoscale devices. There are many studies on n-type nanowire transistors, but very little on p-type oxide nanowires. Recent data on SnO indicates that nanowire devices exhibit better mobility than thin-film transistor devices.

Another area of future potential is gas sensing. Many gas sensors are based on n-type channel materials. However, p-type oxides can be combined with n-type oxides to fabricate junction diode sensors, which, for some applications, can be far more suited than resistance or TFT sensors. Substitutional doping of p-type oxides can also influence their sensitivity to gases and organic vapors as has been shown recently. However, this area is still in its early stages of development and more efforts should be exerted in this direction. Despite some progress in electrochromics, smart window applications require faster color change, nanostructured p-type oxides such as NiO may help in this direction and such studies need to be expanded. For the practical use of RRAM devices, low driving voltage, high ON state to OFF state current ratio, and cyclical reliability are needed. In this respect, nanoparticle embedded NiO based RRAM devices indeed show improvements, however, more studies are required for better understanding the mechanism behind formation and rupture of the conduction filament. This can be done using in-situ microscopy to fully understand the switching mechanism in these systems. In photovoltaic applications, more efforts are needed in optimizing the hole transporting layers. For instance, the p-type mobility of this layer needs to be enhanced. Also, efforts should be made in achieving even better band alignment to the p-semiconductors, to lower the charge collecting barriers, and hence increase the energy conversion efficiency.

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References

[1] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, 24, 2945.

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* **2004**, 432, 488.

[3] R. L. Hoffman, B. J. Norris, J. F. Wager, *Appl. Phys. Lett.* **2003**, 82, 733.

[4] P. F. Carcia, R. S. McLean, M. H. Reilly, G. Nunes, *Appl. Phys. Lett.* **2003**, 82, 1117.

[5] E. M. C. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Gonçalves, A. J. S. Marques, L. M. N. Pereira, R. F. P. Martins, *Adv. Mater.* **2005**, 17, 590.

[6] E. Fortunato, R. Martins, *Phys. Status Solidi RRL* **2011**, 5, 336.

[7] E. Fortunato, R. Barros, P. Barquinha, V. Figueiredo, S.-H. K. Park, C.-S. Hwang, R. Martins, *Appl. Phys. Lett.* **2010**, 97, 052105.

[8] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2008**, 93, 032113.

[9] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Kimura, M. Hirano, H. Hosono, *Phys. Status Solidi A* **2009**, 206, 2187.

[10] H. Hosono, *19th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)* **2012**, p. 1.

[11] A. L. Robinson, *Science* **1984**, 224, 705.

[12] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, *Nature* **2007**, 445, 745.

[13] R. Martins, A. Nathan, R. Barros, L. Pereira, P. Barquinha, N. Correia, R. Costa, A. Ahnood, I. Ferreira, E. Fortunato, *Adv. Mater.* **2011**, 23, 4491.

[14] R. F. P. Martins, A. Ahnood, N. Correia, L. Pereira, R. Barros, P. Barquinha, R. Costa, I. M. M. Ferreira, A. Nathan, E. Fortunato, *Adv. Funct. Mater.* **2013**, 23, 2153.

[15] H. Kawazoe, M. Yasukawa, H. Hyodo, M. Kurita, H. Yanagi, H. Hosono, *Nature* **1997**, 389, 939.

[16] H. Hosono, N. Kikuchi, N. Ueda, H. Kawazoe, *J. Non-Cryst. Solids* **1996**, 200, 165.

[17] H. Raebiger, S. Lany, A. Zunger, *Phys. Rev. B* **2007**, 76, 045209.

[18] A. Togo, F. Oba, I. Tanaka, K. Tatsumi, *Phys. Rev. B* **2006**, 74, 195128.

[19] H. Yanagi, H. Kawazoe, A. Kudo, M. Yasukawa, H. Hosono, *J. Electroceram.* **2000**, 4, 407.

[20] H. Kawazoe, H. Yanagi, K. Ueda, H. Hosono, *MRS Bull.* **2000**, 25, 28.

[21] P. C. Hsu, C. C. Wu, H. Hiramatsu, T. Kamiya, H. Hosono, *ECS J. Solid State Sci. Technol.* **2014**, 3, Q3040.

[22] K. Ueda, T. Hase, H. Yanagi, H. Kawazoe, H. Hosono, H. Ohta, M. Orita, M. Hirano, *J. Appl. Phys.* **2001**, 89, 1790.

[23] T. Mine, H. Yanagi, K. Nomura, T. Kamiya, M. Hirano, H. Hosono, *Thin Solid Films* **2008**, 516, 5790.

[24] H. Yanagi, K. Ueda, H. Ohta, M. Orita, M. Hirano, H. Hosono, *Solid State Commun.* **2001**, 121, 15.

[25] H. Yanagi, T. Hase, S. Ibuki, K. Ueda, H. Hosono, *Appl. Phys. Lett.* **2001**, 78, 1583.

[26] A. Kudo, H. Yanagi, H. Hosono, H. Kawazoe, *Appl. Phys. Lett.* **1998**, 73, 220.

[27] H. Ohta, K.-i. Kawamura, M. Orita, M. Hirano, N. Sarukura, H. Hosono, *Appl. Phys. Lett.* **2000**, 77, 475.

[28] H. Ohta, K. Kawamura, M. Orita, N. Sarukura, M. Hirano, H. Hosono, *Electron. Lett* **2000**, 36, 984.

[29] H. Ohta, M. Orita, M. Hirano, H. Hosono, *J. Appl. Phys.* **2001**, 89, 5720.

[30] H. Hosono, *Thin Solid Films* **2007**, 515, 6000.

[31] K. Ueda, S. Inoue, S. Hirose, H. Kawazoe, H. Hosono, *Appl. Phys. Lett.* **2000**, 77, 2701.

[32] H. Hiramatsu, K. Ueda, H. Ohta, M. Orita, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2002**, 81, 598.

[33] S. Park, D. A. Keszler, M. M. Valencia, R. L. Hoffman, J. P. Bender, J. F. Wager, *Appl. Phys. Lett.* **2002**, 80, 4393.

[34] G. W. Watson, *The Journal of Chemical Physics* **2001**, 114, 758.

[35] A. Walsh, G. W. Watson, *Phys. Rev. B* **2004**, 70, 235114.

[36] L. Y. Liang, Z. M. Liu, H. T. Cao, Z. Yu, Y. Y. Shi, A. H. Chen, H. Z. Zhang, Y. Q. Fang, X. L. Sun, *J. Electrochem. Soc.* **2010**, 157, H598.

[37] H. Yabuta, N. Kaji, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2010**, 97, 072111.

[38] B. S. Li, K. Akimoto, A. Shen, *J. Cryst. Growth* **2008**, 311, 1102.

[39] E. Ruiz, S. Alvarez, P. Alemany, R. A. Evarestov, *Phys. Rev. B* **1997**, 56, 7189.

[40] M. Nolan, S. D. Elliott, *Phys. Chem. Chem. Phys.* **2006**, 8, 5350.

[41] D. O. Scanlon, B. J. Morgan, G. W. Watson, A. Walsh, *Phys. Rev. Lett.* **2009**, 103, 096405.

[42] M. T. Greiner, M. G. Helander, W.-M. Tang, Z.-B. Wang, J. Qiu, Z.-H. Lu, *Nat. Mater.* **2012**, 11, 76.

[43] G. Hautier, A. Miglio, G. Ceder, G. M. Rignanese, X. Gonze, *Nat. Commun.* **2013**, 4, 2292.

[44] G. Hautier, A. Miglio, D. Waroquiers, G. M. Rignanese, X. Gonze, *Chem. Mater.* **2014**, 26, 5447.

[45] H. Yanagi, S.-i. Inoue, K. Ueda, H. Kawazoe, H. Hosono, N. Hamada, *J. Appl. Phys.* **2000**, 88, 4159.

[46] A. N. Banerjee, S. Kundoo, K. K. Chattopadhyay, *Thin Solid Films* **2003**, 440, 5.

[47] H. Gong, Y. Wang, Y. Luo, *Appl. Phys. Lett.* **2000**, 76, 3959.

[48] S. Gao, Y. Zhao, P. Gou, N. Chen, Y. Xie, *Nanotechnology* **2003**, 14, 538.

[49] J. Tate, M. K. Jayaraj, A. D. Draeseke, T. Ulbrich, A. W. Sleight, K. A. Vanaja, R. Nagarajan, J. F. Wager, R. L. Hoffman, *Thin Solid Films* **2002**, 411, 119.

[50] M. Sasaki, M. Shimode, *J. Phys. Chem. Solids* **2003**, 64, 1675.

[51] C. W. Teplin, T. Kaydanova, D. L. Young, J. D. Perkins, D. S. Ginley, A. Ode, D. W. Readey, *Appl. Phys. Lett.* **2004**, 85, 3789.

[52] R. Nagarajan, N. Duan, M. K. Jayaraj, J. Li, K. A. Vanaja, A. Yokochi, A. Draeseke, J. Tate, A. W. Sleight, *Int. J. Inorg. Mater.* **2001**, 3, 265.

[53] M. K. Jayaraj, A. D. Draeseke, J. Tate, A. W. Sleight, *Thin Solid Films* **2001**, 397, 244.

[54] N. Duan, A. W. Sleight, M. K. Jayaraj, J. Tate, *Appl. Phys. Lett.* **2000**, 77, 1325.

[55] Y. Kakehi, S. Nakao, K. Satoh, T. Yotsuya, *Thin Solid Films* **2003**, 445, 294.

[56] R. Nagarajan, A. D. Draeseke, A. W. Sleight, J. Tate, *J. Appl. Phys.* **2001**, 89, 8022.

[57] X. Nie, S.-H. Wei, S. B. Zhang, *Phys. Rev. Lett.* **2002**, 88, 066405.

[58] J. Pellicer-Porres, A. Segura, A. S. Gilliland, A. Muñoz, P. Rodríguez-Hernández, D. Kim, M. S. Lee, T. Y. Kim, *Appl. Phys. Lett.* **2006**, 88, 181904.

[59] J. Tate, H. L. Ju, J. C. Moon, A. Zakutayev, A. P. Richard, J. Russell, D. H. McIntyre, *Phys. Rev. B* **2009**, 80, 165206.

[60] M. Nolan, *Thin Solid Films* **2008**, 516, 8130.

[61] D. O. Scanlon, G. W. Watson, *J. Phys. Chem. Lett.* **2010**, 1, 3195.

[62] M. Fang, H. He, B. Lu, W. Zhang, B. Zhao, Z. Ye, J. Huang, *Appl. Surf. Sci.* **2011**, 257, 8330.

[63] J. Luo, Y. J. Lin, H. C. Hung, C. J. Liu, Y. W. Yang, *J. Appl. Phys.* **2013**, 114, 033712.

[64] H. Ohta, M. Orita, M. Hirano, I. Yagi, K. Ueda, H. Hosono, *J. Appl. Phys.* **2002**, 91, 3074.

[65] A. Kudo, H. Yanagi, K. Ueda, H. Hosono, H. Kawazoe, Y. Yano, *Appl. Phys. Lett.* **1999**, 75, 2851.

[66] K. Ueda, S. Inoue, H. Hosono, N. Sarukura, M. Hirano, *Appl. Phys. Lett.* **2001**, 78, 2333.

[67] S.-i. Inoue, K. Ueda, H. Hosono, N. Hamada, *Phys. Rev. B* **2001**, 64, 245211.

[68] H. Hiramatsu, K. Ueda, H. Ohta, M. Orita, M. Hirano, H. Hosono, *Thin Solid Films* **2002**, 411, 125.

[69] H. Hiramatsu, M. Orita, M. Hirano, K. Ueda, H. Hosono, *J. Appl. Phys.* **2002**, 91, 9177.

[70] H. Hiramatsu, K. Ueda, T. Kamiya, H. Ohta, M. Hirano, H. Hosono, *J. Phys. Chem. B* **2004**, 108, 17344.

[71] H. Hiramatsu, K. Ueda, K. Takafuji, H. Ohta, M. Hirano, T. Kamiya, H. Hosono, *J. Appl. Phys.* **2003**, 94, 5805.

[72] K. Ueda, H. Hosono, *J. Appl. Phys.* **2002**, 91, 4768.

[73] K. Ueda, H. Hosono, *Thin Solid Films* **2002**, 411, 115.

[74] H. Hiramatsu, K. Ueda, K. Takafuji, H. Ohta, M. Hirano, T. Kamiya, H. Hosono, *J. Mater. Res.* **2004**, 19, 2137.

[75] Z. Q. Yao, B. He, L. Zhang, C. Q. Zhuang, T. W. Ng, S. L. Liu, M. Vogel, A. Kumar, W. J. Zhang, C. S. Lee, S. T. Lee, X. Jiang, *Appl. Phys. Lett.* **2012**, 100, 062102.

[76] H. F. Jiang, X. B. Zhu, H. C. Lei, G. Li, Z. R. Yang, W. H. Song, J. M. Dai, Y. P. Sun, Y. K. Fu, *J. Alloys Compd.* **2011**, 509, 1768.

[77] Y. S. Zou, H. P. Wang, S. L. Zhang, D. Lou, Y. H. Dong, X. F. Song, H. B. Zeng, *RSC Adv.* **2014**, 4, 41294.

[78] B. K. Meyer, A. Polity, D. Reppin, M. Becker, P. Hering, P. J. Klar, T. Sander, C. Reindl, J. Benz, M. Eickhoff, C. Heiliger, M. Heinemann, J. Blasing, A. Krost, S. Shokovets, C. Muller, C. Ronning, *Phys. Status Solidi B* **2012**, 249, 1487.

[79] U. D. Lanke, M. Vedawyas, *Nucl. Instrum. Methods Phys. Res., Sect. B* **1999**, 155, 97.

[80] S. Åsbrink, L. J. Norrby, *Acta Crystallogr., Sect. B* **1970**, 26, 8.

[81] M. A. Rafea, N. Roushdy, *J. Phys. D: Appl. Phys.* **2009**, 42, 015413.

[82] K. Matsuzaki, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2008**, 93, 202107.

[83] W. H. Brattain, *Rev. Mod. Phys.* **1951**, 23, 203.

[84] W. Y. Ching, Y.-N. Xu, K. W. Wong, *Phys. Rev. B* **1989**, 40, 7684.

[85] D. Wu, Q. Zhang, M. Tao, *Phys. Rev. B* **2006**, 73, 235206.

[86] M. Heinemann, B. Eifert, C. Heiliger, *Phys. Rev. B* **2013**, 87, 115111.

[87] E. Fortunato, V. Figueiredo, P. Barquinha, E. Elamurugu, R. Barros, G. Goncalves, S. H. K. Park, C. S. Hwang, R. Martins, *Appl. Phys. Lett.* **2010**, 96, 192102.

[88] A. O. Musa, T. Akomolafe, M. J. Carter, *Sol. Energy Mater. Sol. Cells* **1998**, 51, 305.

[89] A. Mittiga, E. Salza, F. Sarto, M. Tucci, R. Vasanthi, *Appl. Phys. Lett.* **2006**, 88, 163502.

[90] R. Jayakrishnan, *Mater. Sci. Semicond. Process.* **2013**, 16, 1608.

[91] Y. S. Jeong, H. Kim, H. S. Lee, *J. Alloys Compd.* **2013**, 573, 163.

[92] K. J. Saji, S. Populoh, A. N. Tiwari, Y. E. Romanyuk, *Phys. Status Solidi A* **2013**, 210, 1386.

[93] S. W. Lee, Y. S. Lee, J. Heo, S. C. Siah, D. Chua, R. E. Brandt, S. B. Kim, J. P. Mailoa, T. Buonassisi, R. G. Gordon, *Adv. Energy Mater.* **2014**, 4, 1301916.

[94] T. Minami, Y. Nishi, T. Miyata, *Appl. Phys. Lett.* **2014**, 105, 212104.

[95] A. Wagner, M. Stahl, N. Ehrhardt, A. Fahl, J. Ledig, A. Waag, A. Bakin, *Proceedings of SPIE* **2014**, 8987, 898726.

[96] L. D. Wang, Y. X. Zhao, G. H. Wang, H. Zhou, C. Geng, C. Q. Wu, J. W. Xu, *Sol. Energy Mater. Sol. Cells* **2014**, 130, 387.

[97] A. Zakutayev, C. M. Caskey, A. N. Fioretti, D. S. Ginley, J. Vidal, V. Stevanovic, E. Tea, S. Lany, *J. Phys. Chem. Lett.* **2014**, 5, 1117.

[98] M. Pavan, S. Ruhle, A. Ginsburg, D. A. Keller, H. N. Barad, P. M. Sberna, D. Nunes, R. Martins, A. Y. Anderson, A. Zaban, E. Fortunato, *Sol. Energy Mater. Sol. Cells* **2015**, 132, 549.

[99] J. Zhang, J. Liu, Q. Peng, X. Wang, Y. Li, *Chem. Mater.* **2006**, 18, 867.

[100] S. Deng, V. Tjoa, H. M. Fan, H. R. Tan, D. C. Sayle, M. Olivo, S. Mhaisalkar, J. Wei, C. H. Sow, *J. Am. Chem. Soc.* **2012**, 134, 4905.

[101] M. K. Wu, J. R. Ashburn, C. J. Torng, P. H. Hor, R. L. Meng, L. Gao, Z. J. Huang, Y. Q. Wang, C. W. Chu, *Phys. Rev. Lett.* **1987**, 58, 908.

[102] J. B. Torrance, A. Bezinge, A. I. Nazzal, T. C. Huang, S. S. P. Parkin, D. T. Keane, S. J. LaPlaca, P. M. Horn, G. A. Held, *Phys. Rev. B* **1989**, 40, 8872.

[103] A. Chen, S. Haddad, Y.-C. Wu, T.-N. Fang, Z. Lan, S. Avanzino, S. Pangrle, M. Buynoski, M. Rathor, W. Cai, N. Tripsas, C. Bill, M. VanBuskirk, M. Taguchi, *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International* **2005**, 746.

[104] A. Chen, S. Haddad, Y. C. Wu, Z. Lan, T. N. Fang, S. Kaza, *Appl. Phys. Lett.* **2007**, 91, 123517.

[105] J. C. Park, J. Kim, H. Kwon, H. Song, *Adv. Mater.* **2009**, 21, 803.

[106] J. Y. Xiang, J. P. Tu, X. H. Huang, Y. Z. Yang, *J. Solid State Electrochem.* **2008**, 12, 941.

[107] H. A. Al-Jawhari, *Mater. Sci. Semicond. Process.* **2015**, 40, 241.

[108] K. Matsuzaki, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Phys. Status Solidi A* **2009**, 206, 2192.

[109] W. Seiler, E. Millon, J. Perriere, R. Benzerga, C. Boulmer-Leborgne, *J. Cryst. Growth* **2009**, 311, 3352.

[110] A. Subramaniyan, J. D. Perkins, R. P. O'Hayre, S. Lany, V. Stevanovic, D. S. Ginley, A. Zakutayev, *APL Mater.* **2014**, 2, 022105.

[111] C. R. Iordanescu, D. Tenciu, I. D. Feraru, A. Kiss, M. Bercu, D. Savastru, R. Notonier, C. E. A. Grigorescu, *Dig. J. Nanomater. Biostruct.* **2011**, 6, 863.

[112] X. Zou, G. Fang, L. Yuan, M. Li, G. Wenjie, X. Zhao, *IEEE Electron Device Lett.* **2010**, 31, 827.

[113] X. Zou, G. J. Fang, J. W. Wan, X. He, H. N. Wang, N. S. Liu, H. Long, X. Z. Zhao, *IEEE Trans. Electron Devices* **2011**, 58, 2003.

[114] K. R. Balasubramaniam, V. M. Kao, J. Ravichandran, P. B. Rossen, W. Siemons, J. W. Ager, *Thin Solid Films* **2012**, 520, 3914.

[115] F.-Y. Ran, M. Taniguti, H. Hosono, T. Kamiya, *J. Disp. Technol.* **2015**, accepted.

[116] J. W. Park, H. Jang, S. Kim, S. H. Choi, H. Lee, J. Kang, S. H. Wei, *J. Appl. Phys.* **2011**, 110, 103503.

[117] J. Deuermeier, J. Gassmann, J. Brotz, A. Klein, *J. Appl. Phys.* **2011**, 109, 113704.

[118] H. J. Li, C. Y. Pu, C. Y. Ma, S. Li, W. J. Dong, S. Y. Bao, Q. Y. Zhang, *Thin Solid Films* **2011**, 520, 212.

[119] V. X. Hien, J. L. You, K. M. Jo, S. Y. Kim, J. H. Lee, J. J. Kim, Y. W. Heo, *Vacuum* **2015**, 111, 60.

[120] I. Shogo, M. Takahiro, A. Katsuhiro, *Jpn. J. Appl. Phys.* **2000**, 39, L786.

[121] S. Y. Sung, S. Y. Kim, K. M. Jo, J. H. Lee, J. J. Kim, S. G. Kim, K. H. Chai, S. J. Pearton, D. P. Norton, Y. W. Heo, *Appl. Phys. Lett.* **2010**, 97, 222109.

[122] A. Dindar, J. B. Kim, C. Fuentes-Hernandez, B. Kippelen, *Appl. Phys. Lett.* **2011**, 99, 172104.

[123] Y. S. Lee, M. T. Winkler, S. C. Siah, R. Brandt, T. Buonassisi, *Appl. Phys. Lett.* **2011**,

98, 192115.

[124] F. M. Li, R. Waddingham, W. I. Milne, A. J. Flewitt, S. Speakman, J. Dutson, S. Wakeham, M. Thwaites, *Thin Solid Films* **2011**, 520, 1278.

[125] V. Figueiredo, E. Elangovan, R. Barros, J. V. Pinto, T. Busani, R. Martins, E. Fortunato, *J. Disp. Technol.* **2012**, 8, 41.

[126] D. W. Nam, I. T. Cho, J. H. Lee, E. S. Cho, J. Sohn, S. H. Song, H. I. Kwon, *J. Vac. Sci. Technol., B* **2012**, 30, 060605.

[127] Z. Q. Yao, S. L. Liu, L. Zhang, B. He, A. Kumar, X. Jiang, W. J. Zhang, G. Shao, *Appl. Phys. Lett.* **2012**, 101, 042114.

[128] V. Figueiredo, J. V. Pinto, J. Deuermeier, R. Barros, E. Alves, R. Martins, E. Fortunato, *J. Disp. Technol.* **2013**, 9, 735.

[129] Q. Huang, L. Wang, X. F. Bi, *J. Phys. D: Appl. Phys.* **2013**, 46, 505101.

[130] C. Y. Jeong, J. Sohn, S. H. Song, I. T. Cho, J. H. Lee, E. S. Cho, H. I. Kwon, *Appl. Phys. Lett.* **2013**, 102, 082103.

[131] S. Joonsung, S. Sang-Hun, N. Dong-Woo, C. In-Tak, C. Eou-Sik, L. Jong-Ho, K. Hyuck-In, *Semicond. Sci. Technol.* **2013**, 28, 015005.

[132] I. J. Park, C. Y. Jeong, U. Myeonghun, S. H. Song, I. T. Cho, J. H. Lee, E. S. Cho, H. I. Kwon, *IEEE Electron Device Lett.* **2013**, 34, 647.

[133] H. A. Al-Jawhari, J. A. Caraveo-Frescas, *Adv. Mater. Res. (Durnten-Zurich, Switz.)* **2014**, 856, 215.

[134] Y. S. Jung, H. W. Choi, K. H. Kim, *Jpn. J. Appl. Phys.* **2014**, 53, 11RA10.

[135] K. C. Sanal, L. S. Vikas, M. K. Jayaraj, *Appl. Surf. Sci.* **2014**, 297, 153.

[136] Z. Chen, X. Xiao, Y. Shao, W. Meng, S. Zhang, L. Yue, L. Xie, P. Zhang, H. Lu, S. Zhang, *12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)* **2014**, p. 1, DOI: 10.1109/ICSICT.2014.7021451.

[137] Y. L. Shen, M. L. Guo, X. H. Xia, G. S. Shao, *Acta Mater.* **2015**, 85, 122.

[138] W.-C. Chen, P.-C. Hsu, C.-W. Chien, K.-M. Chang, C.-J. Hsu, C.-H. Chang, W.-K. Lee, W.-F. Chou, H.-H. Hsieh, C.-C. Wu, *J. Phys. D: Appl. Phys.* **2014**, 47, 365101.

[139] C. Malerba, F. Biccari, C. L. A. Ricardo, M. D'Incau, P. Scardi, A. Mittiga, *Sol. Energy Mater. Sol. Cells* **2011**, 95, 2848.

[140] Y. H. Ko, G. Nagaraju, S. H. Lee, J. S. Yu, *Mater. Lett.* **2014**, 117, 217.

[141] M. Izaki, M. Nagai, K. Maeda, F. B. Mohamad, K. Motomura, J. Sasano, T. Shinagawa, S. Watase, *J. Electrochem. Soc.* **2011**, 158, D578.

[142] W. L. Yu, Y. Z. Lin, X. W. Zhu, Z. G. Hu, M. J. Han, S. S. Cai, L. L. Chen, H. H. Shao,

J. Appl. Phys. **2015**, 117, 045701.

[143] A. Eskandari, P. Sangpour, M. R. Vaezi, *Mater. Chem. Phys.* **2014**, 147, 1204.

[144] H. Nagai, T. Suzuki, H. Hara, C. Mochizuki, I. Takano, T. Honda, M. Sato, *Mater. Chem. Phys.* **2012**, 137, 252.

[145] S. Y. Kim, C. H. Ahn, J. H. Lee, Y. H. Kwon, S. Hwang, J. Y. Lee, H. K. Cho, *ACS Appl. Mat. Interfaces* **2013**, 5, 2417.

[146] W. Yu, M. Han, K. Jiang, Z. Duan, Y. Li, Z. Hu, J. Chu, *J. Raman Spectrosc.* **2013**, 44, 142.

[147] D. Dhakal, T. Waechtler, S. E. Schulz, T. Gessner, H. Lang, R. Mothes, A. Tuchscherer, *J. Vac. Sci. Technol., A* **2014**, 32, 041505.

[148] D. Munoz-Rojas, M. Jordan, C. Yeoh, A. T. Marin, A. Kursumovic, L. A. Dunlop, D. C. Iza, A. Chen, H. Wang, J. L. M. Driscoll, *AIP Adv.* **2012**, 2, 042179.

[149] J. D. Kwon, S. H. Kwon, T. H. Jung, K. S. Nam, K. B. Chung, D. H. Kim, J. S. Park, *Appl. Surf. Sci.* **2013**, 285, 373.

[150] H. Itoh, Y. Suzuki, T. Sekino, J. C. Valmalette, S. Tohno, *J. Ceram. Soc. Jpn.* **2014**, 122, 361.

[151] P. Pattanasattayavong, S. Thomas, G. Adamopoulos, M. A. McLachlan, T. D. Anthopoulos, *Appl. Phys. Lett.* **2013**, 102, 163505.

[152] J. Q. Li, Z. X. Mei, D. Q. Ye, H. L. Liang, Y. P. Liu, X. L. Du, *J. Cryst. Growth* **2012**, 353, 63.

[153] D. Nunes, A. Pimentel, P. Barquinha, P. A. Carvalho, E. Fortunato, R. Martins, *J. Mater. Chem. C* **2014**, 2, 6097.

[154] S. H. Jeong, E. S. Aydil, *J. Vac. Sci. Technol., A* **2010**, 28, 1338.

[155] I. Takumi, S. Shin-ichi, I. Yoshitaka, *Jpn. J. Appl. Phys.* **2014**, 53, 05FF06.

[156] M. Vaseem, A. R. Hong, R. T. Kim, Y. B. Hahn, *J. Mater. Chem. C* **2013**, 1, 2112.

[157] A. Seko, A. Togo, F. Oba, I. Tanaka, *Phys. Rev. Lett.* **2008**, 100, 045702.

[158] J. P. Allen, D. O. Scanlon, S. C. Parker, G. W. Watson, *J. Phys. Chem. C* **2011**, 115, 19916.

[159] A. Tricoli, M. Righettoni, A. Teleki, *Angew. Chem. Int. Ed.* **2010**, 49, 7632.

[160] R. E. Presley, C. L. Munsee, C. H. Park, D. Hong, J. F. Wager, D. A. Keszler, *J. Phys. D: Appl. Phys.* **2004**, 37, 2810.

[161] J. Watson, *Sens. Actuators* **1984**, 5, 29.

[162] H. Li, X. Huang, L. Chen, *Solid State Ionics* **1999**, 123, 189.

[163] J. Safaei-Ghomi, H. Shahbazi-Alavi, E. Heidari-Baghbahadorani, *RSC Adv.* **2014**, 4,

50668.

[164] X. Q. Pan, L. Fu, *J. Appl. Phys.* **2001**, 89, 6048.

[165] X. Q. Pan, L. Fu, *J. Electroceram.* **2001**, 7, 35.

[166] J. F. Wager, B. Yeh, R. L. Hoffman, D. A. Keszler, *Curr. Opin. Solid State Mater. Sci.* **2014**, 18, 53.

[167] J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschlogl, H. N. Alshareef, *ACS Nano* **2013**, 7, 5160.

[168] H. Luo, L. Y. Liang, H. T. Cao, Z. M. Liu, F. Zhuge, *ACS Appl. Mat. Interfaces* **2012**, 4, 5673.

[169] S. Hwang, Y. Y. Kim, J. H. Lee, D. K. Seo, J. Y. Lee, H. K. Cho, *J. Am. Ceram. Soc.* **2012**, 95, 324.

[170] W. Guo, L. Fu, Y. Zhang, K. Zhang, L. Y. Liang, Z. M. Liu, H. T. Cao, X. Q. Pan, *Appl. Phys. Lett.* **2010**, 96, 042113.

[171] L. Y. Liang, Z. M. Liu, H. T. Cao, X. Q. Pan, *ACS Appl. Mat. Interfaces* **2010**, 2, 1060.

[172] L. Y. Liang, Z. M. Liu, H. T. Cao, Y. Y. Shi, X. l. Sun, Z. Yu, A. H. Chen, H. Z. Zhang, Y. Q. Fang, *ACS Appl. Mat. Interfaces* **2010**, 2, 1565.

[173] K. Nomura, T. Kamiya, H. Hosono, *Adv. Mater.* **2011**, 23, 3431.

[174] C. D. Dimitrakopoulos, P. R. L. Malenfant, *Adv. Mater.* **2002**, 14, 99.

[175] L. Y. Liang, H. T. Cao, *ECS Trans.* **2012**, 50, 289.

[176] L. Y. Liang, Z. M. Liu, H. T. Cao, W. Y. Xu, X. L. Sun, H. Luo, K. Cang, *J. Phys. D: Appl. Phys.* **2012**, 45, 085101.

[177] H. Hosono, Y. Ogo, H. Yanagi, T. Kamiya, *Electrochem. Solid-State Lett.* **2011**, 14, H13.

[178] N. F. Quackenbush, J. P. Allen, D. O. Scanlon, S. Sallis, J. A. Hewlett, A. S. Nandur, B. Chen, K. E. Smith, C. Weiland, D. A. Fischer, J. C. Woicik, B. E. White, G. W. Watson, L. F. J. Piper, *Chem. Mater.* **2013**, 25, 3114.

[179] L. Y. Liang, H. T. Cao, X. B. Chen, Z. M. Liu, F. Zhuge, H. Luo, J. Li, Y. C. Lu, W. Lu, *Appl. Phys. Lett.* **2012**, 100, 263502.

[180] H. Hayashi, S. Katayama, R. Huang, K. Kurushima, I. Tanaka, *Phys. Status Solidi RRL* **2015**, 9, 192.

[181] M. Liao, Z. W. Xiao, F. Y. Ran, H. Kumomi, T. Kamiya, H. Hosono, *ECS J. Solid State Sci. Technol.* **2015**, 4, Q26.

[182] T. Toshihiko, S. Yuichi, K. Takafumi, O. Hiroaki, T. Yasuo, *Appl. Phys. Express* **2011**, 4, 071101.

[183] Y. Kim, J. H. Jang, J. S. Kim, S. D. Kim, S. E. Kim, *Mater. Sci. Eng., B* **2012**, 177, 1470.

[184] Y. Kim, J. Um, S. Kim, S. E. Kim, *ECS Solid State Lett.* **2012**, 1, P29.

[185] K. C. Sanal, M. K. Jayaraj, *Mater. Sci. Eng., B* **2013**, 178, 816.

[186] P. C. Hsu, W. C. Chen, Y. T. Tsai, Y. C. Kung, C. H. Chang, C. J. Hsu, C. C. Wu, H. H. Hsieh, *Jpn. J. Appl. Phys.* **2013**, 52, 05DC07.

[187] P. C. Hsu, W. C. Chen, Y. T. Tsai, Y. C. Kung, C. H. Chang, C. C. Wu, H. H. Hsieh, *Thin Solid Films* **2014**, 555, 57.

[188] J. Um, B.-M. Roh, S. Kim, S. E. Kim, *Mater. Sci. Semicond. Process.* **2013**, 16, 1679.

[189] J. Um, S. E. Kim, *ECS Solid State Lett.* **2014**, 3, P94.

[190] P. C. Hsu, C. J. Hsu, C. H. Chang, S. P. Tsai, W. C. Chen, H. H. Hsieh, C. C. Wu, *ACS Appl. Mat. Interfaces* **2014**, 6, 13724.

[191] H. Luo, L. Y. Liang, Q. Liu, H. T. Cao, *ECS J. Solid State Sci. Technol.* **2014**, 3, Q3091.

[192] T. Yang, J. Zhao, X. Li, X. Gao, C. Xue, Y. Wu, R. Tai, *Mater. Lett.* **2014**, 139, 39.

[193] Y.-H. Jiang, I. C. Chiu, P.-K. Kao, J.-C. He, Y.-H. Wu, Y.-J. Yang, C.-C. Hsu, I. C. Cheng, J.-Z. Chen, *Appl. Surf. Sci.* **2015**, 327, 358.

[194] S. Y. Sung, K. M. Jo, S. Y. Kim, J. H. Lee, J. J. Kim, S. K. Park, J. S. Lim, Y. W. Heo, *J. Nanoelectron. Optoelectron.* **2012**, 7, 475.

[195] J. A. Caraveo-Frescas, H. N. Alshareef, *Appl. Phys. Lett.* **2013**, 103, 222103.

[196] H. A. Al-Jawhari, J. A. Caraveo-Frescas, M. N. Hedhili, H. N. Alshareef, *ACS Appl. Mat. Interfaces* **2013**, 5, 9615.

[197] H. A. Al-Jawhari, J. A. Caraveo-Frescas, M. N. Hedhili, *J. Electron. Mater.* **2015**, 44, 117.

[198] P. K. Nayak, J. A. Caraveo-Frescas, Z. Wang, M. N. Hedhili, Q. X. Wang, H. N. Alshareef, *Sci. Rep.* **2014**, 4, 4672.

[199] Z. Wang, H. A. Al-Jawhari, P. K. Nayak, J. A. Caraveo-Frescas, N. Wei, M. N. Hedhili, H. N. Alshareef, *Sci. Rep.* **2015**, 5, 9617.

[200] M. A. Khan, J. A. Caraveo-Frescas, H. N. Alshareef, *Org. Electron.* **2015**, 16, 9.

[201] S. W. Z. Meng, L. T. Zhang, X. Xiao, S. D. Zhang, Ieee, *21st International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)* **2014**, p105.

[202] A. Sharma, M. Varshney, K. D. Verma, Y. Kumar, R. Kumar, *Nucl. Instrum. Methods Phys. Res.* **2013**, 308, 15.

[203] R. Martins, V. Figueiredo, R. Barros, P. Barquinha, G. Goncalves, L. Pereira, I.

Ferreira, E. Fortunato, *Proceedings of SPIE* **2012**, 8263, 826315.

[204] Y.-J. Han, Y.-J. Choi, I.-T. Cho, S. H. Jin, J.-H. Lee, H.-I. Kwon, *IEEE Electron Device Lett.* **2014**, 35, 1260.

[205] M. U, Y. J. Han, S. H. Song, I. T. Cho, J. H. Lee, H. I. Kwon, *J. Semicond. Technol. Sci.* **2014**, 14, 666.

[206] I. C. Chiu, I. C. Cheng, *IEEE Electron Device Lett.* **2014**, 35, 90.

[207] Y.-J. Han, Y.-J. Choi, C.-Y. Jeong, D. Lee, S.-H. Song, H.-I. Kwon, *IEEE Electron Device Lett.* **2015**, 36, 466.

[208] S. Hwang, J. H. Lee, Y. Y. Kim, M. G. Yun, K. H. Lee, J. Y. Lee, H. K. Cho, *J. Nanosci. Nanotechnol.* **2014**, 14, 8908.

[209] I. T. Cho, M. U, S. H. Song, J. H. Lee, H. I. Kwon, *Semicond. Sci. Technol.* **2014**, 29, 045001.

[210] I. C. Chiu, Y. S. Li, M. S. Tu, I. C. Cheng, *IEEE Electron Device Lett.* **2014**, 35, 1263.

[211] Dhananjay, C.-W. Chu, C.-W. Ou, M.-C. Wu, Z.-Y. Ho, K.-C. Ho, S.-W. Lee, *Appl. Phys. Lett.* **2008**, 92, 232103.

[212] C.-W. Ou, Dhananjay, Z. Y. Ho, Y.-C. Chuang, S.-S. Cheng, M.-C. Wu, K.-C. Ho, C.-W. Chu, *Appl. Phys. Lett.* **2008**, 92, 122113.

[213] M. U, H. I. Kwon, I. T. Cho, S. H. Jin, J. H. Lee, *J. Korean Phys. Soc.* **2014**, 65, 286.

[214] H. N. Lee, H. J. Kim, C. K. Kim, *Jpn. J. Appl. Phys.* **2010**, 49, 020202.

[215] T. Toyama, Y. Seo, T. Konishi, H. Okamoto, R. Morimoto, Y. Nishikawa, Y. Tsutsumi, *Thin Solid Films* **2014**, 555, 148.

[216] H. N. Lee, B. J. Song, J. C. Park, *J. Disp. Technol.* **2014**, 10, 288.

[217] X. X. Li, L. Y. Liang, H. T. Cao, R. F. Qin, H. L. Zhang, J. H. Gao, Z. G. Fei, *Appl. Phys. Lett.* **2015**, 106, 132102.

[218] J. H. Han, Y. J. Chung, B. K. Park, S. K. Kim, H.-S. Kim, C. G. Kim, T.-M. Chung, *Chem. Mater.* **2014**, 26, 6088.

[219] I. Barbul, A. L. Johnson, G. Kociok-Kohn, K. C. Molloy, C. Silvestru, A. L. Sudlow, *ChemPlusChem* **2013**, 78, 866.

[220] T. Wildsmith, M. S. Hill, A. L. Johnson, A. J. Kingsley, K. C. Molloy, *Chem. Commun.* **2013**, 49, 8773.

[221] H. S. Jarrett, A. W. Sleight, H. H. Kung, J. L. Gillson, *J. Appl. Phys.* **1980**, 51, 3916.

[222] H. Mizoguchi, M. Hirano, S. Fujitsu, T. Takeuchi, K. Ueda, H. Hosono, *Appl. Phys. Lett.* **2002**, 80, 1207.

[223] H. Hosono, *Jpn. J. Appl. Phys.* **2013**, 52, 090001.

[224] D. J. Singh, R. C. Rai, J. L. Musfeldt, S. Auluck, N. Singh, P. Khalifah, S. McClure, D. G. Mandrus, *Chem. Mater.* **2006**, 18, 2696.

[225] A. R. Nagaraja, N. H. Perry, T. O. Mason, Y. Tang, M. Grayson, T. R. Paudel, S. Lany, A. Zunger, *J. Am. Ceram. Soc.* **2012**, 95, 269.

[226] S. Narushima, H. Mizoguchi, K. Shimizu, K. Ueda, H. Ohta, M. Hirano, T. Kamiya, H. Hosono, *Adv. Mater.* **2003**, 15, 1409.

[227] H. Ohta, H. Mizoguchi, M. Hirano, S. Narushima, T. Kamiya, H. Hosono, *Appl. Phys. Lett.* **2003**, 82, 823.

[228] T. Kamiya, S. Narushima, H. Mizoguchi, K. Shimizu, K. Ueda, H. Ohta, M. Hirano, H. Hosono, *Adv. Funct. Mater.* **2005**, 15, 968.

[229] H. J. Kim, I. C. Song, J. H. Sim, H. Kim, D. Kim, Y. E. Ihm, W. K. Choo, *J. Appl. Phys.* **2004**, 95, 7387.

[230] M. Dekkers, G. Rijnders, D. H. A. Blank, *Appl. Phys. Lett.* **2007**, 90, 021903.

[231] S. Kim, J. A. Cianfrone, P. Sadik, K.-W. Kim, M. Ivill, D. P. Norton, *J. Appl. Phys.* **2010**, 107, 103538.

[232] F. Schein, H. von Wenckstern, H. Frenzel, M. Grundmann, *IEEE Electron Device Lett.* **2012**, 33, 676.

[233] F. J. Klupfel, F. L. Schein, M. Lorenz, H. Frenzel, H. von Wenckstern, M. Grundmann, *IEEE Trans. Electron Devices* **2013**, 60, 1828.

[234] F.-L. Schein, M. Winter, T. Böntgen, H. von Wenckstern, M. Grundmann, *Appl. Phys. Lett.* **2014**, 104, 022104.

[235] P. Schlupp, F.-L. Schein, H. von Wenckstern, M. Grundmann, *Adv. Electronic Mater.* **2015**, 1, 1400023.

[236] H. von Wenckstern, D. Splith, S. Lanzinger, F. Schmidt, S. Müller, P. Schlupp, R. Karsthof, M. Grundmann, *Adv. Electronic Mater.* **2015**, 1, 1400026.

[237] S. Samanta, S. M. Saini, *J. Electron. Mater.* **2014**, 43, 3659.

[238] N. Mansourian-Hadavi, S. Wansom, N. H. Perry, A. R. Nagaraja, T. O. Mason, L. H. Ye, A. J. Freeman, *Phys. Rev. B* **2010**, 81, 075112.

[239] S. Nirpendra, S. Udo, *Europhys. Lett.* **2013**, 104, 37002.

[240] D. Munoz Ramo, P. D. Bristowe, *J. Chem. Phys.* **2014**, 141, 084704.

[241] D. O. Scanlon, G. W. Watson, *Phys. Chem. Chem. Phys.* **2011**, 13, 9667.

[242] S. Samanta, *Opt. Mater.* **2015**, 45, 141.

[243] M. N. Amini, H. Dixit, R. Saniz, D. Lamoen, B. Partoens, *Phys. Chem. Chem. Phys.* **2014**, 16, 2588.

[244] O. Volnianska, P. Boguslawski, *J. Appl. Phys.* **2013**, 114, 033711.

[245] O. Volnianska, P. Boguslawski, *J. Phys. D: Appl. Phys.* **2014**, 47, 465101.

[246] J. D. Perkins, T. R. Paudel, A. Zakutayev, P. F. Ndione, P. A. Parilla, D. L. Young, S. Lany, D. S. Ginley, A. Zunger, N. H. Perry, Y. Tang, M. Grayson, T. O. Mason, J. S. Bettinger, Y. Shi, M. F. Toney, *Phys. Rev. B* **2011**, 84, 205207.

[247] H. Sato, T. Minami, S. Takata, T. Yamada, *Thin Solid Films* **1993**, 236, 27.

[248] M. D. Irwin, B. Buchholz, A. W. Hains, R. P. H. Chang, T. J. Marks, *PNAS* **2008**, 105, 2783.

[249] J. L. McNatt, *Phys. Rev. Lett.* **1969**, 23, 915.

[250] J. Hugel, C. Carabatos, *Journal of Physics C-Solid State Physics* **1983**, 16, 6713.

[251] M. T. Greiner, Z.-H. Lu, *Npg Asia Materials* **2013**, 5, e55.

[252] N. F. Mott, *Philos. Mag.* **1961**, 6, 287.

[253] J. Hubbard, *Proc. R. Soc. Lond. Ser. A: Math. Phys. Sci.* **1963**, 276, 238.

[254] J. Hubbard, *Proc. R. Soc. Lond. Ser. A: Math. Phys. Sci.* **1964**, 277, 237.

[255] J. Hubbard, *Proc. R. Soc. Lond. Ser. A: Math. Phys. Sci.* **1964**, 281, 401.

[256] J. Zaanen, G. A. Sawatzky, J. W. Allen, *Phys. Rev. Lett.* **1985**, 55, 418.

[257] S. Lany, J. Osorio-Guillén, A. Zunger, *Phys. Rev. B* **2007**, 75, 241203.

[258] T. Dutta, P. Gupta, A. Gupta, J. Narayan, *J. Appl. Phys.* **2010**, 108, 083715.

[259] N. Alidoust, E. A. Carter, *Phys. Chem. Chem. Phys.* **2015**, 17, 18098.

[260] M. Z. Sialvi, R. J. Mortimer, G. D. Wilcox, A. M. Teridi, T. S. Varley, K. G. U. Wijayantha, C. A. Kirk, *ACS Appl. Mat. Interfaces* **2013**, 5, 5675.

[261] J. Nagai, G. D. McMeeking, Y. Saitoh, *Sol. Energy Mater. Sol. Cells* **1999**, 56, 309.

[262] S. C. Chen, C. K. We, T. Y. Kuo, W. C. Peng, H. C. Lin, *Thin Solid Films* **2014**, 572, 51.

[263] J. H. Park, J. Seo, S. Park, S. S. Shin, Y. C. Kim, N. J. Jeon, H.-W. Shin, T. K. Ahn, J. H. Noh, S. C. Yoon, C. S. Hwang, S. I. Seok, *Adv. Mater.* **2015**, 27, 4013.

[264] A. Agrawal, H. R. Habibi, R. K. Agrawal, J. P. Cronin, D. M. Roberts, R. Caronpopowich, C. M. Lampert, *Thin Solid Films* **1992**, 221, 239.

[265] S. Pereira, A. Goncalves, N. Correia, J. Pinto, L. Pereira, R. Martins, E. Fortunato, *Sol. Energy Mater. Sol. Cells* **2014**, 120, 109.

[266] Y. R. Park, K. J. Kim, *J. Cryst. Growth* **2003**, 258, 380.

[267] C.-C. Wu, C.-F. Yang, *ACS Appl. Mat. Interfaces* **2013**, 5, 4996.

[268] E. Thimsen, A. B. F. Martinson, J. W. Elam, M. J. Pellin, *J. Phys. Chem. C* **2012**, 116, 16830.

[269] H. Shimotani, H. Suzuki, K. Ueno, M. Kawasaki, Y. Iwasa, *Appl. Phys. Lett.* **2008**, 92, 242107.

[270] S. Takami, R. Hayakawa, Y. Wakayama, T. Chikyow, *Nanotechnology* **2010**, 21, 134009.

[271] J. Jiang, X. Wang, Q. Zhang, J. Li, X. X. Zhang, *Phys. Chem. Chem. Phys.* **2013**, 15, 6875.

[272] S. Liu, R. Liu, Y. Chen, S. Ho, J. H. Kim, F. So, *Chem. Mater.* **2014**, 26, 4528.

[273] K. Matsubara, S. Huang, M. Iwamoto, W. Pan, *Nanoscale* **2014**, 6, 688.

[274] Y. Ohya, M. Ueda, Y. Takahashi, *Jpn. J. Appl. Phys.* **1996**, 35, 4738.

[275] H. Ohta, M. Hirano, K. Nakahara, H. Maruta, T. Tanabe, M. Kamiya, T. Kamiya, H. Hosono, *Appl. Phys. Lett.* **2003**, 83, 1029.

[276] N. Müenzenrieder, C. Zysset, L. Petti, T. Kinkeldei, G. A. Salvatore, G. Troester, *Solid-State Electron.* **2013**, 87, 17.

[277] M. Tyagi, M. Tomar, V. Gupta, *Mater. Res. Bull.* **2015**, 66, 123.

[278] S. Seo, M. J. Lee, D. H. Seo, E. J. Jeoung, D. S. Suh, Y. S. Joung, I. K. Yoo, I. R. Hwang, S. H. Kim, I. S. Byun, J. S. Kim, J. S. Choi, B. H. Park, *Appl. Phys. Lett.* **2004**, 85, 5655.

[279] L. Myoung-Jae, S. I. Kim, C. B. Lee, Y. Huaxiang, A. Seung-Eon, B. S. Kang, K. H. Kim, J. C. Park, C. J. Kim, S. Ihun, S. W. Kim, G. Stefanovich, J. H. Lee, S. J. Chung, Y. H. Kim, P. Youngsoo, *Adv. Funct. Mater.* **2009**, 19, 1587.

[280] H. D. Lee, B. Magyari-Kope, Y. Nishi, *Phys. Rev. B* **2010**, 81, 193202.

[281] I. M. Chan, T. Y. Hsu, F. C. Hong, *Appl. Phys. Lett.* **2002**, 81, 1899.

[282] F. Jiang, W. C. H. Choy, X. Li, D. Zhang, J. Cheng, *Adv. Mater.* **2015**, 27, 2930.

[283] H. Ohta, M. Kamiya, T. Kamaiya, M. Hirano, H. Hosono, *Thin Solid Films* **2003**, 445, 317.

[284] S. Bai , M. Cao , Y. Jin , X. Dai , X. Liang , Z. Ye , M. Li , J. Cheng, X. Xiao , Z. Wu , Z. Xia , E. Sun , E. Wang , Y. Mo , F. Gao , F. Zhang, *Adv. Energy Mater.* **2014**, 4, 1301460.

[285] M. D. Irwin, J. D. Servaites, D. B. Buchholz, B. J. Leever, J. Liu, J. D. Emery, M. Zhang, J.-H. Song, M. F. Durstock, A. J. Freeman, M. J. Bedzyk, M. C. Hersam, R. P. H. Chang, M. A. Ratner, T. J. Marks, *Chem. Mater.* **2011**, 23, 2218.

[286] D. S. Ginley, H. Hosono, D. C. Paine, *Handbook of Transparent Conductors*, Springer, New York **2010**.

[287] A. Facchetti, T. J. Marks, *Transparent electronics: from synthesis to applications*, John Wiley & Sons, New York **2010**.

[288] J. A. Caraveo-Frescas, *PhD Thesis, Transparent Oxide Semiconductors for Emerging Electronics*, King Abdullah University of Science and Technology, Thuwal, Saudi Arabia, **2013**.

[289] H. Frenzel, A. Lajn, M. Grundmann, *Physica Status Solidi-Rapid Research Letters* **2013**, 7, 605.

[290] Y. Kim, Y. Kim, H. Lee, *J. Disp. Technol.* **2014**, 10, 995.

[291] J. H. Lee, D. N. Liu, S. T. Wu, *Introduction to Flat Panel Displays*, John Wiley & Sons, New York **2008**.

[292] A. C. Tickle, *Thin-Film Transistors -A New Approach to Microelectronics*, Wiley, New York **1969**.

[293] P. Barquinha, *PhD thesis, Transparent Oxide Thin-Film Transistors: production, characterization and integration*, Universidade Nova de Lisboa, Lisbon, Portugal **2010**.

[294] D. Hong, G. Yerubandi, H. Q. Chiang, M. C. Spiegelberg, J. F. Wager, *Crit. Rev. Solid State Mater. Sci.* **2008**, 33, 101.

[295] R. F. Pierret, *Semiconductor Fundamentals*, Addison-Wesley, MA, USA, **1996**.

[296] P. K. Weimer, *Field-Effect Transistors: Physics, Techhnology, and Applications*, Prentice Hall , Upper Saddle River, NJ, USA, **1966**.

[297] T. Ytterdal, Y. Cheng, T. A. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design*, John Wiley & Sons, New York **2003**.

[298] N. L. Dehuff, E. S. Kettenring, D. Hong, H. Q. Chiang, J. F. Wager, R. L. Hoffman, C.-H. Park, D. A. Keszler, *J. Appl. Phys.* **2005**, 97, 064505.

[299] W. J. Park, H. S. Shin, B. D. Ahn, G. H. Kim, S. M. Lee, K. H. Kim, H. J. Kim, *Appl. Phys. Lett.* **2008**, 93, 083508.

[300] R. L. Hoffman, *J. Appl. Phys.* **2004**, 95, 5813.

[301] F. Zhou, B. S. Yeh, K. A. Archila, J. F. Wager, *ECS J. Solid State Sci. Technol.* **2014**, 3, Q3027.

[302] S. M. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons, New York **1981**.

[303] C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Prentice Hall, **2009**.

[304] L. Liao, B. Yan, Y. F. Hao, G. Z. Xing, J. P. Liu, B. C. Zhao, Z. X. Shen, T. Wu, L. Wang, J. T. L. Thong, C. M. Li, W. Huang, T. Yu, *Appl. Phys. Lett.* **2009**, 94, 113106.

[305] T. Yu, X. Zhao, Z. X. Shen, Y. H. Wu, W. H. Su, *J. Cryst. Growth* **2004**, 268, 590.

[306] E. Fortunato, V. Figueiredo, P. Barquinha, E. Elamurugu, R. Barros, G. Goncalves, S. H. K. Park, C. S. Hwang, R. Martins, *Appl. Phys. Lett.* **2010**, 96, 239902.

[307] X. Zou, G. J. Fang, L. Y. Yuan, N. S. Liu, H. Long, X. Z. Zhao, *Thin Solid Films* **2010**,

518, 4446.

[308] X. Zou, G. J. Fang, L. Y. Yuan, N. S. Liu, H. Long, Ieee, *IEEE Int. Conf. Electron Devices Solid-State Circuits* **2009**, p. 217.

[309] C. S. Kang, H.-J. Cho, K. Onishi, R. Nieh, R. Choi, S. Gopalan, S. Krishnan, J. H. Han, J. C. Lee, *Appl. Phys. Lett.* **2002**, 81, 2593.

[310] J. W. Han, M. Meyyappan, *Appl. Phys. Lett.* **2011**, 98, 192102.

[311] W. B. Jackson, *Phys. Rev. B* **1988**, 38, 3595.

[312] A. Yelon, B. Movaghar, H. M. Branz, *Phys. Rev. B* **1992**, 46, 12244.

[313] H.-H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, C.-C. Wu, *Appl. Phys. Lett.* **2008**, 92, 133503.

[314] E. Fortunato, N. Correia, P. Barquinha, L. Pereira, G. Goncalves, R. Martins, *IEEE Electron Device Lett.* **2008**, 29, 988.

[315] K. Okamura, B. Nasr, R. A. Brand, H. Hahn, *J. Mater. Chem.* **2012**, 22, 4607.

[316] D. B. Granato, J. A. Caraveo-Frescas, H. N. Alshareef, U. Schwingenschlögl, *Appl. Phys. Lett.* **2013**, 102, 212105.

[317] D. B. Granato, J. A. Caraveo-Frescas, H. N. Alshareef, U. Schwingenschlögl, *Appl. Phys. Lett.* **2013**, 102, 212105.

[318] J. Y. W. Seto, *J. Appl. Phys.* **1975**, 46, 5247.

[319] K. Nomura, T. Kamiya, H. Hosono, *Appl. Phys. Lett.* **2011**, 99, 053505.

[320] K. Hoshino, D. Hong, H. Q. Chiang, J. F. Wager, *IEEE Trans. Electron Devices* **2009**, 56, 1365.

[321] P. K. Nayak, Z. Wang, D. H. Anjum, M. N. Hedhili, H. N. Alshareef, *Appl. Phys. Lett.* **2015**, 106, 103505.

[322] A. Olziersky, P. Barquinha, A. Vilà, L. Pereira, G. Gonçalves, E. Fortunato, R. Martins, J. R. Morante, *J. Appl. Phys.* **2010**, 108, 064505.

[323] W. B. Jackson, J. M. Marshall, M. D. Moyer, *Phys. Rev. B* **1989**, 39, 1164.

[324] A. V. Gelatos, J. Kanicki, *Appl. Phys. Lett.* **1990**, 57, 1197.

[325] F. R. Libsch, J. Kanicki, *Appl. Phys. Lett.* **1993**, 62, 1286.

[326] S. Sambandan, D. Striakhilev, A. Nathan, *J. Disp. Technol.* **2006**, 2, 52.

[327] J.-M. Lee, I.-T. Cho, J.-H. Lee, H.-I. Kwon, *Appl. Phys. Lett.* **2008**, 93, 093504.

[328] C. In-Tak, L. Jeong-Min, L. Jong-Ho, K. Hyuck-In, *Semicond. Sci. Technol.* **2009**, 24, 015013.

[329] T.-C. Chen, T.-C. Chang, C.-T. Tsai, T.-Y. Hsieh, S.-C. Chen, C.-S. Lin, M.-C. Hung, C.-H. Tu, J.-J. Chang, P.-L. Chen, *Appl. Phys. Lett.* **2010**, 97, 112104.

[330] Y.-C. Chen, T.-C. Chang, H.-W. Li, S.-C. Chen, J. Lu, W.-F. Chung, Y.-H. Tai, T.-Y. Tseng, *Appl. Phys. Lett.* **2010**, 96, 262104.

[331] I.-J. Park, C.-Y. Jeong, M. U., S.-H. Song, I.-T. Cho, J.-H. Lee, E.-S. Cho, H.-I. Kwon, *IEEE Electron Device Lett.* **2013**, 34, 647.

[332] J. Lee, J. Young Jung, D. Hwan Kim, J.-Y. Kim, B.-L. Lee, J.-I. Park, J. Won Chung, J. Seok Park, B. Koo, Y. Wan Jin, S. Lee, *Appl. Phys. Lett.* **2012**, 100, 083302.

[333] R. Martins, I. Ferreira, E. Fortunato, *Phys. Status Solidi RRL* **2011**, 5, 332.

[334] Y. Nakamura, Y. Yoshida, Y. Honaga, S. Fujitsu, *J. Eur. Ceram. Soc.* **2005**, 25, 2167.

[335] S. Sheng, G. Fang, C. Li, S. Xu, X. Zhao, *Phys. Status Solidi A* **2006**, 203, 1891.

[336] H. Hiramatsu, K. Ueda, H. Ohta, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2005**, 87, 211107.

[337] K. Tonooka, H. Bando, Y. Aiura, *Thin Solid Films* **2003**, 445, 327.

[338] S. Jeong, E. S. Aydil, *J. Cryst. Growth* **2009**, 311, 4188.

[339] K. Kwak, K. Cho, S. Kim, *J. Nanosci. Nanotechnol.* **2013**, 13, 3433.

[340] J.-Y. Feng, C.-F. Hu, X.-P. Qu, *12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)* **2014**, p. 1, DOI: 10.1109/ICSICT.2014.702.1183.

[341] Y. H. Ok, K. R. Lee, B. O. Jung, Y. H. Kwon, H. K. Cho, *Thin Solid Films* **2014**, 570, 282.

[342] A. Polman, H. A. Atwater, *Nat. Mater.* **2012**, 11, 174.

[343] L. Zhu, G. Shao, J. K. Luo, *Semicond. Sci. Technol.* **2011**, 26, 085026.

[344] L. Zhu, G. Shao, J. K. Luo, *Solid State Sci.* **2012**, 14, 857.

[345] L. Zhu, J. K. Luo, G. Shao, W. I. Milne, *Sol. Energy Mater. Sol. Cells* **2013**, 111, 141.

[346] R. Sathyamoorthy, K. M. Abhirami, B. Gokul, S. Gautam, K. Chae, K. Asokan, *Electron. Mater. Lett.* **2014**, 10, 743.

[347] Z. Wang, P. K. Nayak, A. Albar, N. Wei, U. Schwingenschlögl, H. N. Alshareef, *Adv. Mater. Interfaces* **2015**, 1500374.

[348] J. F. Gibbons, W. E. Beadle, *Solid-State Electron.* **1964**, 7, 785.

[349] J. W. Park, D. Y. Kim, J. K. Lee, *J. Vac. Sci. Technol., A* **2005**, 23, 1309.

[350] I. Austin, in *Semiconductor Effects in Amorphous Solids*, North Holland, Amsterdam 1970, 477.

[351] Y. Doo Hyun, K. Si Joon, J. Joohye, L. Hyun Soo, K. Hyun Jae, *J. Mater. Chem.* **2012**, 22, 17568.

[352] M. K. Hota, J. A. Caraveo-Frescas, M. A. McLachlan, H. N. Alshareef, *Appl. Phys. Lett.* **2014**, 104, 152104.

[353] M. K. Hota, M. N. Hedhili, Q. Wang, V. A. Melnikov, O. F. Mohammed, H. N. Alshareef, *Adv. Electronic Mater.* **2015**, 1, 1400035.

[354] R. Waser, M. Aono, *Nat. Mater.* **2007**, 6, 833.

[355] M.-J. Lee, S. I. Kim, C. B. Lee, H. Yin, S.-E. Ahn, B. S. Kang, K. H. Kim, J. C. Park, C. J. Kim, I. Song, S. W. Kim, G. Stefanovich, J. H. Lee, S. J. Chung, Y. H. Kim, Y. Park, *Adv. Funct. Mater.* **2009**, 19, 1587.

[356] D.-H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim, C. S. Hwang, *Nat. Nanotechnol.* **2010**, 5, 148.

[357] C.-H. Cheng, F.-S. Yeh, A. Chin, *Adv. Mater.* **2011**, 23, 902.

[358] B. Cho, S. Song, Y. Ji, T.-W. Kim, T. Lee, *Adv. Funct. Mater.* **2011**, 21, 2806.

[359] J. G. Simmons, Verderbe.Rr, *Proceedings of the Royal Society of London Series a-Mathematical and Physical Sciences* **1967**, 301, 77.

[360] T. W. Hickmott, *Journal of Vacuum Science & Technology* **1969**, 6, 828.

[361] Y. J. Park, I.-S. Bae, S. J. Kang, J. Chang, C. Park, *IEEE Trans. Dielectr. Electr. Insul.* **2010**, 17, 1135.

[362] R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, D. M. De Leeuw, *Nat. Mater.* **2005**, 4, 243.

[363] J. A. Caraveo-Frescas, M. A. Khan, H. N. Alshareef, *Sci. Rep.* **2014**, 4, 5243.

[364] C. T. Black, C. Farrell, T. J. Licata, *Appl. Phys. Lett.* **1997**, 71, 2041.

[365] R. C. G. Naber, K. Asadi, P. W. M. Blom, D. M. de Leeuw, B. de Boer, *Adv. Mater.* **2010**, 22, 933.

[366] K. H. Lee, G. Lee, K. Lee, M. S. Oh, S. Im, S.-M. Yoon, *Adv. Mater.* **2009**, 21, 4287.

[367] S. J. Kang, I. Bae, Y. J. Park, T. H. Park, J. Sung, S. C. Yoon, K. H. Kim, D. H. Choi, C. Park, *Adv. Funct. Mater.* **2009**, 19, 1609.

[368] R. H. Kim, H. J. Kim, I. Bae, S. K. Hwang, D. B. Velusamy, S. M. Cho, K. Takaishi, T. Muto, D. Hashizume, M. Uchiyama, P. Andre, F. Mathevet, B. Heinrich, T. Aoyama, D.-E. Kim, H. Lee, J.-C. Ribierre, C. Park, *Nat. Commun.* **2014**, 5, 3583.

[369] Y. Wang, Q. Niu, C. Hu, W. Wang, M. He, Y. Zhang, S. Li, L. Zhao, X. Wang, J. Xu, Q. Zhu, S. Chen, *Opt. Lett.* **2011**, 36, 1521.

[370] H.-Y. Chen, J. Hou, S. Zhang, Y. Liang, G. Yang, Y. Yang, L. Yu, Y. Wu, G. Li, *Nat. Photonics* **2009**, 3, 649.

[371] C. G. Granqvist, E. Avendano, A. Azens, *Thin Solid Films* **2003**, 442, 201.

[372] C. G. Granqvist, *J. Eur. Ceram. Soc.* **2005**, 25, 2907.

[373] C. G. Granqvist, *Sol. Energy Mater. Sol. Cells* **2008**, 92, 203.

[374] G. A. Niklasson, C. G. Granqvist, *J. Mater. Chem.* **2007**, 17, 127.

[375] R. J. Mortimer, *Annual Review of Materials Research,* **2011**, 41, 241.

[376] C. G. Granqvist, *Adv. Mater.* **2003**, 15, 1789.

[377] E. Avendano, L. Berggren, G. A. Niklasson, C. G. Granqvist, A. Azens, *Thin Solid Films* **2006**, 496, 30.

[378] A. Urbano, F. F. Ferreira, S. C. deCastro, R. Landers, M. C. A. Fantini, A. Gorenstein, *Electrochim. Acta* **2001**, 46, 2269.

[379] N. Penin, A. Rougier, L. Laffont, P. Poizot, J. M. Tarascon, *Sol. Energy Mater. Sol. Cells* **2006**, 90, 422.

[380] J. Zheng, W. Minghong, Q. Zheng, X. Hong, *Nanotechnology* **2003**, 14, 458.

[381] X. H. Xia, J. P. Tu, J. Zhang, X. L. Wang, W. K. Zhang, H. Huang, *Sol. Energy Mater. Sol. Cells* **2008**, 92, 628.

[382] R. C. Tenent, D. T. Gillaspie, A. Miedaner, P. A. Parilla, C. J. Curtis, A. C. Dillon, *J. Electrochem. Soc.* **2010**, 157, H318.

[383] A. Tricoli, M. Righettoni, A. Teleki, *Angew. Chem. Int. Ed.* **2010**, 49, 7632.

[384] H.-J. Kim, J.-H. Lee, *Sens. Actuators, B* **2014**, 192, 607.

[385] N. Barsan, C. Simion, T. Heine, S. Pokhrel, U. Weimar, *J. Electroceram.* **2010**, 25, 11.

[386] M. Huebner, C. E. Simion, A. Tomescu-Stanoiu, S. Pokhrel, N. Barsan, U. Weimar, *Sens. Actuators, B* **2011**, 153, 347.

[387] H.-J. Kim, K.-I. Choi, K.-M. Kim, C. W. Na, J.-H. Lee, *Sens. Actuators, B* **2012**, 171, 1029.

[388] K.-M. Kim, H.-M. Jeong, H.-R. Kim, K.-I. Choi, H.-J. Kim, J.-H. Lee, *Sensors* **2012**, 12, 8013.

[389] J.-W. Yoon, H.-J. Kim, I.-D. Kim, J.-H. Lee, *Nanotechnology* **2013**, 24, 444005.

[390] N. G. Cho, H.-S. Woo, J.-H. Lee, I.-D. Kim, *Chem. Commun.* **2011**, 47, 11300.

[391] K.-I. Choi, H.-R. Kim, K.-M. Kim, D. Li, G. Cao, J.-H. Lee, *Sens. Actuators, B* **2010**, 146, 183.

[392] Y. Ushio, M. Miyayama, H. Yanagida, *Sens. Actuators, B* **1993**, 12, 135.

[393] Y. Ushio, M. Miyayama, H. Yanagida, *Sens. Actuators, B* **1994**, 17, 221.

[394] W. J. Park, K. J. Choi, M. H. Kim, B. H. Koo, J.-L. Lee, J. M. Baik, *ACS Appl. Mat. Interfaces* **2013**, 5, 6802.

[395] K. Hikita, M. Miyayama, H. Yanagida, *J. Am. Ceram. Soc.* **1994**, 77, 1961.

[396] K. Hikita, M. Miyayama, H. Yanagida, *J. Am. Ceram. Soc.* **1995**, 78, 865.

[397] Y. Caglar, D. D. Oral, M. Caglar, S. Ilican, M. A. Thomas, K. Wu, Z. Sun, J. Cui, *Thin*

Solid Films **2012**, 520, 6642.

[398] J. Tamaki, T. Maekawa, N. Miura, N. Yamazoe, *Sensors and Actuators B-Chemical* **1992**, 9, 197.

[399] H.-R. Kim, K.-I. Choi, K.-M. Kim, I.-D. Kim, G. Cao, J.-H. Lee, *Chem. Commun.* **2010**, 46, 5061.

[400] H.-R. Kim, A. Haensch, I.-D. Kim, N. Barsan, U. Weimar, J.-H. Lee, *Adv. Funct. Mater.* **2011**, 21, 4456.

[401] K.-I. Choi, M. Huebner, A. Haensch, H.-J. Kim, U. Weimar, N. Barsan, J.-H. Lee, *Sens. Actuators, B* **2013**, 183, 401.

Figures and Captions

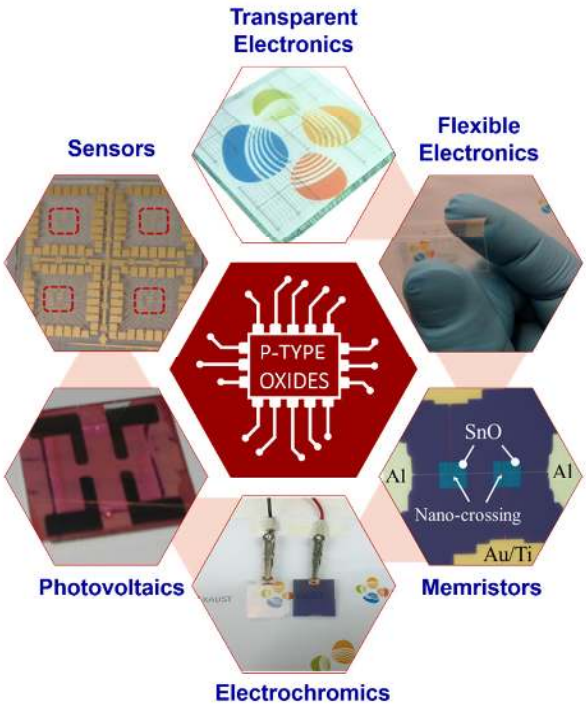

Figure 1. A variety of functional devices fabricated in our laboratory using p-type oxide active layers, which demonstrates their potential in various applications.

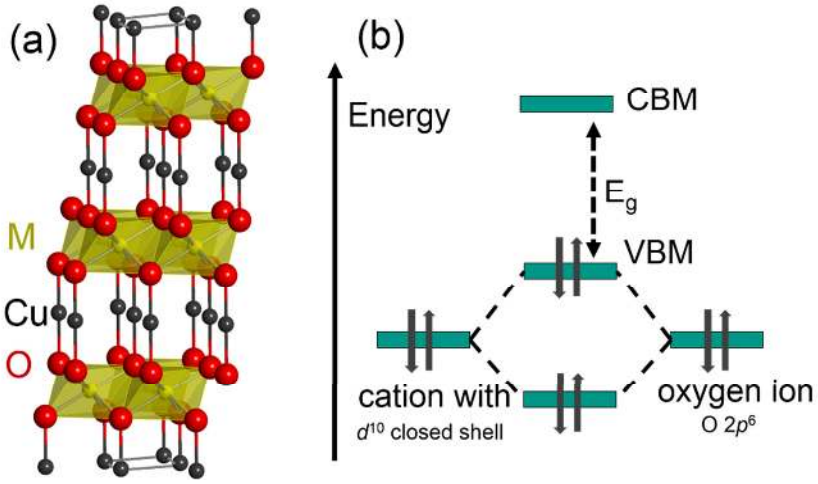

Figure 2. (a) Crystal structure of $CuMO_2$ delafossites. (b) Schematic illustration of the valence band maximum (VBM) hybridization in the chemical design concept.

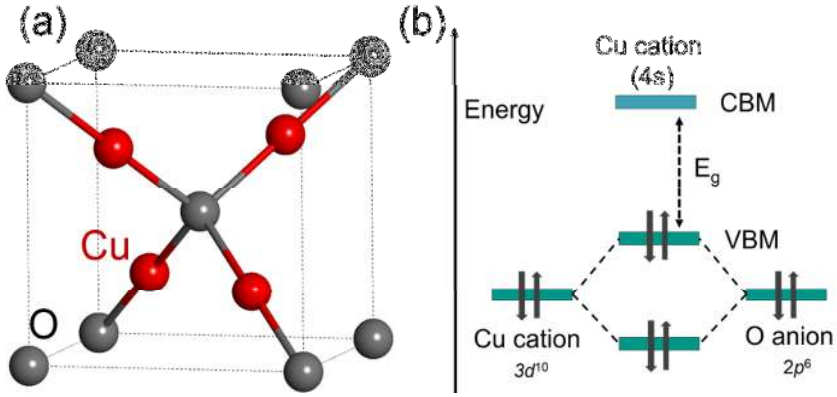

Figure 3. (a) Crystal structure of Cu_2O. (b) Schematic illustration of the valence band maximum (VBM) hybridization in Cu_2O.

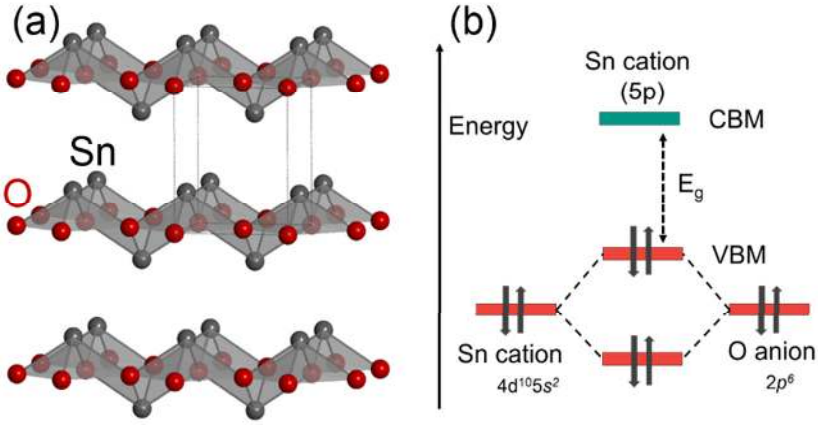

Figure 4. (a) Crystal structure of SnO. (b) Schematic illustration of the valence band maximum (VBM) hybridization in SnO.

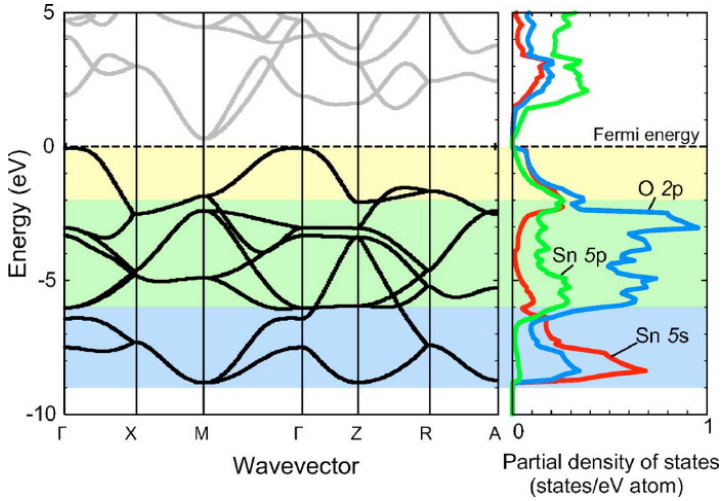

Figure 5. Band structure (left) and PDOS (right) of the unit cell of the SnO perfect crystal. The energy of the highest occupied band at the Γ point is set to 0 eV. The highest occupied state is located between the Γ and M points. The lowest unoccupied state is given at the M point. The background of the band structure and PDOS figures denotes three characteristic energy regions in the valence band. Reproduced with permission.[18] Copyright 2006, American Physical Society.

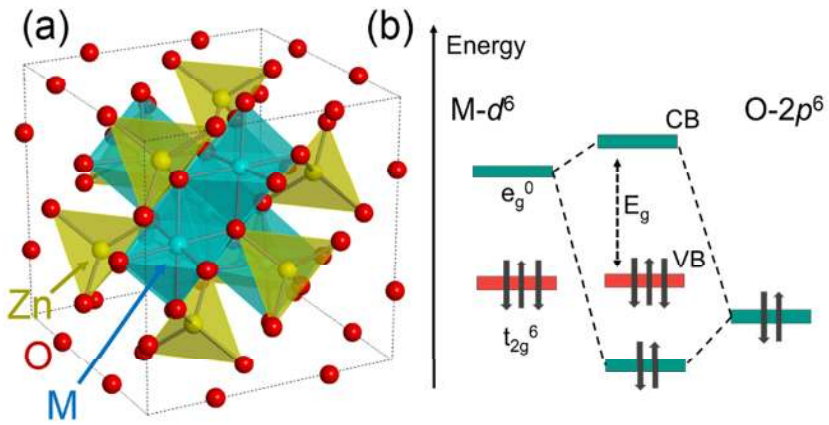

Figure 6. (a) Crystal structure of ZnM_2O_4 spinel. (b) Schematic of M d orbital splitting and the hybridization near the valence band maximum (VBM).

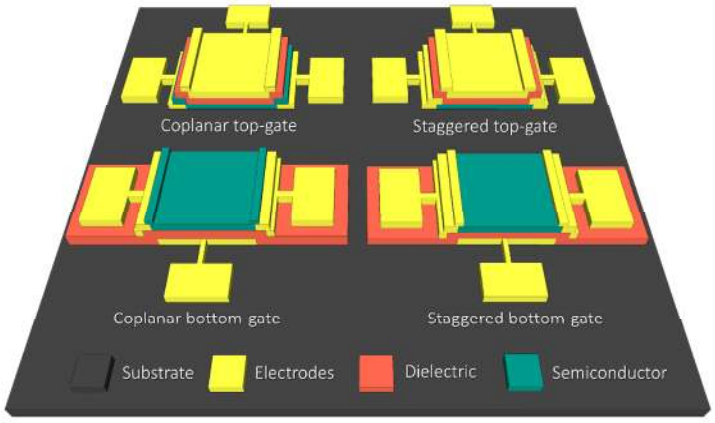

Figure 7. Typical structures of thin-film transistors.

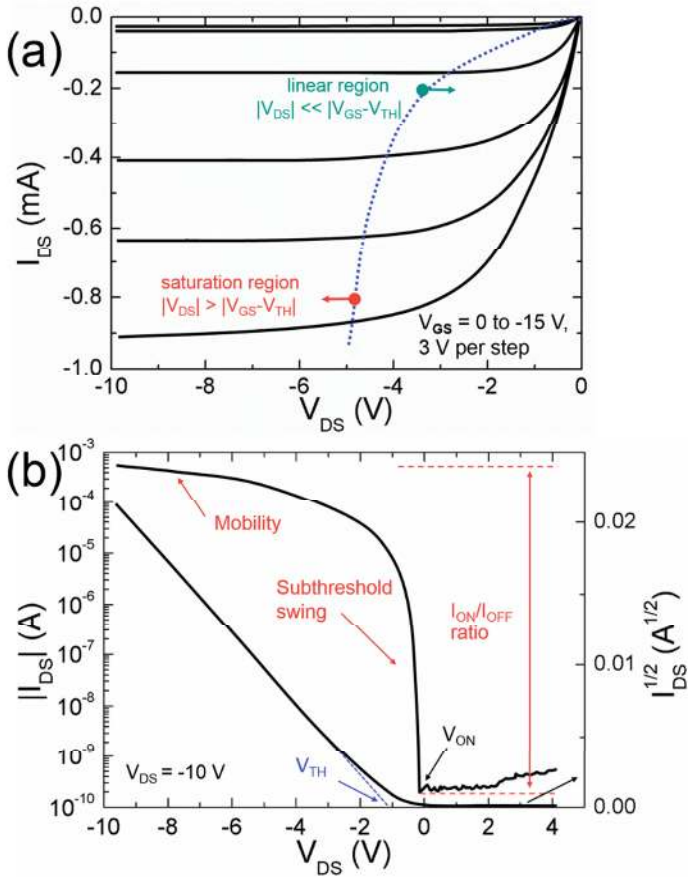

Figure 8. Typical (a) output and (b) transfer characteristics of a p-type thin-film transistor (TFT).

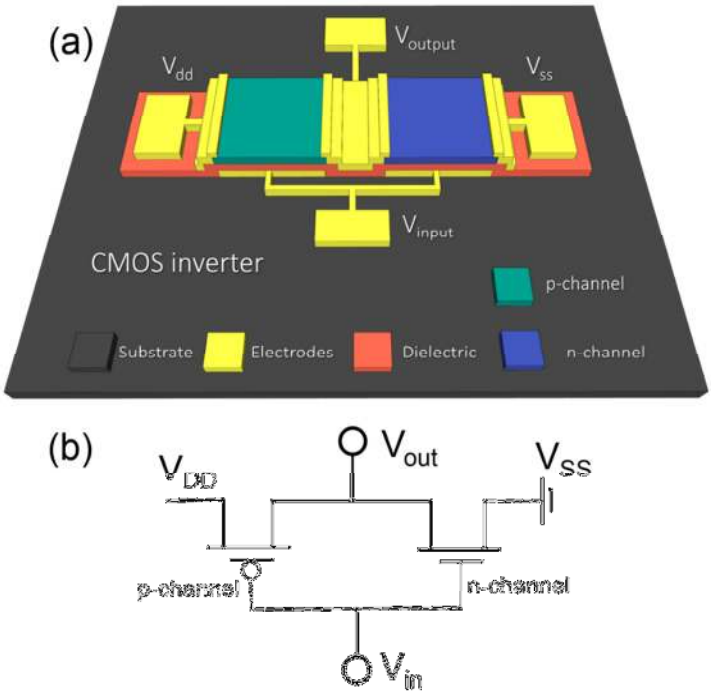

Figure 9. (a) Typical structure and (b) schematic circuit diagram of a complementary metal oxide semiconductor (CMOS) inverter.

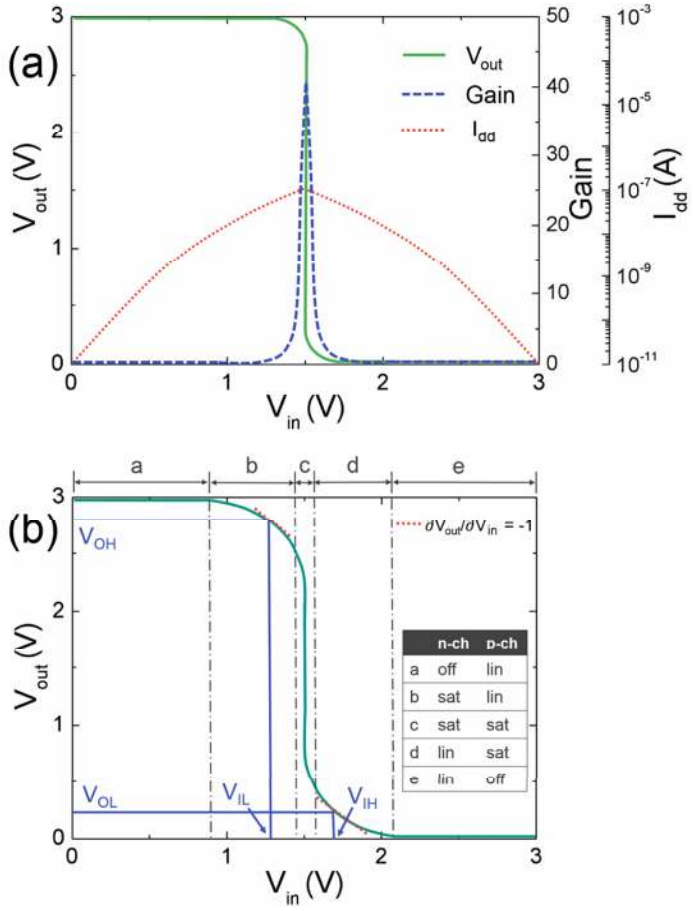

Figure 10. Typical VTC curve of a CMOS inverter during operation. (a) Gain and I_{dd} are shown with the VTC curve, (b) noise margins extraction and different operation regimes of CMOS inverter.

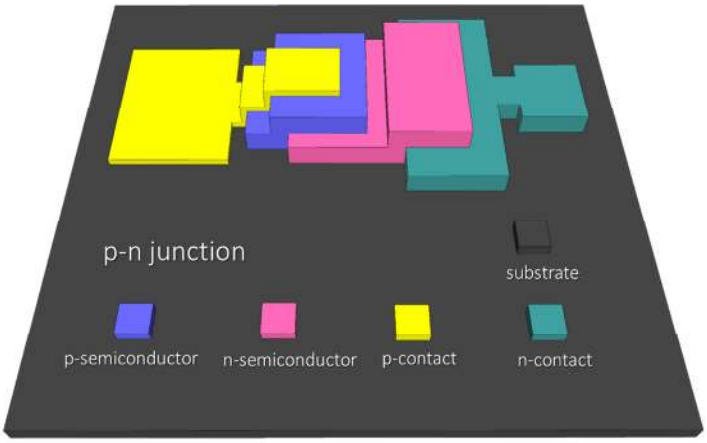

Figure 11. Typical structure of a p-n junction diode.

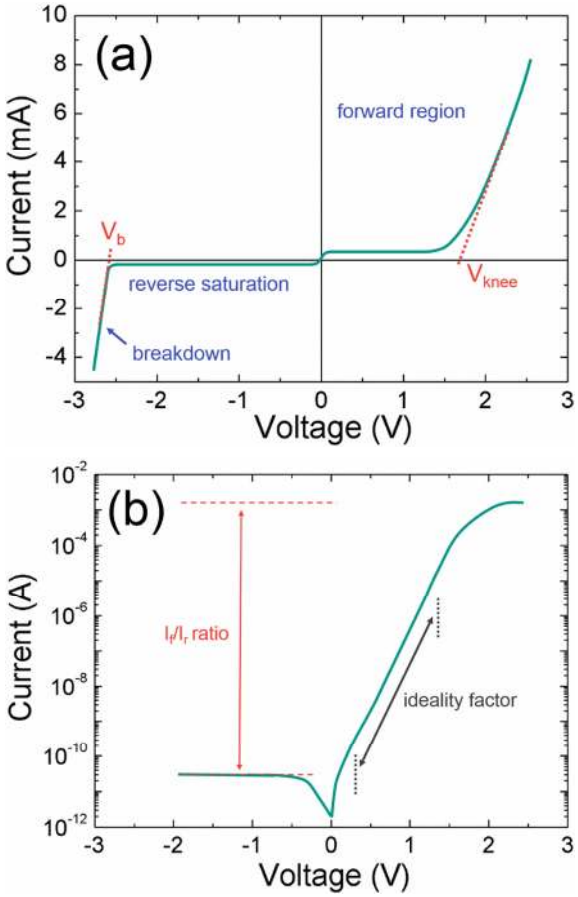

Figure 12. Typical current-voltage curve characteristics of diodes plotted on (a) linear, and (b) log scales.

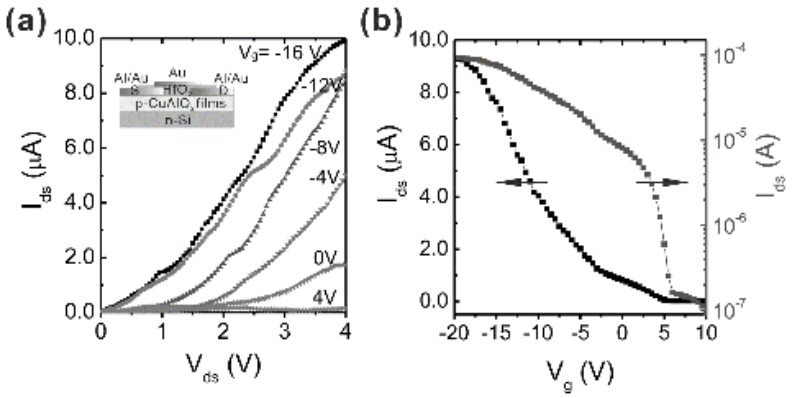

Figure 13. (a) Output characteristics of top-gate TFTs built using Cu-O/$CuAlO_2$ alloy films with V_{GS} ranging from +4 to -16 V in steps of 4 V. (b) I_{DS}-V_{GS} plots of the same device at V_{DS} = -3V. Inset in (a) depicts the schematic device structure of the $CuAlO_2$-based TFTs. Reproduced with permission.[75] Copyright 2012, American Institute of Physics.

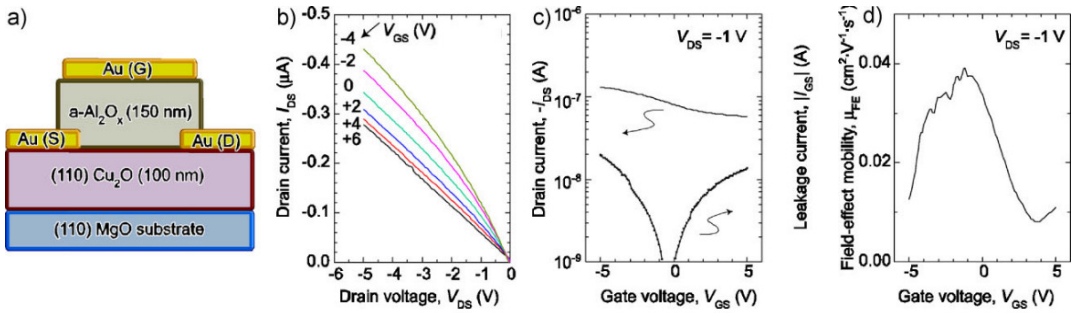

Figure 14. (a) Device structure of a top-gate TFT using the (110) Cu_2O epitaxial channel. (b) Output and (c) transfer characteristics, and (d) calculated μ_{FE} of the (110) Cu_2O TFT. Reproduced with permission.[108]

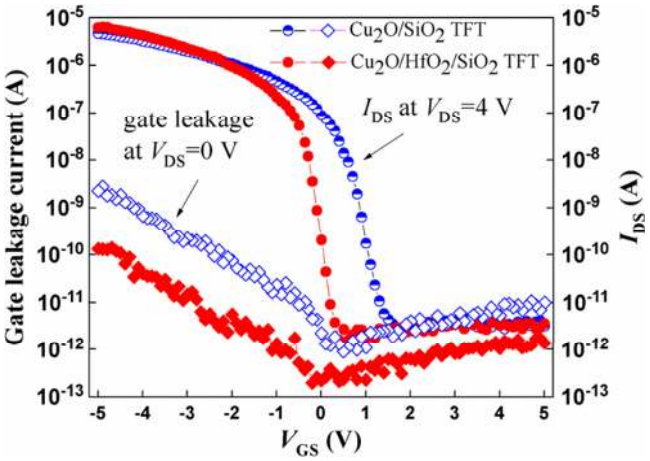

Figure 15. Transfer characteristics of Cu_2O TFTs (W/L = 500 μm/20 μm) with HfO_2/SiO_2-stacked and SiO_2 dielectrics, V_{GS} was swept from 5 to -5 V, at V_{DS} = -4 V. Gate-leakage currents of these Cu_2O TFTs are also depicted, where V_{GS} was swept from 5 to -5 V, at V_{DS} = 0 V. Reproduced with permission. [113] Copyright 2011, IEEE.

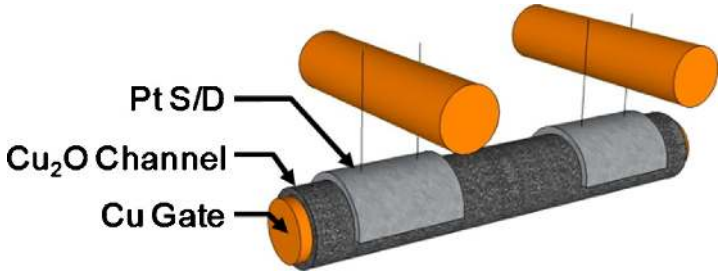

Figure 16. Schematic diagram of Cu_2O transistor on Cu wire. Inner core Cu wire and outer shell Cu_2O film are used for the gate and channel, respectively. Source and drain pads are made by thermally evaporated Pt, and the source and drain interconnection is made by cross-woven Cu wire. Reproduced with permission.[310] Copyright 2011, American Institute of Physics.

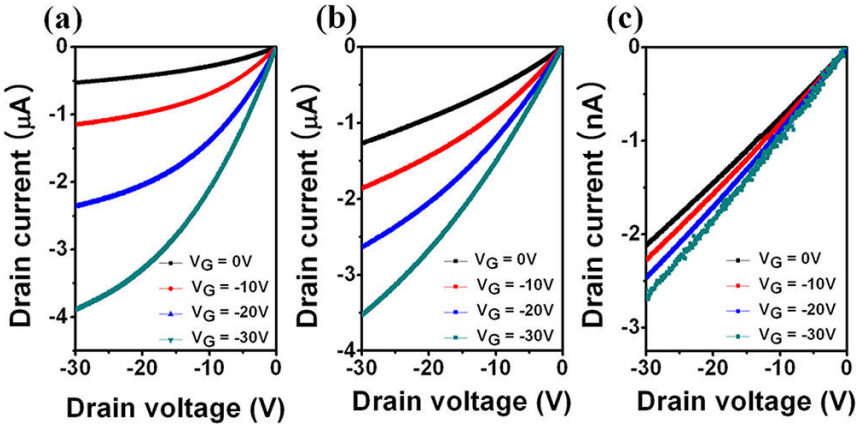

Figure 17. Output characteristics of copper oxide TFTs annealed at different oxygen partial pressures (P_{O2}) of (a) 0.04, (b) 0.2, and (c) 0.9 Torr. V_{DS} is swept from 0 to -30 V and V_{GS} is varied from 0 to -30 V. Reproduced with permission.[145] Copyright 2013, American Chemical Society.

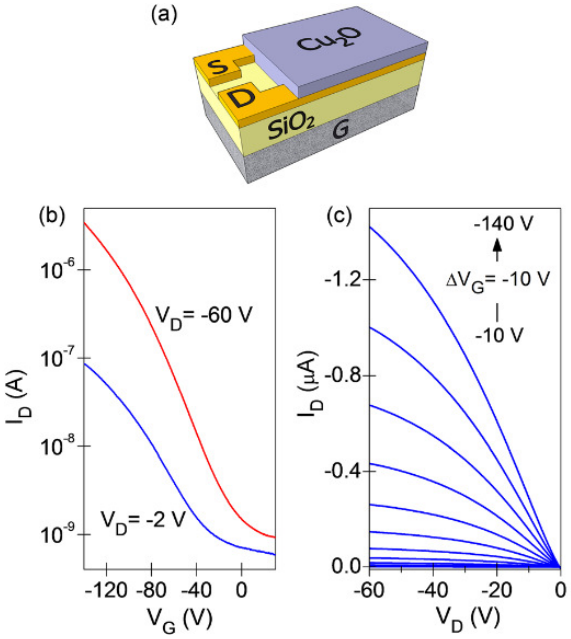

Figure 18. (a) Schematic of the coplanar bottom-gate transistor architecture used to study charge transport in spray-coated Cu_2O films. The devices employ a heavily doped Si electrode acting as the common gate, a thermally grown layer of SiO_2 acting as the gate dielectric, and lithographically patterned gold source/drain electrodes as the hole-injecting contacts. A representative set of results from electrical characterization of Cu_2O TFTs showing (b) transfer and (c) output characteristics. The dimensions of the transistor studied here are W=10 mm and L=20 µm. Reproduced with permission.[151] Copyright 2013, American Institute of Physics.

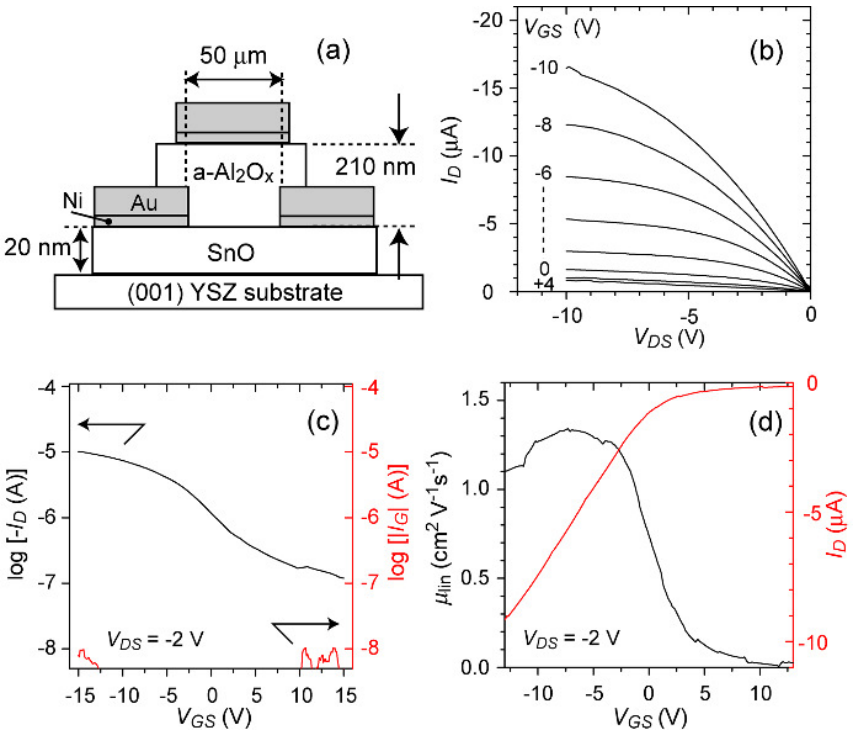

Figure 19. (a) Structure of a top-gate SnO TFT. (b) Output characteristics. (c) Transfer characteristics at V_{DS}= -2 V. (d) Field-effect mobility in the linear region, as a function of V_{GS}. Reproduced with permission.[8] Copyright 2008, American Institute of Physics.

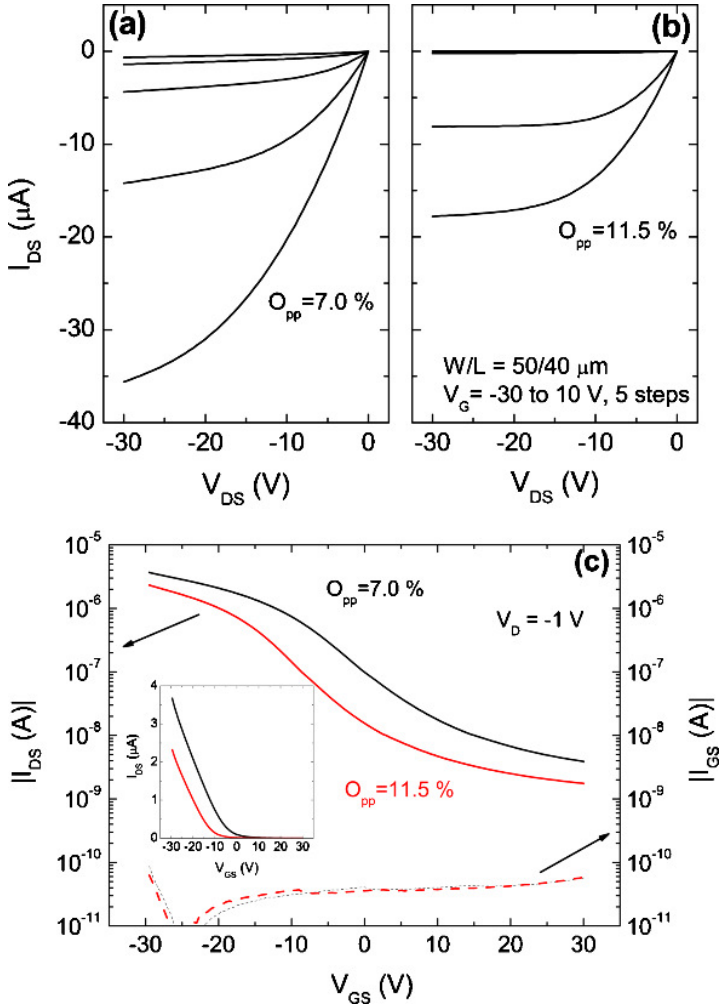

Figure 20. Output characteristics for p-type TFTs, where SnO_x is produced with (a) Opp=7.0 and (b) Opp=11.5%. (c) Transfer characteristics for SnO_x TFTs annealed in air at 200 °C, where SnO_x is produced with Opp=7.0 and 11.5%. The inset shows the I_{DS}-V_{GS} plots represented in linear scale, for V_T extraction. Reproduced with permission.[7] Copyright 2010, American Institute of Physics.

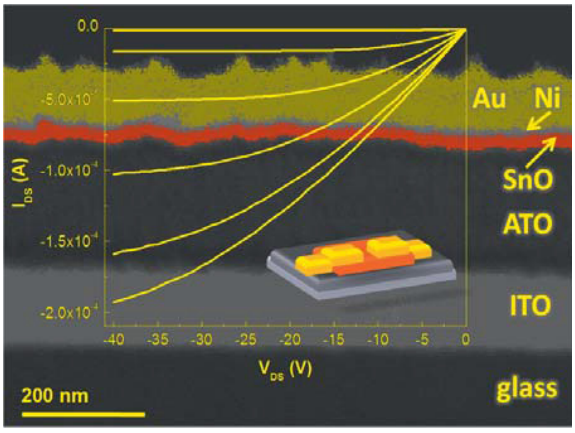

Figure 21. Typical output characteristics of SnO_x p-channel TFT (gate voltage is varied from 0 V to -50 V in -10 V steps) in front of a SEM cross section where there is clearly shown all the constituent layers. Reproduced with permission.[6]

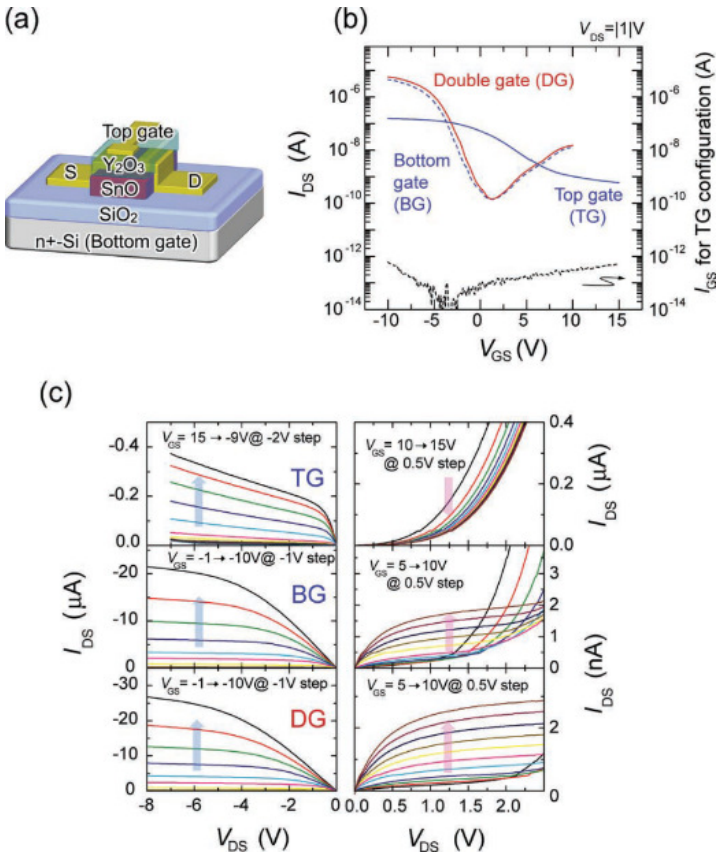

Figure 22. (a) Structure of a double-gated SnO TFT. SiO_2 and Y_2O_3 layers were used as the bottom and top gate insulators, respectively. (b) Variation of transfer curves for top gate (TG, blue solid line), bottom gate (BG, blue dashed line) and dual gate (DG, red line) bias operations. (c) Output characteristics of the same TFTs under p-channel (left) and n-channel (right) operation. Reproduced with permission.[173]

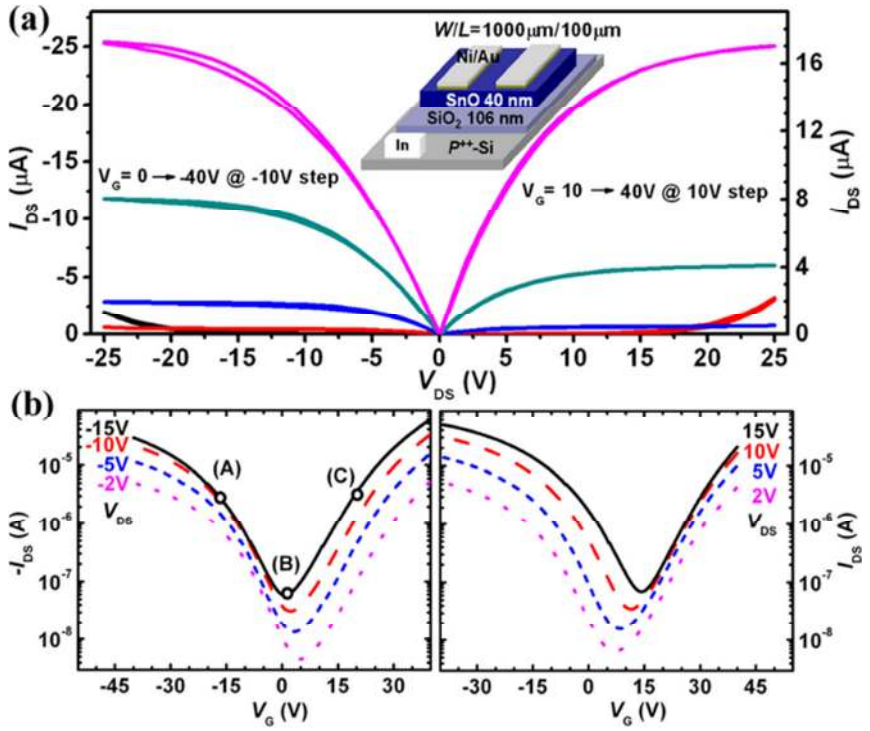

Figure 23. (a) Output characteristics of the ambipolar SnO TFT under p-channel (left) and n-channel (right) operations. The inset shows the schematic diagram of the SnO TFTs. (b) Transfer characteristics of the same TFT at $V_{DS} < 0$ (left) and $V_{DS} > 0$ (right). Reproduced with permission.[179] Copyright 2012, American Institute of Physics.

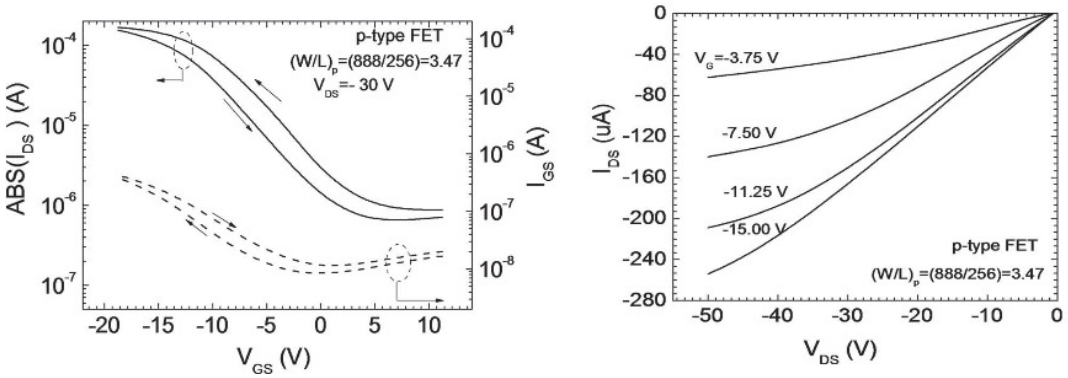

Figure 24. Transfer (left) and output (right) characteristics of p-channel FET on paper substrate and dielectric for W/L ratio of 3.47. Adapted with permission.[14]

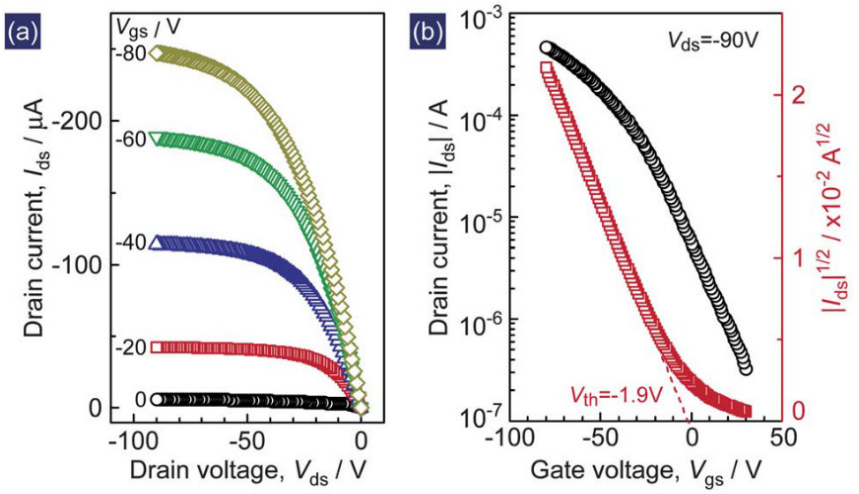

Figure 25. (a) The output and (b) transfer characteristics of the solution processed SnO TFT. Reproduced with permission.[315] Copyright 2012, Royal Society of Chemistry.

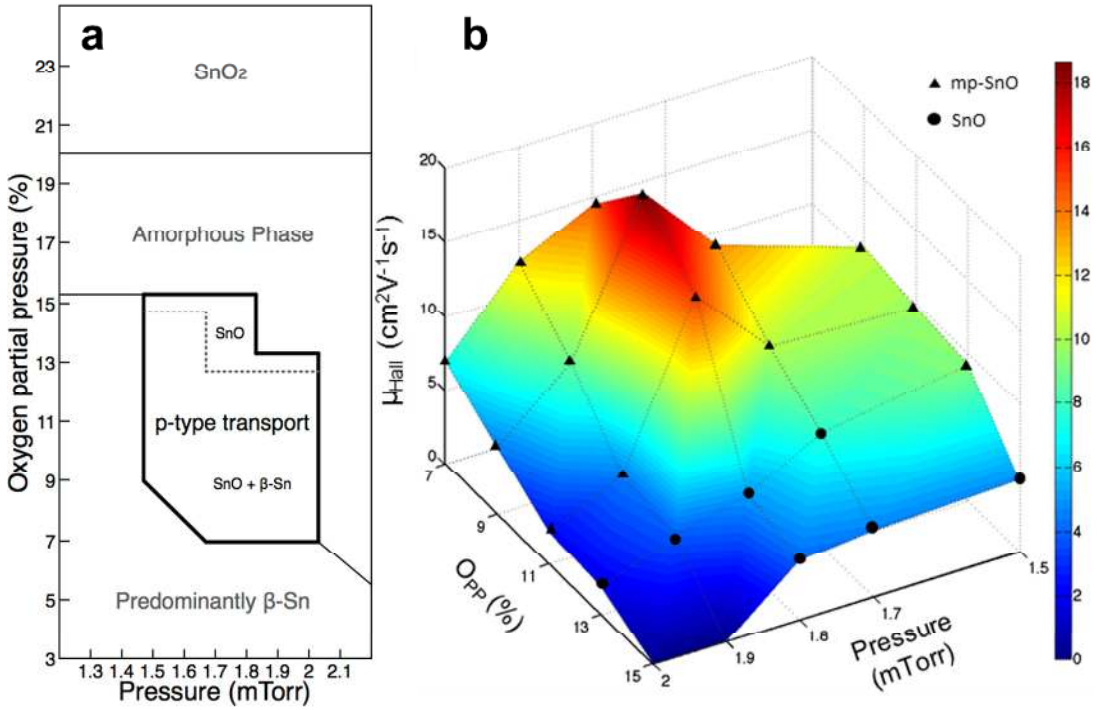

Figure 26. (a) Phase stability map to obtain p-type tin monoxide, which occurs in a very narrow window of deposition conditions. (b) Room temperature Hall mobility of the films deposited in the pressure range from 1.5 to 2.0 mTorr and 7% to 15% Opp. The point at 7% Opp, 1.5 mTorr showing n-type conduction as well as the 15% OPP at 1.9 mTorr and 2.0 mTorr showing unreliable measurements, are set to zero. A maximum Hall mobility of 18.7 cm^2 V^{-1} s^{-1} is obtained at 1.8 mTorr, 9% OPP. Adapted with permission.[167] Copyright 2013, American Chemical Society.

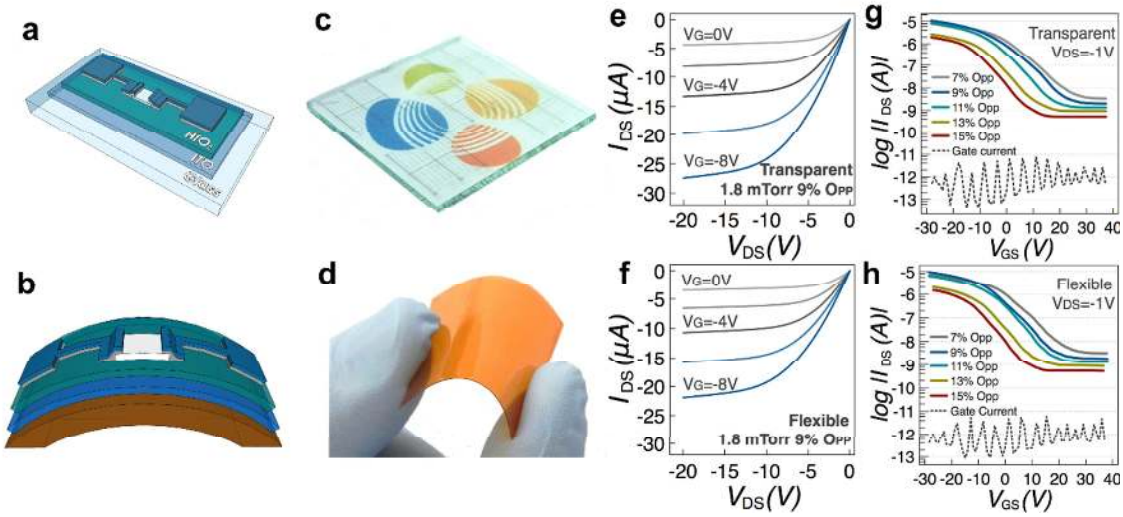

Figure 27. SnO based TFTs. Schematic of fully transparent device (a) on glass, and (b) on flexible plastic substrates. Photographs of (c) actually fully transparent device, and (d) actual flexible devices. (e, g) Output and transfer characteristics of devices fabricated on glass (fully transparent) and (f, h) devices fabricated on polyimide (flexible), with a channel width of 50 μm and length of 50 μm. The gate currents of all the devices were around 10^{-12} amps. Reproduced with permission.[167] Copyright 2013, American Chemical Society.

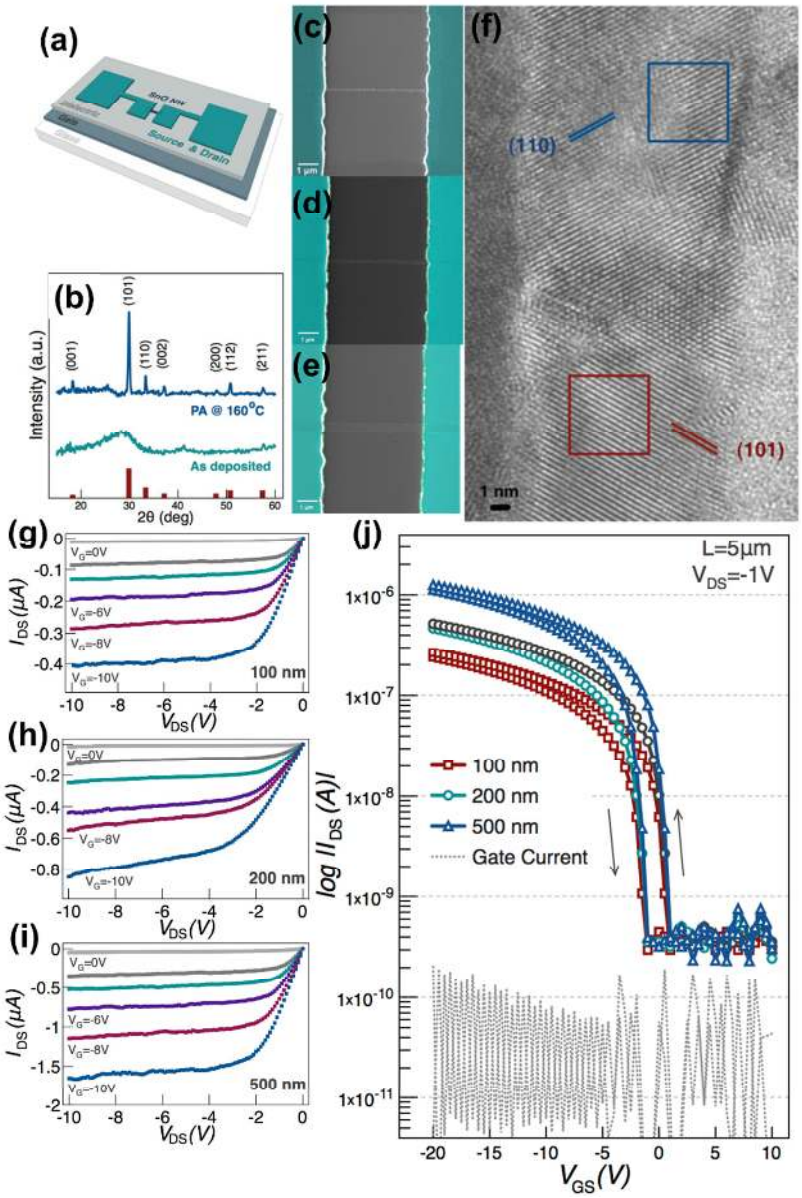

Figure 28. (a) Schematic of SnO nanowire FET. (b) X-ray diffraction patterns of amorphous as-deposited SnO films and crystalline SnO films after annealing in air at 160 °C. Top view scanning electron microscopy image of fabricated device with channel length of 5 μm and channel width defined by the nanowire planar width of (c) 100 nm, (d) 200 nm and (e) 500nm, scale bar 1 μm. (f) HRTEM image of the SnO nanowire, viewed vertically. Output characteristics of (g) 100 nm, (h) 200 nm, and (i) 500 nm p-type SnO nanowire transistors (NW-FETs), respectively. (j) Transfer characteristics of SnO NW-FETs annealed at 160 °C as a function of nanowire width when using HfO_2 as gate dielectric. Adapted with permission.[195] Copyright 2013, American Institute of Physics.

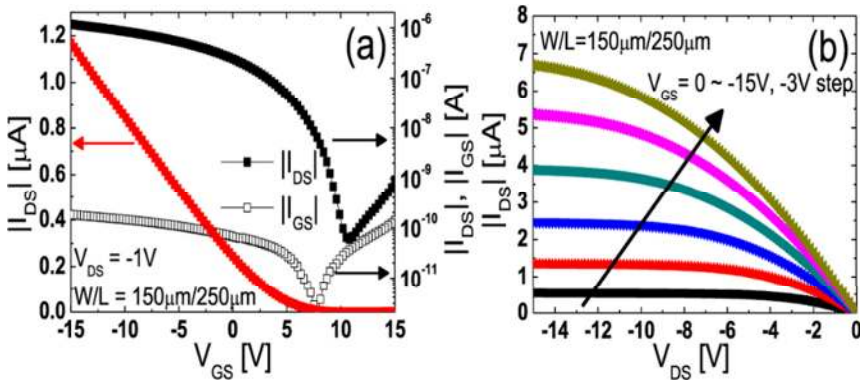

Figure 29. Representative (a) transfer curve and gate leakage current, and (b) output characteristics of the bottom-gate SnO TFTs. Reproduced with permission.[204] Copyright 2014, IEEE.

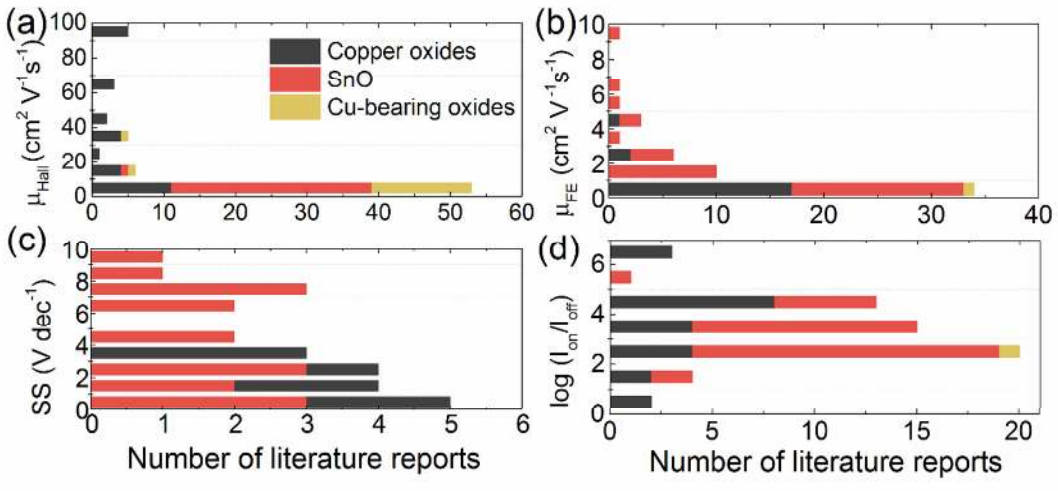

Figure 30. Graphical summary of the reviewed literature reports showing (a) Hall mobility of p-type thin films; (b) field-effect mobility, (c) subthreshold swing, and (d) I_{on}/I_{off} ratio of p-type TFTs incorporating binary and ternary p-type oxides.

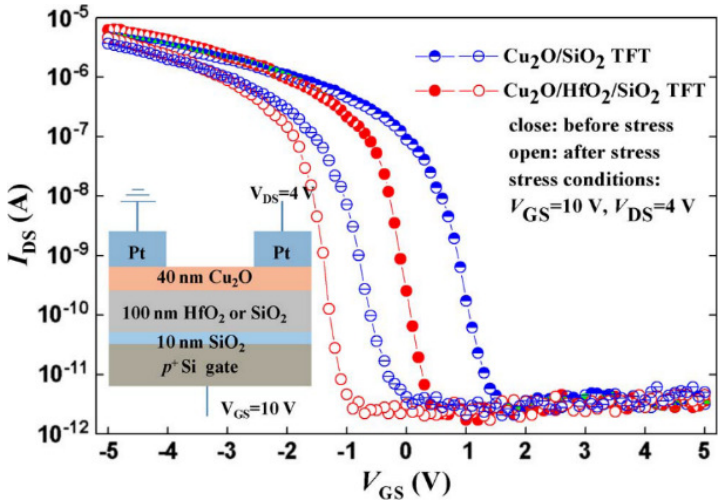

Figure 31. Evolution of the transfer curves after gate-bias voltage stressing of Cu_2O TFTs with the HfO_2/SiO_2-stacked and SiO_2 dielectrics, respectively. Stressing conditions: V_{GS} = 10 V, V_{DS} = 4 V, and stressing duration = 3600 s. The inset shows device schematic during the stressing test. Reproduced with permission.[113] Copyright 2011, IEEE.

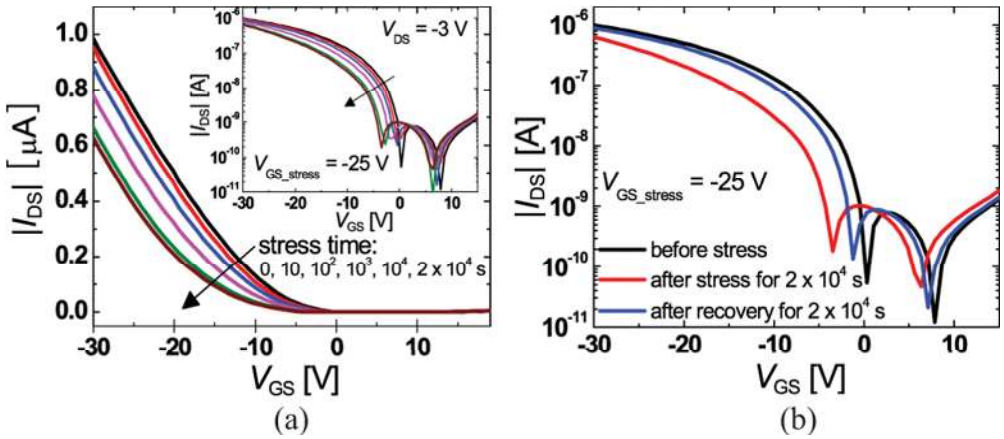

Figure 32. (a) Linear plot of the transfer curves under a negative gate bias stress condition (V_{GS} = -25 V, V_{DS} = 0 V) as a function of an applied stress time. The inset represents the transfer curves on a logarithmic scale. (b) Transfer curve shift during the recovery phase (V_{GS} = V_{DS} = 0 V) after terminating the gate bias stress. Reproduced with permission.[132] Copyright 2013, IEEE.

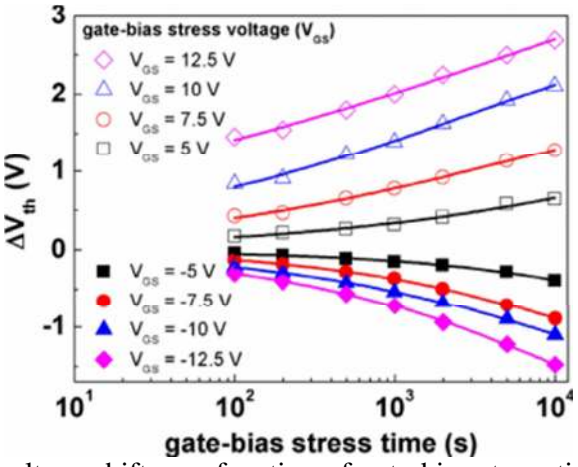

Figure 33. Threshold voltage shift as a function of gate-bias stress time under various gate-bias stress voltages at both polarities. Reproduced with permission.[206] Copyright 2014, IEEE.

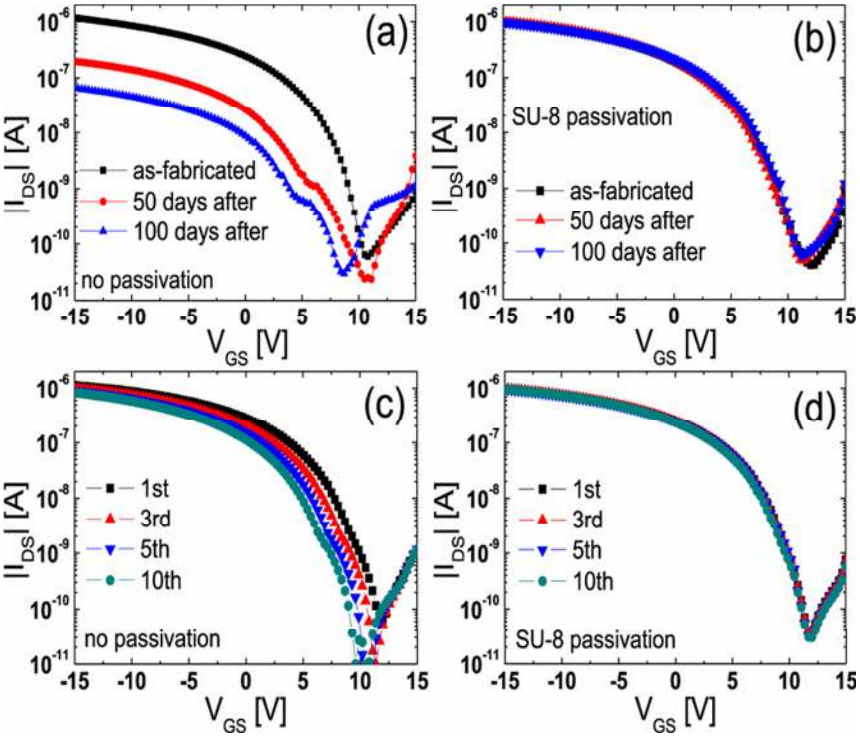

Figure 34. Long term stability of SnO TFTs (a) without and (b) with a SU-8 passivation layer. Series of transfer curves obtained from the devices (c) without and (d) with a SU-8 passivation layer, where the gate voltage sweeps were repeated for 10 times from 15 V to -15 V. Reproduced with permission.[204] Copyright 2014, IEEE.

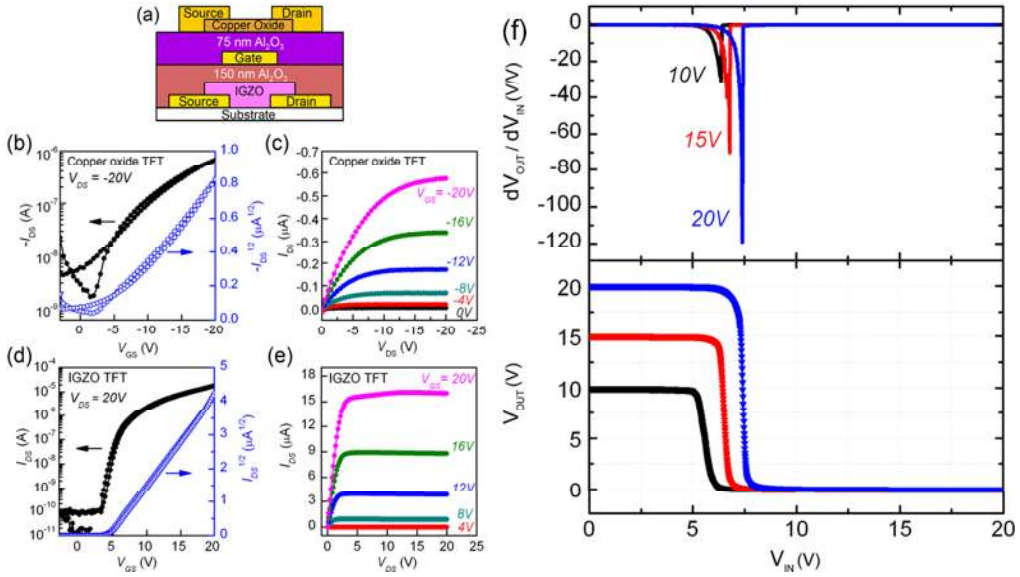

Figure 35. (a) Schematic of a vertically stacked p-channel copper oxide transistor fabricated on top of an n-channel a-GIZO transistor on a flexible PES substrate. Representative (b) hysteresis transfer and (c) single sweep output characteristics of copper oxide p-channel TFTs with W=4000 µm and L=180 µm. Representative (d) hysteresis transfer and (e) single sweep output characteristics of a-GIZO n-channel TFTs with W=400 µm and L=180 µm. (f) Voltage transfer characteristics and static DC gains of the inverter at different supply voltages of 5, 10, and 20 V. Adapted with permission.[122] Copyright 2011, American Institute of Physics.

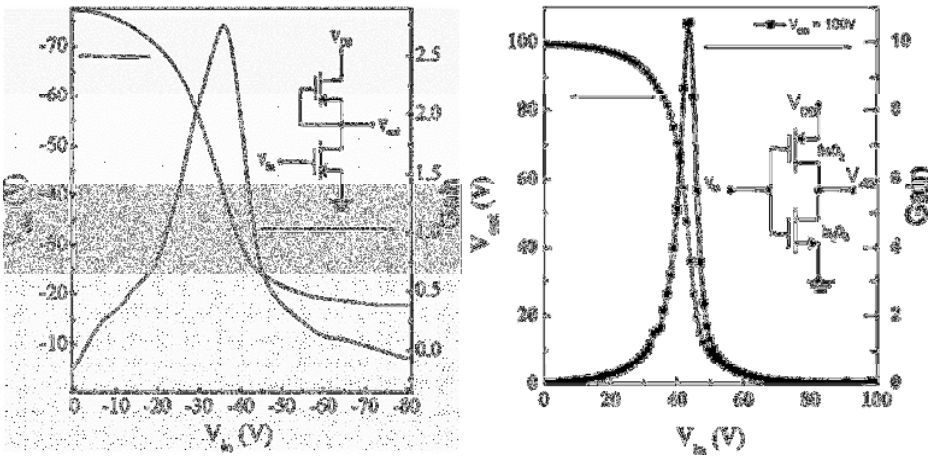

Figure 36. Voltage transfer curves and their corresponding gains of the (left) SnO_x-SnO_x inverters and (right) SnO_x-In_2O_3 CMOS inverter. (Insets) Schematic diagrams of inverter circuit. Adapted with permission.[211, 212] Copyright 2008, American Institute of Physics.

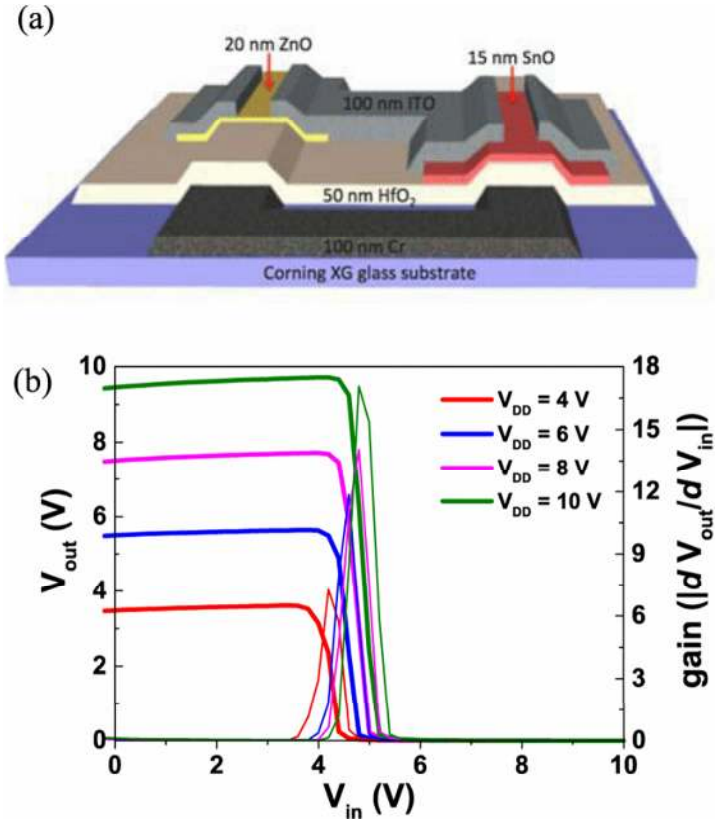

Figure 37. (a) Schematic cross section of a complementary TFT inverter based on a p-channel SnO TFT and an n-channel ZnO TFT on glass substrates. (b) The static voltage transfer characteristics and voltage gain curves at different supply voltages (V_{dd}) of the complementary oxide-TFT inverter with a geometric aspect ratio of 5. Reproduced with permission.[210] Copyright 2014, IEEE.

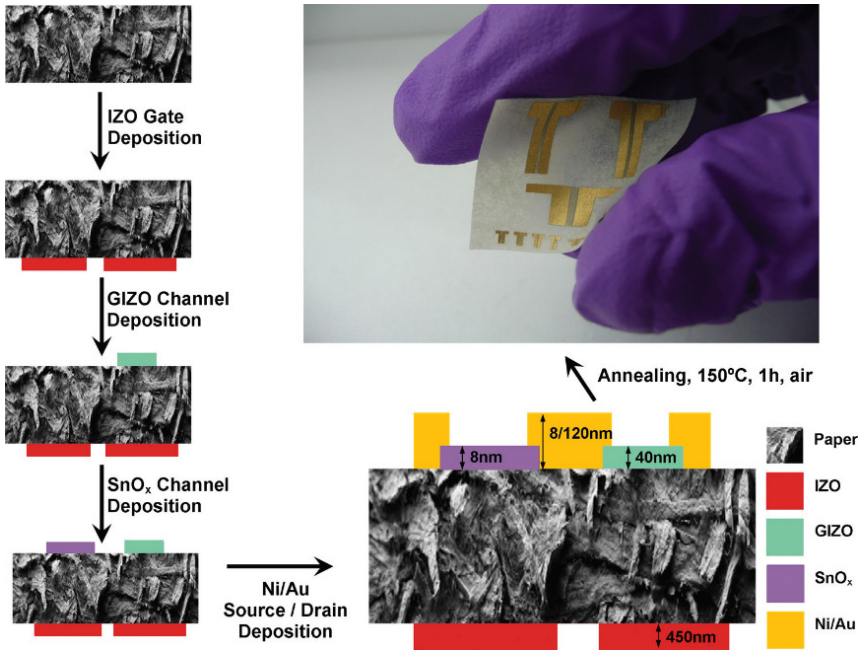

Figure 38. Cross-sectional schematic of the fabrication sequence of the paper CMOS showing all layers that constitute the final device and how they are interconnect as well as an image of the real device. Reproduced with permission.[13]

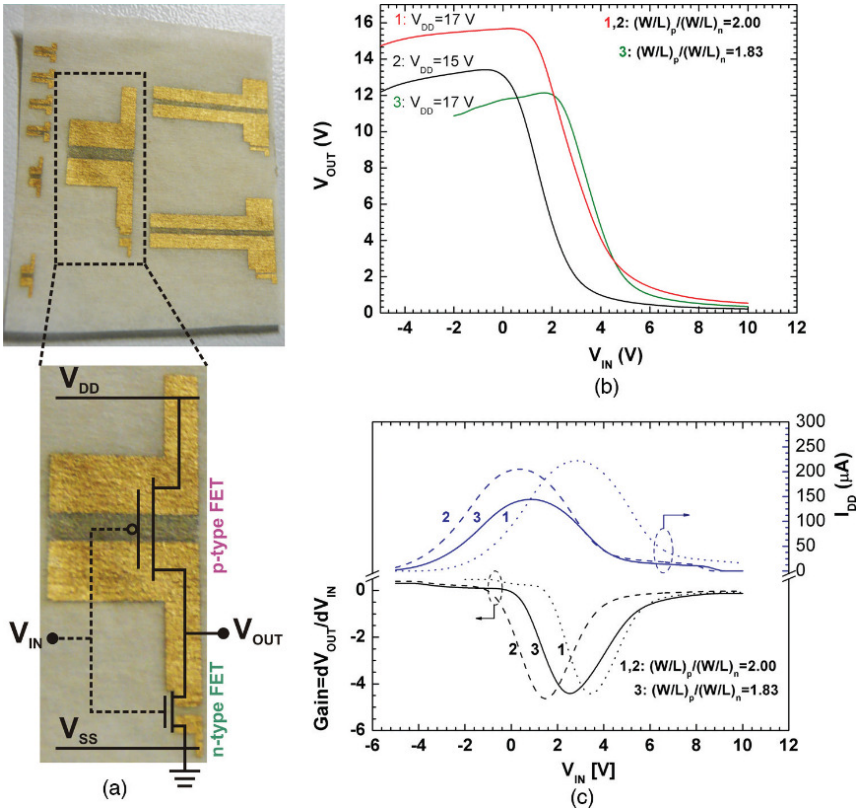

Figure 39. (a) Image of the CMOS on paper where the large $(W/L)_p$ = 20.8 and small $(W/L)_n$ = 10 correspond to the p-FET and n-FET, respectively. (b) VTCs of the CMOS inverter for the different configurations. (c) Gain and circuit leakage current, I_{DD}, for different configurations. Reproduced with permission.[13]

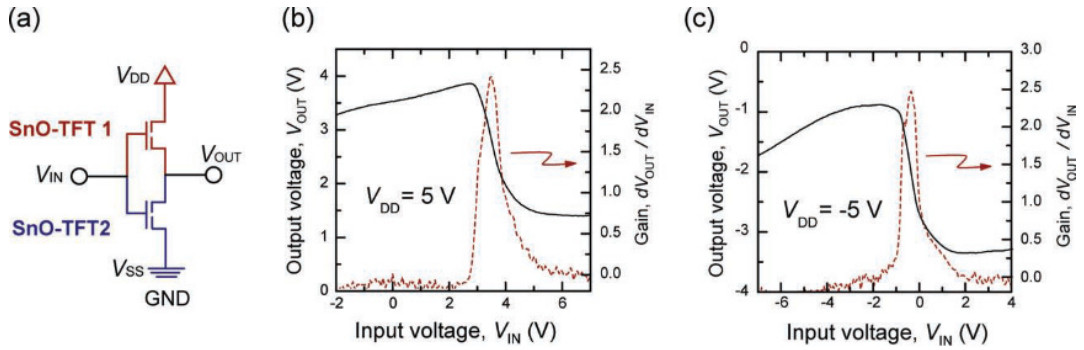

Figure 40. (a) Diagram of inverter circuit composed of two SnO ambipolar TFTs. Inverter characteristics for (b) first and (c) third quadrants with supply voltages (V_{dd}) of ±5 V, respectively. The red dashed lines show the voltage gain characteristics. Reproduced with permission.[173]

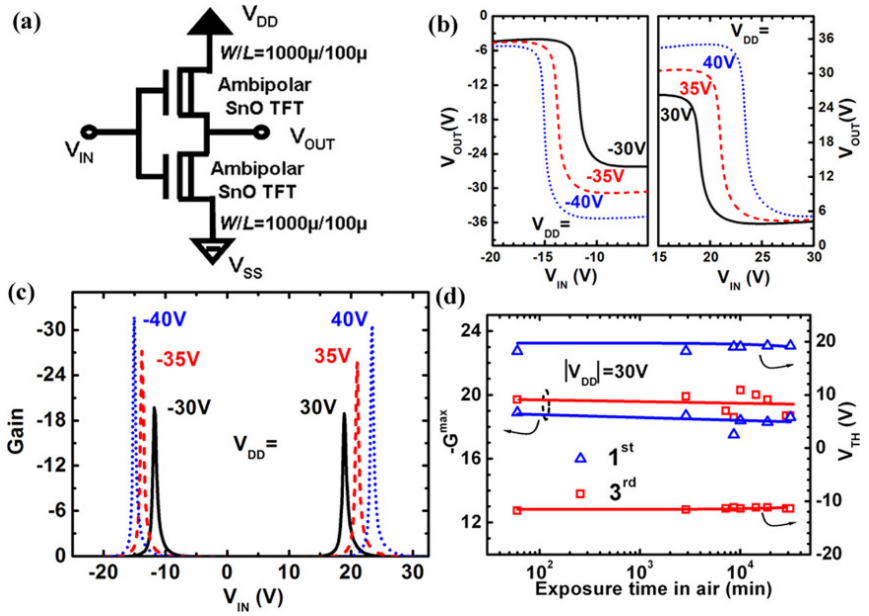

Figure 41. (a) SnO ambipolar inverter circuit diagram. (b) VTCs of the CMOS-like inverter in the first (right) and third (left) quadrants, respectively. (c) Differential gain as a function of input voltage (V_{in}). (d) Evolution of the maximum gain (G_{max}) and V_{th} at $|V_{dd}| = 30$ V in the first and third quadrants as a function of exposure time to ambient air over a period of 3 weeks. Reproduced with permission.[179] Copyright 2012, American Institute of Physics.

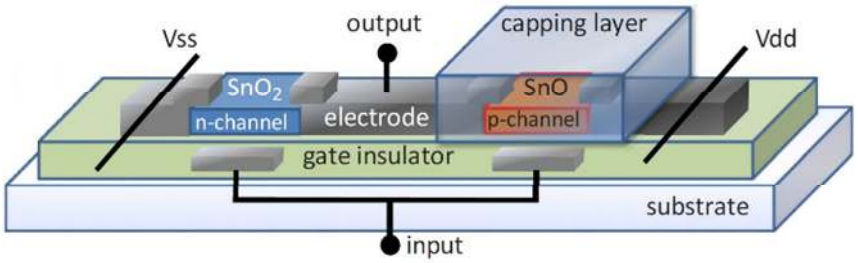

Figure 42. A conceptual design of an SnO-based complimentary (CMOS) circuit. Reproduced with permission.[37] Copyright 2010, American Institute of Physics.

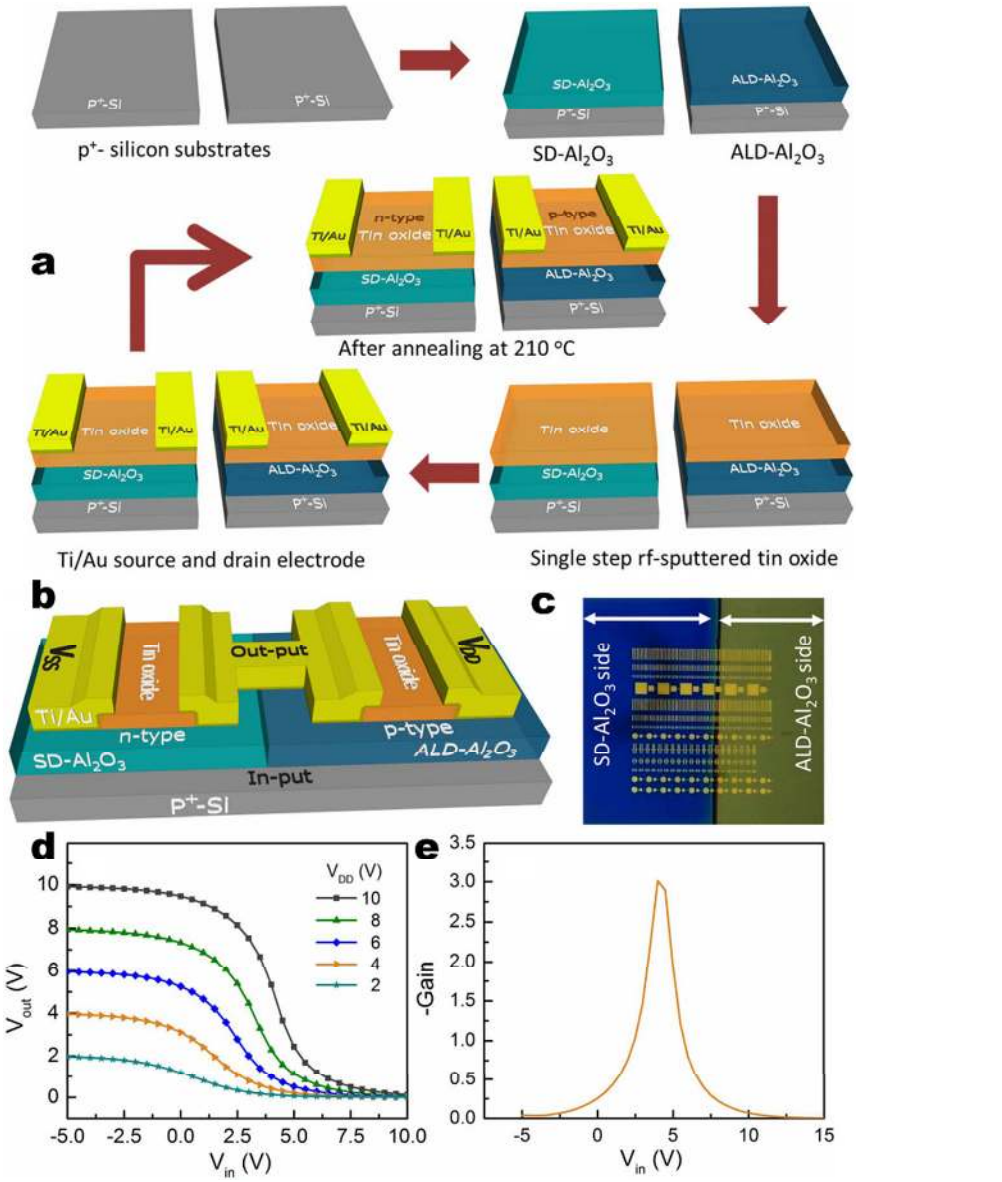

Figure 43. (a) TFTs with tin oxide n- and p-channels formed simultaneously using single step deposition of tin oxide channels on solution deposited (SD)-Al_2O_3 and ALD-deposited Al_2O_3 gate dielectrics, respectively. (b) Schematic of the CMOS inverter device structure and (c) top-view image of the actual device with both n- and p-type tin oxide TFTs. (d) Voltage transfer and (e) gain characteristics of the CMOS inverter. Adapted with permission.[198] Copyright 2014, Nature Publishing Group.

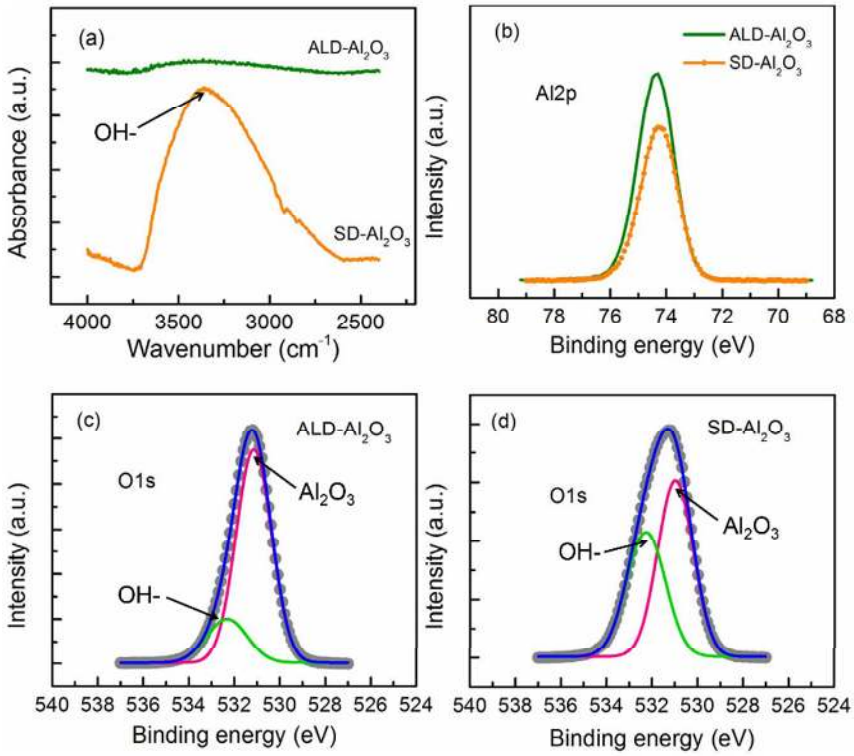

Figure 44. FT-IR and XPS spectra of aluminum oxide dielectrics. (a) FT-IR spectra of ALD-Al_2O_3 and SD- Al_2O_3 thin films, (b) XPS Al2p peaks of ALD-Al_2O_3 and SD-Al_2O_3 thin films, XPS O1s peak of (c) ALD-Al_2O_3 and (d) SD-Al_2O_3 thin films. Adapted with permission.[198] Copyright 2014, Nature Publishing Group.

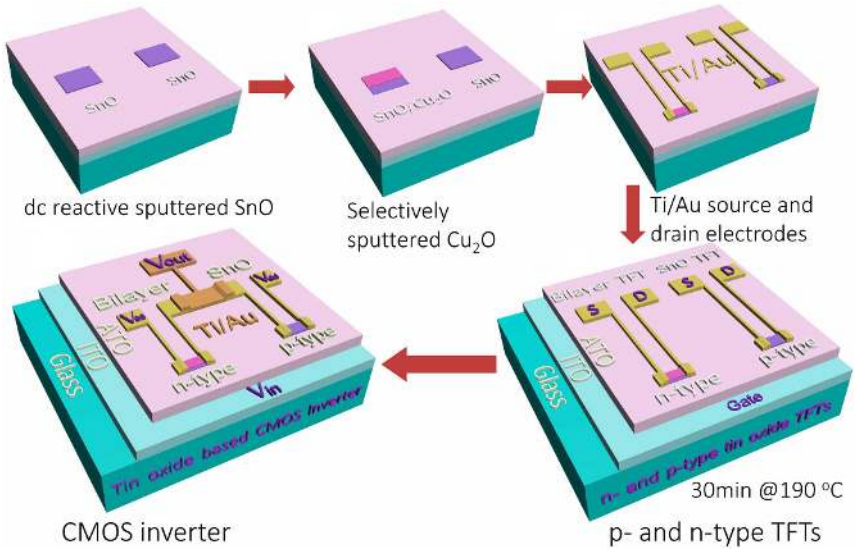

Figure 45. Flow diagram showing TFTs and CMOS inverter fabrication process. Reproduced with permission.[199] Copyright 2015, Nature Publishing Group.

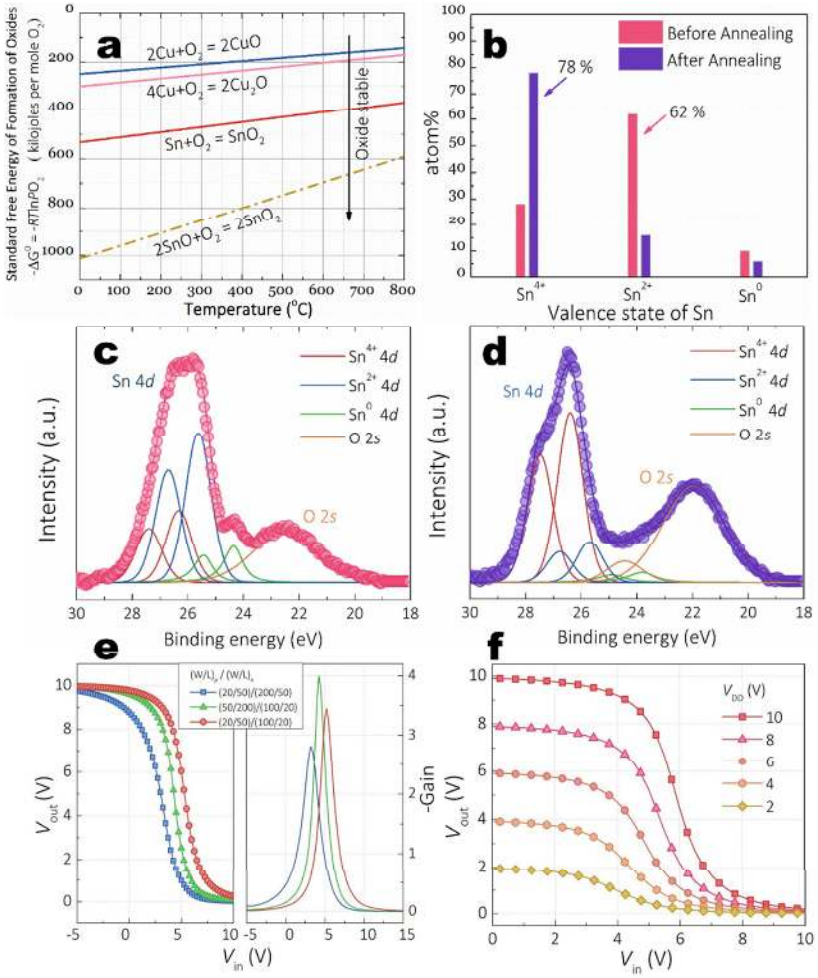

Figure 46. (a) Ellingham diagram of the bilayer system. (b) Atomic content of the various valence states of Sn before and after annealing the bilayer samples. XPS Sn 4d and O 2s peaks for (c) before and (d) after annealing the bilayer samples. (e) Voltage transfer and gain characteristics of CMOS inverters with variable channel size ratios. (f) Voltage transfer curves of optimized CMOS inverter. Adapted with permission.[199] Copyright 2015, Nature Publishing Group.

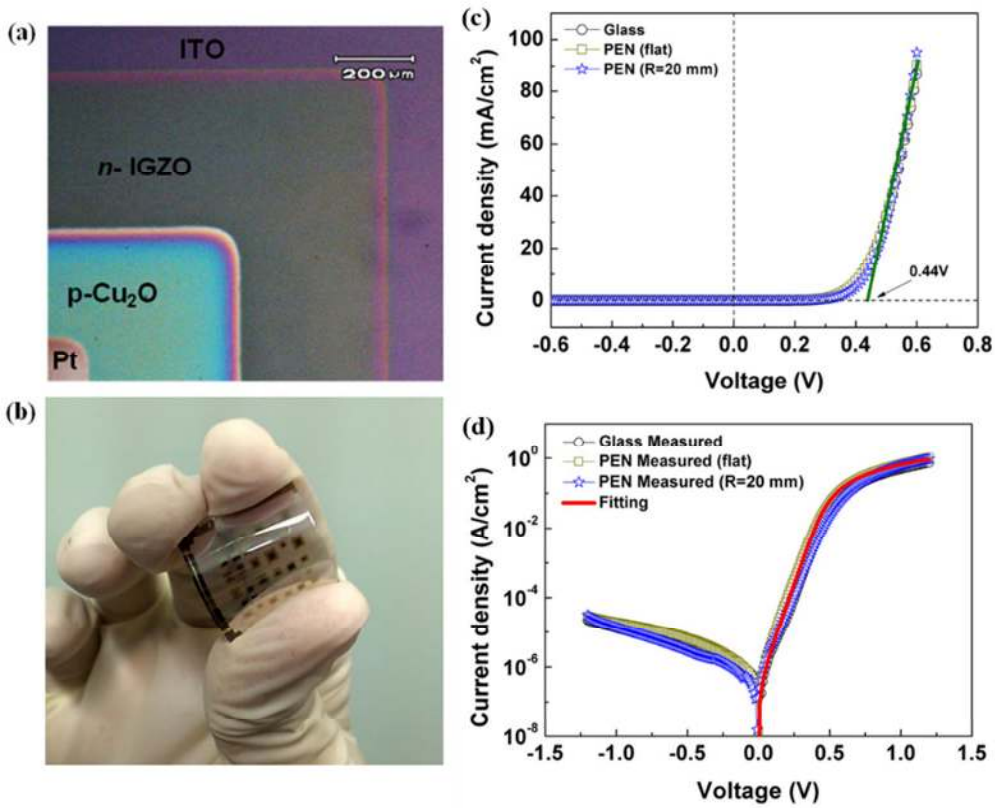

Figure 47. Micrograph showing (a) the various layers of the fabricated n-GIZO/p-Cu_2O diode, and (b) the diodes fabricated on PEN plastic substrate. J-V characteristics of the n-GIZO/p-Cu_2O heterojunction diodes on the glass substrate and on the PEN plastic substrate (either flat or bent to a radius of curvature R=20 mm): (c) in the linear scale and (d) in the semi-log scale. Adapted with permission.[138] Copyright 2014, IOP Publishing.

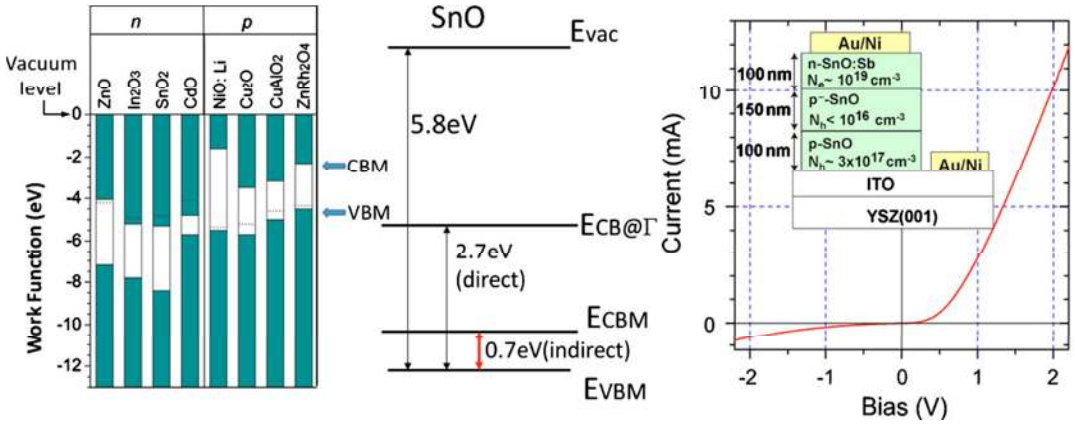

Figure 48. (left) Band alignment of n- and p-type oxide semiconductors. The broken line indicates the Fermi level in the sample used for ultraviolet photoelectron spectroscopy measurements. (middle) The energy levels determined for SnO by hard X-ray-photoemission spectroscopy. (right) I-V curve for the p-n junction. Adapted with permission.[177] Copyright 2011, The Electrochemical Society.

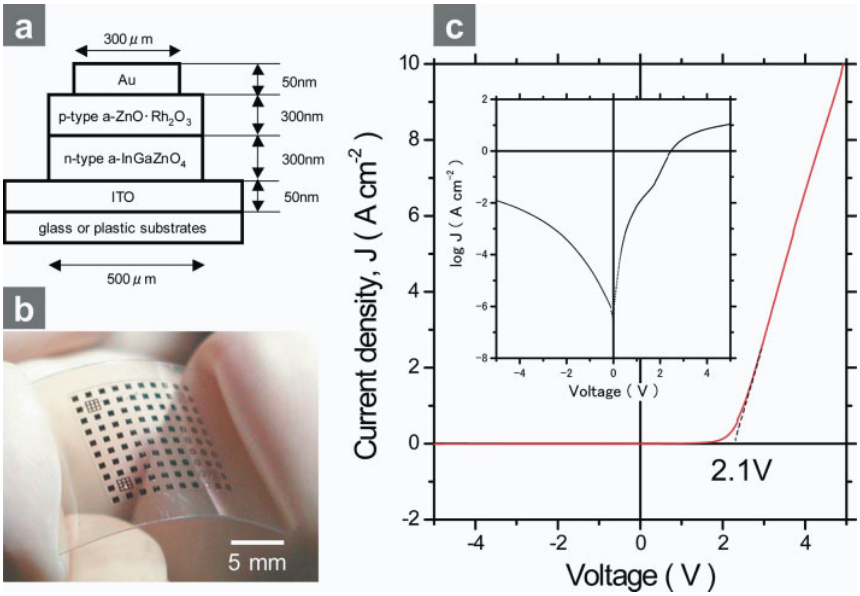

Figure 49. A p-n junction diode composed of all amorphous oxide semiconductors. (a) Schematic of the p-n junction structure. (b) A photograph of a flexible device on a plastic sheet. (c) Current density-voltage (J-V) characteristic. The inset shows a logarithmic plot of J-V characteristic. The device shows a distinct rectifying characteristic with a threshold voltage of 2.1 V and on-off current ratio of 10^3 at ±5 V. Reproduced with permission.[226]

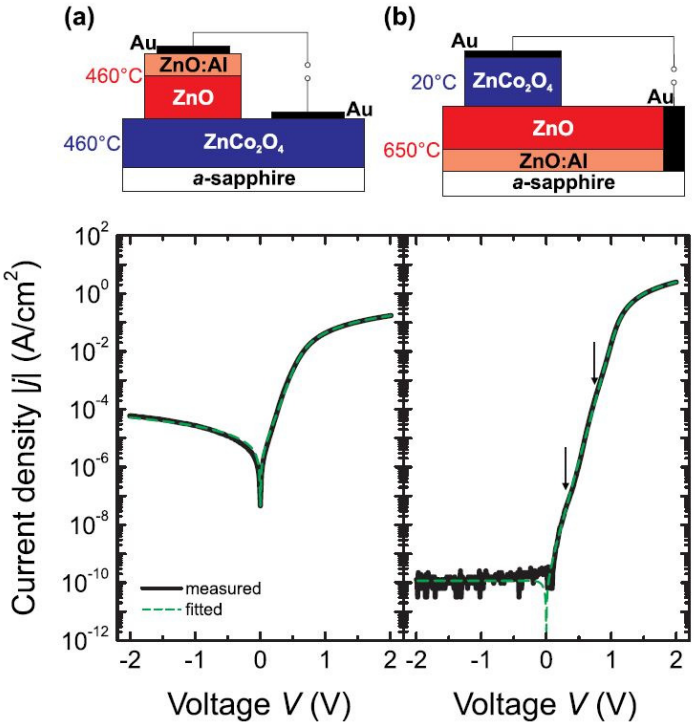

Figure 50. Sketches of the (a) ZnO/ZCO or (b) ZCO/ZnO diode structure and corresponding measured and fitted j-V characteristics of the highest rectifying diodes. Growth temperatures of respective oxide films are labeled. Arrows in (b) indicate slight kinks which are due to small interface regions with lower barrier. Reproduced with permission.[234] Copyright 2014, American Institute of Physics.

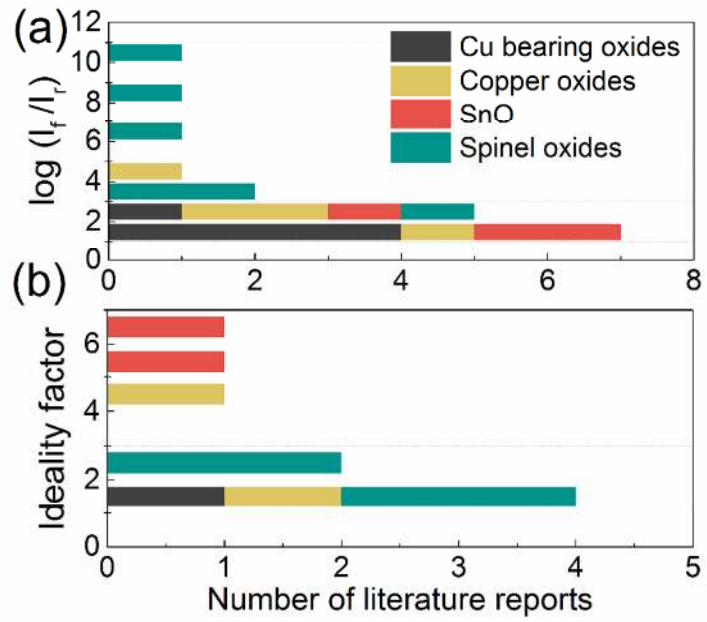

Figure 51. Graphical summary of the reviewed literature reports showing (a) forward and reverse current (I_f/I_r) ratios, and (b) ideality factors of oxide based p-n junction diodes.

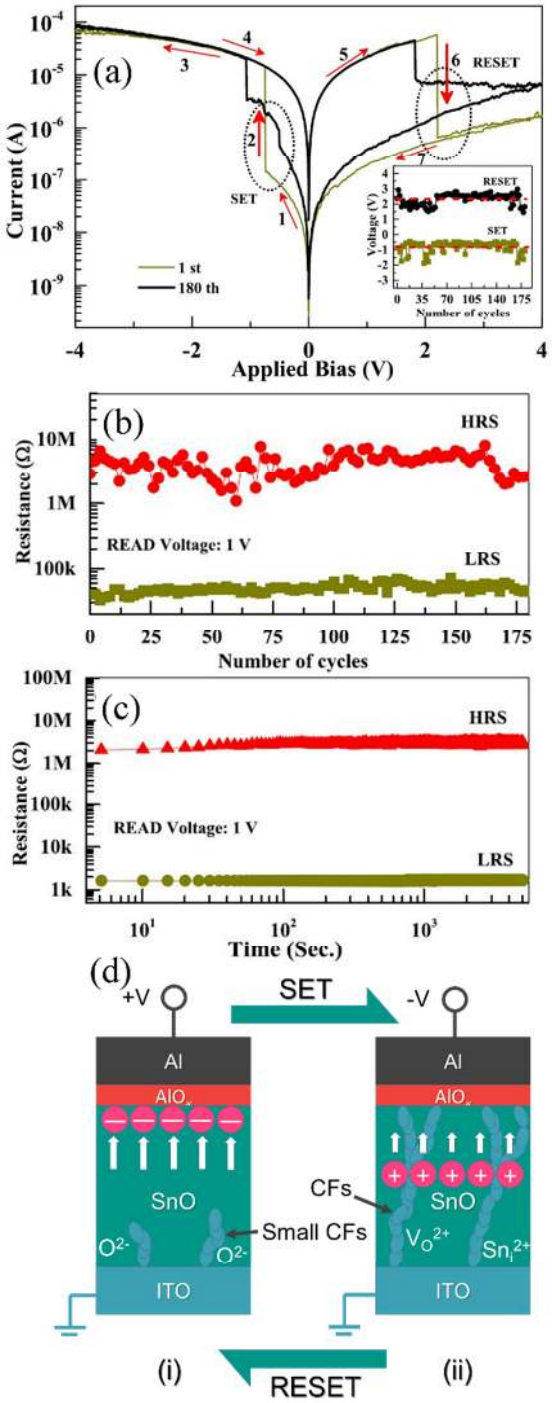

Figure 52. (a) Bipolar reversible and nonvolatile RS characteristics of as-deposited SnO memory device and variation of the V_{SET} and V_{RESET} during the dc switching cycling measurement (inset). (b) DC switching cycle test and (c) retention characteristics of the ITO/SnO/Al memory structure. (b) The proposed physical model to explain the switching mechanism in SnO RS devices for (i) HRS and (ii) LRS state. CF: conducting filaments. Adapted with permission.[352] Copyright 2014, American Institute of Physics.

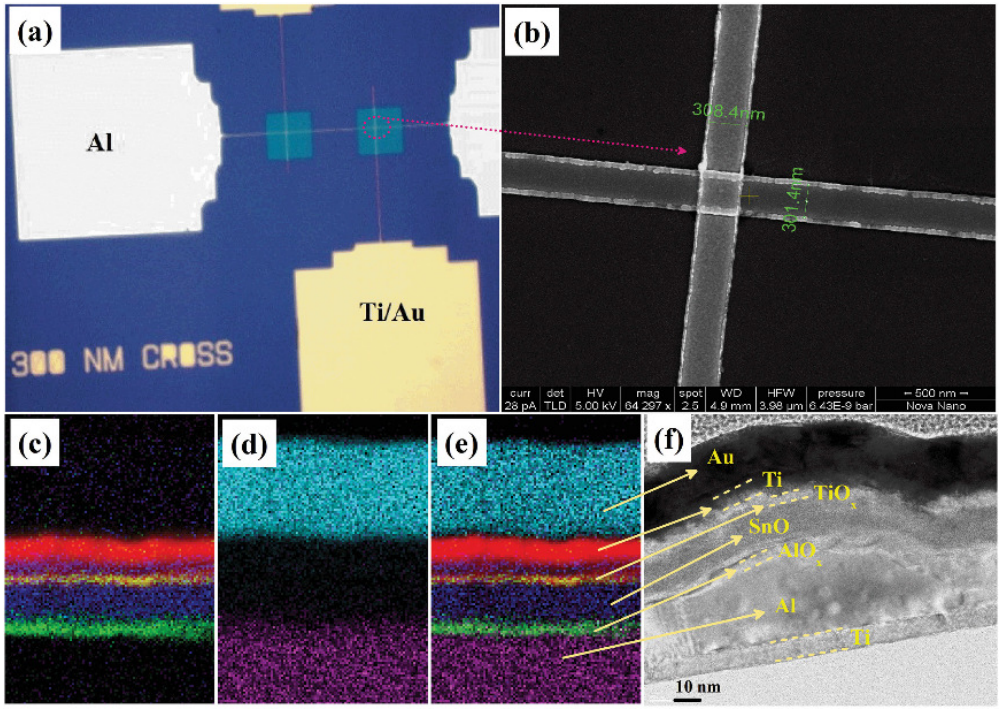

Figure 53. (a) Optical microscopy image of the fabricated device. (b) Scanning electron microscope imaging of a cross-point device structure (top view). (c) EELS, (d) EDS, and (e) EELS + EDS combined mapping of different elements. (f) Corresponding cross-sectional TEM image of the device. Reproduced with permission.[353]

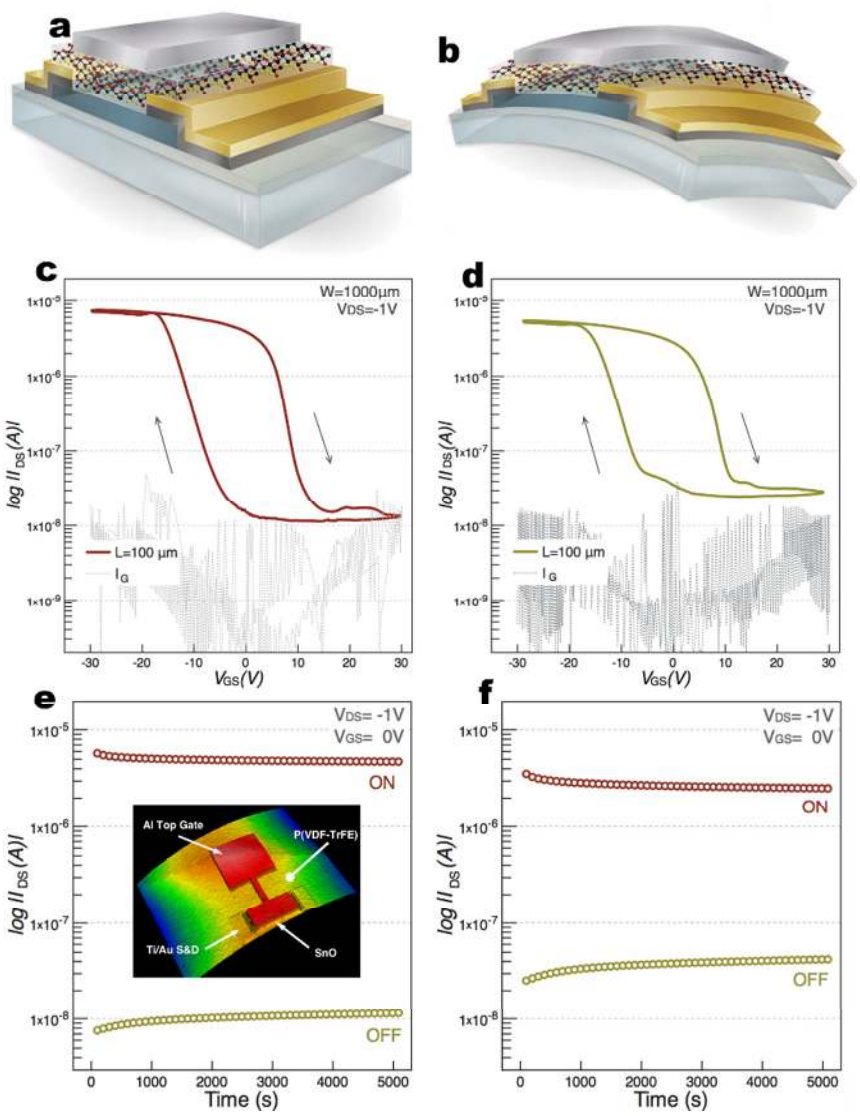

Figure 54. Schematic showing the structure of the devices: (a) on glass substrate, and (b) on polyimide substrate. The specific layers that make the device include (from bottom to top): substrate, 200 nm Si_3N_4 layer, 30 nm SnO active layer, 10 nm Ti/40 nm Au source and drain contacts, 300 nm P(VDF-TrFE) ferroelectric layer and 80 nm Al top gate. FeFET static characteristics, transfer characteristics at V_{DS}= -1 V of the (c) rigid and (d) flexible devices. Retention characteristics of (e) rigid device and (f) flexible device, the ON/OFF states were produced at gate voltages of -30/+30 V with a 1 sec pulse and the retention was measured at zero gate bias condition. The inset of (e) shows the 3D profiler image for device on rigid substrate. Adapted with permission.[198] Copyright 2014, Nature Publishing Group.

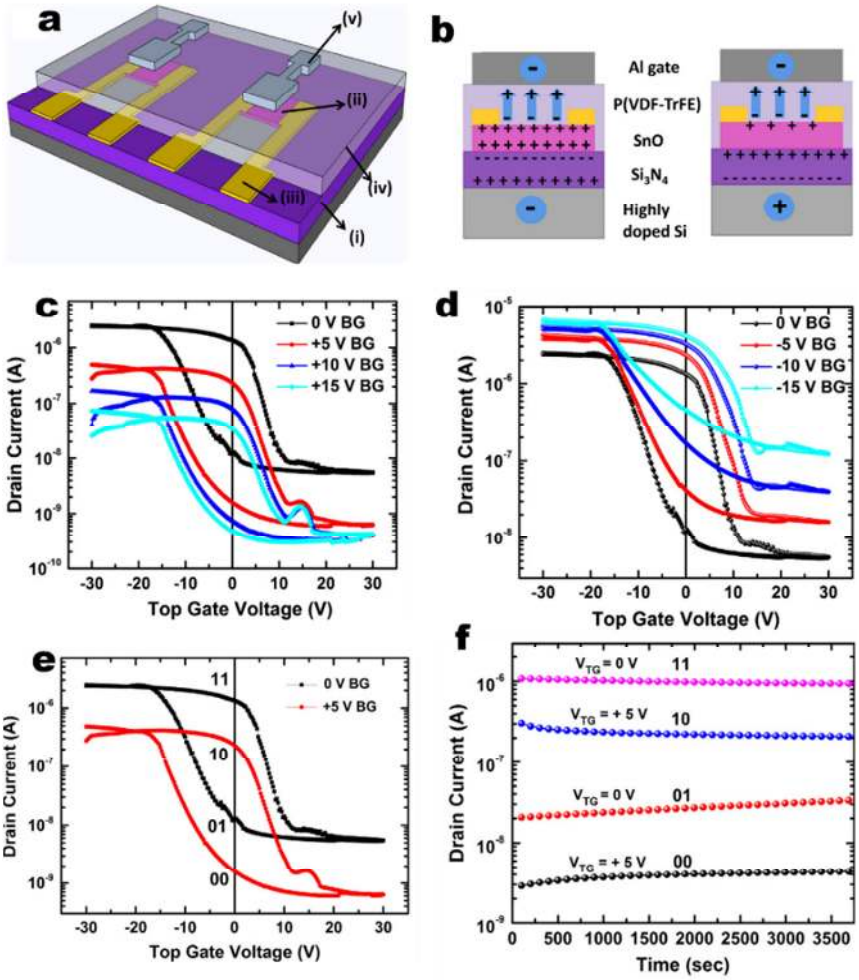

Figure 55. (a) Schematic 3-D cross section of dual gate ferroelectric transistors fabricated on highly doped p-type Si substrates with (i) 200 nm thick Si_3N_4, (ii) 30 nm thick SnO, (iii) 40 nm thick Ti/Au, (iv) 200 nm thick P(VDF-TrFE) and (v) 80 nm thick Al. (b) Illustration showing the charge accumulation and depletion in the SnO channel upon dual gate bias. Figure on left shows the additional accumulation of charges in bottom channel upon negative bottom gate bias. Figure on right shows depletion of charges from both channels upon positive bottom gate bias. Transfer characteristics (I_{DS}-V_{TG}) of the top-gate FeFET in the linear regime at V_{DS} = -1 V with (c) positively biased bottom gate from 0 to +15 V and (d) negatively biased bottom gate from 0 to -15 V. (e) Transfer characteristics (I_{DS}-V_{TG}) of the top gate FeFET in the linear regime at V_{DS} = -1 V with floating bottom gate (0 V) and positively biased bottom gate +5 V. (b) Retention characteristics of the top-gate FeFET i.e. measurement of drain current as a function of time with top gate voltage (V_{BG} = 0 V), drain voltage (V_{DS} = -1 V) and different gate biases to bottom gate (V_{TG} = 0 or 5 V). Adapted with permission.[200] Copyright 2015, Elsevier B.V.

Tables

Table 1. A brief summary of the properties of ternary Cu-bearing oxide or chalcogenide thin films.

Film	Method[a)]	Substrate[b)]	T_{dep}[c)] [°C]	T_{PDA}[c)] [°C]	μ_{Hall} [$cm^2 V^{-1} s^{-1}$]	N_h [cm^{-3}]	T%[d)] [%]	E_{opt}[e)] [eV]	Seebeck [$\mu V K^{-1}$]	σ [$S cm^{-1}$]	E_A[f)] [eV]	Year	Ref
$CuAlO_2$	PLD	(0001) Al_2O_3	700	-	10.4	1.3×10^{17}	60-70	3.50	183	9.5×10^{-2}	0.20	1997	[15]
$SrKCu_2O_2$: K	PLD	Quartz	300	300	0.46	6.1×10^{17}	60	3.25	260	4.8×10^{-2}	0.10	1999	[26]
$CuAlO_2$	PLD	(0001) Al_2O_3	690	690	0.13	2.7×10^{19}	70	3.50	214	3.4×10^{-1}	0.22	2000	[45]
$CuAlO_2$	MOCVD	Quartz	745	-	0.16	1.8×10^{19}	50	3.75	-	2	0.12	2000	[47]
$CuGaO_2$	PLD	(0001) Al_2O_3	700	-	0.23	1.7×10^{18}	80	3.60	560	6.3×10^{-2}	-	2001	[22]
$CuYO_2$: Ca	TE	(001) MgO	500	600	1	-	40-50	3.50	275	~1	-	2001	[53]
$CuCrO_2$: Mg	RFMS	Quartz	600	600	1	-	50	3.10	150	2.2×10^{2}	0.02	2001	[56]
LaCuOS	RFMS	Quartz	RT	800	0.2	2.0×10^{15}	60	3.10	713	6.4×10^{-5}	0.24	2002	[71]
LaCuOSe	R-SPE	(001) MgO	RT	1000	8	2.0×10^{19}	-	-	150	24	-	2003	[69]
$CuAlO_2$	HT	Glass	400	300	3.6	5.4×10^{18}	60	3.75	203	2.4	0.14	2003	[48]
$CuGaO_2$	PLD	(001) YSZ	750	1215	0.8	1.0×10^{18}	-	-	-	1.3×10^{-1}	-	2008	[23]
$CuAlO_2$	RFMS	(0001) Al_2O_3	RT	900	0.4	3.0×10^{18}	-	3.45	-	-	-	2011	[62]
$CuAlO_2$: Mg	SC	(0001) Al_2O_3	RT	900	0.427	7.6×10^{16}	75	3.58	-	5.2×10^{-3}	0.25	2011	[76]
$CuAlO_2$: CuO	RFMS	Si/SiO_2	940	-	39.5	4.3×10^{15}	-	3.79	-	2.7×10^{-2}	0.23	2012	[75]
$Cu_{0.83}AlO_{2.16}$	RFMS	Glass	500	-	0.82	1.5×10^{15}	-	-	-	1.9×10^{-4}	-	2013	[63]
$CuAlO_2$	PLD	(0001) Al_2O_3	650	1000	8.14	2.7×10^{17}	85	3.54	-	6×10^{-2}	-	2014	[77]

The parameters are taken from best Hall mobility sample in these literature reports. [a)]Method: preparation method. (HT: Hydrothermal method; MOCVD: metal organic chemical vapor deposition; PLD: pulsed laser deposition; RFMS: radio frequency magnetron sputtering. R-SPE: reactive solid-phase epitaxy; SC: spin coating; TE: thermal evaporation.); [b)]Substrate: substrate used in Hall measurement. (YSZ: yttria stabilized zirconia); [c)]T_{dep} and T_{PDA}: Substrate temperature during deposition and post deposition annealing process.(RT: room temperature); [d)]T%: average transmittance in the visible range or extended range according to references; [e)]E_{opt}: optical band gap. [f)]E_A : activation energy calculated from the Arrhenius plot.

Table 2. Summary of the properties of binary copper oxide thin films.

Structure [a]	Method [b]	Substrate [c]	T_{dep} [d] [°C]	T_{PDA} [d] [°C]	μ_{Hall} [$cm^2 V^{-1} s^{-1}$]	N_h [cm^{-3}]	T% [e] [%]	E_{opt} [f] [eV]	Year	Ref
Cu_2O (200)	RFMS	Glass	500	-	60	1.0×10^{15}	-	2.00	2000	[120]
ep-Cu_2O	PLD	(100) MgO	700	-	90	1.0×10^{14}	-	-	2008	[82]
Cu_2O (111)	RFMS	Glass	600	-	256	1.0×10^{14}	-	-	2008	[38]
ep-Cu_2O	PLD	(100) MgO	700	-	90	1.0×10^{14}	-	-	2009	[108]
pc-Cu_2O	RFMS	Glass	RT	200	18.5	3.0×10^{13}	85	2.39	2010	[87, 125]
pc-Cu_2O	PLD	Si/SiO_2	500	-	107	-	-	-	2010	[112]
pc-CuO	MOCVD	Glass/ZnO	350	-	35	6.0×10^{14}	-	2.00	2010	[154]
pc-Cu_2O	DCMS	Quartz	797	-	62	2.7×10^{17}	-	-	2011	[123]
pc-Cu_2O	HiTUS	Glass	RT	225	12.5	-	60	2.20	2011	[124]
pc-Cu_2O	RFMS	Si/SiO_2	RT	500	47.5	-	59	2.70	2012	[126]
nc-Cu_2O	MS	-	RT	-	20.2	1.5×10^{16}	-	-	2012	[127]
ep-Cu_2O	PLD	(001) LSAT	700	-	35	-	-	2.40	2012	[114]
pc-Cu_2O	AALD	Glass	225	-	5.3	1.0×10^{16}	55	2.52	2012	[148]
pc-Cu_2O	SC	Glass	RT	450	4.8	1.7×10^{16}	60	2.30	2012	[144]
pc-Cu_2O	SC	Quartz	RT	800	31.7	2.1×10^{14}	-	-	2012	[146]
pc-Cu_2O	TO	Glass/ATO	RT	200	1.9	1.0×10^{16}	47	2.41	2013	[128]
pc-Cu_2O	RFMS	Si/SiO_2	RT	500	47.5	3.0×10^{14}	-	-	2013	[131]
pc-Cu_2O	SC	Si/SiO_2	RT	400/700 [g]	18.9	1.0×10^{15}	-	-	2013	[145]
pc-Cu_2O	DCMS	Si/SiO_2	RT	200	16	1.0×10^{16}	-	-	2013	[133]
a-Cu_2O	RFMS	Quartz	RT	-	0.243	1.92×10^{19}	-	-	2013	[129]
pc-Cu_2O	PEALD	Glass	100	-	37	5.4×10^{14}	-	2.47	2013	[132]
pc-Cu_2O	RFMS	Glass	RT	-	64	1.0×10^{14}	-	2.15	2013	[92]
pc-CuO	RFMS	Glass	RT	-	0.05	1.6×10^{15}	-	-	2014	[135]
pc-CuO	DCMS	Glass	RT	250	4.577	8.9×10^{17}	-	-	2014	[136]
pc-Cu_2O: N	FTS	Glass	RT	-	3.4	2.0×10^{18}	50	2.48	2014	[134]
pc-Cu_2O: Na	TO	-	1015	400-600	100	10^{13}~10^{16}	-	-	2014	[94]
pc-Cu_2O	Mist-CVD	Glass	350	-	0.2	3.3×10^{15}	50	2.20	2014	[155]
pc-CuO	RFMS	Glass	RT	-	6	1.0×10^{15}	-	1.40	2014	[137]
pc-Cu_2O	RFMS	Glass	RT	-	2.11	1.0×10^{17}	-	-	2014	[138]
pc-Cu_2O	PLD	Si/SiO_2	RT	300	2.1	3.0×10^{16}	-	-	2015	[115]

The parameters are taken from best Hall mobility sample in these literature reports. Explanation for column content and abbreviations are given. [a]Structure: crystal structure. (a: amorphous; ep: epitaxial; nc: nano-crystalline; pc: polycrystalline; (200): orientation.); [b]Method: preparation method for Cu_2O (CuO) thin film. (AALD: atmospheric atomic layer deposition; FTS: Facing target sputtering; HiTUS: high target utilization sputtering; MOCVD: metal organic chemical vapor deposition; PEALD: plasma enhanced atomic layer deposition; PLD: pulsed laser deposition; RF(DC)MS: radio frequency (direct current) magnetron sputtering. SC: spin coat; TO: thermal oxidation.); [c]Substrate: substrate used in Hall measurement. (LSAT: single crystal substrate of $(LaAlO_3)_{0.3}$-$(Sr_2AlTaO_6)_{0.7}$.); [d]T_{dep} and T_{PDA}: Substrate temperature during deposition and post deposition annealing process.(RT: room temperature); [e]T%: average transmittance in the visible range or extended range according to references; [f]E_{opt}: optical band gap; [g]Two step annealing: 400 °C in N_2 for 30 min followed by 700 °C in O_2 for 30 min.

Table 3. Summary of several important tin monoxide thin film properties reported recently.

Structure [a]	Method [b]	Substrate [c]	T_{dep} [d] [°C]	T_{PDA} [d] [°C]	μ_{Hall} [$cm^2 V^{-1} s^{-1}$]	N_h [cm^{-3}]	T % [e] [%]	E_g (dir.) [f] [eV]	E_g (ind.) [f] [eV]	Year	Ref
ep-SnO (*001*)	PLD	(001) YSZ	575	200	2.4	2.5×10^{17}	-	2.70	0.7	2009	[8, 9]
nc-SnO	EBE	Si/SiO_2	RT	-	2.6	5.0×10^{18}	70	2.97	-	2010	[170]
pc-SnO	TE	Si/SiO_2	RT	310	2.83	5.0×10^{17}	70	-	-	2010	[214]
pc-SnO	EBE	SiO_2	RT	600	1.4	2.8×10^{16}	70	2.77	-	2010	[171]
pc-SnO	EBE	Si/SiO_2	RT	400	1.6	1.0×10^{18}	-	-	-	2010	[36]
pc-SnO	RFMS	Glass	RT	200	4.8	10^{16}~10^{18}	85	-	-	2010	[6, 7]
pc-SnO	RFMS	Si	RT	300	0.6	$2\sim9\times10^{17}$	-	-	-	2010	[37]
ep-SnO (*001*)	PLD	(001) YSZ	550	-	2.4	2.5×10^{17}	-	-	-	2010	[177]
pc-SnO	PLD	Si/SiO_2	RT	250	1.9	1×10^{17}	-	-	-	2011	[173]
pc-SnO	RFMS	SiO_2	60	-	0.5	1×10^{19}	-	2.85	0.7	2011	[182]
pc-SnO	RFMS	BS-Glass	300	-	1.2	2.6×10^{17}	-	2.43	-	2012	[183]
pc-SnO	EBE	Si/SiO_2	RT	350	3.9	5.6×10^{15}	60	2.70		2012	[176]
pc-SnO	RFMS	BS-Glass	300	-	1.7	1.4×10^{17}	-	-	-	2012	[184]
pc-SnO	RFMS	SiO_2	RT	200	1.3	6.0×10^{18}	70	2.70	-	2012	[168]
pc-SnO	RFMS	Glass	RT	300	1.2	1.2×10^{17}	50	2.80	-	2013	[185]
pc-SnO	DCMS	Si/SiO_2	RT	180	18.7	2.18×10^{17}	92	2.65	-	2013	[167]
pc-SnO	RFMS	Si/SiO_2	RT	250	3	1.0×10^{18}	70	2.78		2013	[186]
pc-SnO	RFMS	Glass	RT	500	0.64	4.3×10^{17}	-	-	-	2013	[187]
SnO	PLD	(001) YSZ	575	-	7	1×10^{17}	-	2.60	0.7	2013	[178]
nc-SnO	RFMS	BS-Glass	100	-	0.02	1.47×10^{19}	-	-	-	2013	[188]
ep-SnO (*001*)	PLD	(001) YSZ	200	-	2.3	1×10^{17}	40	2.80	-	2014	[180]
nc-SnO	RFMS	Glass	100	300	0.13	7.3×10^{18}	90	5.95	-	2014	[189]
pc-SnO	RFMS	Glass	RT	300	3	7.22×10^{16}	-	2.71	-	2014	[190]
pc-SnO	PLD	Glass	RT	300	1.8	1.0×10^{19}	-	2.70	0.7	2014	[21]
pc-SnO	RFMS	Si/SiO_2	RT	200	1.4	7×10^{17}	-	-	-	2014	[191]
pc-SnO	RFMS	SiO_2	200	-	3.34	2.3×10^{18}	60	-	-	2014	[192]
pc-SnO	ALD	Si/SiO_2	210	-	2.9	3.4×10^{17}	60	2.60	-	2014	[218]
pc-SnO	RFMS	Glass	RT	265	0.78	4.28×10^{17}	40	2.83	-	2014	[193]
pc-SnO (*001*)	PLD	Si/SiO_2	500	-	2	9.0×10^{16}	-	2.68	-	2015	[181]

The parameters are taken from best Hall mobility sample in these literature reports. Explanation for column content and abbreviations in respective column. [a]Structure: crystal structure of SnO. (ep: epitaxial; nc: nano-crystalline; pc: polycrystalline.); [b]Method: preparation method for SnO thin film. (ALD: atomic layer deposition; EBE: electron beam evaporation; PLD: pulsed laser deposition; RF(DC)MS: radio frequency (direct current) magnetron sputtering. TE: thermal evaporation.); [c]Substrate: substrate used in Hall measurement. (BS-Glass: borosilicate glass; YSZ: yttria stabilized zirconia; SiO_2: quartz.); [d]T_{Dep} and T_{PDA}: Substrate temperature during deposition and post deposition annealing process. (RT: room temperature); [e]T%: average transmittance in the visible range or extended range according to references; [f]E_g (dir.) and E_g (ind.): direct and indirect band gap.

Table 4. Summary of the performance of thin-film transistors (TFTs) fabricated using p-type binary copper oxide channel layers.

Type[a)]	Ch.[b)]	Method[c)]	Subs./Diel.[d)]	S&D cont.[e)]	$d_{Ch.}$[f)]	$d_{diele.}$[f)]	V_{th}	V_{on}	T_{dep}[g)]	T_{PDA}/Atm/ PDA time[g)]	μ_{FE}	μ_{Sat}	μ_{Hall}	I_{on}/I_{off}	SS	Yr[h)]	Ref
	(Ch/d/S&D)				[nm]		[V]		[°C]	[°C/-/min]	[$cm^2 V^{-1} s^{-1}$]				[V dec^{-1}]	20-	
C-TG, u	ep-Cu_2O	PLD/PLD/EBE	(100) MgO/AlO_x	Au	100	150	-	-	700	-	0.26	-	90	6.0	-	08	[82]
C-TG, u	ep-Cu_2O	PLD/PLD/EBE	(100) MgO/AlO_x	Au	100	150	-	-	700	-	0.08	-	90	3.0	-	09	[108]
S-BG	pc-Cu_2O NW	-/TO/-	Si/SiO_2	Au	50~100	200	15	32	-	-	95	-	-	1.0×10^6	-	09	[304]
S-BG	pc-Cu_2O	RFMS/-/RFMS	Glass/ATO	IZO	40	220	-12	10	RT	200/Air/600	1.2×10^{-3}	-	18.5	2.0×10^2	-	10	[87]
C-TG, u	pc-Cu_2O	PLD/PLD/RFMS	Si/HfON	Pt	120	20	-0.8	0.5	500	-	-	4.3	107	3.0×10^6	0.18	10	[112]
S-BG	pc-CuO	RFMS/TO/EBE	Si/SiO_2	Ni	75	100	-	12	RT	300/Air/-	0.4	-	-	1.0×10^4	-	10	[121]
S-BG	pc-Cu_2O NW	TO/-/EBE	-	Pt	-	-	0.7	-1	-	-	-	26.3	-	1.0×10^4	-	11	[310]
S-BG, u	pc-Cu_2O	PLD/PLD/EBE	Si/[SiO_2 /HfO_2]	Pt	40	10/100	0.3	0.5	500	-	-	2.7	-	1.5×10^6	0.137	11	[113]
S-BG	-	RFMS/ALD/EBE	PES/ Al_2O_3	Ni	10	75	-4.75	-2	RT	150/O_2/30	-	2.2×10^{-3}	-	3.9×10^2	-	11	[122]
S-BG	pc-Cu_2O	RFMS/-/RFMS	Glass/ATO	IZO	40	220	-	7	RT	200/Air/60	7×10^{-3}	-	18.47	1.0×10^3	-	12	[125]
S-BG	pc-Cu_2O	RFMS/TO/EBE	Si/SiO_2	Ni	45	100	-6.7	3	RT	500/Vac/7[i)]	0.06	-	47.5	1.8×10^4	1.6	12	[126]
S-BG, u	nc-Cu_2O	MS/MS/EBE	PET/AlN	Au	-	100	-4	4	RT		2.4	-	20.2	4.0×10^4	-	12	[127]
S-BG	pc-Cu_2O	TO/-/EBE	Glass/ATO	Ni	40	220	-	7	RT	200/Air/60	1.56×10^{-3}	-	1.9	6.0×10^1	-	13	[128]
S-BG	pc-Cu_2O	RFMS/TO/EBE	Si/SiO_2	Ni	40	100	-6	6	RT	800/Vac/20 s, RTA	0.06	-	-	1.0×10^4	3	13	[130]
S-BG	pc-Cu_2O	RFMS/TO/EBE	Si/SiO_2	Ni	45	100	-7.5	0	RT	500/Vac/7[i)]	0.07	-	47.5	1.1×10^4	2.7	13	[131]
S-BG	pc-Cu_2O	SP/TO/EBE	Si/SiO_2	Ni	100	200	-	-	RT	400/N_2/30 700/O_2/30[i)]	0.16	-	18.9	1.0×10^2	-	13	[145]
S-BG	pc-Cu_2O	RFMS/TO/EBE	Si/SiO_2	Ni	45	100	-11.6	0	RT	800/-/20s RTA	0.05	-	-	1.0×10^4	3.3	13	[132]
C-BG, u	pc-Cu_2O	SprayC/TO/-	Si/SiO_2	Au	40	200	-70	-	RT	200/-/720	3×10^{-4}	-	-	4.0×10^3	30	13	[151]
C-BG	CuO NPs	InkP/TO/EBE	Si/SiO_2	Ag	-	300	0.8	-	100	-/MAA/2	31.2	-	-	7.0×10^3	-	13	[156]
S-BG	pc-Cu_2O	DCMS/PLD/EBE	Si/STO	Pt	30	150	-0.62	-0.1	RT	200/Air/180	0.54	-	16	4.4×10^1	1.64	13	[133]
S-BG, u	pc-CuO	RFMS/-/TE	Glass/ATO	Au	12	200	-15.1	3	RT	-	1.4×10^{-2}	-	0.05	1.0×10^4	3.3	14	[135]
S-BG	pc-CuO	DCMS/-/DCMS	Glass/HfO_2	Ni	40	60	-	-5	RT	250/Air/60	-	5×10^{-3}	4.577	1.0×10^2	-	14	[136]
S-BG	pc-Cu_2O	PLD/TO/EBE	Si/SiO_2	Ti	40	150	-	10	RT	300/N_2, O_2/60	6×10^{-4}	-	2.1	1.0×10^3	-	15	[115]

The parameters are taken from best performing devices in respective literature report(s). Explanation for column content and abbreviations in respective column. [a)]Type: TFT structure. (S: staggered; C: coplanar; BG: bottom gate; TG: top gate; u: unpatterned channel.); [b)]Ch.: channel phase. (ep: epitaxial; nc: nano-crystalline; pc: polycrystalline; NPs: nanoparticles; NW: nanowire.); [c)]Method: preparation method for the channel (ch), dielectric (d) and source & drain electrodes (S&D). (ALD: atomic layer deposition; EBE: electron beam evaporation; InkP: ink-printing; PLD: pulsed laser deposition; RF(DC)MS: radio frequency (direct current) magnetron sputtering; SP: solution process, spin coating; SprayC: spray coating; TE: thermal evaporation; TO: thermal oxidation.); [d)]Subs./Diel.: substrate and dielectric materials. For

substrates: PES: Polyethersulfone. PET: Polyethylene terephthalate. For dielectric materials: ATO: superlattice of TiO_2 and Al_2O_3; [e]S&D cont.: S&D materials that directly contact to channel. (IZO: indium zinc oxide); [f]d_{Ch} and $d_{diele.}$: thickness of channel and dielectric materials; [g]T_{dep}: substrate temperature during deposition. (RT: room temperature) T_{PDA}/Atm/ PDA time: post deposition annealing temperature/annealing atmosphere/annealing time. (RTA: rapid thermal treatment; MAA: microwave assisted annealing.); [h]Yr: year of publication; [i]Two step annealing: 400 ^oC in N_2 for 30 min followed by 700 ^oC in O_2 for 30 min; [j]Annealing performed at sputtering chamber.

Table 5 Summary of the performance of thin-film transistors (TFTs) fabricated using p-type tin monoxide channel layers.

Type [a]	Ch. [b]	Method [c]	Subs./Diel. [d]	S&D cont. [e]	$d_{Ch.}$ [f]	$d_{diele.}$ [f]	V_{th}	V_{on}	T_{dep} [g]	T_{PDA}/Atm/ PDA time [g]	μ_{FE}	μ_{Sat}	μ_{Hall}	I_{on}/I_{off}	SS	Yr [h]	Ref
		(Ch/d/S&D)			[nm]		[V]		[°C]	[°C/-/min]		[$cm^2 V^{-1} s^{-1}$]			[V dec^{-1}]	20-	
S-BG, u	a-SnO_x	TE/-/TE	Si/SiO_2	Ag	7.5	-	30.4	-	-	100/-/60	-	0.011	-	1.0×10^3	2	08	[212]
S-BG, u	a-SnO_x	TE/-/TE	Si/SiO_2	Ag	7.5	300	30	-	100	100/-/60	-	4.7×10^{-3}	-	2.5×10^2	-	08	[211]
C-TG, u	ep-SnO (*00l*)	PLD/PLD/EBE	(001) YSZ/Al_2O_3	Ni	20	210	4.8	-	575	-	1.3	0.7	2.4	1.0×10^2	-	08	[8]
C-TG, u	ep-SnO (*00l*)	PLD/PLD/EBE	(001) YSZ/Al_2O_3	Ni	20	210	5	-	575	-	1.3	0.7	2.4	1.0×10^2	7	09	[9]
C-BG	pc-SnO	TE/TO/RFMS	Si/SiO_2	ITO	100	2000	-	-6	RT	310/Ar/60	-	4×10^{-5}	2.83	1.0×10^2	-	10	[214]
S-BG, u	pc-SnO	EBE/TO/EBE	Si/SiO_2	Ni	100	190	-3.5	1	RT	400/Ar/10 RTA	0.87	0.46	1.6	2.0×10^2	11	10	[36]
S-BG	pc-SnO	RFMS/-/EBE	Glass/ATO	Ti	30	220	-5	-	RT	200/Air/60	1.2	-	4.8	1.0×10^3	-	10	[7]
S-BG	pc-SnO	RFMS/PECVD/-	Si/SiN_x	Pt	50	500	30	-	RT	300/N_2/120	0.24	-	0.6	1.0×10^2	-	10	[37]
S-BG	pc-SnO	RFMS/-/EBE	Paper/Paper	Ni	8	-	1.5	-	RT	150/Air/60	-	1.3	-	1.0×10^2	6.9	11	[13]
S-BG	pc-SnO	PLD/TO/PLD	Si/SiO_2	ITO	15	15	-3.1	2	RT	250/Air/30	0.48	0.78	1.25	1.0×10^4	1.9	11	[173]
S-BG	pc-SnO	RFMS/-/EBE	Glass/ATO	Ni	-	-	-	-	RT	200/-/- RTA	-	4.6	-	7.0×10^4	-	11	[6]
S-BG	pc-SnO (*00l*)	EBE/TO/EBE	Si/SiO_2	Ni	40	106	-	1	RT	400/Ar/10 RTA	0.32	-	-	4.9×10^2	-	12	[175]
S-BG, u	pc-SnO	SC/TO/TE	Si/SiO_2	Ni	17	200	-1.9	-	RT	450/N_2,H_2/120	-	0.13	-	8.5×10^1	-	12	[315]
S-BG	pc-SnO	EBE/TO/EBE	Si/SiO_2	Ti	50	190	-20.5	-7	RT	350/Vac/180	-	0.16	3.9	9.0×10^1	-	12	[176]
S-BG	pc-SnO	EBE/TO/EBE	Si/SiO_2	Ni	40	106	-	1	RT	400/Ar/10 RTA	0.32	0.16	-	-	-	12	[179]
S-BG	pc-SnO	RFMS/-/EBE	Paper/Paper	Ti	8	-	1.4	-	RT	150/-/30	-	1.3	-	1.0×10^2	6.9	13	[14]
S-BG	pc-SnO	DCMS/ALD/EBE	Glass/HfO_2	Ti	15	220	-1	-	RT	180/Air/30	6.75	-	18.7	6.0×10^3	7.63	13	[167]
S-BG	pc-SnO	RFMS/TO/EBE	Si/SiO_2	Ni	25	200	-	-	RT	250/Vac/60 RTA	1.8	-	3	1.3×10^3	-	13	[186]
S-BG	pc-SnO	DCMS/-/EBE	Glass/ATO	Ni	15	220	-5.2	8	RT	200/Air/30	0.66	-	-	3.0×10^2	8.4	13	[196]
S-BG	pc-SnO	DCMS/ALD/EBE	Glass/HfO_2	Ti	15	220	-1.06	2	RT	160/Air/30	10.83	-	-	1.0×10^3	0.76	13	[195]

S-BG	pc-SnO	RFMS/ALD/EBE	Glass/HfO_2	ITO	30	50	2.5	7	RT	250/Air/60	2.14	-	-	1.0×10^3	2	14	[206]
S-BG	pc-SnO	RFMS/TO/EBE	Si/SiO_2	Ni	10	17	-1.1	3	100	-	1.2	-	-	1.2×10^4	-	14	[208]
S-BG	pc-SnO	RFMS/TO/EBE	Si/SiO_2	Ni	25	100	3.6	24	90	230/Air/60	0.59	-	-	3.1×10^3	9.1	14	[209]
S-BG	a-SnO_x	TE/TO/TE	Si/SiO_2	Ag	50	1000	-4.81	-	RT	300/N_2/120[j]	5.59	-	-	1.0×10^2	28.6	14	[216]
S-BG, u	pc-SnO	DCMS/ALD/EBE	Si/Al_2O_3	Ti	15	120	2.5	-	RT	210/Air/30	0.42	-	-	1.0×10^3	-	14	[198]
C-TG	pc-SnO	DCMS/SC/EBE	Glass/P(VDF-TrFE)	Ti	30	300	-11.6	-	RT	200/Air/30	3.3	-	-	2.5×10^2	4.29	14	[198]
S-BG	pc-SnO	RFMS/TO/EBE	Si/SiO_2	Mo	30	200	-	-	RT	260/Vac/60 RTA	0.43	-	3	6.7×10^2	-	14	[190]
S-BG, u	pc-SnO (*001*)	PLD/TO/EBE	Si/SiO_2	Ni	30	150	-	-	RT	300/-/60 [j]	2.18	-	1.8	-	-	14	[21]
S-BG	pc-SnO	RFMS/PECVD/EBE	Si/SiO_x	Ni	10	150	-2.3	0	90	-	4.86	-	-	3.0×10^4	0.7	14	[205]
S-BG	pc-SnO	RFMS/TO/EBE	Si/SiO_2	Ni	24	105	32.5	-	RT	200/Air/120	1.36	0.67	1.4	1.6×10^3	-	14	[191]
C-TG	pc-SnO	DCMS/SC/EBE	Si/P(VDF-TrFE)	Ti	30	200	-	-	RT	200/Air/30	2.7	-	-	2.2×10^2	4	14	[200]
S-BG	pc-SnO	RFMS/ALD/EBE	Glass/HfO_2	ITO	15	50	3.5	10	RT	225/Air/30	0.33	-	-	1.0×10^3	2.5	14	[210]
S-BG	pc-SnO	RFMS/TO/EBE	Si/SiO_2	Ni	10	35	4.1	10	RT	200/-/100s RTA	1.2	1.1	-	2.5×10^4	1.1	14	[204]
S-BG, u	pc-SnO (*001*)	PLD/TO/EBE	Si/SiO_2	Ti	20	150	-6.3	-	500	-	0.34	-	~2	2.7×10^2	47.6	15	[181]
S-BG	pc-SnO	DCMS/-/EBE	Glass/ATO	Ti	10	220	0.87	-	RT	190/Air/30	2.39	-	-	1.0×10^3	7.5	15	[199]
S-BG	pc-SnO	RFMS/TO/EBE	Si/SiO_2	Ni	10	35	0.24	5	RT	250/-/100s RTA	1.8	-	-	1.0×10^5	0.55	15	[207]

The parameters are taken from best performing devices in respective literature report(s). Explanation for column content and abbreviations in respective column. [a)]Type: TFT structure. (S: staggered; C: coplanar; BG: bottom gate; TG: top gate; u: unpatterned channel.); [b)]Ch.: channel phase. (a: amorphous; ep: epitaxial; pc: polycrystalline; (*00l*): orientation.); [c)]Method: preparation method for the channel (ch), dielectric (d) and source & drain electrodes (S&D). (ALD: atomic layer deposition; EBE: electron beam evaporation; PECVD: plasma enhanced chemical vapor deposition; PLD: pulsed laser deposition; RF(DC)MS: radio frequency (direct current) magnetron sputtering; SC: spin coating; TE: thermal evaporation; TO: Thermal oxidization.); [d)]Subs./Diel.: substrate and dielectric materials. For substrates: YSZ: yttria stabilized zirconia. For dielectric materials: ATO: superlattice of TiO_2 and Al_2O_3; P(VDF-trFE): poly vinylidenefluoride-co-trifluoroethylene; [e)]S&D cont.: S&D materials that directly contact to channel. (ITO: indium tin oxide.); [f)]d_{Ch} and d_{diele}. : thickness of channel and dielectric materials; [g)]T_{dep}: substrate temperature during deposition. (RT: room temperature) T_{PDA}/Atm/PDA time: post deposition annealing temperature/annealing atmosphere/annealing time. (RTA: rapid thermal treatment); [h)]Yr: year of publication; [i)]O_2 plasma by ICP for 1h before annealing; [j)]In-situ annealing at 1×10^{-5} Pa, without air exposure between deposition and PDA.

Table 6. Summary of the performance of CMOS inverters fabricated using p-type tin monoxide and various n-type channel layers.

Channel[a]		Mobility		Geometry	Gain	$\|V_{DD}\|$	NM_H[b]	NM_L[b]	Method[c]	Subs./Diele.[d]	Year	Ref
p	n	p	n	$(W/L)_p/(W/L)_n$								
		[cm^2 V^{-1} s^{-1}]				[V]						
SnO_x	SnO_x	0.011	-	-	2.8	80	-	-	TE	Si/SiO_2	2008	[212]
SnO_x	In_2O_3	0.0047	0.054	-	11	100	-	-	TE	Si/SiO_2	2008	[211]
SnO	SnO	0.78	0.0011	1	2.4[e]	5	-	-	PLD	Si/SiO_2	2011	[173]
SnO	GIZO	1.3	23	2.08	4.5	15	9.8	1	RFMS	Paper/Paper	2011	[13, 14]
SnO	SnO	0.32	1.02	1	30.6[e]	40	18.1	7.8	EBE	Si/SiO_2	2012	[175, 179]
SnO	SnO_2	0.42	0.52	1	3	10	-	-	DCMS	Si/Al_2O_3	2014	[198]
SnO	ZnO	0.33	3.5	5	17	10	4.29	4.35	RFMS	Glass/HfO_2	2014	[210]
SnO	SnO_2[f]	2.39	0.23	0.05	4	10	-	-	DCMS	Glass/ATO	2015	[199]

The parameters are taken from best performing inverter in respective report(s). Explanation for column content and abbreviations in respective column. [a]Channel: semiconductor materials used in p and n channels. (GIZO: gallium-indium-zinc-oxide); [b]NM_H and NM_L: high and low noise margin; [c]Method: preparation method for p-channel. (EBE: electron beam evaporation; PLD: pulsed laser deposition; RF(DC)MS: radio frequency (direct current) magnetron sputtering; TE: thermal evaporation.); [d]Subs./Diele.: substrate and dielectric materials. (ATO: superlattice of TiO_2 and Al_2O_3); [e]CMOS Inverter built by SnO based ambipolar TFT; [f]SnO/Cu_2O bilayer for n-channel.

Table 7. Summary of the performance of p-n junction diodes fabricated using p-type ternary Cu-bearing oxides or chalcogenides in combination with various n-type oxide semiconductors.

Materials		Method[a]	T_{dep}[b]	Substrate[c]	μ_{Hall}	N_h	V_{knee}	I_f/I_r	Range[d]	*n*	Year	Ref
p	n		[°C]		[cm^2 V^{-1} s^{-1}]	[cm^{-3}]	[V]		[V]			
$SrCu_2O_2$	ZnO	TE	350	Glass/PI	-	1×10^{17}	0.3-0.6	80	±1.5	1.62	1999	[65]
$SrCu_2O_2$: K	ZnO	PLD	350	(111) YSZ	-	1×10^{18}	1	-	±3	-	2000	[28]
$SrCu_2O_2$: K	ZnO	PLD	350	(111) YSZ	-	5×10^{17}	1.5	-	-	-	2000	[27]
$SrCu_2O_2$: K	ZnO	PLD	350/600	(111) YSZ	-	5×10^{17}	3	-	±5	-	2001	[29]
$CuYO_2$: Ca	ZnO: Al	TE	100	Glass	~1	-	0.4-0.8	190	±3	-	2001	[53]
$CuInO_2$: Ca	$CuInO_2$: Sn	PLD	600	(111) YSZ	-	-	1.8	10	±4	-	2002	[24]
$CuAlO_2$	ZnO	PLD	400	Glass	-	-	0.5	90	±1.5	-	2003	[337]
LaCuOSe	a-GIZO	R-SPE	RT[d]	(001) MgO	8	1×10^{19}	6	10	±8	-	2005	[336]
$SrCu_2O_2$: Ca	ZnO: Al	PLD	350	Quartz	-	-	0.3-0.6	-	±2.5	-	2006	[335]

Explanation for column content and abbreviations in respective column. [a)]Method: preparation method for p-channel. (PLD: pulsed laser deposition; R-SPE: reactive solid-phase epitaxy; TE: thermal evaporation.); [b)]T_{dep}: deposition temperature for p-type semiconductor. (RT: room temperature); [c)]Substrates used in building diode devices. (PI: polyimide; YSZ: yttria-stabilized zirconia.); [d)]Range: applied voltage sweeping range.

Table 8. Summary of the performance of p-n junction diodes fabricated using p-type binary copper oxides in combination with various n-type oxide semiconductors.

Materials		Method[a)]	T_{dep}[b)]	Substrate[c)]	μ_{Hall}	N_h	I_f/I_r	Range[d)]	*n*	V_{knee}	Year	Ref
p	n		[°C]		[$cm^2 V^{-1} s^{-1}$]	[cm^{-3}]		[V]		[V]		
Cu_2O	ZnO	MOCVD	350	Glass	-	-	-	±3	-	0.5-1	2009	[338]
Cu_2O	ZnO	ED	100	Glass	-	-	-	±2	4.3	0.9	2013	[91]
Cu_2O	ZnO	PEALD	100	PET	37	5.4×10^{14}	-	±2	-	1.2	2013	[132]
CuO	ZnO	RFMS	RT	Glass	1.3	1×10^{18}	450	±1.25	-	0.66	2013	[92]
Cu_2O	GIZO	RFMS	RT	PEN	2.11	1.02×10^{17}	3.4×10^{4}	±1.2	1.4	44	2014	[138]
Cu_2O	GIZO	DCMS	RT	Glass	-	-	40	±3	-	2	2014	[340]
Cu_2O	ZnO	Sol-Gel	RT	Glass	-	-	487	±7	-	2	2014	[341]

Explanation for column content and abbreviations in respective column. [a)]Method: preparation method for p-channel. (ED: electrodeposition; MOCVD: metal organic chemical vapor deposition; PEALD: plasma enhanced atomic layer deposition; RF(DC)MS: radio frequency (direct current) magnetron sputtering.); [b)]T_{dep}: deposition temperature for p-type copper oxides; [c)]Substrates (PET: polyethylene terephthalate; PEN: polyethylene naphthalate); [d)]Range: applied voltage sweeping range.

Table 9. Summary of the performance of p-n junction diodes fabricated using p-type tin monoxide in combination with various n-type oxide semiconductors.

Materials		Method[a)]	T_{dep}[b)]	Substrate[c)]	μ_{Hall}	N_h	I_f/I_r	Range[d)]	*n*	V_{knee}	year	Ref
p	n		[°C]		[$cm^2 V^{-1} s^{-1}$]	[cm^{-3}]		[V]		[V]		
SnO	SnO:Sb	PLD	550	(001) YSZ	2.4	2.5×10^{17}	-	±2.2	-	0.7	2011	[177]
SnO	ZnO	RFMS	RT	Glass	-	2×10^{18}	12	±4.5	11.2	3	2013	[185]
SnO	SnO_2	TE	300	Glass	-	-	-	±10	21.5	3.5	2014	[346]
SnO	SnO_2	RFMS	100	Glass	0.13	7.3×10^{18}	-	±7	-	2.3	2014	[189]
SnO	Si	EBE	RT	Si	-	1×10^{17}	58	±2	5.5	1.1	2015	[217]
SnO	SnO_2:Sb	RFMS	200	(100) SiO_2	3.34	2.3×10^{18}	510	±6	6.4	2.9	2015	[192]
SnO	SnO_2	DCMS	RT	Glass	5.27	1.9×10^{17}	10^3	±3	3.39	3.27	2015	[347]

Explanation for column content and abbreviations in respective column. [a)]Method: preparation method for p-channel. (EBE: electron beam evaporation; PLD: pulsed laser deposition; DC/RFMS: direct current/radio frequency magnetron sputtering; TE: thermal evaporation.); [b)]T_{dep}: deposition temperature for p-type SnO. (RT: room temperature); [c)]Substrates (YSZ: yttria-stabilized zirconia); [d)]Range: applied voltage sweeping range.

Table 10. Summary of the performance of p-n junction diodes fabricated using p-type spinel oxides in combination with various n-type oxide semiconductors.

Materials[a]		Method[b]	T_{dep}	Substrate [c]	μ_{Hall}	N_h	V_{knee}	I_f/I_r	Range[d]	*n*	Year	Ref
p	n		[°C]		[$cm^2 V^{-1} s^{-1}$]	[cm^{-3}]	[V]		[V]			
a-$ZnRh_2O_4$	a-GIZO	RFMS	RT	Quartz/ Polyester	0.09	-	2.1	1×10^3	±5	2.3	2003	[226, 228]
ep-$ZnRh_2O_4$	ZnO	R-SPE	RT	(111) YSZ	-	-	2	-	±5	-	2003	[227]
a-$ZnCo_2O_4$	a-GIZO	PLD	RT	(0001) Al_2O_3	1	2×10^{17}	2.5	1×10^2	±7	-	2010	[231]
$ZnCo_2O_4$	ZnO	PLD	RT	Al_2O_3	-	-	-	1.2×10^8	±2	-	2012	[232]
a- $ZnCo_2O_4$	ZnO	PLD	RT	Al_2O_3	0.01~0.06	$0.5\sim2\times10^{21}$	-	2×10^{10}	±2	2.04	2014	[234]
a- $ZnCo_2O_4$	a-ZTO	PLD	RT	Glass	-	-	-	4×10^6	±1.6	2	2015	[235]
$ZnCo_2O_4$	In_2O_3: Mg	PLD	RT	(001) YSZ	-	-	-	1×10^3	±1	2	2015	[236]

[a]a: amorphous, ep: epitaxial; [b] deposition method for p-type semiconductors. (PLD: pulsed laser deposition; RFMS: radio frequency magnetron sputtering; R-SPE: reactive solid phase epitaxy.); [c]Substrates (YSZ: yttria-stabilized zirconia); [d]Range: applied voltage sweeping range.

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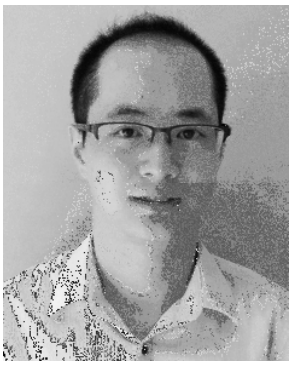

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TOC Entry

Recent progress in hole-transporting (p-type) oxide materials and devices is reviewed. Material design strategies to improve the transport properties of five classes of oxides are discussed, including ternary Cu-bearing oxides, binary copper oxides, tin monoxide, spinel oxides and nickel oxides. In addition, performance of semiconductor electronic devices based on p-type oxides is reviewed including thin-film transistors, CMOS inverters, p-n junction diodes, memory devices, gas sensors, and electrochromics. The recent successes and the hurdles that stand in the way of commercial adoption of p-type semiconductors are discussed.

Keyword: p-type oxides, transparent electronics, thin-film transistors, oxide diodes, oxide CMOS

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Recent Developments in p-type Oxide Semiconductor Materials and Devices

ToC figure