# Recent trends in bias temperature instability

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Several trends occurring in the past few years in our understanding of bias temperature instability (BTI) are reviewed. Among the most important is the shift toward analyzing BTI relaxation with the tools originally developed for describing low-frequency noise. This includes the interpretation of the time, temperature, voltage, and duty cycle dependences. It is shown that a wealth of information about gate oxide defect properties can be obtained from deeply scaled devices and correctly modeled based on nonradiative multiphonon theory. It is then shown how detailed understanding of individual defect properties can allow interpreting the variability issues of future complementary metal-oxide semiconductor technologies. This is complemented by showing the most promising technological solutions for BTI. © *2011 American Vacuum Society.* [DOI: 10.1116/1.3521505]

## I. INTRODUCTION

Among the critical reliability issues facing present and future deeply downscaled complementary metal-oxide semiconductor (CMOS) devices is the so-called bias temperature instability (BTI). While BTI in n-channel field effect transistor (nFET) devices was generally ascribed to charge trapping in (the high-*k* portion of) the gate oxide, the interpretation of BTI in p-channel FET (pFET) devices still generates controversy.[1–3] Although in the past often relegated to a secondary issue, we have long argued that central to the correct understanding of BTI is the interpretation of the so-called BTI recovery.[4–7] This phenomenon in pFET devices has been previously described by backdiffusion of hydrogen into substrate/gate oxide interface states.[8] The so-called reaction-diffusion model based on this assumption is still popular, especially in the design community,[9] despite being inconsistent with some crucial observations.[10]

One of the most intriguing properties of BTI relaxation is the lack of its characteristic time scale, especially in pFETs, suggesting some type of *dispersion* in the underlying mechanism.[5,7,11] In CMOS technologies, a response on many time scales is typical for low-frequency noise [and its manifestation as random telegraph noise (RTN) in deeply scaled devices], suggesting that BTI recovery is, in fact, caused by the same defects.[12,13] This connection is crucial for most arguments presented in this article.[14]

We start by briefly reviewing the elementary definitions and experimental observations of BTI and proceed to develop the link between BTI recovery and low-frequency noise. We then show that many properties of gate oxide defects can be directly extracted from BTI relaxation measurements in deeply scaled devices and review the noise-inspired model capable to fully describe these properties. Afterward we show how the understanding of gate oxide defect properties can be used to explain variability of BTI in deeply scaled technologies as well as possible technological solutions for both nFETs and pFETs.

## II. BRIEF OVERVIEW OF BTI

BTI is a consequence of charging of defect states in the gate oxide and at its interface.[2] The defects could be both pre-existing and generated during device operation. The trapped charge results in a shift of the device parameters, such as its threshold voltage $V_{th}$, channel mobility, transconductance, and subthreshold slope, and generally a decrease of the FET's drive current. The name is derived from the phenomenon being strongly accelerated by *temperature T* and *gate bias* $V_G$. BTI in *n*-channel FET devices, which are typically biased in circuits at positive $V_G$, is referred to as positive BTI (PBTI), while negative BTI (NBTI) takes place in *p*-channel FETs. Constant $V_G$ stress bias is often referred to as static or "DC" BTI, while periodically interrupted $V_G$ stress is called "AC" or dynamic BTI.

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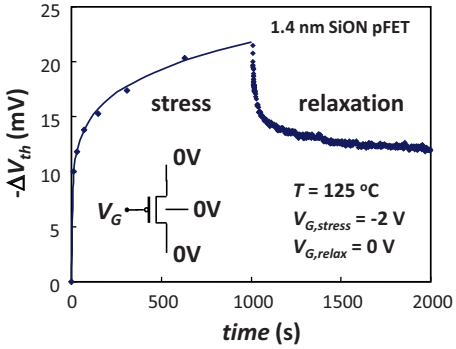


FIG. 1. (Color online) Shift in pFET threshold voltage is observed during negative gate bias stress. When the stress bias is removed, a recovery of the effect is seen (note that $V_{th} \sim 0$ V for this device). Inset illustrates the bias applied at FET terminals during the BTI measurement.

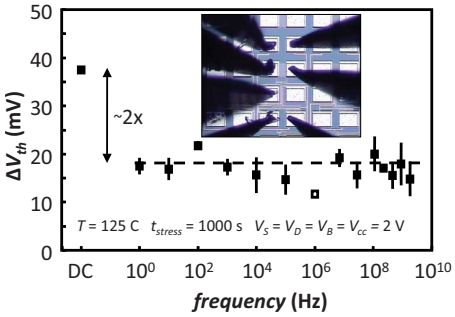


FIG. 2. (Color online) $V_{th}$ shifts due to 50% AC unipolar NBTI stress in pFETs are seen independent of frequency in the entire frequency range of 1 Hz–2 GHz. The $V_{th}$ shift of the corresponding DC NBTI stress obtained on an identical device is shown for comparison. Inset: Micrograph of the *on-chip* circuit for the DC and AC BTI measurements consisting of a ring oscillator, a frequency divider, a buffer, a pass-gate-based multiplexer, and the device under test (Ref. 17).

## III. STATIC BTI

Figure 1 illustrates the typical gradual shift of pFET threshold voltage $\Delta V_{th}$ during accelerated stress at elevated $T$.[5] The stress data are typically measured at several $V_G$'s and $\Delta V_{th}$ is extrapolated to 10 years at the circuit operating voltage $V_{DD}$ (or $V_{DD}+10\%$). The extrapolated $\Delta V_{th}$ must be below a given value (typically 30 or 50 mV) for the technology to qualify.

This simple extrapolation procedure is, however, complicated by $\Delta V_{th}$ decreasing immediately after the stress bias is removed, as illustrated in Fig. 1.[15] As we will discuss henceforth, this *recovery*, or *relaxation*, component $R$ typically proceeds simultaneously on many time scales, making it difficult to determine its beginning or end and thus separating it from the final *nonrecoverable*, or *permanent*, component $P$.[2,6] This $\Delta V_{th}$ relaxation is thus a crucial problem for BTI measurement, interpretation, and extrapolation. Understanding the recoverable component is central to unraveling the BTI mechanism.

## IV. DYNAMIC BTI

In many CMOS applications, such as logic, the majority of the FETs are constantly switched and thus exposed to *dynamic* stress.[16] Figure 2 documents that NBTI is present at frequencies up to the gigahertz range, i.e., there does not appear to be any "cut-off" time constant of the degradation mechanism above ~1 ns.[17] Furthermore, the AC bias signal reduces BTI with respect to the DC stress. This provides some additional reliability margin, which can be factored in during the application design phase.[9]

In an arbitrary FET of an arbitrary digital circuit, the average probability of a signal being high can vary between 0% and 100%. The dependence of BTI on the *duty cycle* [called *duty factor* (DF) here], however, has been seldom studied experimentally. A NBTI $\Delta V_{th}$-DF dependence with an inflection point around DF ~50%, first reported in Ref. 17, is shown in Fig. 3.[12] Below we will show that this distinctive shape is a fundamental feature of NBTI relaxation.

## V. STATES WITH WIDELY DISTRIBUTED TIME SCALES: SIMILARITY BETWEEN BTI RELAXATION AND LOW-FREQUENCY NOISE

Long, log($t$)-like behavior of $\Delta V_{th}$ without a characteristic time scale is typically observed in both the initial portion of NBTI degradation[13,18] and the recovery phase. Figure 4(a) illustrates that the *rate of degradation* $d\Delta V_{th}/dt_{relax}$ (Ref. 7) extracted from the log($t_{relax}$)-like $\Delta V_{th}$ NBTI relaxation transient after even a very short 0.1 s stress follows $1/t_{relax}$ for over 7 decades. Such behavior is a signature of states with discharging time constants covering as many decades.[19]

Incidentally, *superposition of states with widely distributed time scales* is the standard explanation of the $1/f$ noise spectra,[20] which are clearly observed in our pFETs [Fig. 4(b)]. This obvious similarity leads us to argue that the same states with widely distributed time scales, in fact, play a fundamental role in both NBTI and noise measurements. As will be shown below, this connection is crucial for understanding the properties of the defects contributing to BTI.

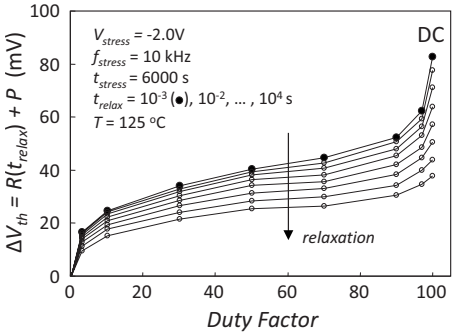


FIG. 3. Total degradation $\Delta V_{th}$ after 6000 S of unipolar NBTI stress shows a distinctive dependence on the DF. In particular, a weak dependence or a "plateau" between ~10% and ~90% is observed, complemented by rapid $\Delta V_{th}$ increase for the outermost DF values. Data at different relaxation times are shown.

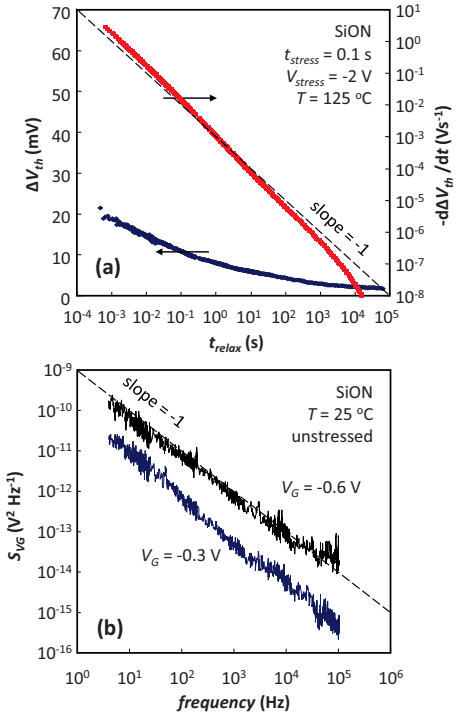


FIG. 4. (Color online) (a) Characteristic long, log-like $\Delta V_{th}$ relaxation trace is observed after even short (pulselike) NBTI stress. The *rate* of recovery $d\Delta V_{th}/dt_{relax}$ following $\sim 1/t_{relax}$ for $\sim 7$ decades is a signature of states with discharging time constants covering as many decades. (b) Gate-referred noise spectra measured on the same (unstressed) devices show clear $1/f$ dependence, routinely explained by a superposition of states with widely distributed time scales.

## VI. SEMIQUANTITATIVE MODEL FOR BTI RELAXATION

In order to visualize this common property it is beneficial to consider an equivalent circuit representing states with widely distributed time scales.[19] We start by noting that in either NBTI relaxation or $1/f$ noise measurements, no maximum or minimum cut-off times are typically observed.[12] For the sake of simplicity we therefore assume here that the time constants are log-uniformly distributed from times much shorter than the switching time of a pFET to very long, corresponding to the lifetime of a CMOS application. Such states with widely distributed time scales are then represented by "RC" elements in Fig. 5(a) with the total FET $\Delta V_{th}$

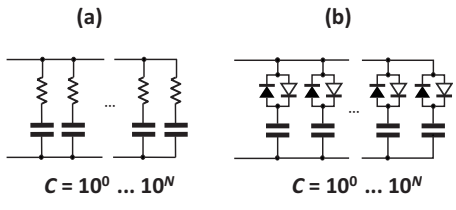


FIG. 5. (a) Equivalent circuit with exponentially increasing capacitances used to emulate defect states with widely distributed time scales such as those active in low-frequency noise. (b) The same circuit modified to account for charging (i.e., capture) and discharge (i.e., emission) time constants being voltage dependent, represented by asymmetric diodes. The sum of voltages on capacitors is assumed to be proportional to FET $\Delta V_{th}$.

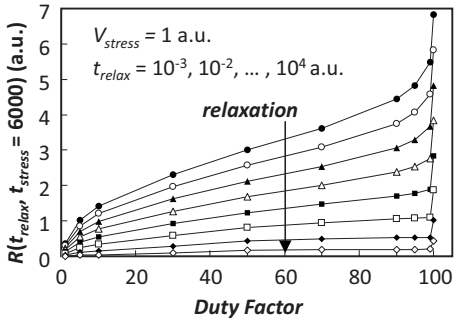


FIG. 6. Plateau in DF dependence of $R$ is also qualitatively well reproduced by the equivalent circuit in Fig. 5(b), as is the decrease with increasing relaxation time (cf. Fig. 3, which, however, shows the sum of $R$ and $P$).

being proportional to the sum of voltages ("occupancies") on all capacitors. For the sake of simplicity, we assume that all RC elements have the same weight and can be partially occupied, which emulates the behavior of a large-area device. We find that most properties of the recoverable component can be reproduced when the Ohmic resistors in Fig. 5(a) are replaced with a *nonlinear* component [simulated by two diodes with different parameters, see Fig. 5(b)], which emulates different charging (i.e., capture) and discharge (i.e., emission) time constants of each defect.[21] Such a circuit correctly reproduces DF (Fig. 6, cf. Fig. 3) and also the loglike relaxation and the loglike initial phase of stress (not shown).[19]

## VII. OBSERVING PROPERTIES OF INDIVIDUAL DEFECTS

Figure 7 shows two typical $\Delta V_{th}$ relaxation transients following positive $V_G$ stress on a single $70 \times 90$ nm$^2$ nFET (i.e., corresponding to PBTI). Conversely to the continuous relaxation curves obtained on large devices, a quantized $\Delta V_{th}$ transient is observed in the deeply scaled devices. In such devices, the relaxation is observed to proceed in discrete voltage steps, with each step corresponding to discharging of a *single* oxide defect.[12,22,23] Upon repeated perturbation, each defect shows up in the relaxation trace with a characteristic

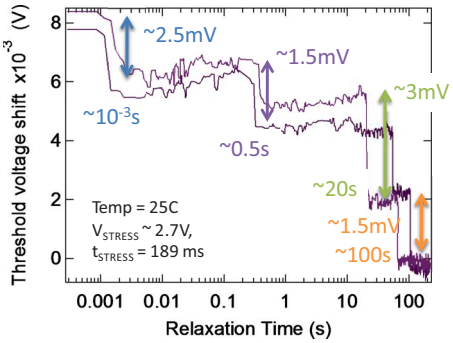


FIG. 7. (Color online) Characteristic $\Delta V_{th}$ transients of a single $70 \times 90$ nm$^2$ 1 nm $SiO_2$/1.8 nm HfSiO nFET device stressed at 25 °C and $V_G$=2.8 V for 184 ms. Four discrete drops are observed, indicating the existence of four active traps at the stress condition.

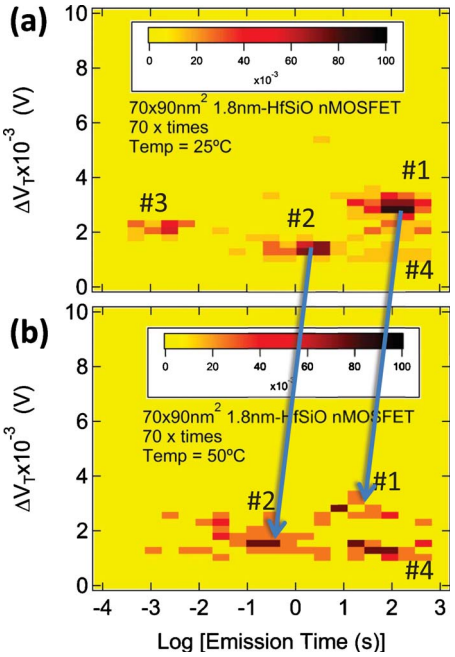


FIG. 8. (Color online) Two-dimensional histograms (TDDS spectra) of the heights and emission times of the steps extracted from 70 $\Delta V_{th}$ transients of the particular device of Fig. 7 at (a) 25 and (b) 50 °C. Four clusters are formed that shift horizontally to shorter emission times with increasing temperature. Note that trap 3 disappears from the experimental window at 50 °C.

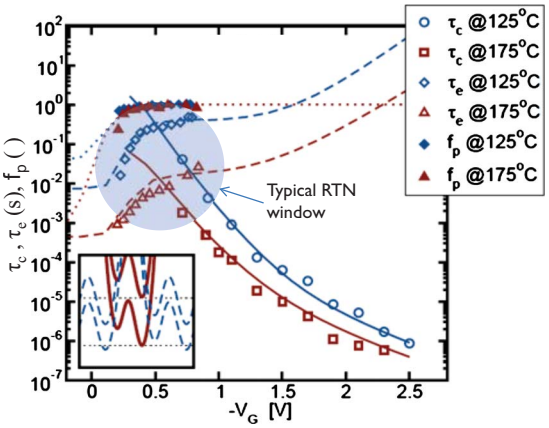


FIG. 9. (Color online) Simulated capture and emission time constants (lines) compared to the experimental TDDS values obtained on $SiO_2$ pFETs (symbols) during NBTI stressing at 125 and 175 °C and varying $V_G$. The experimental occupation probability of the charged state $f_p$ is also indicated. The configuration coordinate diagram is shown in the inset (dashed line: neutral defect state; solid line: charged state potential).

"fingerprint" consisting of its discharge, or *emission* time, and its voltage step.[14]

Figure 8(a) shows the two-dimensional histogram of the heights and the emission times of the steps when the experiment was repeated 70 times at the same stressing and relaxing condition as in Fig. 7.[14] In Fig. 8(a), four clusters are clearly formed that correspond to four active defects in the time window of the experimental setup.

The emission times of each defect are stochastically distributed and follow an exponential distribution. This allows us to determine the average emission time $\tau_e$. The capture time of each trap can be obtained by varying the stress (i.e., charging) time from 240 down to 2 ms. The intensity of the cluster decreases with reducing stress time when the characteristic capture time is in the range of the stress time. The fit of the intensity to $P_c = 1 \exp(-t_{stress}/\tau_c)$ lets us calculate the average capture time $\tau_c$. This technique is known as time dependent defect spectroscopy (TDDS).[14]

In Fig. 8(b), an identical experiment but at 50 °C was repeated on the same device. Note the large horizontal shift of the clusters to shorter emission times with only a 25 °C temperature increase. The Arrhenius plots of the emission and capture times obtained at $T$ from 10 to 50 °C (not shown) provide activation energies of 0.48 eV for emission and 0.25 eV for capture. Similarly thermally activated capture and emission times are also observed in both nFET and pFET (i.e., corresponding to NBTI) with conventional $SiO_2$ gate oxide.[14,23,24] We therefore conclude for all these cases that *both emission and capture in both electron and hole gate oxide traps are without a doubt thermally activated processes*. This experimental fact is incompatible with direct elastic tunneling theories widely used in different oxide trap characterization techniques and calculations. Consequently, a new model that takes into account this thermal dependence has to be considered.

## VIII. MODELING PROPERTIES OF INDIVIDUAL DEFECTS

A model of the above-described properties of individual gate oxide defects can be constructed by drawing on the above similarities with low frequency and RTN.[25] An example of the configuration coordinate diagram of the model is shown in the inset of Fig. 9. Four different configurations of the defect are considered.[14] Two of the states are electrically neutral while two of them correspond to the singly positively charged state. In each charge state the defect is represented by a double well, with the first of the two states being the equilibrium state and the other a secondary (metastable) minimum. The time dynamics of the defect can be described by a simple stochastic Markov process. Broadly, transition rates between states involving charge transfer assume (1) tunneling between the substrate and the defect and (2) nonradiative multiphonon (NMP) theory, which has been often applied to explain RTN.[26,27] Introduction of the NMP theory naturally explains the temperature dependence of both capture and emission time constants observed in the previous section. The wide distribution of time scales is then readily described by a distribution of the overlaps of the potential wells (i.e., a distribution of "potential barriers").[14]

The crucial extension of the NMP theory is the assumption of the relative position of the potential wells changing with gate bias,[14] quite naturally introducing the required strong $V_G$ dependence. As documented in Fig. 9, the model successfully describes the bias as well as the temperature dependences of the characteristic time constants. We also note that, contrary to techniques for the analysis of RTN,

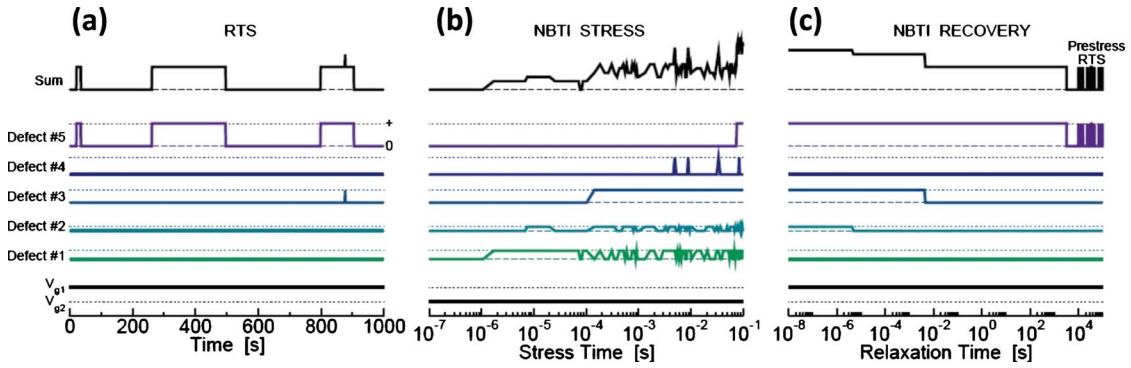


FIG. 10. (Color online) Simulated RTN, stress, and recovery behavior of a nanoscale device using a stochastic solution algorithm of the proposed model. (a) At the threshold voltage ($V_{G1}$), the RTN is dominated by defect 5 with the occasional contribution from defect 3. Defects 1, 2, and 4 remain positively charged within the "simulation/experimental" window. (b) During stress ($V_{G2}$), the capture times are dramatically reduced by the higher (more negative) gate voltage and defects 3 and 5 become predominantly positively charged ($\tau_c \ll \tau_e$). Defects 1, 2, and 4 start producing RTN. (c) During recovery (back at $V_{G1}$), trapped charge is subsequently lost and the dynamic equilibrium behavior is gradually restored.

which only allow monitoring the defect behavior in a rather narrow time window, TDDS can be used to study the defects' capture and emission times over an extremely wide range.

We have previously argued that the phenomenon called NBTI relaxation in pFET devices is, in fact, just a different facet of the well-known low-frequency noise in these devices. While the low-frequency noise corresponds to the channel/gate dielectrics system being in the state of dynamic equilibrium, NBTI relaxation corresponds to the perturbed system returning to this equilibrium.[28] Figure 10 then illustrates this concept on a simulated example of a deeply scaled pFET containing only five active defects.[23] In particular, it shows that the same defects can be responsible both for RTN as well as the NBTI relaxation and the (initial phase of) NBTI stress.

## IX. BTI DISTRIBUTION IN DEEPLY SCALED FETS

As CMOS devices scale toward atomic dimensions, device parameters become statistically distributed. Similarly, parameter *shifts* during device operation, once studied in terms of the average value only, will have to be described in terms of their distribution functions. The understanding of the properties of individual defects helps us to explain this distribution. Namely, much like in the case of RTN,[29,30] we observe the distribution of downsteps $\Delta V_{\mathrm{th}}$ due to *individual* discharging events to be *exponentially* distributed (Fig. 11). The exponential distribution of single-charge $\Delta V_{\mathrm{th}}$ can be understood if nonuniformities in the pFET channel due to random dopant fluctuations are considered.[28–30] A single discharging event in many devices routinely exceeded 15 mV, *and in several devices exceeded 30 mV*, the NBTI lifetime criterion presently used by some groups. For comparison, $\Delta V_{\mathrm{th}}$ of less than 2 mV would be expected based on a simple charge sheet approximation. The large observed step height amplitude is due to the aggressively scaled dimensions of the pFETs used.[28,31]

Since the charge lateral locations are uncorrelated, the overall $\Delta V_{\mathrm{th}}$ distribution can be readily expressed as a convolution of individual exponential distributions [Eq. (1)], with the cumulative distribution function (CDF) given by

$$F_n(\Delta V_{\mathrm{th}}, \eta) = 1 - \frac{\Gamma(n, \Delta V_{\mathrm{th}}/\eta)}{(n-1)!}, \tag{1}$$

where $n$ is the number of active defects in the device. An actual population of stressed devices will consist of devices with a *different* number $n$ of oxide defects in each device. That number will be Poisson distributed.[12,22,28] The *total* $\Delta V_{\mathrm{th}}$ distribution can be therefore obtained by summing distributions $F_n$ weighted by the Poisson probability

$$F_N(\Delta V_{\mathrm{th}}, \eta) = \sum_{n=1}^{\infty} \frac{e^{-N} N^n}{n!} F_n(\Delta V_{\mathrm{th}}, \eta), \tag{2}$$

where $N$ is the mean number of defects in the FET gate oxide and is related to the oxide trap (surface) density $N_{\mathrm{ot}}$ as $N = WLN_{\mathrm{ot}}$ (note that $N$ is not an integer). The CDF of Eq. (2) is plotted in Fig. 12 for several values of $N$. For comparison, measured total $\Delta V_{\mathrm{th}}$ distributions for three different stress times from Ref. 22 are excellently fitted by the derived analytical description.

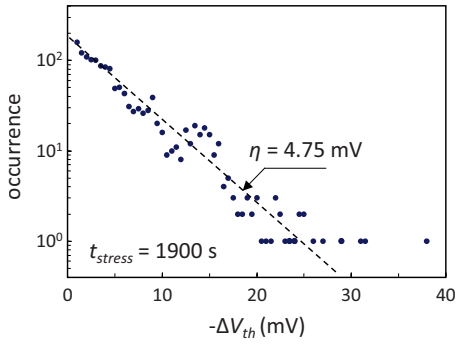


FIG. 11. (Color online) Histogram of NBTI transient individual step heights measured on 72 devices shows a clear exponential distribution. The average $V_{\mathrm{th}}$ shift $\eta$ corresponding to a single carrier discharge is $4.75 \pm 0.30$ mV in the pFETs with metallurgic length $L=35$ nm, width $W=90$ nm, and $HfO_2$ dielectrics with EOT=0.8 nm.

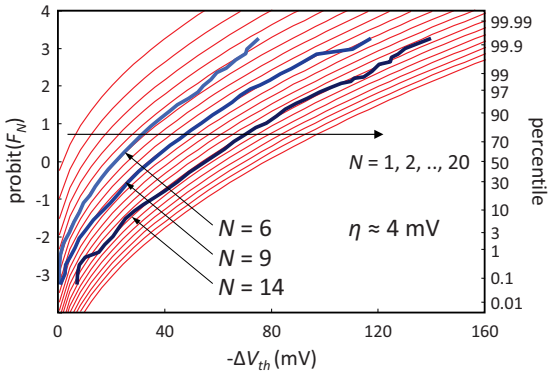


FIG. 12. (Color online) Eq. (2) in a probit plot rescaled to fit experimental distributions from Fig. 10 of Ref. 22, with the corresponding values of $N$ and $\eta$ readily extracted.

The advantage of describing the total $\Delta V_{\text{th}}$ distribution in terms of Eq. (2) is its relative simplicity and tangibility of the variables. The analytical description allows, among other things, to calculate NBTI threshold voltage shifts in an unlimited population of devices, a feat impossible through device simulations. This illustrates how a detailed understanding of the properties of individual defects can be beneficial to explaining real-world technological issues.

## X. TECHNOLOGICAL SOLUTIONS

Once the underlying BTI mechanisms are understood, we can attempt to influence the defect properties to beneficial ends. Below we discuss two possible technological solutions for both PBTI and NBTI.

## XI. IMPROVING PBTI WITH RARE-EARTH INCORPORATION

PBTI was considered a minor problem in technologies based on $SiO_2$. It arose as a reliability issue when high-$k$ materials were incorporated into the gate stack. However, when rare earths were introduced to adjust the nFET initial threshold voltage, this issue was mitigated, as can be seen in Fig. 13. A significant reduction of PBTI is observed in planar nFETs with lanthanum with respect to a lanthanum-free reference.[32]

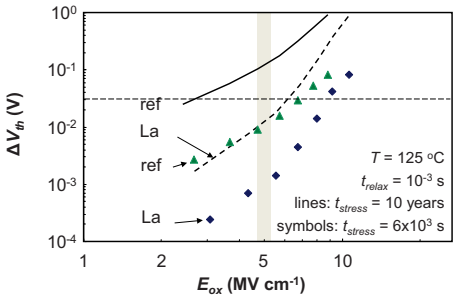


FIG. 13. (Color online) Significant reduction of PBTI threshold voltage shift is observed in planar nFETs with La passivation ("La") over the reference stack ("ref") without passivation. Simplified power-law projection to 10 years shows passivated stack having sufficient reliability ($\Delta V_{\text{th}} < 30$ mV) at ~5 MV/cm operating field.

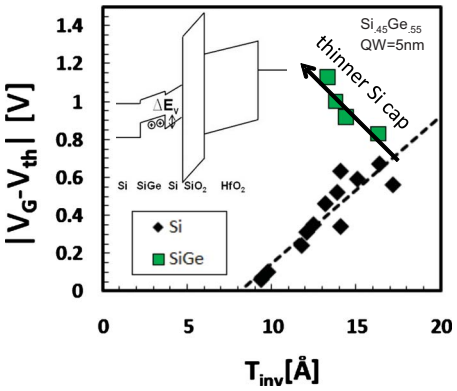


FIG. 14. (Color online) Plot of the operating overdrive voltage $|V_G - V_{\text{th}}|$ for 10 year lifetime assuming a 30 mV threshold voltage shift criterion vs the inversion capacitance-equivalent thickness $T_{\text{inv}}$ for Si channel devices with different processing used as a reference and for SiGe pFETs. For low $T_{\text{inv}}$, Si devices $|V_G - V_{\text{th}}|$ are below the expected operating voltage. In contrast to that, optimized SiGe devices show improved lifetime. Inset: Gate-stack band diagram in inversion. Si cap acts as a barrier $\Delta E_V$ for holes.

Positive BTI in nFETs with high-$k$ materials like $HfO_2$ has been linked to oxygen vacancies, which produce a defect level in the upper part of the oxide band gap. Group III elements compensate unpaired electrons around the oxygen vacancy in $HfO_2$ and the defects are "passivated" by being pushed up toward the conduction band minimum.[33] Such states are not easily accessible to nFET channel electrons, resulting in the significant reduction of negative charge capture in the stack and hence the reduction of PBTI.

## XII. IMPROVING NBTI IN HIGH-MOBILITY SIGE PFETS

Reduction of gate-stack equivalent oxide thickness (EOT), which is one of the most efficient ways to improve FET performance, enhances NBTI due to increased oxide electric field. As a consequence, 10 year lifetime can be guaranteed for sub-1 nm EOT Si pFETs only at gate overdrive voltages far below the expected operating voltages (Fig. 14).

Another way to improve FET performance is the use of high-mobility substrates such as buried-channel SiGe.[34] Because of the valence band offset between the SiGe and the Si cap (see inset of Fig. 14), inversion channel holes are confined in the SiGe layer, which therefore acts as a quantum well (QW) for holes. The Si cap lowers the inversion capacitance as compared to the accumulation capacitance. For these devices it is therefore necessary to report the capacitance-equivalent thickness in inversion ($T_{\text{inv}}$, evaluated at $V_G = V_{\text{th}} - 0.6$ V) which will be affected by the thickness of the Si cap.[35]

As can be seen from Fig. 14, SiGe-based device gate stacks significantly increase operating gate overdrive while still guaranteeing 10 year device lifetime and at the moment seem to be the only solution to the NBTI issue for sub-1 nm EOT devices. We have recently observed that both increasing the Ge content in the channel and increasing the SiGe QW

thickness reduce NBTI. Most intriguingly, a *reduction* of Si cap thickness also diminishes NBTI.[35] The most likely hypothesis explaining all three trends appears to be the energetic decoupling of the buried channel and the gate oxide defects.[36]

## XIII. CONCLUSIONS

In this article we have reviewed some of the shifts occurring in the past few years in our understanding of BTI. Among the most significant one we emphasize analyzing BTI relaxation with the tools originally developed for describing low-frequency noise. This includes the interpretation of the time, temperature, voltage, and duty cycle dependences of BTI. In step with the CMOS downscaling trend we have shown that a wealth of information about defect properties can be obtained from deeply scaled devices and how this information can prepare us to interpret the variability issues of future technologies. This theme was complemented by showing the most promising technological solutions for BTI.

## ACKNOWLEDGMENTS

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