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Recent trends in neuromorphic engineering

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Abstract

Neuromorphic Engineering has emerged as an exciting research area, primarily owing to the paradigm shift from conventional computing architectures to data-driven, cognitive computing. There is a diversity of work in the literature pertaining to neuromorphic systems, devices and circuits. This review looks at recent trends in neuromorphic engineering and its sub-domains, with an attempt to identify key research directions that would assume significance in the future. We hope that this review would serve as a handy reference to both beginners and experts, and provide a glimpse into the broad spectrum of applications of neuromorphic hardware and algorithms. Our survey indicates that neuromorphic engineering holds a promising future, particularly with growing data volumes, and the imminent need for intelligent, versatile computing.

Keywords: Neuromorphic engineering, Neuromorphic hardware, Neuromorphic algorithms, Neuromorphic applications, Neuromorphic circuits, Neuromorphic systems, Neuromorphic devices

Background

Of late, increasing data volumes have posed a challenge to computing systems in terms of their scalability, particularly those that rely on intensive computation. The key challenge has been to handle the data volumes in such systems, owing to their complex, asynchronous and power-drawing nature [1]. Neuromorphic engineering presents itself as a possible, potential and promising solution to problems of this nature [2, 3]. The broad spectrum of algorithms, devices, circuits and systems that are inspired by the working of mammalian neural systems constitutes of neuromorphic engineering.

To motivate the context of this article, Fig. 1 presents a graph showing the number of research publications and patents in the domain of neuromorphic engineering over the last ten years. These are clearly indicative of a growing trend in favor of research and developments in neuromorphic hardware, which form the impetus for reviewing research in this domain.

In this review, we look at recent work in the neuromorphic engineering domain in order to obtain a holistic view on research directions being pursued, while also being able to infer possible outcomes and future directions. Neuromorphic engineering has evolved significantly since it was first conceived by Mead [4]. In this review, we largely refer to very recent works with an aim to discern recent trends in the domain. A summary

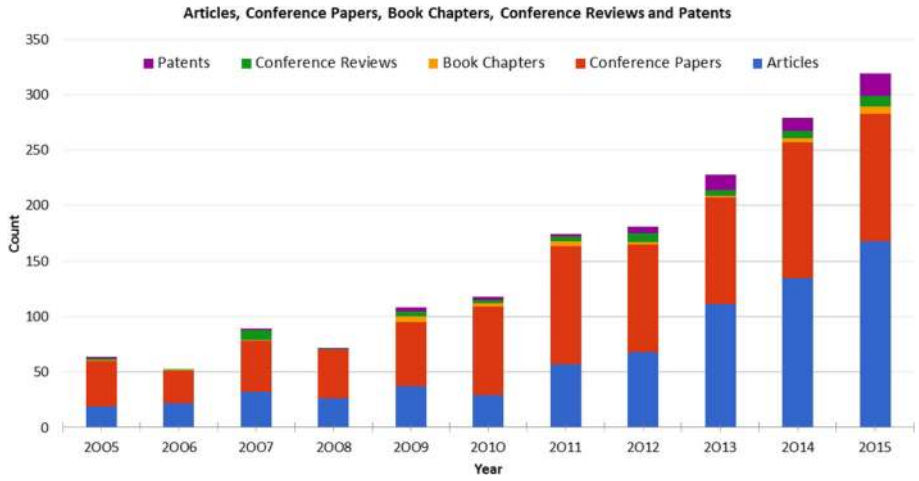

Fig. 1 Publications and patents in neuromorphic engineering: Based on data collected over the last ten years generated from Scopus using the search term *"neuromorphic"*

of research directions in neuromorphic engineering along the dimensions representing neuromorphic circuits, devices and systems, respectively, is illustrated in Fig. 2, along with references pertaining to the specific works that have been cited in our review. All discussions henceforth are restricted primarily to the aforementioned time period.

There have been several recent review articles in the literature on neuromorphic engineering. A review of methods, issues and challenges in neuromorphic engineering was presented by Ahmed et al. [5], that provides a primer to the domain. It also highlights challenges and open research areas. A comprehensive tutorial by Rajendran et al. [6] details algorithms, devices and systems, while emerging memory techniques have been discussed in [7]. DeSalvo et al. [8] present large-scale energy efficient neuromorphic systems based on resistive memory technologies, as well as for low-power embedded devices [9]. Research directions in applications pertaining to vision, auditory and olfactory applications have been discussed by Vanarse et al. [10].

The rest of the review is organized as follows. Section "Algorithms" discusses recent algorithms developed in the neuromorphic engineering domain. This is followed by a discussion of hardware implementations in Section "Hardware", which includes neuromorphic devices and circuits. We then discuss recent applications in Section "Recent applications". Finally, conclusions and future outlook are presented in Section "Conclusions and future outlook".

Algorithms

Several machine learning algorithms dealing with big data have evolved till date that harness the compute power of server class machines for optimization [11]. Though offline storage space is often abundant, it is the complexity of the approaches employed in such systems, both in storage and time, that has become crucial to their viability. Newer techniques, for example those that use stochastic approximations to learning algorithms allow us to deal with big data. These have allowed us to simulate approaches in tractable time, given the luxury of heavy computational resources. The important challenge that still needs to be addressed is the feasibility in hardware implementation of these algorithms

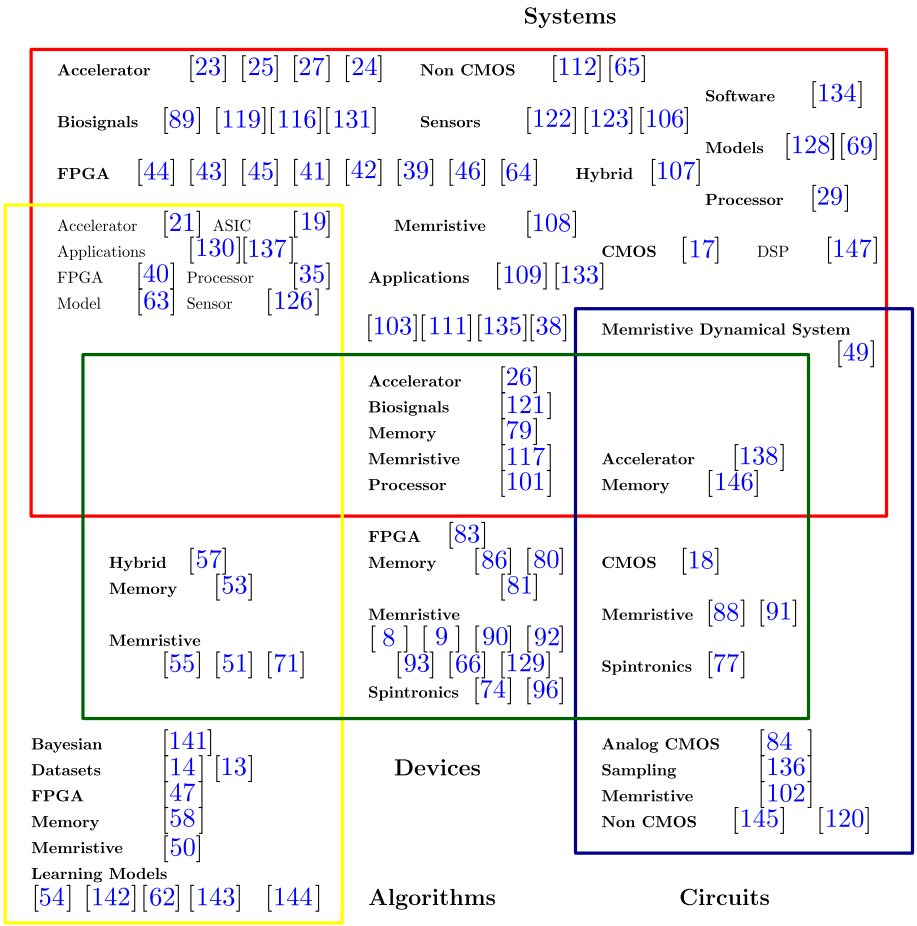

Fig. 2 Directions in neuromorphic engineering: This figure categorizes research papers published in 2015 into algorithms, circuits, devices and systems, based on the nature of the primary contribution. The reader can view this figure in the supplementary material (Additional file 1) provided with the manuscript to click on the hyperlinks and navigate to the corresponding reference in the bibliography section [141–147]

and approaches, that is eventually critical for realizing practical applications, such as on embedded platforms. The storage and computational capacity available on such platforms is limited, hence the algorithms need to have a low computational complexity, that translates to low-power requirements in hardware. This is where research in neuromorphic engineering seeks to provide new directions.

The quest for modelling algorithms that mimic, and eventually better the decision-making ability of the human brain has been a significant research thrust since recent times. This has been challenging not only because of the complex architecture of the brain, but also because this requires a diverse inter-disciplinary approach combining biomedical and engineering sciences. Progress in areas of research such as artificial intelligence and machine learning have been able to achieve this to some extent. For instance, of late the evolution of deep learning approaches has led to development of vision systems which can scale to large datasets. However, the computational requirements of these architectures is a luxury not available on hardware platforms. Conventional architectures based on the Von Neumann model were based on the principle that data moved between storage and memory for processing. However, the growing size of datasets has made this

model infeasible and maximizing memory-processor co-localization is needed. A possible solution lies in working towards computationally efficient learning architectures which can have sparse representations, hence being efficiently implementable for practical applications. This fuels the development of newer algorithms for neuromorphic computing. A few significant developments in neuromorphic engineering are summarized in Fig. 3.

Datasets

A challenge for the works in this domain has also been the availability of datasets. To this end, Orchard et al. [12] have worked towards converting conventional static datasets to neuromorphic datasets, that not only maintains their compatibility with existing vision systems for benchmarking performance, but also involves *"creation of information"* which is required for realizing the true benefit of neuromorphic systems. Tan et al. [13] have detailed broader perspectives, motivation and guidelines in this direction. The challenge in availability of datasets for closed-loop neuromorphic systems has been addressed by Stewart et al. [14] in their work on developing benchmarks for such systems using a minimal solution in a physical embodiment. A visual navigation dataset for neuromorphic systems has been developed by Barranco et al. [15]. An effort for benchmarking bio-inspired solutions via neuromorphic architectures on parallel computing platforms has been made by Diamond et al. [16]. Newer research directions in neuromorphic engineering are majorly directed to address these issues, and we review recent trends in neuromorphic engineering for hardware implementations in the following section.

Hardware

Neuromorphic hardware encompasses a broad spectrum, including CMOS, memristive or special devices in combination with CMOS, DSPs, GPUs, FPGAs, accelerators and others, as summarized in Fig. 4. We look at recent developments in these domains, attempting to lay greater emphasis on works that look at addressing challenges presented by the large data sizes in particular.

Digital CMOS solutions

A 65 nm CMOS neuromorphic processor has been designed for unsupervised online learning by Seo and Seok [17] with 1.2 k digital neurons and 4.7 k latch-based synapses. A CMOS motion sensor for biologically motivated expansion/contraction has been

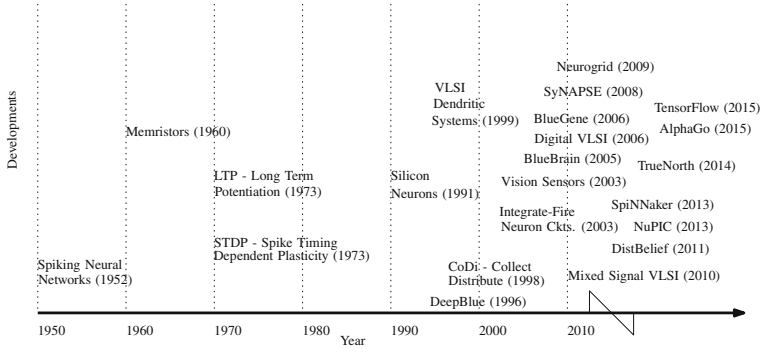

Fig. 3 Timeline of developments in neuromorphic engineering

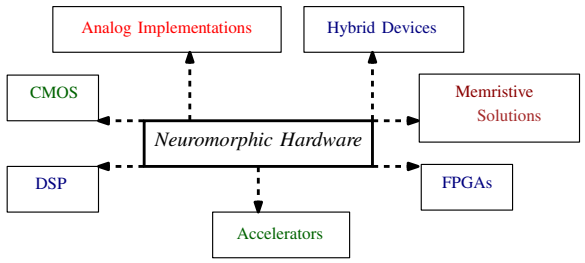

Fig. 4 Summary of neuromorphic hardware

developed by Chiang et al. [18] which has been found to be suitable for applications such as robotic movement. Knag et al. [19] developed an ASIC with a computer-vision accelerator for a sparse-coding neural net to learn and extract features from images and video.

Accelerators

Several neuromorphic accelerators have also been designed; a comparison of them with machine learning approaches has been presented by Du et al. [20]. Chen et al. [21] present a low area ($3.02mm^2$) and power ($485mW$) neuromorphic accelerator for implementation of deep and convolutional neural networks. Darwin [22], by Shen et al., is a neuromorphic hardware co-processor for spiking neural networks on 180nm CMOS technology. NS23 by Shahsavari [23] is a scalable spiking neural network simulator with memristors for computer vision tasks. Conti et. al. [24] develop a low-power parallel accelerator called the PULP (Parallel processing Ultra-Low Power platform) for kernel based image processing and vision tasks. Mahajan et al. [25] develop TABLA, a framework to generate accelerators for machine learning algorithms via stochastic approximations for their FPGA realization. A reconfigurable computing accelerator for various neural network topologies has been developed by Liu et al. [26].

PuDianNao [27] by Liu et al. is a neuromorphic accelerator which can run seven machine learning algorithms, viz. *k-means*, *k-nearest* neighbors, naive bayes, support vector machines, linear regression, classification trees and deep neural networks. Bojnordi et al. [28] develop a memristive Boltzmann machine for large scale combinatorial optimization and deep learning. They demonstrate their accelerator on the graph partitioning and boolean satisfiability problems, and obtain 57× higher performance and 25× lower energy. Neuromorphic accelerators for mobile platforms were presented by Kim et. al. [29] with speedups ranging from 23–126 % and power reduction of upto 22 % by using inter and intra neuron parallelism.

GPUs and DSPs

The growth in volumes of data has also propelled investigation into neuromorphic architectures for Graphics Processor Units (GPUs). Though tractable processing speedup has been achieved [30, 31], large memory requirements present a challenge [32]. In this context. Garcia et al. [33] developed a low-memory requiring system using an evolutionary algorithm for configuration selection and validated their system on optical flow benchmarks. Carlson et al. [34] presented a simulation environment for large-

scale spiking neural nets with evolutionary parameter tuning which harnessed the processing power of GPUs. More recently, Cheung et al. [35] developed *"NeuroFlow"*, a scalable platform for spiking neural nets on FPGA. Their system could simulate upto 400,000 neurons in real-time with a speedup of 2.83 times than that of GPUs. Liu et al. [36] present a optical flow sensor inspired by biological approaches which combines a silicon retina vision sensor with a DSP microcontroller.With recent trends in large-scale machine learning moving towards algorithms requiring heavy computational power, one can expect further developments in this direction gaining significance in the future.

FPGA

Yi et al. [37] presented a FPGA based encoder and reservoir design for neuromorphic processors. INsight by Chung et. al. [38] is an energy-efficient architecture for large-scale neural networks, which obtains an accuracy of 97.64 % on a handwritten image recognition dataset. FPGAs have been used for implementation of a convolutional spiking network for classifying musical notes by Escudero [39] as well as for biomimetic pattern generation [40]. Feedforward neural nets have been presented by Wang et al. [41] while spiking neural nets on FPGA have been evaluated by Rodrigues et al. [42] and Wu et al. [43]. Neuron-astrocyte signalling has been implemented by Nazari et al. [44], image dewarping by Molin et al. [45], event-driven vision processing by Yousefzadeh et al. [46] and Bayesian arithmetic stochastic synthesis by Duarte et al. [47].

Non-CMOS and hybrid solutions

Principles of design for network-based neuromorphic systems have been presented by Partzsch et al. [48]. A reconfigurable memristive dynamical system has been presented by Bavandpour et al. [49], which can be applied to learning and dynamical systems. Memristive crossbar circuits have also been demonstrated to be suitable for efficient neural network training by Irina et al. [50], where they show low error rates using batch and stochastic training approaches for a handwritten digit recognition dataset. Neuro-inspired devices have been developed for unsupervised learning by Chabi et al. [51, 52], as well as for an inference engine by Querlioz et al. [53]. A general model for voltage-controlled memristors has been developed by Kvatinsky et al. [54]. Further, Prezioso et al. [55] present transistor-free metal-oxide memristor crossbars for binary image classification using a single layer perceptron. Memristor-based self healing circuits have been presented by Gu et al. [56]. Sampath et al. [57] present a CMOS-memristor based FPGA architecture for memory cells.

Deep neural networks have been presented by Bichler et al. [58], with the specific focus for development of non-volatile memories, while deep spiking nets have been discussed by Neil et al. [59]. Goal-driven deep learning has been explored by Yamins et al. [60]. Fast and energy-efficient neurmorphic computing by Convolutional Neural Networks [61] and backpropagation [62] has been presented by Esser et al.

Models for large-scale spiking neural networks have been explored by Krichmar et al. [63], Wu et. al. [64] and Wang et al. [65]; while aspects related to plasticity of such networks in memristive devices has been studied by Saïghi et al. [66]. Garbin et al. [67] present phase-change memory (PCM) devices as binary probabilistic synapses in a neuromorphic system for visual pattern recognition. Suri et al. [68] analyze the resistance-drift

effect in PCMs, which have also been used to develop a large scale neural network by Burr et al. [69] and Boybat et al. [70]. Online gradient descent training has been implemented using memristor-based neural networks by Soudry et al. [71]. In the context of network-based algorithms for machine learning, neuromorphic architectures for deep neural networks have been presented by Indiveri. [72].

Stochastic memristive synapses based on spintronics have been presented by Vincent et al. [73, 74]. Zhang et al. [75] present a stochastic switching multi-level cell spin transfer torque MRAM. Zhao et al. [76] develop logic fabrics using spintronics, while energy-efficient architectures have been presented by Locatelli et al. [77]. Spintronics for low-power computing has been discussed in detail in the tutorial by Zhang et al. [78].

Analog implementations

There have also been several hardware implementations based on memristors independently for memories as well as in conjunction with other devices. Challenges in designing neuromorphic analog non-volatile memories have been discussed by Eryilmaz et al. [79], while Taha et al. [80] present the design of auto-associative memory using a multi-valued memristive memory cell. Reliability issues faced in using non-volatile memories as hardware synapses have been presented by Shelby et al. [81], while large crossbar arrays have been demonstrated by Virwani et al. [82]. Analog computing via multi-gate programmable resistive graphene devices has been presented by Calayir et al. [83], while a chaos-based CMOS analog neuron has been developed by Zhao et al. [84].

Moon et al. [85] present a PCMO ($Pr_{0.7}Ca_{0.3}MnO_3$) based resistive switching analog memory device. Mott memories have been discussed by Zhou et al. [86] The importance of enforcing criticality as a set-point for the purpose of developing adaptive neuromorphic hardware has been discussed by Srinivasa et al. [87]. A neuromorphic crossbar circuit based on analog memristors has been developed by Xu et al. [88], which demonstrates that recognition rates of upto 82.5 % on an average can be achieved. Ghaderi et al. [89] investigate cognitive signal processing on programmable analog hardware.

Synaptic devices for visual systems using Resistive RAMs have been presented by Kang et al. [90], while multistate registers have been developed by Patel et al. [91]. Vertical RRAMs have been explored for cochlea and convolutional neural nets by Piccolboni [92], while OxRAM synapses for CNNs have been presented by Garbin et al. [93]. ReRAM devices for neuromorphic computing have been explored by Jang et al. [94], while an artificial synapse using a memristive switch has been modelled by Wang et al. [95].

Zhang et al. [96] present an approach for energy-efficient neuromorphic computing for stochastic learning using multiple perpendicular in-plane magnetic tunnel junctions. Binary Conductive-Bridge RAM (CBRAM) synapses for bio-inspired computing has been presented by Suri et al. [97, 98], while Querlioz et al. [99] discuss stochastic resonance in an analog current-mode circuit.

Recent applications

The realm of applications for neuromorphic engineering continue to grow at an incredible rate. Newer applications keep emerging, and their comprehensive review could well be non-exhaustive. For the sake of brevity, we restrict our review to recently developed applications.

Applications in vision and robot control

There have been several challenges in the computer vision domain which have benefited by the use of biologically inspired computing approaches, and hardware implementation is imminent for their practical application. These involve tasks ranging from relatively simpler image classification to complex tasks such as robot movement planning, object recognition/detection, among others. Most of these involve processing of large datasets, as image or video sequences are fairly large in size, resulting in high area and power consumption.

A system for object detection to enhance the safety of drivers has been described by Han et. al. [100], and achieves upto 99 % detection rate. An on-chip implementation has been presented by Kim et al. [101], while a memristive threshold logic circuit for detecting fast moving objects was presented by Maan et al. [102]. Event-based 3D pose estimation using neuromorphic systems has been discussed by Valeiras et al. [103]. Event-based computation of motion flow has been presented in the work by Giulioni [104], specifically the extraction of optical flow from a visual scene.

Neuromorphic sensors for robotic vision have been benchmarked in terms of power consumption by Censi et al. [105] against conventional CMOS sensors, while sensors for high speed signal estimation have been developed by Mueller et al. [106]. A visual pattern recognition system has been developed using memristor array and CMOS neuron by Chu et al. [107], which has been successfully demonstrated for the task of digit recognition. Another such system by Lorenzi et al. [108] has been developed for recognition of binary images.

Applications in biomedical and biosignal engineering

Applications for biochemical systems for DNA strain displacement have been presented in the work by Chiang et al. [109]. Biological real-time neuromorphic system has been found in [110]. Population coding of neural activity has been done using a Trainable Analogue Block approach by Thakur et al. [111].

Neuromorphic hardware design has also been inspired by the motivation to model the behavior of the human brain [112–115]. One aspect in doing this involves investigating brain signals that may be acquired by various modalities (invasive or non-invasive) and developing systems to infer how these vary with the presented stimulus, which is analogous to development of brain-computer interfaces. This involves several challenges: the noise and non-stationarity inherent in these data acqusition modalities, the size of the datasets and the restrictions imposed by the acquisition modality. These are often common to all biomedical signals acquired; and multi-modal setups are often beneficial, but more challenging to implement on a common hardware platform. Works in this domain include an event-based neuromorphic Electroencephalogram (EEG) recording system by Corradi et al. [116]. Park et al. [117] memristive synapse neural network to recognize human thoughts corresponding to imagined speech of three vowels of the English alphabet. Scott et al. [118] develop a framework for spatio-temporal modelling of brain data called as NeuCube.

Recording of EEG from the ear has been facilitated by the characterization of recordings done using this modality by Mikkelsen et al. [119]. A neuromorphic system mimicking schizophrenia has been developed by Barzegarjalali [120]. The broader context of

biosignal processing has been explored by Kudithipudi [121], where they design and analyze a neuromemristive reservoir computing architecture for this purpose.

Applications in perception engineering

Applications based on integration with sensory modalities of humans have been widely explored. These include applications based on tactile sensor arrays by Lee et al. [122] and Ros et al. [123]. Corradi et al. [124] discuss directions for development of a neuromorphic vestibular system, while an autonomous neuromorphic cognition system has been proposed by Chicca et al. [125]. Applications such as texture categorization using neuromorphic inspired touch have been explored by Rongala et al. [126], while emotion recognition has been presented by Diehl et al. [127]. This area continues to be an exciting yet complex domain to explore, and one can envisage future research directions guided towards these.

Other applications

A neuromorphic framework for elastic wave dynamics has been presented by Katayama et al. [128]. Nanomorphic memristors have been used in designing neuromorphic fabric by Manem et al. [129] that can evaluate boolean functions as well as train a perceptron neural net for images.

A system that can classify musical notes has been presented by Cerezuela-Escudero et al. [39] on FPGA using a convolutional spiking neural network which gave high accuracies even in the presence of noise. A neuromorphic approach to the cocktail party problem implemented on FPGA has been presented by Thakur et al. [130]. Medical assistive applications such as retinal implants and sensory substitution have been explored by Gaspar et al. [131]. A neurmorphic character recognition system has been simulated by Sheri et al. [132] using PCMO memristors.

High speed serial interfaces have been presented in the work by Jablonski et al. [133] for bit-serial SATA AER inter-FPGA communication. A neuromorphic system for Electronic Design Automation (EDA) called the AutoNCS has been presented by Wen et al. [134]. A mixed-signal design for a neuromorphic analog-to-digital converter has been presented by Xu et al. [135].

A VLSI circuit for random sampling has been presented by Chien et al. [136] for uniform, exponential and bimodal distributions. A neuromorphic microphone has been incubated by Smith [137]. An authentication system accelerated by a neuromorphic hardware has been presented by Suri et al. [138] using the CM1K chip. It achieves recognition accuracy of 91 % with power requirement ranging from 487-668 μJ for training and testing on a benchmark dataset.

Conclusions and future outlook

A consolidated summary of developments in neuromorphic devices and circuits is presented in Table 1. From among the publications considered in this review, we have chosen those which have provided quantifiable results in terms of design area, power consumption/energy dissipation and performance and have summarized the results in the table.

Table 1 Summary of trends in Neuromorphic Engineering

S. No.	Type	Area	Power/Energy	Performance	Remarks
			GPU		
1	Multi-GPU, Garcia et al. [33]			3.71× speedup	Motion Estimation System
			Non CMOS		
2	Memristive Dynamical System, Bavandpour et al. [49]	4n memristors and no switch for implementing an n-cell system		Similar to Cellular Memristive Dynamical System (CMDS)	FitzHugh-Nagumo (FHN), Adaptive Exponential (AdEx) integrate and fire, and Izhikevich neuron models
3	Spiking Deep Neural Nets, Indiveri et al. [72]	cxQuad (43.79 mm^2), ROLLS (51.4 mm^2)	cxQuad(945uW @1.8 V), ROLLS (4 mW @1. 8V)	Upto 100 % accuracy on toy problems	Event-based convolutional stage for feature extraction connected to a spike-based learning stage for feature classification.
			Accelerators		
4	Memristive Boltzmann Machine, Bojnordi et al. [28]		25 × lower energy compared to multicore system, fully utilized accelerator chip consumes 1.3W	57× higher performance compared to multicore system	Hardware Accelerator for Combinatorial Optimization and Deep Learning
5	Processor (PuLP), Conti et al. [24]	Overall cluster area is 1.2 mm^2.	Peak theoretical energy efficiency of 211 GOPS/W, achieved upto 192 GOPS/W	Scaled over a 1× to 354× range,	Parallel Ultra Low-power Processor for ConvNet-based detector for smart surveillance, 4 Open-RISC cores, 64 kB of L2 memory and 24 kB of TCDM fabricated in 28nm STMicroelectronics FD-SOI technology
6	Processor (Mobile), Kim et al. [29]	Area overhead of 9 %	energy-savings of 22 %	Average speedups of 126 % and 23 % over CPU and a state-of- the-art MLP accelerator	Neural Network Accelerator for Mobile Application Processors, applied for edge detection
7	Memristor Based Crossbar, Liu et al. [26]	0.943 mm^2 (M-net) and 1.793 mm^2 (D-net)	184.2× (25.23 ×) energy saving over MLP(AAM)	178.4 × (27.06 ×) performance speedup over MLP(AAM)	RENO: Reconfigurable Neuromorphic Computing Accelerator benchmarked with Multi-layer perceptron and Auto-associative memory
8	Accelerator for machine learning, Liu et al. [27]	3.51 mm^2	596 mW	1.20 × faster than NVIDIA K20M GPU	PuDianNao: A Polyvalent Machine Learning Accelerator

Table 1 Summary of trends in Neuromorphic Engineering (*Continuation*)

S. No.	Type	Area	Power/Energy	Performance	Remarks
9	Hardware Co-processor, Shen et al. [22]	$5 \times 5\ mm^2$	0.84 mW/MHz with 1.8 V power supply	92.7 % classification accuracy	Darwin Neuromorphic co-processor unit for spiking and artificial neural nets
			FPGA		
10	Accelerator for large scale neural networks, Chung et al. [38]	$3.02\ mm^2$	485mW	117.87 × faster, and it can reduce the total energy by 21.08 ×	For convolutional and deep neural networks
			Digital CMOS		
11	CMOS Motion Sensor, Chiang et al. [18]	$4 \times 4\ mm^2$, 86.2 % fill factor	13.2 mW	6.8 % for ± X motion, 3.5 % for ± Y motion, and 6 % for ± Z motion	Motion sensor for Z-motion direction/velocity detection
12	ASIC Neural Network, Knag et al. [19]	3.06 mm × 65 nm CMOS ASIC test chip	6.67 mW for a 140 Mpixel/s throughput at 35 MHz.	Memory bit error rate of 0.01	ASIC for image and video feature extraction
			Analog		
13	Vertical Resistive RAM, Piccolboni et al. [92]	Area gain of 3-10		98 % recognition rate	For Cochlea and CNN applications
			Applications		
14	CMOS Analog VLSI Circuit, Chien et al. [136]	330 μ m × 210 μ m		Theoretically linear relationship between output ISI distribution and input current	Spike-based random sampling
15	Memristor Array+CMOS Neuron, Chu et al. [107]			55–100 % recogntion rate based on noise level	Digit recognition task
16	Neuromorphic Bio-amplifier, Corradi et al. [116]	$0.178\ mm^2$	90 μ W	96 % classification accuracy	EEG bio-amplifier has a programmable gain of 45–54 dB, with a Root Mean Squared (RMS) input-referred noise level of 2.1 μ V
17	Arithmetic Units, Kim et al. [148]	121 μm^2	0.111 mW	0.098 % error rate	Approximate adders and comparators
18	Processor + on-chip learning, Kim et al. [101]	$1.8\ mm^2$	5.7pJ/pixel	classification accuracy to 90 %	256 neurons, 83K synapses for Spiking LCA with classification for object detection
19	Tactile Sensors for Touch ,Lee et al. [122]	$37 \times 43.5\ cm^2$ active sensor area		4096 element tactile sensor array that can be sampled at over 5 kHz	Kilohertz Kilotaxel Tactile Sensor Array for Investigating Spatiotemporal Features

Table 1 Summary of trends in Neuromorphic Engineering (*Continuation*)

S. No.	Type	Area	Power/Energy	Performance	Remarks
20	RRAM Multistate Register, Lorenzi et al. [108]	2.8–5.2 μm^2	6.5 % energy reduction	40 % improvement over switch-on-event processor	Multistate register for continuous flow multithreading
21	CM1K chip, Suri et al. [138]		668 μJ for learning and 487 μJ for recognition, while operating at 25 MHz	91 % recognition accuracy	Multi-modal authentication (person identification) system based on simultaneous recognition of face and speech data
22	Switched Capacitor Circuit, Mayr et al. [110]	600 μm $\times$ 600 μm	1.9 mW	Short and Long term plasticity, 8k synapses	Closed loop interface to in-vitro cortical neuron cultures.

Indiveri et al. [139] opine that future neuromorphic systems would be an integration of research in several domains, viz. VLSI circuits, emerging VLSI technologies, control of robotic platforms, neural computation and biological, cognitive architectures. The recent publications in this domain reviewed in this paper clearly augment this claim. With developing systems increasing focus on handling big datasets, the use of bio-inspired algorithms and architectures has become imperative, and shall certainly pave the way forward for future research directions in neuromorphic engineering. We present an illustration of future directions in Fig. 5.

It is clear that advances in technology are allowing for faster devices that are smaller. The diversifying nature of progress in the neuromorphic engineering domain mandates the urgent and strong need of standardization, benchmarking and road-mapping, primarily among various design elements such as neuron blocks, weight blocks, algorithms, communication protocols and test datasets. A look at how integration has progressed in VLSI indicates that power consumption and interconnection complexity have become the most critical hurdles in building larger systems on chip.

We believe that this observation holds pointers for the evolution of neuromorphic systems. In a system with N interacting modules, the data flows and interconnections tend to grow as $\alpha N \times N$, or αN^2. Communication, therefore, consumes more power than the dissipation within individual modules. This is also true for the area of modules on VLSI

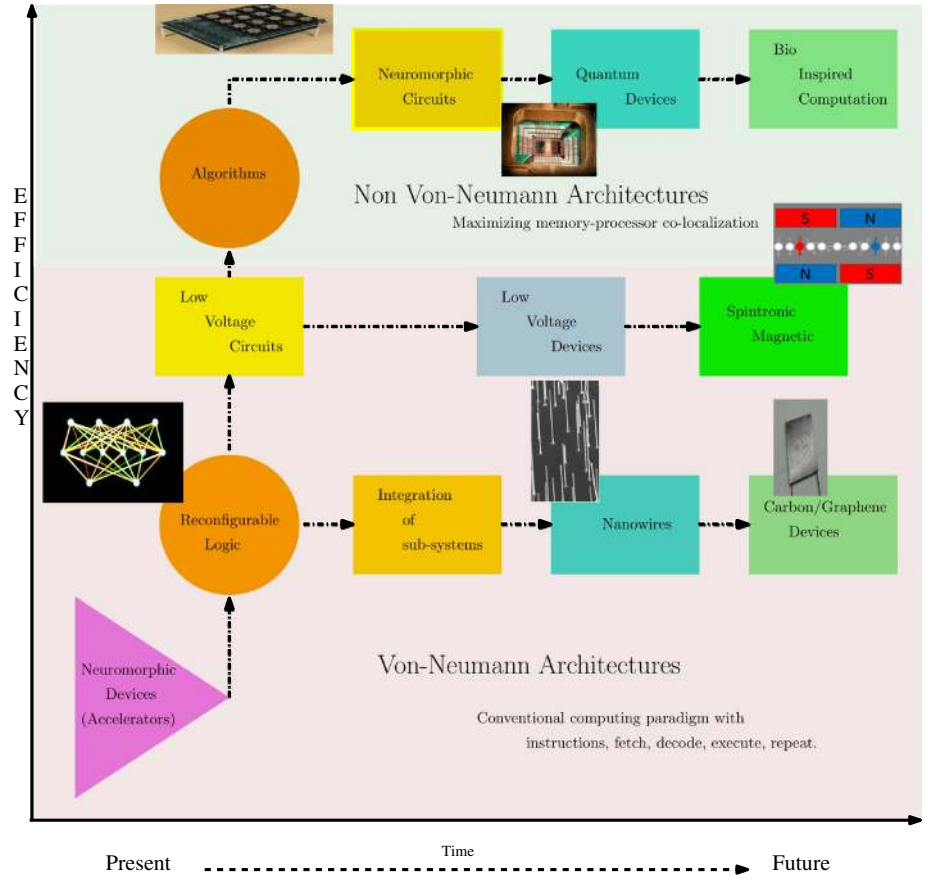

Fig. 5 Future directions in Neuromorphic Engineering. (adapted from IBM research colloquia-2012, Madrid, M. Ritter et. al.)

systems - interconnect occupies more space than logic, and increasingly so. Devices that consume less power are therefore more attractive; technologies that can allow interconnects to scale will tend to dominate. One might expect optical interconnects to become more pervasive. On the algorithms front, sparse representations that lead to reductions in power and area are likely to be more favoured. Coding techniques that make communications more efficient would also be preferred [140]. The last two have a firm mathematical basis, and one might expect to see significant developments along these lines.

Additional file

Additional file 1: Supplementary material. (PDF 104 kb)

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Competing interests
The authors declare that they have no competing interests.

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