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Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application: Topologies, Comprehensive Analysis and Comparative Evaluation

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ABSTRACT Recently, multilevel inverters (MLIs) have gained lots of interest in industry and academia, as they are changing into a viable technology for numerous applications, such as renewable power conversion system and drives. For these high power and high/medium voltage applications, MLIs are widely used as one of the advanced power converter topologies. To produce high-quality output without the need for a large number of switches, development of reduced switch MLI (RS MLI) topologies has been a major focus of current research. Therefore, this review paper focuses on a number of recently developed MLIs used in various applications. To assist with advanced current research in this field and in the selection of suitable inverter for various applications, significant understanding on these topologies is clearly summarized based on the three categories, i.e., symmetrical, asymmetrical, and modified topologies. This review paper also includes a comparison based on important performance parameters, detailed technical challenges, current focus, and future development trends. By a suitable combination of switches, the MLI produces a staircase output with low harmonic distortion. For a better understanding of the working principle, a single-phase RS MLI topology is experimentally illustrated for different level generation using both fundamental and high switching frequency techniques which will help the readers to gain the utmost knowledge for advance research.

INDEX TERMS Control techniques, drives application, fundamental switching frequency, high switching frequency, multilevel inverter (MLI), performance parameters, photovoltaic (PV) systems, reduced component count, renewable energy application.

I. INTRODUCTION

The ever-increasing electrical energy demand has caused intense depletion of conventional energy sources. This has also resulted extensive research in renewable energy source (RES)-based power generations. Especially Solar and wind energy are the two major renewable sources gaining more and more interest among power electronics as well as power system research community instead of their high dependence on varying environmental conditions [1]–[3]. This requires new power converter technologies for desired operation, control, and power management, in order to enhance the power quality and to yield utmost power from RESs [4]–[6].

The essential part of renewable energy power conversion system is an inverter which converts the DC power to AC as required by the grid/loads. A conventional two/three-level inverter is mostly used in small scale industries and

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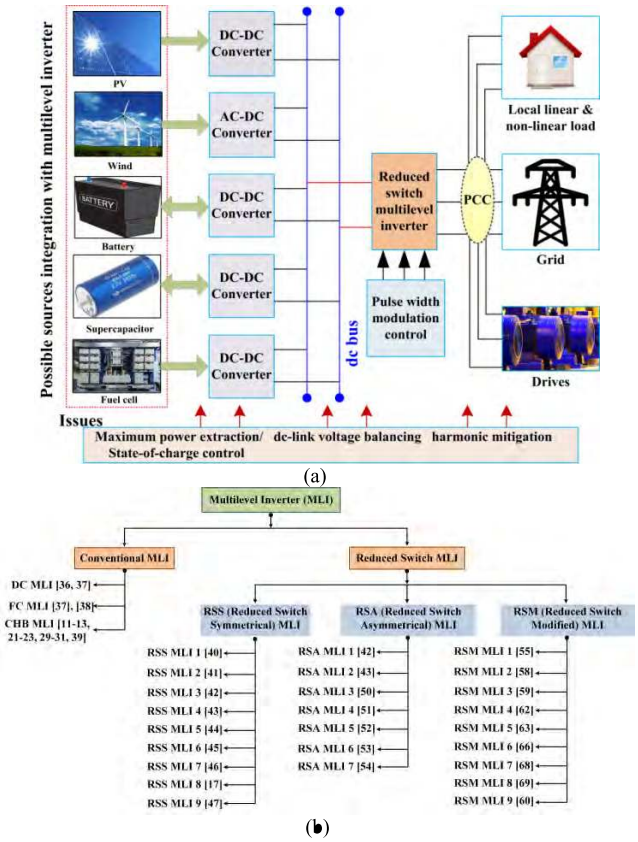


FIGURE 1. **(a) Possible energy sources with reduced switch MLI-based system. (b) Researchers contribution in this field which includes classification of different MLIs.**

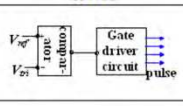
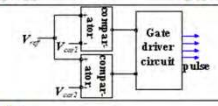
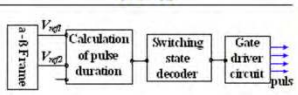
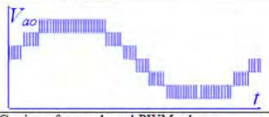
utility applications [7]. However, the output of these inverters contain more harmonics, hence the usage of expensive and bulky low pass passive filters are desired before feeding the power to the utility grid. Further, high voltage stress and high switching loss forbears the application of these inverters in high power application [8]. Consequently multilevel inverters (MLIs) are evolved as best substitute for medium and high power conversion systems. The concept of MLI topology was first introduced in the early 1975 [9] followed by different variations of it [10], [11]. These MLIs continue to receive more and more attention because of their high voltage operation capability, low switching losses, high-efficiency and low electromagnetic interference. MLIs have the ability to meet the increasing demand of power rating with improved power quality through subsequent reduction in the harmonic distortion. MLIs are capable of producing a high-quality staircase ac voltage from different connection of power semiconductor switches and single/several dc voltages through low switching frequency operation and thus mostly preferred for medium and high power conversion systems [12], [13]. The input dc sources can be a battery, fuel cell, supercapacitor, renewable energy system, etc. A generic block diagram with possible integration of different sources with MLI is shown in Fig. 1(a). MLIs are widely used in various applications such as large electric drive, renewable energy conversion, traction, electric vehicle, active power filter, HVDC, and FACTs [14]–[16].

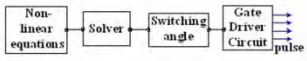
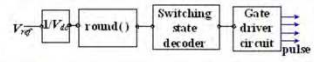
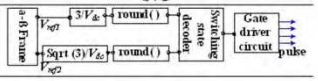
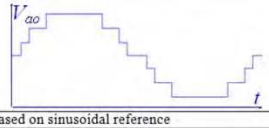
The key features of an MLI are; output waveform with less distortion and less THD content, operation at both fundamental and high switching frequency PWM, a number of redundant switching states, smaller common-mode voltage, etc [12]–[15]. But, one common disadvantage is the need of large number of power semiconductor switches. Each switch requires a gate driver circuit which adds complexity to the system and the overall system cost. Therefore, design of MLIs using low number of components to produce higher output voltage levels are one of the key research issues.

With the advancement in MLI topologies, challenges appeared in controlling and modulation of these inverters. Some lower order dominant harmonics exists in the stepped output voltage waveform produced by an MLI. The major impacts of those harmonics are voltage fluctuation, increase in loss, mal-operation, and it also affects the power quality. With the application of appropriate control scheme for an MLI, the aforesaid issues can be well addressed [17]. Researchers have come with a solution of diverse modulation strategies for controlling the MLI. Overall loss reduction and improvement in harmonic profile are the major objective of most of the control techniques discussed in literature [18]–[32]. Among the two basic types of control strategies, fundamental/low-frequency switching can provide superior performance than high-frequency switching techniques [18]. Conventional pulse width modulation (PWM), sinusoidal PWM and space vector modulation (SVPWM) are high-frequency switching techniques which provide faster transient response [19], [20]. Furthermore, different carrier based PWM techniques are introduced that effectively reduces distortion and lowers the EMI [15]. Carrier based PWM techniques are generally of two types, *i.e.*, phase-shifted PWM (PS-PWM) and level-shifted PWM (LS-PWM) techniques [21], [22]. In a PS-PWM control technique, multiple phase-shifted synchronous carriers are required with synchronization of zero crossing of each carrier and voltage reference [23], whereas in LS-PWM technique only one carrier is enough to implement different voltage levels. The former approach is mostly used to evenly distribute the power among MLI modules and to reduce the harmonic distortion. The LS-PWM technique [24] is again classified into three major categories such as phase disposition PWM (PD-PWM), phase opposition and disposition PWM (POD-PWM), and alternative phase opposition and disposition PWM (APOD-PWM). All these PWM topologies have either bipolar or unipolar type carrier arrangements with a focus on improving the fundamental output voltage and reduction in total harmonic distortion (THD).

High-order harmonics can be suppressed using low-pass filters for improving inverter efficiency. But, lower-order harmonics such as 3rd, 5th, and 7th are dominant in nature and may not be completely eliminated using aforesaid high-frequency switching techniques. A fundamental frequency modulation approach known as selective harmonic

TABLE 1. Classification of control schemes for the MLI.

Parameters	High Switching Frequency			
	SPWM	LSPWM	PSPWM	SVPWM
Principle of Operation				
Output voltage pattern				
Mechanism	Sine wave based reference switching scheme	Carrier reference based PWM scheme		Based on reference vector with variable magnitude and constantly rotating fundamental frequency
Advantage	• No rigorous offline calculation is needed • Easy implementation • No optimization technique required	• Performs superiority in THD minimization • Easy implementation	• DC voltage ripples can be minimized • Less loss • Best suitable for FC and CHB based topology	• Switching redundancy is more • Controlled switching sequence • Low THD
Disadvantage	• Switching loss is more	• Complexity in control over capacitor voltage balance problem • Not suitable for FC and CHB based topology	• More THD • Synchronization is an issue for higher level generation	• Switching scheme is very complex • Clarke transformation is required for 1-ph application
Reference	[19, 47, 54, 96, 97, 99]	[21, 24, 58, 83, 90]	[22, 23, 43, 44, 90-92, 94, 95]	[19, 20, 67, 73, 75, 80, 82, 100]

Parameters	Fundamental/ Low switching Frequency		
	SHE	NLC	SVC
Principle of Operation			
Output voltage pattern			
Mechanism	Based on offline/online calculation	Based on sinusoidal reference	Reference based switching scheme
Advantage	• Switching loss and electromagnetic interference are less • THD can be minimized up to a very low level • Applicable for higher power application	• Better quality output voltage • Ripples in load current are very less • Computational time and complexity are very less	• For higher level output it efficiently reduces THD and ripple in the output waveform • Best suitable for higher level application
Disadvantage	• Includes offline calculation and difficulty in implementation of optimization techniques • With the increment of levels number of non-linear equation increases though resulting in the number of harmonic eliminated increase, which increases MLI output voltage quality	• Not efficient in dynamic performance • Finding nearest level is not simpler always • THD minimization is not competent	• Lower order dominant harmonics can't be eliminated • Appropriate synthesis of nearest vector is difficult
Reference	[17, 25-27, 30, 47, 132-141]	[31, 32, 62, 77]	[12, 13]

elimination (SHE) or programmed PWM technique [25], [26] is thus used to determine optimal switching angles to eliminate specific low-order harmonics by solving nonlinear transcendental equations. Colonical competitive algorithm (CCA), genetic algorithm (GA), bee algorithm (BA), cuckoo search algorithm (CSA), particle swarm optimization (PSO), bat optimization algorithm (BOA), etc. are few evolutionary optimization SHE techniques critically surveyed for MLIs in [27]. An approach closely based on SHE called as selective harmonic mitigation technique has been analyzed in [28]–[30]. Nearest level control (NLC) is another fundamental frequency modulation technique frequently used in MLIs [31], [32]. Some evidence regarding the different switching control strategies are summarized in Table 1.

A review on the traditional MLI topologies for various applications was disclosed in [13]–[15]. The authors in [33] discussed on quantitative and qualitative aspects nine different reduced switch MLI (RS MLI) topologies and a review on only few cross-connected sources-based MLI topologies has been detailed in [4]. Agrawal and Jain [34] have studied only six RS MLI topologies for grid-tied applications. An assessment on detailed insight to various control techniques with different RS MLI topologies has been proposed in [35]. These enormous research developments on RS MLI topologies necessitate special focus on this area which can discuss on its application and practical implementation.

Next section presents a brief overview on conventional MLI topologies. Uniqueness of this review article lies in its key focus on the various most recently developed MLI topologies under three different categories such as symmetric, asymmetric and modified configurations illustrated in Section III. This section also includes a comparison among MLI topologies with respect to switch count, number of dc source, peak inverse voltage (PIV) rating, total standing voltage (TSV) on the switches, and switching loss. Section IV includes a discussion on aforementioned reduced switch symmetric H-bridge type MLI (RSS MLI), reduced switch asymmetrical H-bridge type MLI (RSA MLI), and reduced switch modified MLI (RSM MLI) topologies. The classification of RS MLI topologies considered for review in this work is shown in Fig. 1(b). Some of the parameters required for the performance evaluation of an MLI are presented in section V. In section VI, experimental results for one of the single-phase MLI topology using reduced component count are presented for illustration purpose only which shows the staircase output of the 5-level, 7-level, and 9-level MLIs with

TABLE 2. Classification & features of conventional MLI.

Parameters	Diode clamped MLI (DC MLI) [36], [37]	Flying capacitor MLI (FC MLI) [37], [38]	Cascaded H-bridge MLI (CHB MLI) [12], [13], [21]–[23], [29]–[31], [39]
Switch count in terms of number of level (N_l)	$2(N_l\text{-}1)$	$2(N_l\text{-}1)$	$2(N_l\text{-}1)$
Number of dc sources	1	1	$(N_l\text{-}1)/2$
Number of diodes	$(N_l\text{-}1)*(N_l\text{-}2)$	0	0
Number of capacitors	$(N_l\text{-}1)$	$N_l*(N_l\text{-}1)/2$	0
Zero level generation	Clamping diodes and switches	Clamping capacitors and switches	Only semiconductor switches/diode
Key features	• Requires only one dc source as input • Highly reliable and more efficient structure in fundamental switching frequency	• Only one isolated dc source is involved • More flexibility to control active and reactive power	• Lesser components are involved • Scalable, simplicity, and highly modular circuit layout
Shortcomings	• For higher level generation, large number of capacitors and clamping diodes are required • Voltage balancing is difficult	• Involves larger number of capacitors to get higher levels • The structure becomes bulky & expensive for high power application	• More number of semiconductor switches are involved • Requires a number of isolated dc sources
Suggested applications	• Low - medium voltage • Ac motor drive applications and PV application	• Low - medium voltage • Drives application	• Medium - high voltage • Drives, electric vehicle, and renewable energy applications

two different control techniques. SHE is a popular fundamental switching technique which completely eliminates the dominant lower order harmonics which is thus used for the controlling the developed MLI topology on the other hand to show the difference between the fundamental and high switching frequency techniques; SPWM (high switching frequency) control technique is also implemented. Section VII briefly summarizes the technical challenges, current research focus, and future development perspective of MLI. Concluding remarks are drawn in Section VIII.

II. CONVENTIONAL MULTILEVEL INVERTER TYPES

MLIs are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with an improved harmonic spectrum and attain higher voltage with a limited maximum device rating. With the proper arrangement of power switching semiconductor devices and voltage sources, a multilevel output can be produced. An overview of three conventional MLI types, *i.e.*, diode clamped MLI (DC MLI), flying capacitor MLI (FC MLI), and cascaded H-bridge MLI (CHB MLI) are summarized in Table 2.

III. REDUCED SWITCH MLI TOPOLOGIES

Although the aforementioned conventional topologies finds numerous applications, but all these topologies needs excess number of power components. So, in the last couple of decades the focus of research on MLI among the researchers is to reduce the device count. Reducing the total number of switches, diodes, capacitor, voltage source can improve the reliability as well as can reduce the overall cost, loss, etc. In this regard, several new RS MLI topologies have been proposed recently and continuous research is still going on to further reduce the requirement of number of components.

This paper presents a compressive review on some recently developed topologies which are most suitable in different applications such as machine drives, FACTs, and renewable energy systems. These topologies can be used in grid-tied as well as in standalone applications. RS MLI topologies are broadly categorized into three types, *i.e.*, RSS MLI, RSA MLI, and RSM MLI. The modified type MLI includes all the hybrid and topologies which are not based on H-bridge.

A. REDUCED SWITCH SYMMETRIC H-BRIDGE TYPE MLI (RSS MLI)

The term symmetric indicates that, all the dc sources used in the circuit are equal in magnitude. Babaei *et al.* proposed a new cascaded MLI in [40]. The basic unit of the proposed MLI contains two unidirectional semiconductor switches with one dc source. As compared to the conventional CHB MLI, a significant reduction in switch count has been marked in this topology. But, the reduction in switch count is not competitive when compared to recently developed RSS MLI topologies discussed in this work. Furthermore, higher TSV restricts it in high voltage applications. Fig. 2(a) depicts the schematic diagram of this topology. A new MLI topology with nine different algorithms for the determining the magnitude of dc voltage source has been proposed in [41]. This MLI type has a basic unit consisting of six unidirectional switches and two dc sources. This MLI topology has been shown in Fig. 2(b). Fig. 2(c) shows a novel MLI topology discussed in [42] for low-voltage applications. In this literature, an attempt is made to reduce the number of voltage source requirement. For the multilevel generation in the output, two capacitors are used in each module. The capacitor rating is half the rating of the voltage source used in the MLI and the number of capacitor increases with the increase in number of levels. Although the rating of the capacitor is reduced compared to a single capacitor, but the total number of components are more for producing higher levels. The complexity in charging and voltage balancing issues may also arise in such a condition. This MLI can operate in both symmetric and asymmetric mode. In [43], the authors have

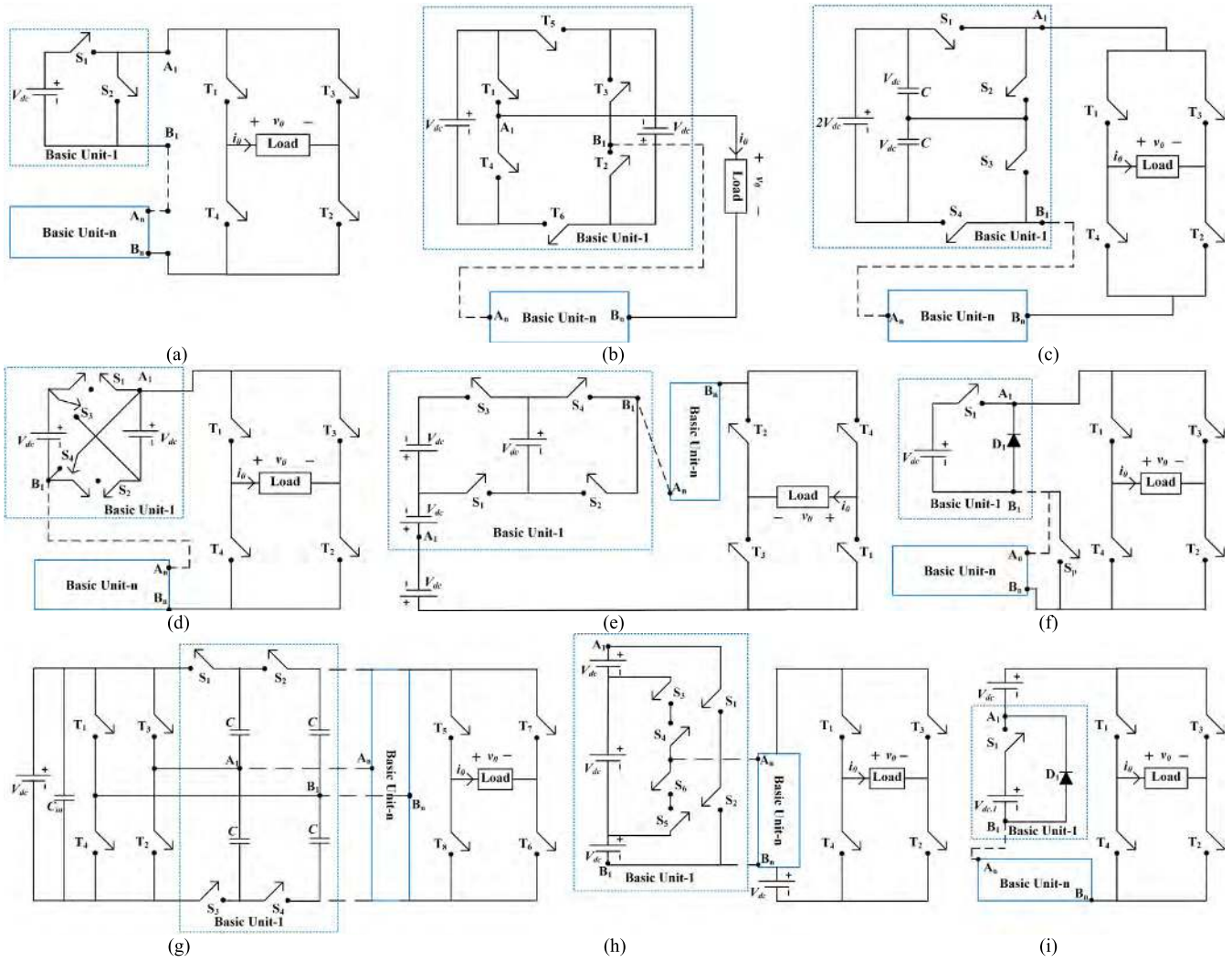


FIGURE 2. Generalized schematic of the RSS MLI topologies (a) RSS MLI 1. (b) RSS MLI 2. (c) RSS MLI 3. (d) RSS MLI 4. (e) RSS MLI 5. (f) RSS MLI 6. (g) RSS MLI 7. (h) RSS MLI 8. (i) RSS MLI 9.

proposed a new cascaded MLI which can be formed by the cascaded connection of several basic units containing four switches and two dc sources per basic unit. Involvement of two bi-directional switches in the basic unit causes more standing voltage. A schematic of this topology has been shown in Fig. 2(d).

Basic unit of another symmetrical MLI proposed in the literature [44] contains three equal magnitude dc sources with four switches. In order to generate higher number of levels, cascaded connection of desired number of basic units has to be made with one extra series connected dc source. Negative polarity voltage is obtained with the help of H-bridge. A significant reduction in number of switches and lowering of total voltage stress is a major advantage of this topology, thus it can be recommended for higher power and higher voltage applications. This topology can also be used as an alternative to the conventional topology for RES applications, as it uses less number of switches than a CHB MLI & with same number of dc sources. This topology has been illustrated in Fig. 2(e).

Wang *et al.* proposed a novel cascaded MLI containing switched diodes [45]. This topology shown in Fig. 2(f) effectively reduces the need of large number of switches as compared the conventional CHB MLI and cascaded half bridge topology presented in [40], but contains some additional diodes. The proposed topology is basically divided into two stages. First stage is responsible for the level generation and the second stage which is nothing but the H-bridge helps in polarity generation. One attractive feature of this topology is that the first stage contains a spike removal switch which removes the high voltage spikes produced at the base. Again to avoid the fluctuations of dc source in case of renewable application, the author had developed clock phase-shifting one-cycle control strategy. Due to the high voltage rating of spike removal switch and H-bridge switches, the topology is restricted to medium voltage application only.

TABLE 3. Comparison between RSS MLI topologies for producing N_l output voltage levels.

Parameters	CHB MLI [21]–[23]	RSS MLI [40]	RSS MLI [41]	RSS MLI [42]	RSS MLI [43]	RSS MLI [44]	RSS MLI [45]	RSS MLI [46]	RSS MLI [17]	RSS MLI [47]
N_{sw}	$2(N_l-1)$	(N_l+3)	$3(N_l-1)/2$	(N_l+3)	$3(N_l+5)/2$	$2(N_l+3)/3$	$(N_l+9)/2$	$2(N_l+11)/3$	(N_l+1)	$(N_l+5)/2$
N_l	$2n+1$	$2n+1$	$4n+1$	$4n+1$	$4n+1$	$6n+3$	$2n+1$	$6n+1$	$6n+3$	$2n+3$
N_{dc}	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/4$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$	1	$(N_l-1)/2$	$(N_l-1)/2$
N_d	0	0	0	0	0	0	$(N_l-1)/2$	0	0	$(N_l-3)/2$
N_c	0	0	0	0	0	0	0	$2(N_l+1)/3$	0	0
TSV	$2(N_l-1)$	$3(N_l-1)$	$2(N_l-1)$	$2(N_l-1)$	$3.5(N_l-1)$	$3N_l-5$	$3N_l-4$	$(8N_l+4)/3$	$(23N_l-45)/6$	$(5N_l-7)/2$
PIV	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$

A novel MLI based upon switched-capacitor modular structure has been presented in [46]. This topology shown in Fig. 2(g) was proposed to be controlled using an optimized SPWM technique such that energy conversion efficiency and power density will be enhanced. In [17], a hybrid cascaded MLI containing one H-bridge shown in Fig. 2(h) has been discussed. Reduction in switch count to reduce the cost as well as the THD was significantly achieved and GA-based SHE-PWM approach has been utilized for the control of MLI. This proposed topology can find its suitability in renewable power generation system involving PV and fuel cells.

In [47], a novel RS MLI is introduced. Compared with the conventional MLI and few recently developed MLIs [24], [48], [49], the proposed MLI shown in Fig. 2(i) has a drastic reduction in number of switches. It requires less than 50% of total switches that are used in the conventional CHB MLI. Lower order harmonics are most dominant in the output of an MLI. Using filters the harmonic profile can be improved, but still there is an impact of lower order dominant harmonics. The author has taken an attempt to eliminate some particular lower order harmonics by calculating optimal switching angles using the SHE technique. To solve the non-linear transcendental equations involved with the SHE technique, author had developed a modified particle swarm optimization technique. As a whole, issues related to large number of switches and harmonic elimination has been addressed by the authors. This topology can find its suitability in higher voltage or high power application and with renewable energy integration. Table 3 summarizes the comparison of RSS MLI topologies with regard to switch count (N_{sw}), dc source count (N_{dc}), number of diodes (N_d), number of capacitors (N_c), TSV, and PIV.

B. REDUCED SWITCH ASYMMETRICAL H-BRIDGE TYPE MLI (RSA MLI)

An MLI is said to be asymmetric when all the input dc sources used are not equal in magnitude. The main goal of developing the asymmetric MLI is to generate higher number of output voltage levels with the same number of switches and dc sources that are used in symmetric MLI. A variety of relation can be considered for the unequal dc sources. In this paper the relation is taken in a geometric progression manner with the multiplication factor of '3' for a comparative analysis. Fig. 3(a) shows an asymmetrical structure of cascaded H-bridge MLI (ACHB MLI) [11] which presents a new pathway for producing staircase output using non-identical dc sources. A schematic of RSA MLI topologies [42], [43] shown in Fig. 3(b) & 3(c) can operate both in symmetric and asymmetric mode. Description on these topologies is given in Section IIIA.

The authors in [50] conferred a modularized MLI configuration having the basic unit consisting of two switches and one dc source. In the asymmetric mode the modularization is lost because of unequal dc sources, but still the proposed topology can be extended with a proportional factor. The polarity generation switch faces more voltage stress than the level generation switches and these switches operate at the fundamental switching frequency. Switching pulse generation based on unipolar PWM technique has been outlined in detail. The author had verified that the obtained total harmonic distortion (THD) in asymmetric mode operation satisfies the IEEE-519 standard. Other performance parameters such as crest factor and distortion factor are also evaluated for different modulation indices. The proposed topology doesn't require any clamping diode and capacitors, so the voltage balancing problem is completely eradicated. In addition, a considerable reduction in number of switches has been observed in comparison with the conventional MLI topologies. The representation of this topology is unveiled in Fig. 3(d).

The authors in [51] conferred a novel cascaded switched diode topology which can operate in both symmetric and asymmetric mode. The structure of this MLI has been shown in Fig. 3(e) which is the combination of a basic unit and an H-bridge. The basic unit produces a staircase output voltage which is connected to an H-bridge for the polarity generation. The basic unit consists of a dc source, one switch, and one diode. The author has also developed a cascaded structure of this topology. A drastic reduction in number of switch has been observed to generate a particular level of output voltage as compared to a CHB MLI topology. The author has suggested an algorithm for the determination of magnitude of dc sources. Requirement of extra diode puts a limit to the number of level generation by the MLI topology.

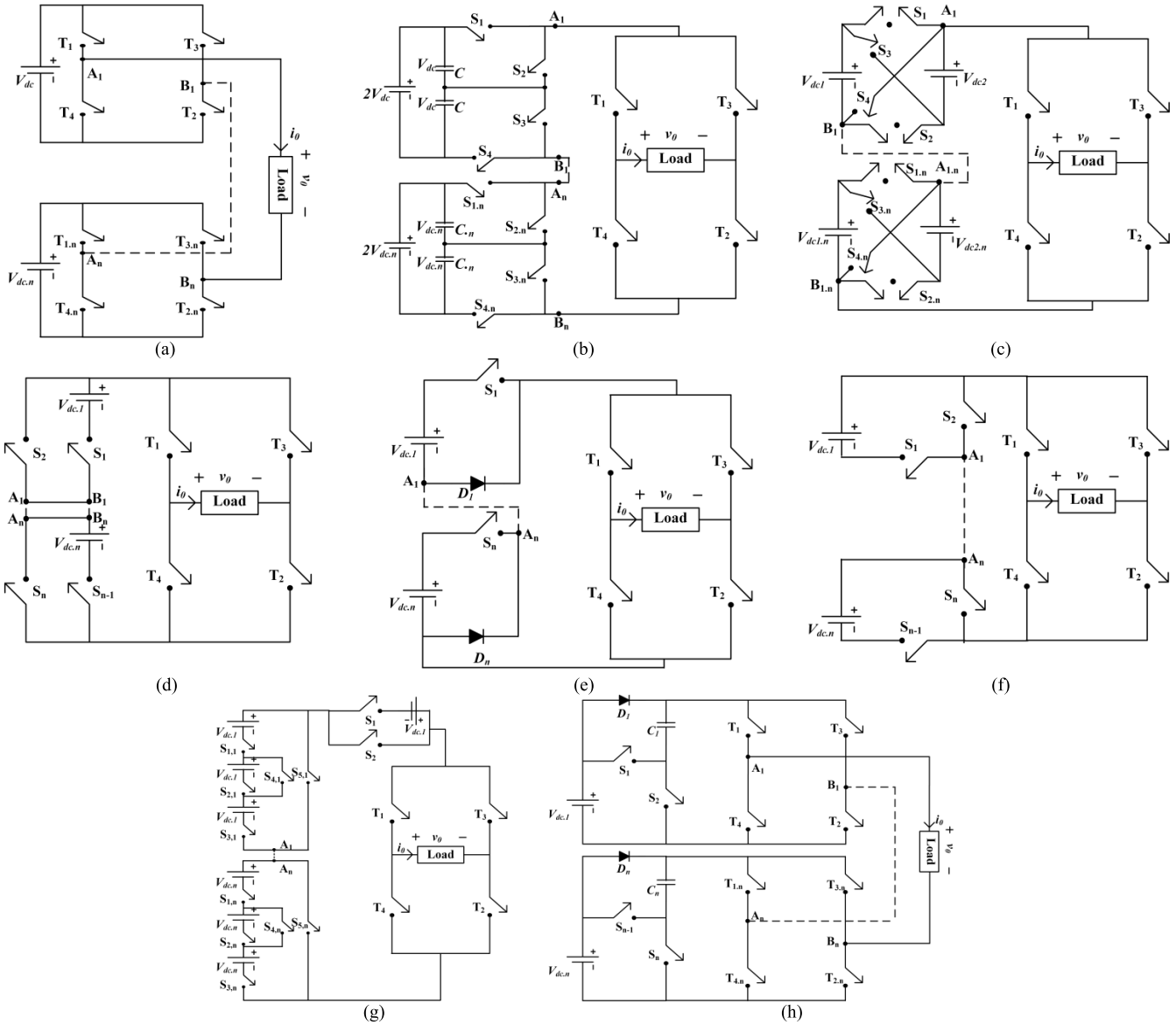


FIGURE 3. Generalized schematic of the RSA MLI topologies (a) ACHB MLI. (b) RSA MLI 1. (c) RSA MLI 2. (d) RSA MLI 3. (e) RSA MLI 4. (f) RSA MLI 5. (g) RSA MLI 6. (h) RSA MLI 7.

Another novel RS MLI topology containing a half-bridge cell as basic unit has been proposed in the literature [52]. The half-bridge cell consists of an isolated dc source and two switches. This MLI has been derived by the combination of series connected half-bridge cells and an H-bridge. The generalized topology has been shown in Fig. 3(f). Author has suggested that in order to minimize the switching loss, the switches in H-bridge has to be turned off at zero voltage and should be turned on at both zero voltage and zero current. The diode clamped and flying capacitor structure of the same MLI type has also been analyzed by the author. The main feature of this topology is the requirement of reduced number of switches; however the high voltage rating H-bridge switches limits its application to medium voltage level.

The MLI structure shown in Fig. 3(g) presented in the literature [53] can be used for medium to high voltage applications. The authors have given an equal attention towards the reduction of both TSV and component count. One additional compact network has been utilized in series with the basic units to further boost the voltage levels. Another MLI topology in the literature [54] is based upon the cascade connection of H-bridges. This topology shown in Fig. 3(h) is very much suitable for high switching frequency distribution system. However, in asymmetrical mode of operation, capacitance sizing and voltage balancing problems may arise. To confront this issue, additional voltage balancing circuit need to be introduced in the aforesaid situation. Table 4 gives a comparison of RSA MLI topologies with regard to N_{sw}, N_{dc}, N_d, N_c, TSV, and PIV.

TABLE 4. Comparison between RSA MLI topologies with respect to number of dc sources used.

Parameters	ACHB MLI [11]	RSA MLI [42]	RSA MLI [43]	RSA MLI [50]	RSA MLI [51]	RSA MLI [52]	RSA MLI [53]	RSA MLI [54]
N_{sw}	$4m$	$4(m+1)$	$3m+4$	$2m+4$	$m+4$	$2m+4$	$(5m+13)/3$	$6m$
N_l	3^m	$2(3^m)-1$	$2(3^{m/2})-1$	3^m	3^m	3^m	$3^{(m+2)/3}$	$2(3^m)-1$
N_d	0	0	0	0	m	0	0	m
N_c	0	$2m$	0	0	0	0	0	m
TSV	$2(3^m-1)$	$3(3^m-1)$	$2(3^{(m+2)/2}-2)$	$3(3^m-1)$	$2.5(3^m-1)$	$3(3^m-1)$	$19(3^{(m-1)/3})-15$	$5(3^m-1)$
PIV	$(3^m-1)/2$	$(3^m-1)/2$	$(3^{m/2}-1)$	$(3^m-1)/2$	$(3^m-1)/2$	$(3^m-1)/2$	$1.5(3^{(m-1)/3})-1$	(3^m-1)

C. REDUCED SWITCH MODIFIED MLI (RSM MLI)

Topologies without an H-bridge are considered in this section. Basically H-bridge topologies are more suitable for the low and medium voltage application. More voltage stress on the H-bridge switches of these topologies narrows down the applicability in high voltage application. In turn efficiency may reduce when used in high voltage applications. These issues have lead to devise some new topologies which have inherent feature of polarity generation. Some recently developed topologies of this category are discussed in this section.

Based on the switched dc source Gupta *et al.* introduced a new topology [55] consisting of the dc sources alternately in opposite polarity across the switches. A schematic of this topology has been illustrated in Fig. 4(a). The main aim of the topology is to produce a large number of levels in the output by reducing the total component count. Total component count in this MLI is less than the conventional MLI topologies, but due to the use of bi-directional switches, the voltage stress and switching loss is more than few recently developed topologies discussed earlier in this work. Total voltage stresses across the switches, diodes, and the isolated dc sources of this topology are same as a CHB MLI topology. Furthermore this topology possess a limited number of redundant switching states as compared to the conventional topologies, hence the cells under fault condition can't be bypassed. It can be said that, modularity and the fault tolerant capacity of this topology is less than the CHB MLI topology.

The topology shown in Fig. 4(a) has a structural similarity with the packed U cell (PUC) MLI analyzed in the literature [56]. This MLI consists of a single dc source and a dc-link capacitor, thus the requirement of dc sources is drastically reduced compared to conventional CHB MLI as the level increases. Number of switches used in this topology is same as the MLI shown in Fig. 4(a) for producing 5-levels in the output. Availability of more redundant switching states is an additional advantage of this topology which reduces the voltage balancing concern. Requirement of sensors for controlling the MLI & maintaining the desired capacitor voltage can also be reduced as suggested by the authors. A modified version of this topology detailed in the literature [57] is also suitable for PV applications. An MLI topology with cascaded basic blocks was proposed by Mokhberdoran and Ajami in [58]. The topology contains the series connection of fundamental blocks. The combination of six switches, two dc sources and eight diodes makes fundamental block. Fig. 4(b) depicts the circuit diagram of this topology. Author has validated the topology in both symmetric and asymmetric mode and found that the asymmetric mode produces a high resolution output voltage waveform for the same number of basic block. The proposed topology requires less number of switches as compared to the conventional MLIs, but not compared other recently proposed RS MLIs. Also, it requires large number of extra diodes to form a basic block which can be considered as a limitation of the topology. However, this topology is suitable in medium and high voltage applications. A new cascaded MLI topology was proposed in the literature [59]. Fig. 4(c) shows the generalized circuit topology of this MLI. The power circuit of this cascaded MLI consists of two dc sources, two different bridges and one auxiliary bi-directional current steering circuit. One among the two dc sources is split in two equal half by the auxiliary circuit, so in overall three dc sources are used in each power circuit. A carrier-based PWM strategy has been adopted for controlling the MLI and the superiority of this MLI has been validated through comparison with well-known MLI topologies disclosed in the literature [43], [60], [61].

A novel hybrid T-type topology was proposed in [62] for high efficiency application. An attempt was made to reduce the switching loss by reducing the requirement of large number of switches. The topology requires only one voltage source as shown in Fig. 4(d). A number of capacitors are connected for the multiple level generations in the output. Availability of redundant switching states avoids the capacitor voltage balancing problem and improves the fault-tolerant capability. An interesting control method based on phase-disposition PWM (PD-PWM) method has been analyzed for controlling the operation of MLI through capacitor voltage balancing. The proposed controlled scheme can be easily generalized for high power MLIs. The efficacy of this topology has been validated with different transient test cases such as change in nominal frequency; change in switching frequency, and at different modulation indices.

A novel envelope type RSA MLI was proposed in [63]. The proposed MLI module consists of four dc sources, six unidirectional switches, and two bi-directional switches. Each module produces thirteen level output voltage waveform without any additional circuit. This topology achieves a drastic reduction in number of switches and there are no

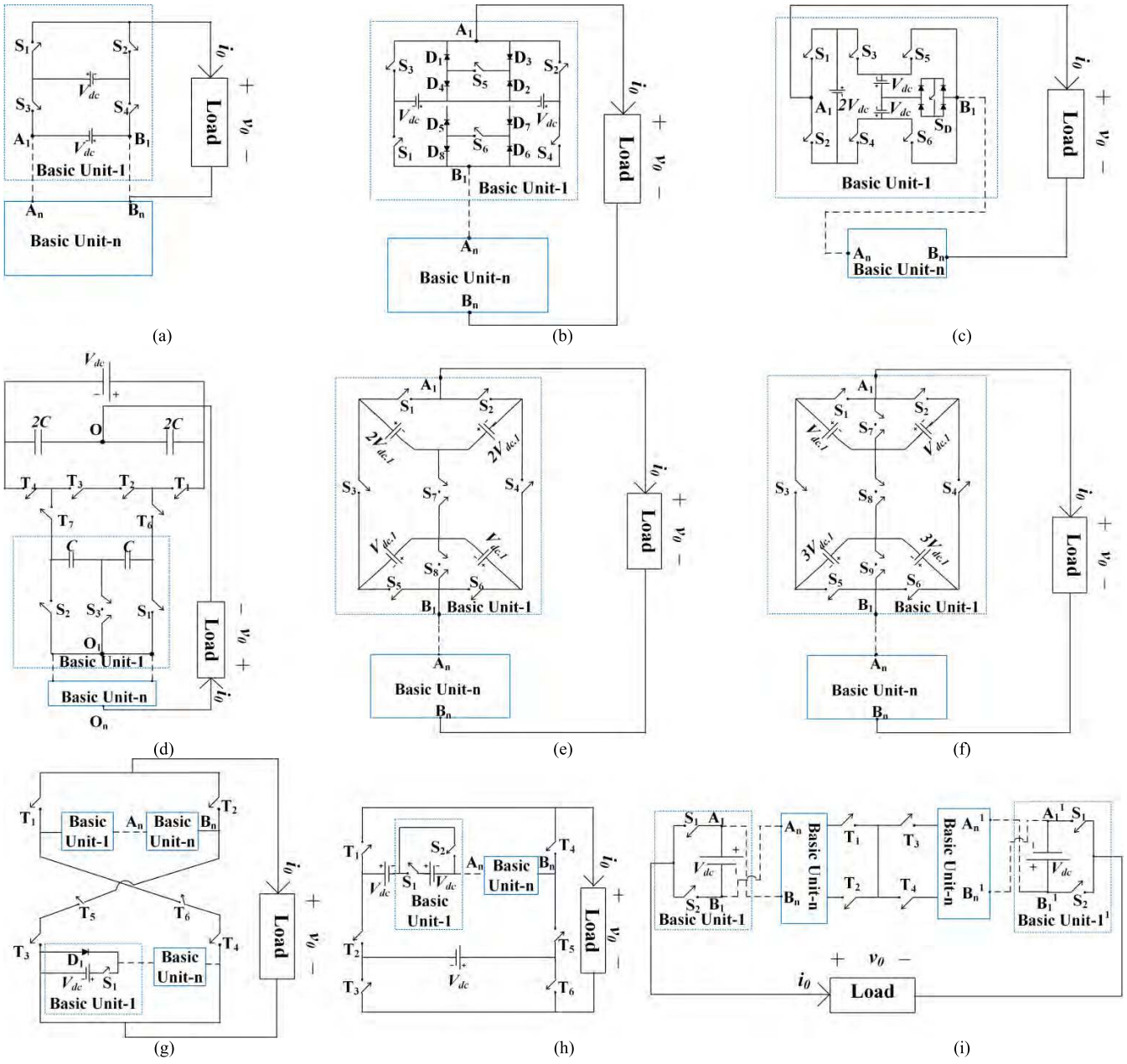


FIGURE 4. Generalized schematic of the RSM MLI topologies (a) RSM MLI 1. (b) RSM MLI 2. (c) RSM MLI 3. (d) RSM MLI 4. (e) RSM MLI 5. (f) RSM MLI 6. (g) RSM MLI 7. (h) RSM MLI 8. (i) RSM MLI 9.

diodes/capacitors are used, so the complexity and voltage balancing problems are avoided. Modularity of the topology can be achieved by cascading the E-type modules. Fig. 4(e) depicts the generalized structure of the topology. Author had applied SHE-PWM technique to control the MLI by calculating optimum switching angles which results in low THD. Lower voltage stress on the switch and lower THD makes this topology suitable for high voltage and high power applications. Authors have also critically analyzed the superiority of this MLI compared to recently developed topologies in [40], [42], [58], [64], [65]. A new square T-type module-based RSA MLI was proposed by the same authors in [66]. Fig. 4(f) shows the generalized structure of this topology. Four dc sources and twelve switches constitute a module and each module generates a seventeen level output voltage. To achieve more levels the cascaded connection of modules can be made. A nearest level control method is used for generating switching pulses which reduces computational burden of the processor. Moreover the ability of generating more levels, less THD with a demand of less number of switches and dc sources makes the topology superior among other topologies developed in [40]–[42], [65], [67].

Authors in [68] investigated a new crisscross switched RSA MLI comprising of semi half-bridge cells. One semi

TABLE 5. Comparison between RSM MLI topologies for producing N_l output voltage levels.

Parameters	RSM MLI [55]	RSM MLI [58]	RSM MLI [59]	RSM MLI [62]	RSM MLI [63]	RSM MLI [66]	RSM MLI [68]	RSM MLI [69]	RSM MLI [60]
N_{sw}	(N_l+1)	$3(N_l-1)/2$	$7(N_l-1)/8$	(N_l+5)	$5(N_l-1)/6$	$3(N_l-1)/4$	$(N_l+11)/2$	(N_l+1)	$3(N_l-1)/2$
N_l	$2n+1$	$4n+1$	$8n+1$	$4n+1$	$12n+1$	$16n+1$	$2n+1$	$2n+5$	$2n+1$
N_{dc}	$(N_l-1)/2$	$(N_l-1)/2$	$3(N_l-1)/8$	1	$(N_l-1)/3$	$(N_l-1)/4$	$(N_l-1)/2$	$(N_l-1)/2$	$(N_l-1)/2$
N_d	0	$2(N_l-1)$	$(N_l-1)/2$	0	0	0	$(N_l-1)/2$	0	0
N_c	0	0	0	$(N_l+3)/2$	0	0	0	0	0
TSV	$2(N_l-1)$	$5(N_l-1)/2$	$13(N_l-1)/16$	$(N_l+9)/4$	$5(N_l-1)/3$	$5(N_l-1)/2$	$9(N_l-1)/4$	$3N_l-7$	$3(N_l-1)$
PIV	$(N_l-1)/2$	(N_l-1)	$11(N_l-1)/8$	1	$5(N_l-1)/12$	$(N_l-1)/2$	$(N_l-3)/2$	N_l-1	$2(N_l-1)$

half-bridge cell is composed of one dc source, one diode, and one switch. To generate higher levels, more semi half-bridge cells can be connected in series fashion. The generalized structure is formed by connecting the string of series connected semi half-bridge cells in crisscross manner through the switches as shown in Fig. 4(g). The proposed topology achieves its purpose of staircase output by using reduced number of switches and having less standing voltage. However, the requirement of extra diodes increases with the addition of output voltage levels. A new structure of cascaded MLI with the aim of improving the system performance has been investigated in [69]. This proposed topology is represented in Fig. 4(h). The generalized structure consists of series connected cells, six main switches and one dc source with a proper arrangement. The combination of one dc source and two switches forms a sub-cell of this configuration. The main feature of the topology is that without requirement of any diodes and capacitors, more levels can be generated with less number of switches (almost 50% less as required by conventional CHB MLI) resulting in less standing voltage and low peak inverse voltage. To reduce the voltage stress, inverter cost as well the installation area a novel cascaded MLI was analyzed in [60] which can operate in both symmetric and asymmetric mode requiring less number of switches. Fig. 4(i) unveils the proposed topology. Although the superiority of this topology is found over conventional CHB MLI in terms of reduced number of switches, but the standing voltage of the proposed topology is more as compared to CHB MLI restricting the application to low and medium voltage applications. A comparison of RSM MLI topologies with regard to N_{sw}, N_{dc}, N_d, N_c, TSV, and PIV is detailed in Table 5.

IV. DISCUSSION

Different MLI topologies have been reviewed in the previous section. It is clear from the review that in order to verify the feasibility, several switching techniques have been investigated by the researchers. The theoretical studies have been validate using simulation platform as well as verified using experimental tests. Different controllers such as microcontroller, digital signal processor (DSP), dSpace have been utilized for the experimental tests. So, in this section all the aforementioned RSS MLI, RSA MLI, and RSM MLI topologies have been summarized in Table 6, 7, and 8, respectively in term of switching pulse generation techniques, simulation/experimental validation, design specifications, calculated parameters, and different application suggested by the author. This will help the researchers to opt suitable switching technique, controller, etc. while designing a new MLI topology for various applications.

V. PERFORMANCE ANALYSIS OF MLI

As discussed in the previous section, a variety of RS MLIs are proposed by the researchers in the last decade. These should be chosen carefully keeping in view of the optimal performance parameters. Main parameter which decides the performance, cost, and complexity of an MLI are as follows:

A. OVERALL COST ANALYSIS

It is noteworthy that with increase in component count, overall cost of the MLI increases. Higher cost is the primary reason that forbear a conventional MLI topology from use in different applications. Thus, it is essential to compute the total cost while designing the novel RS MLI topologies. Mainly number of semiconductor switches, number of drivers, diodes count, and number of capacitors involved in an MLI decide the cost. In addition, TSV and PIV are to be given equal importance while selecting the rating of these components, which contributes to the overall cost. In this regard, cost of few insulated-gate-bipolar transistors (IGBT) switches, diodes with a fixed current rating of 75 A for a wide range of voltage, cost of mostly used isolated driver circuits, cost of the isolated dc sources (50 A rating) and cost of capacitors with a fixed capacitance of 3.3 mF that can be used for designing various RS MLI topologies are tabulated in Table 9. It is important to note that, the considered component ratings are just to illustrate the sample cost evaluation for an MLI; however the parameter/cost will vary based on the supply rating and market growth.

B. LOSS

Loss in the inverter occurs mainly due to the operation of switching devices. The most significant losses occur in the inverter are switching loss and conduction loss.

TABLE 6. Remarks on RSS MLI topologies.

Ref.	Objective of paper	Switching pulse Generation	Simulation / Experiment performed using	Parameters calculated	Peak output voltage (V), N_l, & f_o (Hz)	Application Suggested	Remarks
RSS MLI [40]	To develop a new RS MLI with reduced cost and installation area	Fundamental switching technique	PSCAD & 89C52 ATMEL microcontroller	THD	100, 11, 60	Medium voltage application	The author is only concerned about generating switching angle to operate MLI, not about the minimization of THD
RSS MLI [41]	To develop a new RS MLI which is cost effective as well as having less blocking voltage	Fundamental switching technique	89C52 ATMEL	TSV	240, 49, 60	Drive and & renewable energy integration	All the switches used are unidirectional and have less blocking voltage, switches with low rating can be used
RSS MLI [42]	To develop novel cascaded MLI with reduction in requirement of dc sources	Modified PS-PWM	PSCAD & ATMEGA32A	THD	311/115.6, 13/9, 50	Medium voltage application	Although it requires less no. of dc sources, but the voltage balancing problem is the major concern as it requires two capacitors for one basic unit
RSS MLI [43]	development of new crisscross cascaded MLI having the modularity property	Vertical phase shifted sinusoidal PWM	MATLAB/SIMULINK & dsPIC30F4011	Loss, THD	600/450, 13/31, 50	PV with & energy storage devices	involvement of bidirectional switches make blocking voltage more and increases in switching losses
RSS MLI [44]	To develop a new MLI which can enhance the circuit performance in terms of reduction in cost, switch and power loss	Multi-carrier sub-harmonic Pwm	MATLAB/SIMULINK & ATMEGA64	THD	490, 15, 50	Renewable energy with storage devices such as super capacitor & battery	Total PIV is more, but more dc sources makes it suitable for renewable energy application
RSS MLI [45]	To develop a new switched-diode MLI with reduced size and cost and high voltage spikes removal from the output voltage	Clock phase shifted one cycle control	MATLAB/SIMULINK & dSpace DS1104	DC ripple, THD	160, 5, 50	Renewable energy integration	Although this topology removes the high voltage spikes, but due to the requirement of extra diodes, it is not cost-effective solution for medium-voltage application
RSS MLI [46]	To develop an MLI based on switched-capacitor in order to improve the power density and energy conversion efficiency	SPWM technique	MATLAB/SIMULINK & DSP TMS320F28335	Power processed by capacitors, THD, TSV	120, 7, 50	Standalone or grid connected application	The topology have higher energy conversion efficiency with multiple voltage levels at output but higher TSV limits it to high voltage application
RSS MLI [17]	To develop a improved sub- module based MLI utilizing reduced number of switches	SHE-PWM technique	MATLAB/SIMULINK & National Instrument (NI) data acquisition device	Efficiency	120, 9, 50	Renewable energy application involving PV and fuel cells	Best suitable for medium/high voltage application as TSV is comparatively less than other MLIs
RSS MLI [47]	To develop a new MLI which requires less no. of active switches and mitigation of dominant lower order harmonics	Modified PSO-based SHE technique	MATLAB/SIMULINK & ATMEGA16	TSV, THD	60, 7, 50	Renewable energy and drives application	This topology requires less no. of active switches, less standing voltage and also the low-order harmonics are removed using new algorithm making it more suitable for medium/high power applications

1) SWITCHING LOSS

Switching loss occurs due to the change in state of a switch. It can be determined by calculating average energy loss in turn-on (t_{on}) and turn-off (t_{off}) intervals of the switch. The mathematical expression for the switching loss for a particular switch can be formulated as [55];

$$S_{loss} = \frac{1}{6} V_{dc} I_{sw} (t_{on} + t_{off}) f_{sw} \tag{1}$$

where, V_{dc} is the standing voltage of the switch, $I_{sw}$is the current passing through the switch, $f_{sw}$is the switching frequency. For the sake of a fair comparison, it is assumed that all the switches are made up of Silicon material and carry an equal current through it; also the switching intervals are same. Hence the simplified expression for the switching loss can be given as

$$S_{loss} = k V_{dc} f_{sw} \tag{2}$$

where,

$$k = \frac{1}{6} I_{sw} (t_{on} + t_{off}) \tag{3}$$

Switching loss calculation for the MLI topologies in which all the switches face an equal standing voltage can be done as per (2). For example, CHB MLI has the TSV of $2(N_l - 1)V_{dc}$ resulting the total switching loss as $2k(N_l - 1)f_{sw}V_{dc}$, but for the topology presented in [40], the H-bridge switches have a standing voltage of $2V_{dc}$,so these switches operate with fundamental frequency (f_0) whereas all the level generation switch have an equal standing voltage of V_{dc} and they will operate with switching frequency (f_{sw}) resulting the total switching loss as $k(N_l - 1)(f_s + 2f_0)V_{dc}$. In a similar manner switching loss for all the topologies are calculated and illustrated in Fig. 5 (∗NA: MLI is unable to produce the desired level). Fig. 5(a)-(c) depicts the comparison among RSS MLI topologies, RSA MLI topologies, and RSM MLI

TABLE 7. Remarks on RSA MLI topologies.

Ref.	Objective of paper	Switching pulse Generation	Simulation / Experiment performed using	Parameters calculated	Peak output voltage (V), N_l, & f_o (Hz)	Application Suggested	Remarks
RSA MLI **[42]**	To generate more output voltage levels with a reduction in no. of switches and isolated dc sources	Modified PS-PWM	PSCAD & ATMEGA32A	THD	311/115.6, 13/9, 50	Medium voltage application	Although it requires less no. of device count and less dc sources to generate a particular level, but still it is not recommended for higher voltage and higher voltage level application due to the capacitor voltage balancing problem
RSA MLI **[43]**	Design of a novel crisscross cascaded MLI with reduction in device count with a property of easy modularization	Vertical phase shifted sinusoidal PWM	MATLAB/SIMULINK & dsPIC 30F4011	Loss, THD	600/450, 13/31, 50	Renewable energy application	For higher voltage application, requirement of no. of switch is less, but with that the total standing voltage increases hence not recommended for higher voltage application. Also the involvement of bi-directional switch increases the cost.
RSA MLI [50]	To develop a new MLI topology requiring less no. of switches	Unipolar PWM strategy	MATLAB/SIMULINK & dSpace DS1104	Distortion factor, THD	96/180, 9/31, 50	PV application	Significant reduction in no. of switches and voltage stress is achieved. Easy control using reduced no. of carriers
RSA MLI [51]	To design a new symmetric, asymmetric switched diode MLI requiring minimum device count	Fundamental switching technique	MATLAB/SIMULINK & ATMEL microcontroller	Efficiency, THD	105/192, 15/25, 50	Renewable energy integration and high voltage application	Reduction in blocking voltage & reduced switch count makes this topology suitable for higher voltage application, but with the increase in no. of output voltage levels, additional diodes are required
RSA MLI [52]	To design a new class of MLI which minimizes the requirement of switches, clamping diodes and flying capacitors	Staircase modulation	MATLAB/SIMULINK & TMS320F240	Distortion factor	120, 13, 100	Permanent magnet motor drives, distributed PV power generation	Complex switching scheme, reduction n component count than the conventional MLI topologies
RSA MLI [53]	To develop a compact basic unit which can operate both in symmetric and asymmetric mode	Fundamental switching control	89C5T ATMEL	TSV	140, 15, 50	Medium to high voltage applications	Drastic reduction in switch count is achieved. Number of levels can be further enhanced with the proposed methods of selecting dc source magnitude
RSA MLI [54]	To design a new MLI based upon switched capacitor module best suitable for high switching frequency power distribution network	Symmetrical phase shift modulation	PSIM	THD, loss, efficiency	48, 9, 2500	Grid connected PV application, EV network	The MLI topology involves less components than CHB MLI. It is observed that, capacitor ripple voltage is less for high switching frequency application which cannot be guaranteed for low frequency applications

topologies, respectively. To perform a fair comparison of switching loss among the MLI topologies, different parameters are chosen as: $k = 1$, switching frequency $(f_s) = 1$ kHz, fundamental frequency $(f_0) = 50$Hz, $V_{dc} = 1$p.u.

2) CONDUCTION LOSS

Conduction loss is directly proportional to the number of switches associated in generating a particular voltage level. Hence for more the number of conducting switches in the current path more will be the conduction loss. For example, $(N_l - 1)$ switches are always in the conducting path for an N_l-level CHB MLI.

C. CONTROL COMPLEXITY FOR DRIVE APPLICATION

Performance improvement of the RS MLI powered variable speed drives is a major concern now a day. Authors in [70] have critically reviewed major issues such as common mode voltage elimination, voltage balancing, etc. related to MLI powered motor drives. Solution to these issues for open end stator winding multilevel converter drives is analyzed in [71]–[75]. In this configuration one inverter is responsible to supply active power fed from the dc source while the other helps to increase the levels at output thereby improve the power quality. Reduction in voltage stress, switching loss, switch count has been achieved using these structures.

Torque and flux control are major issues when a RS MLI is used for drive applications. MLI powered motor drives are basically controlled by three methods known as scalar control, vector control, and direct torque control (DTC). Scalar control regulates the ratio of voltage and frequency to have a control over torque. The stator current has torque and flux producing components which are regulated separately in vector control method. In contrast, DTC directly relates to the switching state to have a control over torque without the need of stator current regulation [76], [77]. Moreover, authors in [78], [79] have derived a control scheme to reduce the torque ripples using MLI powered induction motor drives. dc-link voltage balancing is another key issue of concern in drives application which makes the whole system unstable. Various control algorithms have been investigated in [80]–[84] to assist the voltage balancing problem. Fault tolerant control is

TABLE 8. Remarks on RSM MLI topologies.

Ref.	Objective of paper	Switching pulse Generation	Simulation / Experiment performed using	Parameters calculated	Peak output voltage (V), N_l, & f_o (Hz)	Application Suggested	Remarks
RSM MLI [55]	To design a new MLI consisting of floating input dc sources connected in opposite polarity alternately in which the device count can be reduced	Multi-carrier PWM	MATLAB/SIMULINK & dSpace DS1103	THD	48, 5, 50	Renewable energy integration, medium voltage application, electric vehicle application	Reduction in device count is achieved, but modularity and fault tolerant capability are less compared to conventional CHB MLI
RSM MLI [58]	To develop a new MLI operating in both symmetric and asymmetric modes which substantially reduces the no. of device count	Sinusoidal PWM switching	MATLAB/SIMULINK & dsPIC30F4011	Loss	400/480/375/360, 9/25/31/49, 50	High / medium voltage application	Proposed MLI requires large no. of diodes which is not a feasible property, asymmetric mode of operation in this MLI brings a superior enhancement quality than the symmetrical mode of operation
RSM MLI [59]	To develop novel cascaded MLI with reduced device count and allowing integration of renewable sources	Single carrier PWM switching	MATLAB/SIMULINK & PLECS software	THD	200/400, 9/17, 50	Renewable energy integration and high voltage application	Significant reduction in no. of active switches, total standing voltage and switching loss is achieved, but at the cost of extra diodes and bi-directional switches
RSM MLI [62]	To develop a novel hybrid MLI for high-efficiency application with a reduced device count and redundant switching states	Modified PD-PWM	MATLAB/SIMULINK & dSpace DS1103	-	100, 5, 20/50	Medium voltage application	Capacitor voltage balancing problem is removed due to redundant switching states and fault tolerant capability is improved. The reduced TSV of the power switches makes it suitable for medium voltage application
RSM MLI [63]	To devise a novel E-type module based MLI that can generate staircase output with less device count	SHE-PWM technique	MATLAB/SIMULINK & ATMEGA16	THD	300, 13, 10/50/100	High voltage / power application	Low voltage stress and reduction in device count makes this topology popular in high voltage application
RSM MLI [66]	To develop a novel square type MLI using unequal dc sources and less no. of components	NLC technique	MATLAB/SIMULINK & dSpace DS1104	THD	96/192, 17/33, 50	PV application, high voltage / power application	Easily modularized to achieve more output voltage levels with less no. of switch and less voltage stress on it
RSM MLI [68]	To design a new modularized MLI with less voltage stress and reduced device count	PD-PWM control	MATLAB/SIMULINK & dSpace DS1104	THD	300, 9/13/15/21, 50	Renewable energy application	Although the reduction in voltage stress and easy modularity is achieved, but at the cost of extra diodes making the topology unsuitable for high voltage application
RSM MLI [69]	Semi-cascaded MLI design with substantial improvement in all performance parameters	Fundamental switching technique	MATLAB/SIMULINK	THD	80, 9, 50	Medium voltage application	Possibility of symmetric and asymmetric modes of operation with lesser device count. For higher output voltage levels with less no. of dc sources, the topology can be operated in asymmetric mode
RSM MLI [60]	To devise a novel cascaded MLI operating in both symmetric and asymmetric modes with reduction in device count, gate driver circuits, and installation area	Fundamental switching technique	MATLAB/SIMULINK & dsPIC30F4011	THD	400/480, 9/17, 50	PV integration	With the increment in no. of levels, the voltage stress increases and also there is a significant increment in number of active switches making the topology expensive

an additional feature for drives application of an MLI which has been addressed in [85], [86]. Few RS MLI topologies for induction motor drives application with different control strategies has been suggested in [24], [84].

D. CONTROL COMPLEXITY FOR RENEWABLE ENERGY INTEGRATION

Renewable energy sources such as wind and solar significantly contributes to present total power generation which is due to advancement in MLI topologies. Megawatt range wind power generation using multilevel VSIs has been researched in [87]–[90]. Authors have addressed issues such as equal power distribution, MPP tracking, switching frequency regulation, reduction of switching stress, dc-link capacitor voltage balancing, and fault ride-through in such applications of MLI.

On the other hand to meet the energy demand PV systems as clean power generation are widely harvested in integration with MLIs. MPP tracking and dc-link voltage balancing are the key issues in such applications of RS MLI. In [91]–[96], independent MPPT control as well as dc-link voltage control has been addressed for different PV RS MLI structures, when MLI is fed through individual dc-links integrated to number of PV strings. Flexibility, control, dc-bus voltage regulation, etc. can be enhanced by feeding power from multiple

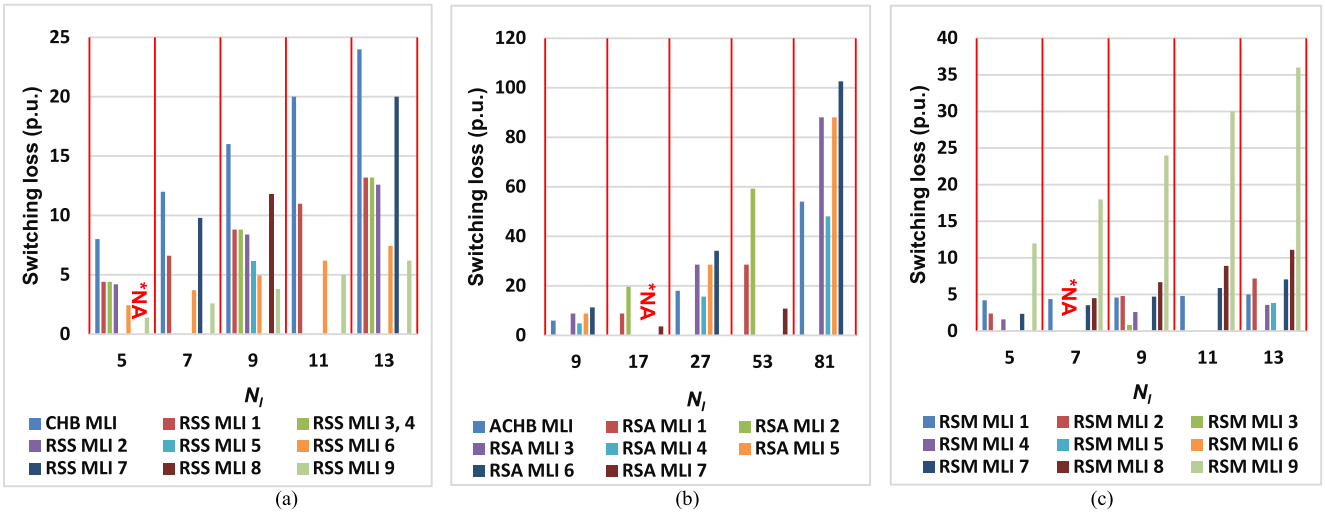


FIGURE 5. Comparison among MLI topologies with respect to variation of switching loss Vs N_l (a) RSS MLI. (b) RSA MLI. (c) RSM MLI.

TABLE 9. Cost evaluation of an MLI.

Component name	Component number	Voltage rating (V)	Unit price# (USD)
IGBTs (75 A)	IXGH60N30C3	300	3.89
	IXGH72N60B3	600	5.70
	IXGH50N90B2	900	5.96
	IXGH32N100A3	1000	6.87
	IXGH40N120A2	1200	8.12
	IXGH25N160	1600	10.48
	IXGH32N170	1700	16.78
	IXBH20N360	3600	35.49
Discrete diodes (75 A)	APT60S20	200	5.91
	APT75DQ60	600	4.74
	APT75DQ100	1000	4.90
	APT75DQ120	1200	7.02
Driver circuits	TLP250	--	2.04
	TLP350	--	2.83
	HCPL-316J	--	6.17
	HCPL-3120	--	3.25
	HCNW-3120	--	5.06
	HCPL-3180	--	3.85
	IR2110	--	1.84
	MCT2E	--	0.37
	MOC3021	--	0.43
Isolated dc power supplies (50 A)	TL250048 (2.5 kW)	48	1504.5
	N8759A (5 kW)	100	6821
	N6702C (1.2 kW)	150	4199
Capacitors (3.3 mF)	LLS2A332MELA	100	4.96
	LLG2D332MELC50	200	9.87
	LQR2V332MSEG	350	51.51
	LQR2G332MSEG	400	65.73
	LNX2H332MSEH	500	111.08
	LNX2J332MSEJ	630	216.07

#Infineon Technologies, IXYS Corporation, www.digikey.in, www.mouser.in

PV strings to RS MLI through a common dc-bus [97]. Number of RS MLI topologies in [57], [94], [98]–[100] has also been analyzed for PV application. A level doubling network based multilevel PV power generation system for generating higher voltage levels utilizing reduced number of switches has been proposed by authors in [101], [102]. In which, low-frequency ripples, appropriate control of RS MLI using PWM technique, and MPP tracking have also been addressed by the authors for PV application. In addition to tracking MPP [103], suitable control techniques such as power sharing control in [104], reactive power control in [95], [105], and common-mode voltage balance control in [99], [100] has been analyzed as elegant solution for RS MLI-based PV power generation system.

VI. EXPERIMENTAL ILLUSTRATION

From the comparative study it is found that both fundamental switching frequency modulation schemes and high switching frequency scheme have their advantages in their own way of application. Fundamental control scheme produces less switching loss than high-frequency PWM techniques while distortion in the load current waveform can be minimized with high switching frequency PWM techniques. To illustrate the fundamental switching control scheme, PSO-based SHE control technique is implemented whereas for the high-frequency PWM technique, SPWM control technique is implemented. These experimental results of a single-phase RSS MLI prototype model described in [47] are presented for illustration purpose only, which shows basic difference in low and high-frequency switching control of the MLIs. Isolated dc power supplies of 25 V are used in the experimental design and the nominal operating frequency is assumed as 50 Hz. Test has been conducted using linear *R-L* load of 100 Ω - 150 mH.

The experiments are carried out in three different stages for producing 5-level, 7-level, and 9-level voltage outputs using only 5, 6, and 7 active switches, respectively. Fig. 6(a)-(c) shows the output voltage and load current waveforms with corresponding harmonic spectra of voltage waveform. By the use of SHE-PWM control scheme, the targeted 3rd order harmonic from the output voltage of 5-level RSS MLI is eliminated. Similarly, 3rd and 5th order harmonics from the

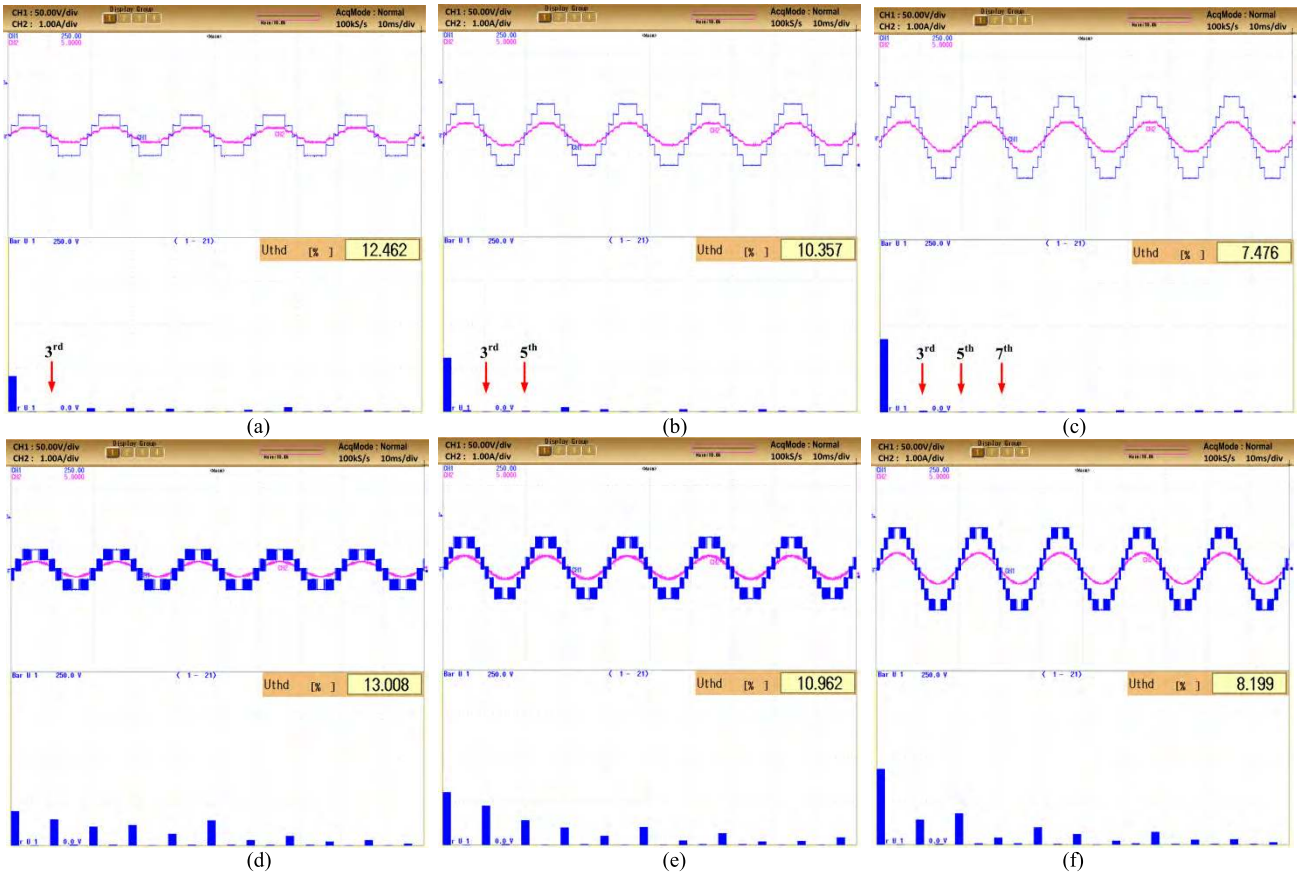


FIGURE 6. Experimental results of the RSS MLI: Staircase output voltage (y-axis 50 V/div; x-axis 10 ms/div), sinusoidal load current (y-axis 1 A/div; x-axis 10 ms/div), and output voltage harmonic spectra (harmonic order from 1st to 21st) with SHE-PWM (a) 5-level MLI. (b) 7-level MLI. (c) 9-level MLI. with SPWM (d) 5-level MLI. (e) 7-level MLI. (f) 9-level MLI.

output voltage of 7-level RSS MLI, and 3rd, 5th, & 7th order harmonics from the output voltage of 9-level RSS MLI are successfully eliminated. The voltage THD is calculated taking harmonic order up to 49th. It is important to note that, the triplen harmonics are more dominant in a single-phase structure and absent in the line-to-line voltages of three-phase MLI. Hence in a three-phase MLI the harmonic order other than 3rd harmonic can be targeted for elimination. Due to a low-pass filter type operation, a clean sinusoidal current can be observed in the load which can be made more sinusoidal-like by using large value of inductor. In all the cases although the harmonic spectra of load current are not shown, it has very less harmonic content. On the other hand, SPWM control scheme is also implemented for the RSS MLI in which the reference sinusoidal wave has a fundamental frequency of 50 Hz and the carrier signals have a frequency of 5 kHz. The resulted output voltage and current waveforms are shown in Fig. 6(d)-(f) with corresponding FFT analysis. Form the waveforms it is clearly visible that SHE-PWM technique produces a small distortion in the current waveform which can be improved by SPWM control scheme. But the obtained THD is less with SHE-PWM control scheme than the SPWM control technique.

VII. CHALLENGES, CURRENT RESEARCH FOCUS, AND FUTURE DEVELOPMENT TRENDS

Current and future RS MLI topology design have to deal with various issues such as compact module based MLI design, device stress/standing voltage, high voltage spikes, thermal stress, and power losses. Apart from the design aspect, continuous effort has also been made to operate different MLI topologies efficiently, *i.e.*, technical challenges such as dc-link voltage balancing, fault ride through control, power-decoupling, harmonic control, and power quality control. Most of the current literature work suggests solution for these issues considering conventional MLI topologies. Thus, future research should be extensively directed towards design and control of RS MLI to address the above-discussed issues.

Deployment of wide band-gap devices in RS MLI topologies can be one of the future developments in this field. This can bring a number of advantages together. For example, the High-temperature capability of SiC devices can be used to minimize cooling loops thereby enhancing power density. Also, there is a possibility of reducing the drive footprint and its associated cost by improving the power density. An integrated motor drive can be feasible in future for medium and high power applications with the application of SiC devices.

TABLE 10. Challenges and current scenario of MLI system.

Major Issue	Detailed technical challenges/issues that need to be addressed	Current scenario				
		MLI type & suggested literature	MLI control scheme	Controller used to control MLI	Power electronic switches used in MLI design	N_l, f_{sw} (Hz), & f_o (Hz)
Design of compact module MLI with low power loss, reduced thermal stress, and higher efficiency	• Modular circuit realization with less number of components and sources • Device stress & standing voltage • Protection from thermal overloading • Reduced power loss and higher efficiency • Overall design cost & size • Undesirable voltage spikes, voltage balancing, voltage boosting • Output quality	RSM MLI [58]	Fundamental frequency switching PWM	dsPIC30F4011	BUP403 IGBT	9/25/31/49, --, 50
		RSM MLI [55]	Multi-carrier PWM	dSpace DS1103	IRF460 MOSFET	5, 1k, 50
		RSM MLI [59]	Single carrier fundamental frequency switching PWM	--	IXYS FII40-06D IGBT	9/17, --, 50
		E-type RS MLI [63]	SHE-PWM	ATMEGA16	12N60A4D IGBT	13, --, 50
		T-type RS MLI [106]	Thermal stress relief PWM	DSP TMS320F28335	IGBTs	5, 5k, 50
		Square T-type RS MLI [66]	NLC	ATMEGA16	12N60A4D IGBT	33/289, --, 50
		Compact module RS MLI [107]	SHE & SPWM	Real time software & NI data acquisition	SiC MOSFETs	7/13,--, 50
		Compact module RS MLI [108]	Parabolic SPWM	dSpace DS1104	SKM75GB063D IGBT	9, 2.5k, 50
		Packed U-cell RS MLI [56]	Self voltage balancing PWM	dSpace DS1103	SCT2080KE MOSFET	5, 2k, 50
		Packed U-cell RS MLI [57]	Self voltage balancing PWM	dSpace DS1103	FGH30N60LSD IGBT	7, 2k, 50
Capacitor voltage balancing	• Charging/discharging cycle • Reduced capacitor voltage ripple, current ripple, & fluctuation • Limiting the high rate of change in current • Premature failure & EMI reduction • Neutral point & flying capacitor voltage balancing in the entire modulation range • Balanced throughout performance of the MLI	FC MLI [38]	PS-PWM	DSP TMS320F28335	--	7, 4k, 50
		Packed U-cell RS MLI [56]	Self voltage balancing PWM	dSpace DS1103	SCT2080KE MOSFET	5, 2k, 50
		DC MLI [109]	Modified PS-PWM	--	--	5, 2k, 50
		FC MLI [110]	Knapsack PWM	dsPIC30F4011	IRF740 MOSFET	13, 3k, 50
		CHB MLI [111]	SPWM	dSpace DS1006	PP75B060 IGBT	7, 800, 50
		Stacked RS MLI [84]	SVPWM	DSP TMS320F28335 & FPGA	IGBTs	9, 2k, 50
		Quasi-Z source (qZS) MLI [112]	PS-PWM	FPGA Virtex 5	--	7, 1k, 50
		DC MLI [113]	SPWM	--	IGBTs	5, 20k, 50
MLI for renewable energy power conditioning	• Maintaining power quality • Dealing with partial shading imbalance • Maximum power tracking with power, energy, & dc-link voltage balancing • Avoid unbalanced current injection into the grid • Low leakage current, low total power loss, & high efficiency • Low-voltage ride through grid-code capability & support during fault	qZS MLI [114]	SPWM	DSP TMS320F28335	--	7, 10k, 50
		CHB MLI [115]	Hybrid multicarrier PWM	Xilinx FPGA	PM50RSD120 IGBT	5, 3k, 50
		RS MLI [116]	Logical switching state selection PWM	Arduino Mega 2560	12N60A4D IGBT	7, 5k, 50
		RS MLI [94]	PS-PWM	dSpace DS1104	K75T60 IGBT	9, 3k, 50
		CHB MLI [111]	SPWM	dSpace DS1006	PP75B060 IGBT	7, 800, 50
		Single dc bus CHB MLI [97]	PS-PWM	dSpace DS1103	FSBB30CH60 IGBT	7, 4.1k, 50
		RSA MLI [117]	Hybrid PWM	DSP TMS320F28335	IRFP4868, IRFP4568 MOSFET	27, 10k, 60
		Level doubling MLI [102]	SPWM	DSP TMS320F28377	IPMPS22A76 IGBT module	5, 25k, 50
		CHB MLI [96]	PS-PWM	dSpace DS1104	SKM50GB063D IGBT	7, 2k, 50
		Packed U-cell RS MLI [57]	Self voltage balancing PWM	dSpace DS1103	FGH30N60LSD IGBT	7, 2k, 50
		Modified HB MLI [118]	POD-PWM	--	5SDF10H4503 IGCT	5, 800, 50
		CHB MLI [119]	Modified PS-PWM	DSP TMS320F28335 & FPGA	IGBTs	7, 2k, 50
		CHB MLI [120]	PS-PWM	DSP TMS320F28335	IGBT modules	7, 5k, 50
State-of-charge battery storage management in MLI system	• Decentralized/centralized state-of-charge (SOC) control of all storage system in an MLI • Safe operating limit & life of storage system • Charging & discharging cycle control with PWM switching frequency • Storage of additional power and smooth power regulation	CHB MLI [121]	Harmonic reducing algorithm	HT46R24	MOSFETs	7, -, 50
		CHB MLI [122]	Multi-dimensional PWM	dSpace DS1104	IGBTs	5, 1k, 50
		CHB MLI [123]	PS-PWM	--	--	11, 1k, 50
		CHB MLI [124]	Staircase PWM	Arduino	IRFP540n MOSFET	11, -, 50
		qZS MLI [93]	PS-PWM	DSP TMS320F28335	--	7, 10k, 50
		DC MLI [125]	Virtual vector PWM	dSpace DS1006	FDPF3860T MOSFET	7, 10k, 50
Minimization of leakage current and common-mode voltage (CMV) elimination	• Minimization of EMI filter requirement • Use of active/passive circuitry • Minimization of leakage current during zero & intermediate switching state of MLI • Premature motor bearing failure & reliability in drives application	CHB MLI [115]	Hybrid multicarrier PWM	Xilinx FPGA	PM50RSD120 IGBT	5, 3k, 50
		CHB MLI [126]	Zero CMV PWM	DSP TMS320F28335	FGL-60N100-BNTD IGBT	5, 2.1k, 50
		CHB MLI [127]	Zero CMV PWM	DSP TMS320F28335	FGL-60N100-BNTD IGBT	5, 2k, 50
		Cascaded RS MLI [99]	Modified reference PWM	DSP TMS320F28335	--	5, 10k, 50

TABLE 10. *(Continued.)* **Challenges and current scenario of MLI system.**

	• Elimination of high frequency voltage transition • Low switching & conduction losses • Reduction of voltage stress & low-order harmonics in the entire modulation range of operation	Modified CHB MLI [128]	SVPWM	DSP TMS320F28335 & Xilinx FPGA	--	7, 12k, 50
		Cascaded RS MLI [100]	Modified reference PWM	Spartan 6 FPGA	IRF840 MOSFET	5/9, 10k, 50
		RSA MLI [117]	Hybrid PWM	DSP TMS320F28335	IRFP4868, IRFP4568 MOSFET	27, 10k, 60
Power decoupling in MLI	• Capacitor size, cost, & volume reduction • Maintaining power density, stable dc voltage, high system efficiency • Reduction in voltage ripple & harmonics • Avoid increasing the topology complexity • Buffer the ripple frequency other than twice the line frequency	Multi-port CHB MLI [129]	Modified PS-PWM	DSP TMS320F28335	IRFP4868PbF	7, 4k, 60
		Switched-capacitor MLI [46]	Optimized SPWM	DSP TMS320F28335	IRFP260N & IXTK62N25	7, 15k, 50
		CHB MLI [130]	Modified PS-PWM	--	--	7, 3k, 50
		qZS MLI [131]	SPWM	--	--	5, 10k, 50
Harmonic elimination / mitigation in MLI	• Low/fundamental switching frequency operation & low switching loss • Dominant harmonics elimination/mitigation • Triplen harmonic control in single-phase MLI • Reduced mathematical calculation burden • Simultaneous THD reduction along with SHE • Unequal, unbalanced, & variable dc-link voltage control • Obtaining optimum solution for a wide modulation range • Intelligent optimization algorithm based approach • Online/real-time implementation • Dealing with any switching pattern (*i.e.*, unified solution finding ability)	Four-leg DC MLI [132]	SHM-SHE PWM	dSpace DS1106	SiC MOSFET	5, 600, 50
		RS MLI [133]	Modified SHE-PWM	Arduino Mega 2560	12N60A4 IGBTs	7/17, -, 50
		FC MLI [134]	SHE-PWM	Microcontroller	--	5, -, 50
		CHB MLI [30]	SHE-PWM	CORTEX M4 ARM processor	IRF540N MOSFETs	7, -, 50
		RS MLI [47]	SHE-PWM	ATMEGA16	IRFP250	7, -, 50
		CHB MLI [135]	SHE-PAM	--	FGA25N120 IGBT	6, -, 50
		CHB MLI [136]	SHE-PWM	Arduino Due	IPMPS22A76 IGBT modules	7, -, 50
		CHB MLI [137]	Unified SHE-PWM	CORTEX M4 ARM processor	STGIPS30C60 IGBT modules	5, -, 50
		CHB MLI [138]	SHE-PWM	DSP TMS320F28335	--	9, -, 50
		CHB MLI [139]	SHE-PAM	dSpace DS1103	--	5, -, 50
		Modified PUC [140]	SHE-PWM	dSpace DS1103	--	5, -, 50
		CHB MLI [141]	SHE & SHC-PWM	STM32F407 processor	IRFP250N MOSFET	9, -, 50

In such a scenario, new RS MLI design for drives application should take into account issues like premature motor bearing failure, reliability, minimization of leakage current, and common mode voltage (CMV) elimination. Forecast for the value of SiC power semiconductor market is about $1.4B as per the report [142].

Secondly, renewable energy integration through the suitable MLIs to the power grid makes the grid and utility gradually moving towards the future smart grid. This will pose great challenges and opportunities for the development of RS MLI topology and control. Therefore the innovations in this field are certain. To maintain the power quality in such a case, several grid code standards are developed. A lot of research needs to be performed to fulfill these standards and addressing key issues such as maximum power extraction from RESs, unbalanced current injection into the grid, and leakage current. Table 10 summarizes all the technical challenges that need be considered for an efficient RS MLI design. This also includes current research scenario of MLI system.

Renewable energy target in India is 175 GW by 2022 and in Singapore is 350 MW by 2020 through Solar Nova Singapore programme and many other countries are committed to increasing their power generation through renewable sources [143]. In addition, many countries set a target towards emission reduction by introducing and selling all vehicles as electric vehicles within specific timelines [144]. All these initiatives provide opportunities and challenges for the design and development of advanced power converters.

Moreover, the technical stumbling blocks of power electronic systems to sustain high heat and vibration of the harsh machine environment have gradually been overcome through technological developments. Therefore the integrated drive concept will be increasingly attractive for future drive applications from a technical and economic perspective. This, in turn, paves the way for the industry to learn more from this for modularizing electric vehicle propulsion while concurrently minimizing the EMI emissions through removing the long interconnecting cables between the inverter and the machine. Globally, concerns about more efficient utilization of electrical energy, improvement of power quality, reduction of emissions etc. are being increasingly felt. Given this, advances in RS MLI are already happening and are expected to continue.

VIII. CONCLUSION

MLI based topologies are evolved as a robust candidate for power industry for a number of key applications. With the rapid growth in power semiconductor technologies, many MLI topologies have been developed through research utilizing reduced number of components. New RS MLI topologies are still emerging for various advantages such as reduced

cost, optimal size, lesser volume, reduced losses, and high efficiency. A number of RS MLI topologies are developed most recently for different application such as motor drives, renewable energy system integration, FACTs, power filtering, etc. Therefore, this review article has mainly focused on RS MLI topologies based on the three categories, *i.e.*, symmetrical H-bridge based RS MLI, asymmetrical H-bridge based RS MLI, and modified RS MLI topologies. Each topology has been reviewed carefully based on the number of switch count, number of dc sources used, PIV, TSV, and applications. H-bridge based RS MLI structures are highly modular in nature. But, the four H-bridge switches with a higher standing voltage are involved in such topologies for example in [17], [47] which is more compared to most of the RSM MLI topologies. RSA MLI structures play a significant role to synthesize higher levels with the involvement of lesser components. However, the need of extra high rated switches is the key concern in high voltage applications [50], [53]. Involvement of single isolated dc source to synthesize multiple levels is a cost-effective solution as presented in the literature [46], [57]. These topologies are suitable for RES integration especially for PV applications. However, due to involvement of additional capacitors in these MLIs, voltage balancing is the key concern. Furthermore, more such RS MLI topologies considering reduced TSV needs to be developed to well-suit for both PV and wind energy system integration.

The objective of the review is to cover most of the recently proposed MLI and the useful information has been effectively detailed through this review. A comparison based on the types of controller used, different switching techniques and significant remarks are also included. The MLI topology should be chosen carefully keeping in view of the optimal performance parameters. Key parameter deciding the performance, cost, and control complexity of an MLI for PV integration and drives application are discussed. To illustrate the working of MLI, experimental results are included taking a RS MLI topology for different level generation. In this aspect, both fundamental switching frequency (SHE-PWM) and high switching frequency (SPWM) control techniques are implemented. The main aim of implementing both the switching techniques is to provide preeminent knowledge to the readers regarding different control approaches. This review is promising for early stage power engineers working in this area, in the aspects of selecting the suitable topology for the definite application with accurate switching scheme.

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