Reciprocity-Transposition-Based Sinusoidal Pulsewidth Modulation for Diode-Clamped Multilevel Converters

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***Abstract*—Modulation strategies for multilevel inverters have typically focused on synthesizing a desired set of three phase sinusoidal voltage waveforms using a fixed number of dc voltage levels. This results in the average current injection and hence the net power drawn from the multiple dc bus terminals to be unmatched and time varying. Subsequently, the dc-bus voltages are unregulated, requiring corrective control action to incorporated. In this paper, the principle of reciprocity transposition in introduced as a means for modeling the dc-bus current injection simultaneously as the modulation strategy is formulated. Furthermore, a new sinusoidal pulsewidth-modulation strategy that features constant and controllable current injection at the dc-bus terminals while maintaining output voltage waveform quality is introduced. The proposed strategy is general enough to be applied to converters with an even number of levels and an odd number of levels. Analytical results comparing the performance of the proposed modulator with a conventional multiple carrier modulator are presented for example multilevel converters with four and five levels. Computer simulation results verifying the analytical results are presented for a four-level converter.**

***Index Terms*—Multilevel systems, power conversion, pulsewidth modulation.**

I. Introduction

In recent years, multilevel power converters have become popular in high-power three-phase ac applications where they provide various performance advantages over conventional two-level converters. These advantages include reduced voltage stresses on power semiconductor devices, reduced switching stresses, modular realization, and improved waveform quality. In general, these converters incorporate a topological structure that allows a desired output voltage to be synthesized from among set of isolated or interconnected distinct voltage sources. Independent of the topological structure, all modulation algorithms for these converters provide for systematically selecting from among the various input voltage levels to synthesize a desired output voltage waveform. Several modulation approaches that realize this function effectively have been proposed in the past [1]–[9]. Among them are: stepped waveform synthesis [10], [11], programmed harmonic elimination [12], triangular-carrier-waveform-based schemes [13], real-time carrier-based harmonic elimination [14], space-vector-based techniques [15], hysteretic current control [16], and multilevel sigma–delta modulation [17]. All of these techniques have been demonstrated to be effective in performing the primary waveform synthesis function. Typically, in multilevel converters with isolated dc voltage sources such as in cascaded H-bridge converters, implementation of the modulation function of these algorithms have been partitioned between various modules in a manner to equalize power drawn from the different voltage sources [18]–[20]. However, in multilevel converters with interconnected sources such as the diode-clamped multilevel converter such a partitioning between various dc voltage sources that incorporate the multiple levels is not straightforward [21], [22]. As a result, the power drawn from the different voltage sources are varying as a function of modulation level, load level, and load power factor. This further results in unsteady and at times unstable dc voltage levels [9], [21]. Thus, stabilization of voltage levels in the dc bus stack is one of the important concerns that is the focus of many research investigations [21]–[23]. This particularly problematic in singly fed systems where the dc bus stack is fed between the lowest voltage and the highest voltage in the stack. In general, in multiply fed systems that have different dc sources that feed various nodes of the dc-bus stack, the voltages are individually regulated. It has been shown that when bidirectional multilevel converters are connected "back-back" at the dc bus, the dc-bus voltages are stable and do not require any particular voltage-balancing algorithms. However, this result has been specific to a particular modulation algorithm, and it is not clear that it holds true under all conditions. More recently, a voltage self-balancing topology was introduced, which has an inherent capability for balancing the dc stack voltages [24].

Generally, it is well recognized and understood that the fundamental reason for voltage balancing problem is the unequal current injection at the dc terminal of the converter that varies with load current and modulation level. However, this process has not been addressed systematically in the development of the modulation algorithm. More often, the modulation algorithm is developed with the sole objective of output waveform synthesis and the dc power flow problem becomes an unintended, but inevitable consequence of the power converter operation. A dc-voltage-balancing solution is then added on to manage the consequence. It is the objective of this paper to systematically address the dc current injection at the dc levels as a simultaneous problem to output waveform synthesis and not as a consequent problem. Reciprocity transposition is applied to examine the dc current injection for a given modulation algorithm. This

Manuscript received July 4, 2001; revised December 4, 2001. Abstract published on the Internet July 15, 2002.

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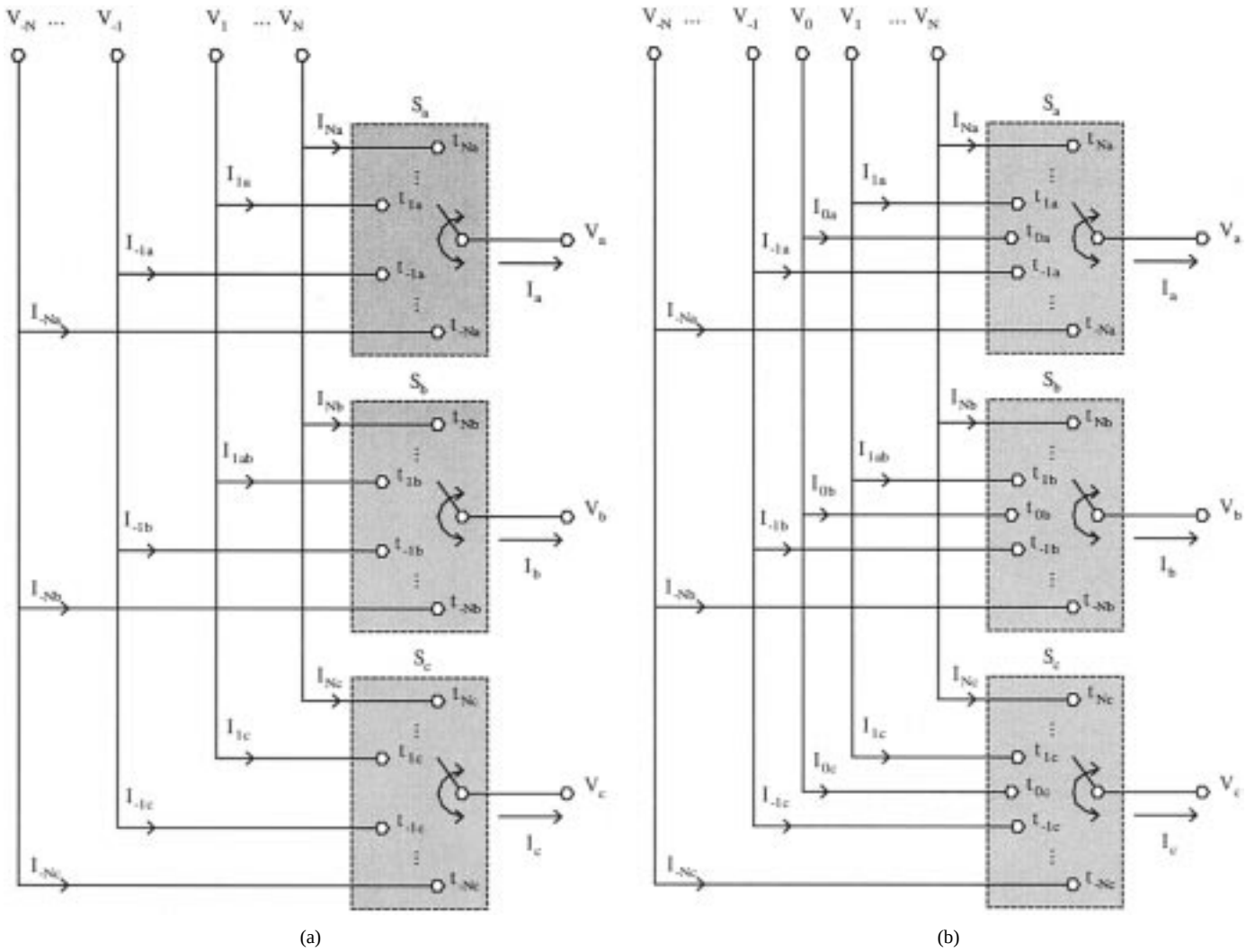
Publisher Item Identifier 10.1109/TIE.2002.803210.



(a) (b)

Fig. 1. Schematic of the switching circuit of a multilevel dc to three phase ac power converter. (a) Even number of levels. (b) Odd number of levels.

approach is well known and has been used as the basis for the development of modulation functions for matrix converters [25]. The dc current injection of a typical carrier based modulation algorithm is determined using the reciprocity transposition approach. The drawbacks of the algorithm from the dc power flow point of view are readily elucidated.

Conditions for obtaining desirable dc current injection properties are developed and applied to develop a modulation algorithm that has superior properties in terms of dc current injection. The results are developed for a general case of an N (odd and even) level converter and demonstrated using a five- and a four-level converter example. Analytical results are verified using computer simulations for the four-level converter. In Section II, the topology of the diode-clamped multilevel converter is briefly reviewed and the reciprocity transposition in power converters is used to develop input–output relationships for the converter. Current injection at various nodes of the multilevel dc-bus stack is determined for a typical multiple triangular carrier modulation algorithm in Section III, along with some of its limitations being identified. In Section IV, a new modulation approach is proposed along with analytical results describing its properties. Computer simulation results from a four-level converter example using conventional as well as the proposed modulation algorithm under typical operating conditions are presented in Section V. Section VI provides a summary of the results.

II. Diode-Clamped Multilevel Converter Modeling

A. Topological Description

A schematic of the switching circuit of a multilevel dc to three phase ac power converter is illustrated in Fig. 1. The illustration of the throws that form the switch as illustrated in Fig. 1 is an abstract representation of the switching structure between the multilevel dc sources and the ac output. In reality, the throws may be realized using any number of techniques, which result in the topological variety among multilevel converters. However, for purpose of describing the modulating properties of the converter, the representation in Fig. 1 is sufficient. To be sure, the topological mapping between the abstract representation and the semiconductor realization will be provided further, so that the models may be useful for studying the operation of the real converter.

The switching circuit of the abstract representation consists of three single pole multithrow switches (S_a, S_b, S_c), one each per phase of the output ac system. The number of throws in

each switch is equal to the number of levels, n of the multilevel converter, which may be even or odd. For notational purposes, let the integer $N = n/2$ and $N = (n-1)/2$ be defined as the maximum index number of the converter for even and odd number of levels, respectively. Thus, each of the three switches in an even-level converter has $2N$ throws and those in an odd-level converter have $2N+1$ throws. Fig. 1(a) and (b) illustrates the switching circuit schematic for an even-level and an odd-level converter, respectively.

The dc bus of the diode clamped n-level converter is formed by a stack of $n-1$ individual dc sources, connected in series so that their polarities are additive. Although these sources may be of different magnitudes, they are assumed to be nominally equal to each other, resulting in a symmetric diode-clamped multilevel converter. The extremities of the series string and each of the junction points between the sources form the terminal of the dc-bus stack. The poles of the switches form the ac output terminals, which feed an inductive load, generally modeled as a balanced set of three-phase stiff currents (I_a, I_b, and I_c). The throws ($t_{Nj}, t_{N-1j}, \ldots t_{N+1j}, t_{-Nj}$), where ($j = a, b, c$) are connected to $2N$ or $2N+1$ stiff voltages ($V_N, V_{N-1}, \ldots V_{-N+1}, V_{-N}$) as illustrated in the figure. For a symmetric odd-level converter, V_0 is equal to zero (or null), and for a symmetric even-level converter V_0 does not exist.

The throws of the switches are assumed ideal as is common in preliminary functional analysis of switching power converters. These assumptions include: 1) negligible forward voltage drop of the switch throws in their on-state; 2) sufficient on-state current carrying capacity and off-state voltage blocking capacity commensurate and compatible with the voltage and current ratings of the system; and 3) negligible transition periods between opening and closing of the switch throws that permit repetitive high-frequency switching. The voltages at the throw terminals of the switch are assumed stiff such that their variations during a switching period can be neglected. Similarly, the switch pole currents are assumed stiff such that their variations over a switching period can be neglected. These assumptions essentially allow the focus to be on the power transfer process and the functional features. In practical power converters, filter elements appropriately applied at the input and output ports of the system would ensure that these assumptions are valid.

In order to maintain continuity of the three phase currents connected to the poles, at least one of the throws of connected to any given pole of the switch has to be closed. Furthermore, each current port may be connected to only one voltage terminal at any given instant of time. Otherwise, two stiff voltages will be short circuited together, resulting in uncontrolled currents through the switch throws. As a result, no more than one throw connected to any given pole may be closed at any given instant of time.

Mathematically, these constraints may be expressed using switching function formulations. Let $H_{ij}(t)$, the switching function of a throw connecting the dc bus stack voltage V_{si} to the current I_j be defined as (1), shown at the bottom of the page. Then,

$$\sum_{i=-N}^{N} H_{ij}(t) = 1, \qquad \text{for } j = a, b, \text{ and } c \tag{2}$$

Furthermore, it is clear that

$$V_j(t) = \sum_{i=-N}^{N} H_{ij}(t) \cdot V_i, \qquad \text{for } j = a, b, \text{ and } c \tag{3}$$

and

$$I_i(t) = \sum_{j=a,b,c} H_{ij}(t) \cdot I_j(t),$$

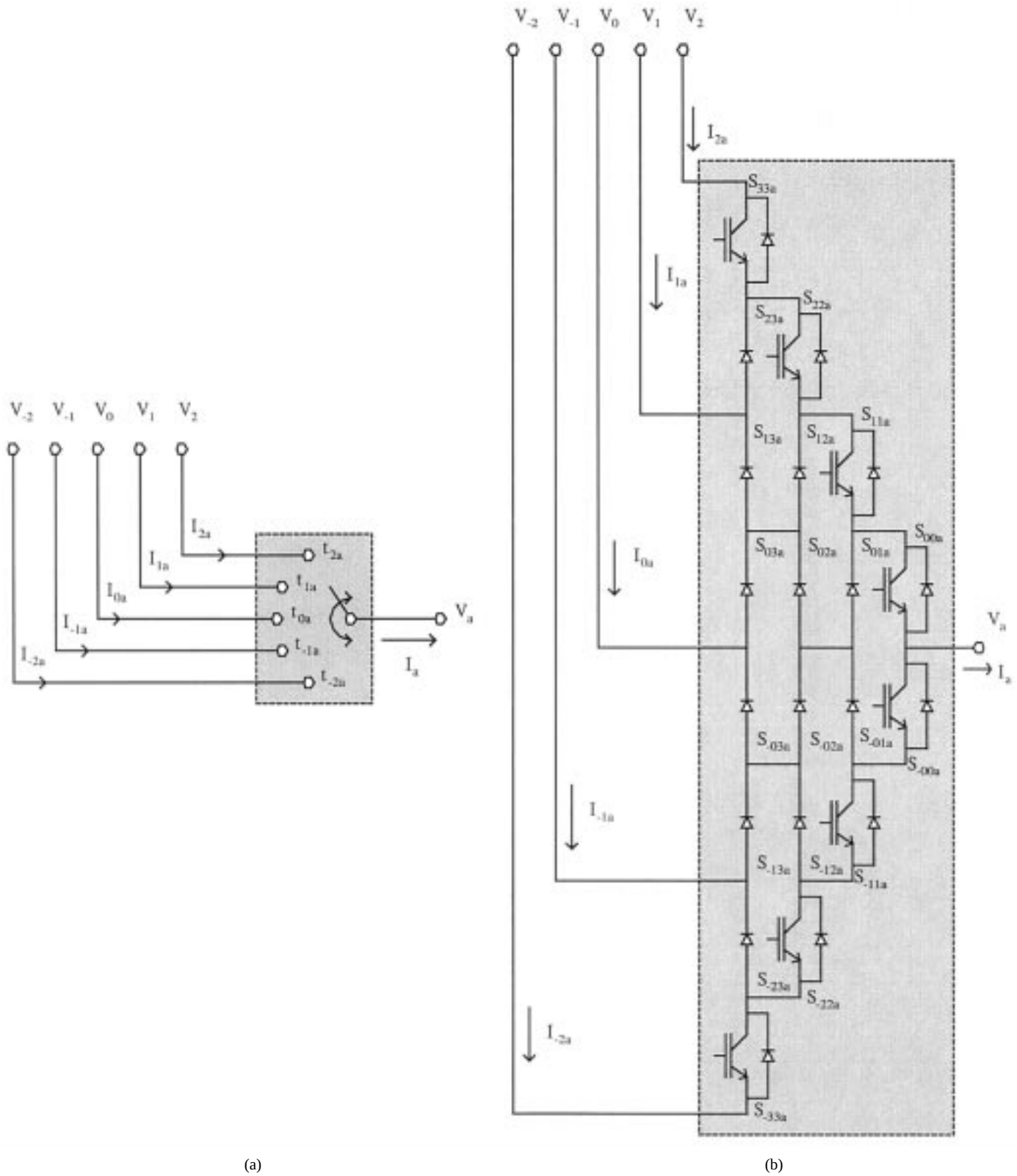
for $j = a, b,$ and c and $i = \pm 1, \pm 2 \ldots \pm N$ for even n or $i = 0, \pm 1, \pm 2 \ldots N$, for odd n. (4)

In Fig. 2, the single-pole multiple-throw switch forming the a phase of a five-level (with $N = 2$, odd) converter is illustrated. Fig. 2(a) represents the ideal switch realization and Fig. 2(b) represents an insulated gate bipolar transistor (IGBT)/diode realization. The complex, but systematic growth of the single pole multithrow switch as the number of levels increases is evident from the figure. The following observations may be made regarding the structure of the realization of a single-pole multiple-throw switch using real semiconductors.

1) The realization of each single pole n-throw switch of the n-level converter consists of $n(n-1)$ individual semiconductor device throws. Among these, $2(n-1)$ are controllable throws that have bidirectional current conducting, unidirectional voltage blocking and current turn-off capability. They may be realized using IGBTs with antiparallel diodes (or equivalent devices) as illustrated in the figure. The remaining $(n-2)(n-1)$ are uncontrolled throws, which may be realized using diodes. In such a realization, all the semiconductors carry the same voltage stress.
2) The semiconductors are grouped into $(n-1)$ series strings that are designated by 0 through $(n-2)$.
3) The pth series string consists of two controllable throws, designated S_{ppj} and S_{-ppj}. Additionally, it consists of $2p$ diodes, designated as S_{qpj}, where $q = -p+1, -p+2, \ldots p-2, p-1$. The semiconductors devices in given series string are connected such that all the diodes in the string point in the same direction, in the order designated $S_{-ppj}, S_{-p-1pj} \ldots, S_{p-1pj}, S_{ppj}$.
4) The midpoint of the zeroth string forms the pole of the switch. The extremities of the string and every alternate junction between the semiconductor throws of the $(n-$

$$H_{ij}(t) = \begin{cases} 1, & \text{if } t_{ij} \text{ is closed} \\ 0, & \text{otherwise} \end{cases} \qquad \text{for } i = \pm 1, \pm 2, \ldots \pm N \text{ for even } n;$$

$$i = 0, \pm 1, \pm 2, \pm N \text{ for odd } n;\ j = a, b \,\&\, c \tag{1}$$



(a) (b)

Fig. 2. (a) Schematic of the single-pole multiple-throw switch of the a phase of a five-level converter. (b) Its realization using the diodes and IGBTs.

2)th (or the longest) string forms the n throws of the switch.

5) The strings are interconnected such that, for all $p < n-3$ and $q = 0, 2, 4, \ldots p$, (a) the cathodes of diodes forming S_{qpj} in the pth string are connected to the cathodes of the diodes forming S_{qp+1j}, in the $(p+1)$th string; (b) the anode of diodes forming S_{-qpj} in the pth string is connected to the anode of the diodes forming S_{-qp+1j}th in the $(p+1)$th string.

6) The switching functions (H_{sqpj}) of the individual semiconductor throws S_{qpj}) for the diode-clamped converter realization may be represented by the set of matrix trans-

formations shown in (5), at the bottom of the page, where $u(.)$ is the unit step function.

The relationships shown in (5) may be used to compute the connectivity of each semiconductor switch throws of the diode clamped n-level converter realization, when the switching functions of the abstract n-level equivalent structure illustrated in Fig. 1 are known. As a result, further modeling and analysis that are developed in the paper can be focused on the switching functions H_{ij}, which may be appropriately transformed to the switching functions H_{sqpj} if necessary.

B. Equivalent Circuit

The power transfer properties between the dc sources and the ac output represented by (3) and (4) may be represented by using a matrix-vector notation, in a more compact form as follows:

$$\mathbf{V_0(t)} = \mathbf{H(t)} \cdot \mathbf{V_s} \tag{6}$$

and

$$\mathbf{I_s(t)} = \mathbf{H(t)}^T \cdot \mathbf{I_0(t)} \tag{7}$$

where

$$\mathbf{V_0(t)} = [V_a(t) \quad V_b(t) \quad V_c(t)]^T$$
$$\mathbf{I_0(t)} = [I_a \quad I_b \quad I_c(t)]^T, \text{ and}$$
$$\mathbf{V_s} = [V_N \quad V_{N-1} \quad \dots \quad V_{-N+1} \quad V_{-N}]^T$$
$$\mathbf{I_s(t)} = [I_N(t) \quad I_{N-1}(t) \quad \dots \quad I_{N+1}(t) \quad I_N(t)]^T$$
$$\mathbf{H(t)} = \begin{bmatrix} H_{Na} & H_{N-1a} & \cdots & H_{-N+1a} & H_{-Na} \\ H_{Nb} & H_{N-1b} & \cdots & H_{-N+1b} & H_{-Nb} \\ H_{Nc} & H_{N-1c} & \cdots & H_{-N+1c} & H_{-Nc} \end{bmatrix}.$$

When the repetition frequency of the switching function (or simply the switching frequency) is much larger than the of the power frequency of the desired ac output voltages, net power transfer between the dc voltages and the ac currents arises from the slowly varying average value of the switching functions. The average value of the switching functions may be readily represented by their time varying duty ratio functions of the particular throw. From the power transfer point of view, the transfer relationships (6) and (7) may be approximated by

$$\mathbf{V_0(t)} = \mathbf{M(t)} \cdot \mathbf{V_s} \tag{8}$$

and

$$\mathbf{I_s(t)} = \mathbf{M(t)}^T \cdot \mathbf{I_0(t)} \tag{9}$$

where the elements (m_{ij}) of the modulation matrix $\mathbf{M(t)}$ may be determined by computing the duty ratio of the elements of the matrix $\mathbf{H(t)}$

$$m_{ij}(\tau) = \frac{1}{T} \int_{\tau}^{\tau+T} H_{ij}(t) \cdot dt \tag{10}$$

with T being the switching period.

Relationships (6) and (7) or (8) and (9) indicate a reciprocal input $\leftrightarrow$ output transfer property similar to a transformer and feature is termed "reciprocity transposition," which is a property of all switching converters [25]. Furthermore, based on the reciprocity transposition, dc/fundamental component equivalent circuit of the multilevel converter system may be drawn as represented in Fig. 3. As may be seen from Fig. 3, the power interchange and waveform synthesis among the dc bus stack and the ac current port depend on the duty ratio of various throws. The

$$\begin{bmatrix} H_{s00j} \\ H_{s-00j} \end{bmatrix} = \begin{bmatrix} 1 & u(I_j) & \cdots & u(I_j) & 0 \\ 0 & u(-I_j) & \cdots & u(-I_j) & 1 \end{bmatrix} \cdot \begin{bmatrix} H_{Nj} \\ H_{N-1j} \\ \vdots \\ H_{-N+1j} \\ H_{-Nj} \end{bmatrix}$$

$$\begin{bmatrix} H_{s11j} \\ H_{s01j} \\ H_{s-01j} \\ H_{s-11j} \end{bmatrix} = \begin{bmatrix} 1 & u(I_j) & \cdots & u(I_j) & 0 & 0 \\ 0 & 0 & \cdots & 0 & u(I_j) & 0 \\ 0 & u(-I_j) & 0 & \cdots & 0 & 0 \\ 0 & 0 & u(-I_j) & \cdots & u(-I_j) & 1 \end{bmatrix} \cdot \begin{bmatrix} H_{Nj} \\ H_{N-1j} \\ \vdots \\ H_{-N+1j} \\ H_{-Nj} \end{bmatrix}$$

$$\begin{bmatrix} H_{s22j} \\ H_{s12j} \\ H_{s02j} \\ H_{s-02j} \\ H_{s-12j} \\ H_{s-22j} \end{bmatrix} = \begin{bmatrix} 1 & u(I_j) & \cdots & 0 & 0 & 0 \\ 0 & 0 & \cdots & u(I_j) & 0 & 0 \\ 0 & u(-I_j) & \cdots & 0 & 0 & 0 \\ 0 & 0 & 0 & \cdots & u(I_j) & 0 \\ 0 & 0 & u(-I_j) & \cdots & 0 & 0 \\ 0 & 0 & 0 & \cdots & u(-I_j) & 1 \end{bmatrix} \cdot \begin{bmatrix} H_{Nj} \\ H_{N-1j} \\ \vdots \\ H_{-N+1j} \\ H_{-Nj} \end{bmatrix}$$

$$\begin{bmatrix} H_{sNNj} \\ H_{sN-1Nj} \\ \vdots \\ H_{s-N+1Nj} \\ H_{s-NNj} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ 0 & u(I_j) & 0 & \cdots & 0 & 0 \\ 0 & u(-I_j) & 0 & \cdots & 0 & 0 \\ 0 & 0 & u(I_j) & \cdots & 0 & 0 \\ 0 & 0 & u(-I_j) & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 & 0 \\ 0 & \cdots & 0 & 0 & u(I_j) & 0 \\ 0 & \cdots & 0 & 0 & u(-I_j) & 0 \\ 0 & \cdots & 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} H_{Nj} \\ H_{N-1j} \\ \vdots \\ H_{-N+1j} \\ H_{-Nj} \end{bmatrix} \tag{5}$$

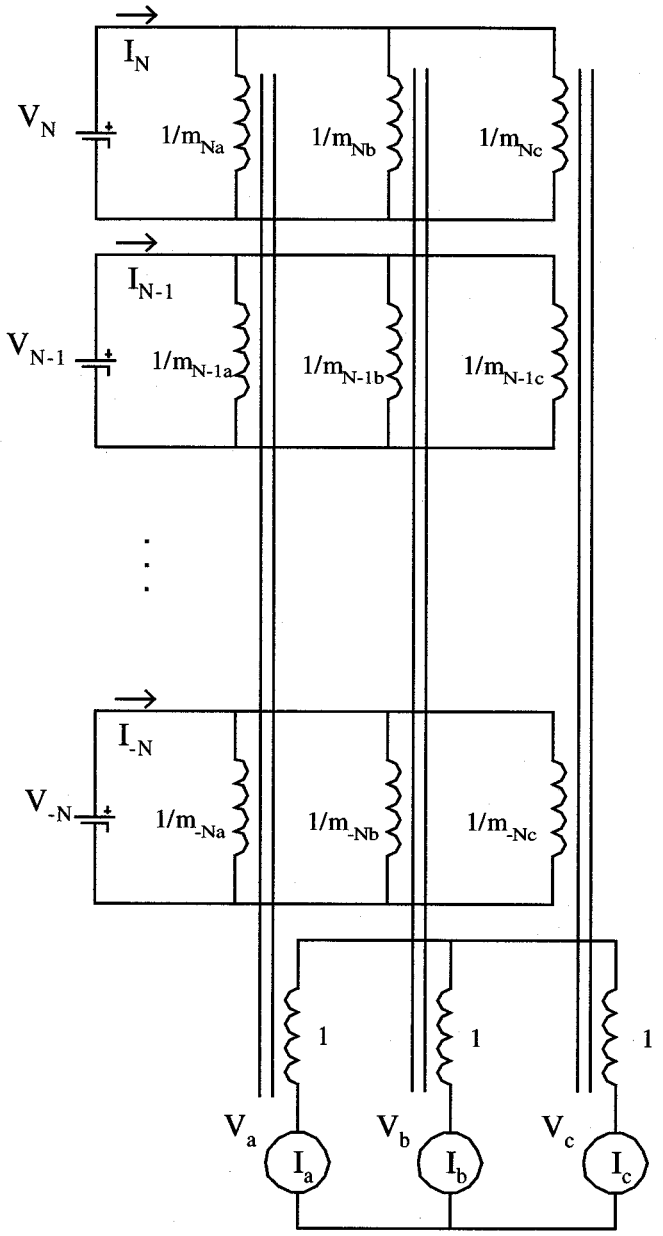


Fig. 3. Transformer-based dc/fundamental component equivalent circuit of the three-phase multilevel converter.

objective of any modulation function is to determine the duty ratio of various throws, $m_{ij}(t)$, or in general the elements of the modulation matrix $\mathbf{M(t)}$ so that any desired power transfer objectives may be fulfilled. The equivalent circuit may be conveniently utilized to study and develop appropriate modulation strategies for the multilevel converter.

III. Analysis of Multiple-Carrier-Based Modulation

Several different modulation techniques for multilevel converters have been proposed with a primary goal of synthesizing a desired set of ac voltage waveforms and a secondary goal for shaping the harmonic spectrum of the output voltage waveforms. Among these, carrier based modulation schemes have been studied quite extensively from the point of view of harmonic characterization [13]. Several variations of the basic technique, which utilize phase shifting of the triangular carrier waveforms to shape the high-frequency harmonic spectrum have been proposed. However, all of the variations are equivalent from the point of view of power transfer phenomenon and low-frequency characteristics. Therefore, the analysis here is limited to the case where all the triangular carrier waveforms are in phase.

In order to develop an analysis technique that can be extended to any number of levels, a few normalizing assumptions are made. The total dc-bus stack voltage, i.e., the difference between V_N and V_{-N} is assumed to be 2 p.u., with the midpoint assumed to be the reference voltage. As a result, the input voltage vector for an n-level converter can be expressed by

$$\mathbf{V_s} = \frac{1}{n-1}\begin{bmatrix} n-1 & n-3 & \cdots & -n+3 & -n+1 \end{bmatrix}^T. \tag{11}$$

The desired three-phase modulating signals with an amplitude of m are given by

$$\mathbf{m(t)} = m\begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix}^T. \tag{12}$$

If the output current amplitude is assumed to be 1 p.u., at a power factor angle of ϕ, the output current vector may be represented by

$$\mathbf{I_0(t)} = \begin{bmatrix} \cos(\omega t - \phi) & \cos\left(\omega t - \frac{2\pi}{3} - \phi\right) & \cos\left(\omega t + \frac{2\pi}{3} - \phi\right) \end{bmatrix}^T. \tag{13}$$

A. Modeling of Multiple-Carrier Modulation

Multiple carrier modulation technique for an n-level converter consists of $n-1$ triangular waveforms with identical peak–peak values as illustrated in Fig. 4. The peak–peak value of each waveform is $2/(n-1)$. Each carrier waveform has a distinct dc bias level such that the excursion of all the waveforms together fit the vertical span between $+1$ and -1 perfectly and none of their excursions overlap each other. Thus, each waveform spans the voltage difference between two adjacent levels of the dc-bus stack. Furthermore, the waveforms divide the vertical space into n zones $(z_N, z_{N-1}, \ldots z_{N+1}, z_{-N})$, each one corresponding to a distinct throw of the single-pole multiple-throw switch. The throws of the switch are operated such that when the modulating function of the particular phase is in a particular zone, the throw corresponding that zone is turned on. For instance, at the time denoted by the arrow in Fig. 4, $m_a(t)$ is in zone z_{-N+1} and throw t_{-N+1a} will be turned on.

B. Matrix Description of Multiple-Carrier Modulation

The modulation technique described above may be modeled mathematically to the extent that the modulation functions for each throw of the switch can be determined from the value of the desired output voltage reference waveform. For this purpose, the interval $[+1 -1]$ is divided into $n-1$ windows. The windows are labeled $(W_{N/N-1}, W_{N-1/N-2}, \ldots W_{-N+1/-N+2}, W_{-N/-N+1})$, such that the window $W_{x/y}$ is bounded in the direction away from zero by V_x and toward zero by V_y. A membership function for the modulating signal corresponding to each window can be defined as being unity when the signal occupies that window and zero otherwise.

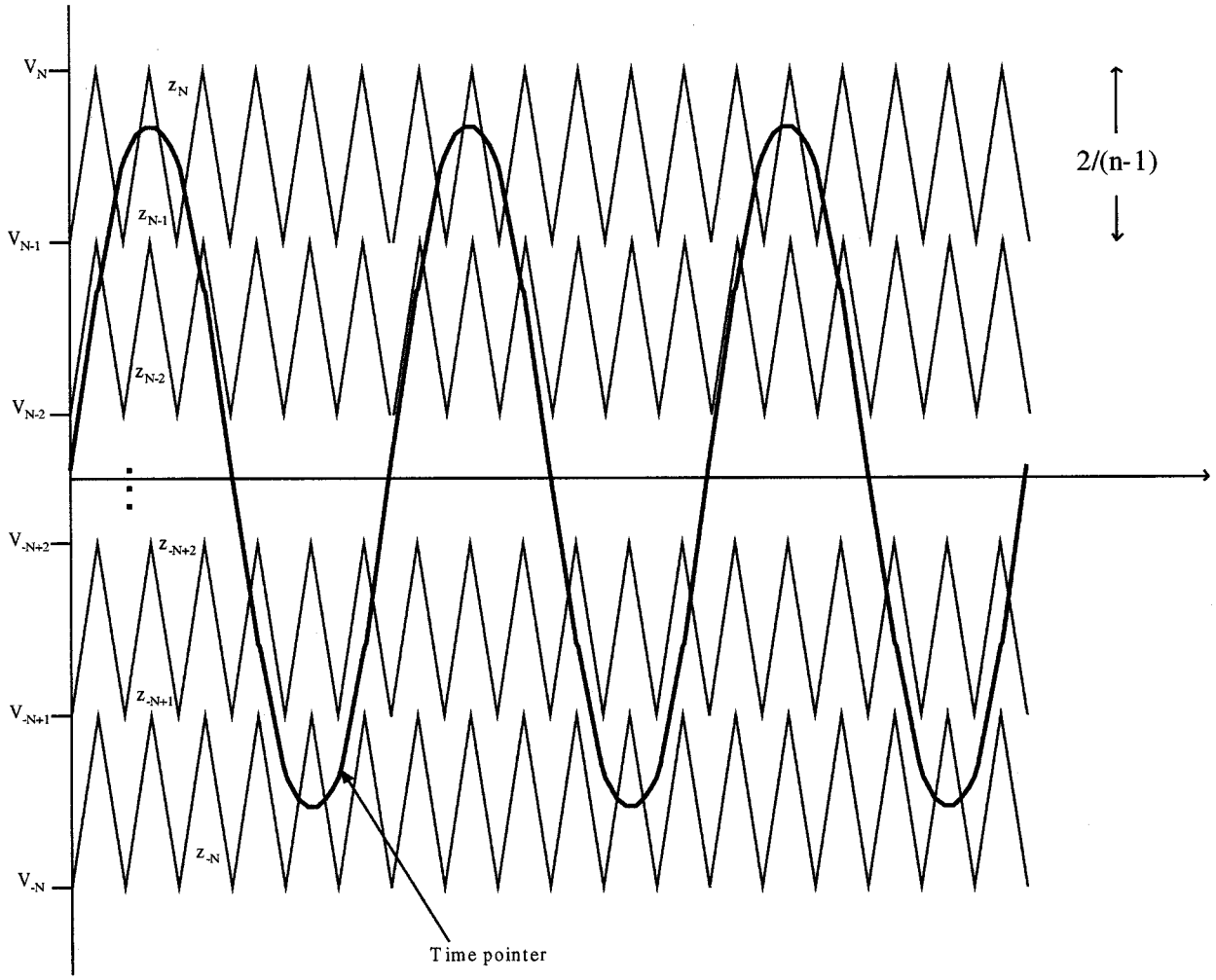


Fig. 4. Illustration of multiple triangular carrier waveforms and modulating waveforms for multilevel converter.

When the modulator is not saturated, the modulating signal $[m(t)]_j$ falls within the interval $[+1\ -1]$ and, hence, will have its membership function corresponding to one window unity and every other one zero. An example of the windows, modulating signal and its membership function for $W_{1/0}$ for a five-level converter is illustrated in Fig. 5.

Using this definition of the membership function, the duty ratio of the ith throw of the jth switch is given by

$$m_{ij}(t) = \frac{[m(\mathbf{t})]_j - V_i}{V_{i+1} - V_i} W_{i+1/i}\,[m(\mathbf{t})]_j + \frac{V_i - [m(\mathbf{t})]_j}{V_{i+1} - V_i} W_{i/i-1}\,[m(\mathbf{t})]_j\,. \quad (14)$$

An example of the modulation function of Throw 1 for a four-level converter is illustrated in Fig. 6. In the case of this modulation strategy, the three-phase output voltage waveforms have an amplitude of m, which also becomes the modulation index.

C. Average Output Voltage and Input Current Waveforms

Using the model for the modulation functions as developed in the above discussion, the output voltages and input currents of diode-clamped converter with any number of levels can be readily determined, given the modulation index and the power factor of the output using (8) and (9).

The average input current waveforms for a five level converter for a modulation index of 0.75, at a power factor of 0.8 is illustrated in Fig. 7. The horizontal axis covers one period of the output waveforms.

It is clear from the figure that the input currents contain a large amount of low-frequency harmonics and this is one of the major sources of voltage variations of the dc-bus levels, especially at low output frequencies. It is also clear that under the chosen operating conditions, the average current drawn from the outer nodes of the dc-bus stack is lower than that from the inner nodes of the dc-bus stack. Moreover, there is a large amount of third harmonic current injected into the midpoint of the dc-bus stack. The nonzero nodes also carry a large amount of third-harmonic current loading.

Since the average current from each node can be calculated using the proposed approach, the average net power injection at each level can be readily determined. In singly fed systems, it is quite clear from the above waveforms that the node voltages would gradually collapse, resulting in a two level converter. However, in multifed systems where each of the nodes of the multilevel bus is fed from an active source, this approach can be used to suitably size the power sources for each of the

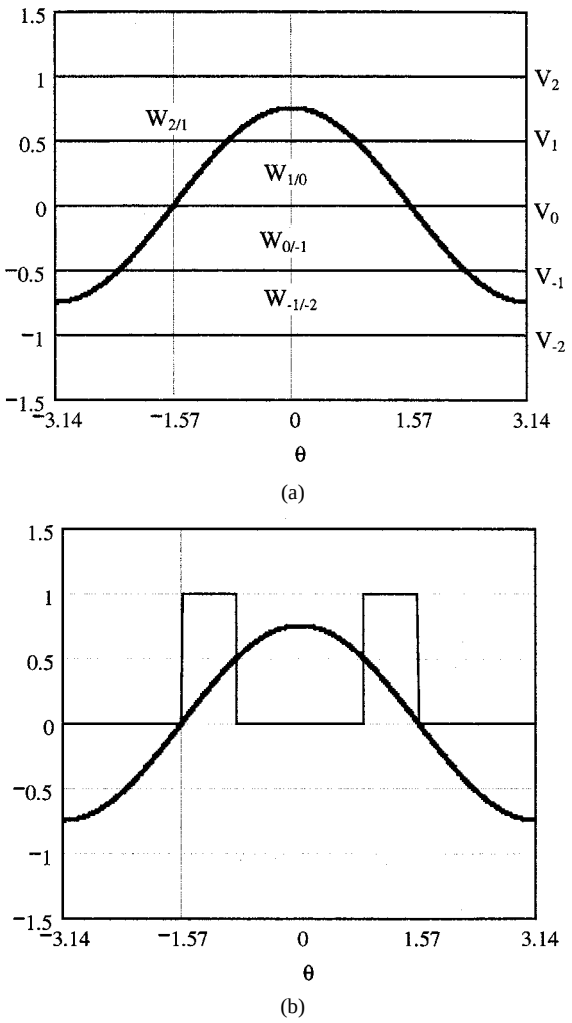


Fig. 5. (a) Carrier windows and modulating waveform for a five-level converter with a modulation index of 0.75. (b) Window membership function for $W_{1/0}$ for the waveform.

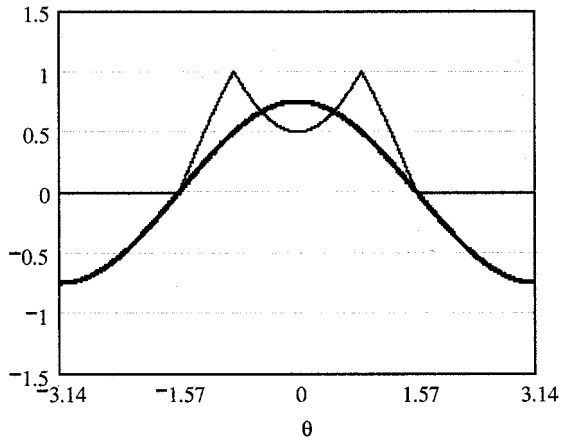


Fig. 6. Example modulation function and modulating waveform for Throw 1 for the five-level converter.

levels under different operating conditions. In a back-to-back system, the source converter and load converter would feed each other, albeit at different frequencies and provide net power balance. Furthermore, the harmonic current injection into the nodes

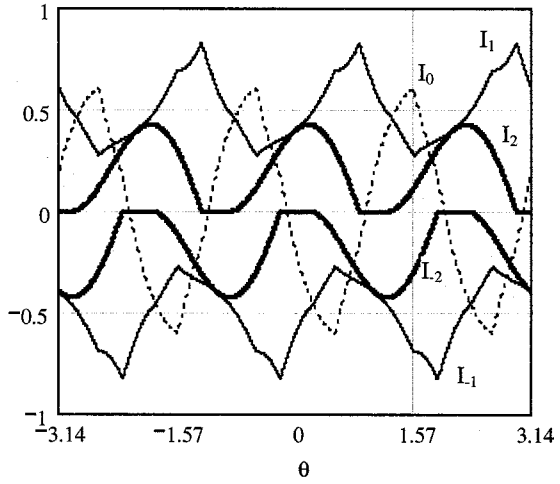


Fig. 7. Average input current waveforms using multiple carrier modulation at a modulation index of 0.75 and power factor of 0.8 for a five-level converter.

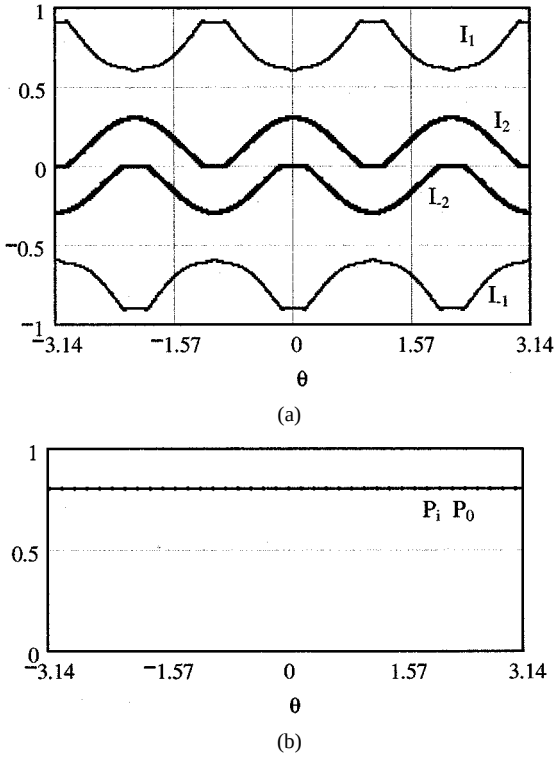


Fig. 8. (a) Average input currents and (b) total input and output power waveforms using multiple carrier modulation at a modulation index of 0.53 and power factor of 1 for a four-level converter.

under different operating conditions may also be determined, thereby enabling appropriate choice of capacitor elements for the bus stack.

Average input currents for a four-level converter are illustrated in Fig. 8, along with total input and total output power waveforms. It is clear that although the individual input current waveforms are rich in harmonics, the total power drawn from the dc-bus stack remains constant, since the output power of a balanced three-phase system is constant. This feature provides the main motivation for the modulation strategy proposed further in the following section.

IV. Reciprocity-Transposition-Based Modulation

Under balanced loading conditions, it would be desirable to draw equal amounts of current from each of the nodes of the dc-bus stack. This would minimize ripple currents in the capacitors. Moreover, if each of the nodes of the dc-bus stack are fed from a different power converter, it would be highly desirable to have the load at the nodes draw constant currents. Furthermore, the currents injected from the top half of the nodes of the dc-bus stack would be positive and the bottom half of the dc-bus stack would be negative for net power flow from the dc bus to the ac output. The direction of currents would reverse under ac-to-dc net power flow conditions.

The load currents drawn from the ac port of the converter would nominally form a balanced three-phase ac system. Rewriting (4) using (10) and (13), the dc current injection into the ith node of the converter may be calculated in terms of the load current and modulation functions as

$$I_i(t) = m_{ia}(t)\cos(\omega t - \phi) + m_{ib}(t)\cos\left(\omega t - \frac{2\pi}{3} - \phi\right) + m_{ic}(t)\cos\left(\omega t + -\frac{2\pi}{3} - \phi\right). \quad (15)$$

From (15), it can be concluded that if $m_{ia}(t)$, $m_{ib}(t)$ and $m_{ic}(t)$ have a common term and/or if they form a balanced three-phase set at frequency ω, then the average value of $I_i(t)$ will reduce to a constant value. The following choice of modulation function realizes exactly that, while also maintaining the desired output voltage

$$m_{ij}(t) = S(V_i)\,\frac{1 + [\mathbf{m(t)}]_j sign(V_i)}{2}. \quad (16)$$

Here, $S(V_i)$ defined as the "sharing function" of a given node, determines the share of the current that will be drawn from the ith node of the dc-bus stack. Typically, the current drawn from the midpoint of the dc-bus stack or the null node should be zero, since that node is not capable of delivering net power under symmetric ac output conditions. As a result, $S(V_0)$ may be chosen to be zero, in case the converter has odd number of levels.

In a symmetric converter, the number of nodes with positive voltages is equal to the number of nodes with negative voltages. For net power flow from the dc ports to ac ports, the sum of currents drawn from the positive nodes will be equal to the sum of currents sunk into the negative nodes, since we desire zero current into the null node in case it is present. Therefore, the sum of all the sharing functions for a given converter should equal 2.

The total current drawn from the positive nodes may be split from among all the positive nodes. Furthermore, for symmetrical operating conditions, the ratio in which the currents are split among the positive nodes would have to be identical to the ratio in which they are split among the negative nodes. For instance, it may be desirable to source/sink 50% of the current from outer most pair of terminals and 25% each from the inner two pairs of terminals in a six-level converter. In that case, $S(V_3) = S(V_{-3})$, $S(V_2) = S(V_{-2})$, and $S(V_1) = S(V_{-1})$, would be chosen to be 0.5, 0.25, and 0.25 respectively. If it is desired to draw equal amount of currents, all the sharing functions would be chosen to be 1/3.

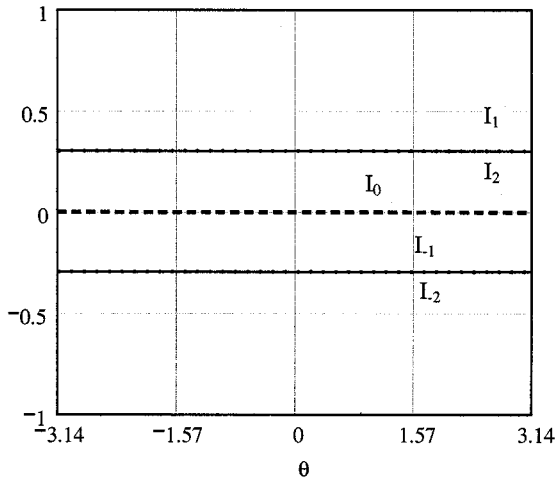


Fig. 9. Average input current waveforms using reciprocity-transposition-based modulation at an effective modulation index of 0.75 and power factor of 0.8 for a five-level converter and current-sharing function 1:1.

It may also be observed from these figures that the variable $S(\cdot)$ controls the amount of the current injected into or drawn out of a given node of the dc bus. Therefore, it may actually be used as a control input to regulate the particular node voltage of the dc-bus stack should a need arise. This feature can be conveniently incorporated into a scheme for maintaining dc-bus regulation as is common with other approaches to modulation, while simultaneously eliminating low-frequency ac components in the dc-bus currents.

The peak output voltage (V_{op}) that is achievable from the converter is a function of the amplitude of the modulating signals and the sharing functions. It can be shown that

$$V_{op} = m\sum_{i>0} V_i \cdot S(V_i). \quad (17)$$

Thus, the modulation index of the system under the proposed strategy for a given m is reduced by the factor equal to the summation term in (17). For instance, the peak output voltage available (at $m = 1$) from a four-level converter (with voltage levels [1 .333 −.333 − 1]) that uses equal current sharing between inner and outer nodes ($S(V_2) = S(V_1) = S(V_{-1}) = S(V_{-2}) = 0.5$) becomes 0.667. This is expected, because, the proposed modulation strategy necessarily utilizes *all* the available voltage levels to synthesize the desired output and, hence, compromises on modulation efficiency. However, by choosing a different set of sharing functions, for instance, with ($S(V_2) = S(V_{-2}) = 1$ & $S(V_{-1}) = S(V_{-1}) = 0$), one is able to restore the maximum voltage attainable from the system to be unity. Thus, through prudent choice of sharing functions at any desired modulation index, it is possible to optimize system performance objectives.

Fig. 9 illustrates the input current waveforms for a five-level converter, at operating conditions identical those in Fig. 7. As may be observed, although the output voltage of the two cases are identical, the average input currents are now constant and equal. The current injection into the null node is zero. In Fig. 10, the input current waveforms are repeated for a 2:1

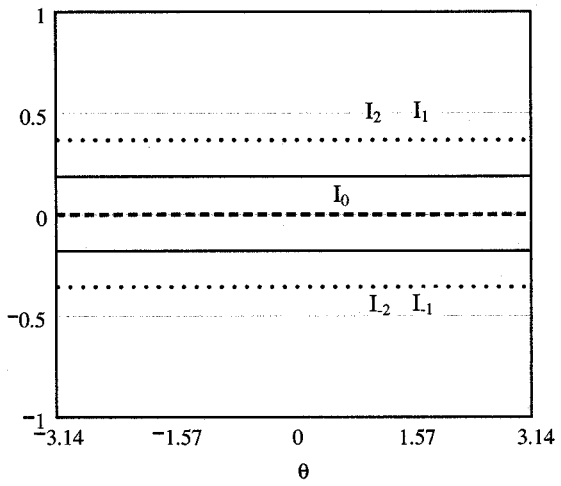


Fig. 10. Average input current waveforms using waveforms using reciprocity-transposition-based modulation at an effective modulation index of 0.75 and power factor of 0.8 for a five-level converter and current-sharing function 2:1.

current-sharing ratio between the outer nodes and the inner nodes, while maintaining current injection into the null node zero and the output voltage at the same amplitude.

It is clear that the sharing functions can be effectively used to steer current into or away from every node without compromising the quality of the desired average output voltage waveforms. However, depending on the sharing functions used, the amplitude (m) of the modulating signals, $\mathbf{m(t)}$, will have to be modified in comparison with the conventional strategy to account for the application of additional voltage levels in order to synthesize the same output voltage level.

In singly fed systems, under steady-state operating conditions, the sharing functions for the inner nodes would be zero and the outermost nodes would be unity. However, the sharing functions may be used actively to maintain the intermediate voltage levels at their appropriate quiescent conditions. Otherwise, the voltage stress across the power semiconductor throws would exceed their design limits, which would compromise the most desirable feature of the diode clamped multilevel converter.

In multifed systems, the voltage levels at the intermediate nodes of the dc bus would be fed from independent dc power sources or from a similar multilevel converter. In such the case, with the proposed modulation approach, the design of the replenishing sources becomes simple because of controlled loading at each of the nodes. Furthermore, the capacitors do not carry any low frequency current injection and, hence, could be of a smaller value. This is particularly significant for motor drive applications, where the output frequencies may be low, and large capacitors will be needed to limit the voltage ripple in the case of conventional modulation techniques.

Fig. 11 shows the input currents drawn from the various nodes for a four-level converter. The instantaneous total input and output power waveforms are also plotted. They may be compared with the results from Fig. 8 using a conventional modulator. These results illustrate the efficacy of the proposed modulation algorithm in suitably controlling the dc-bus power flow in both even- and odd-level converters.

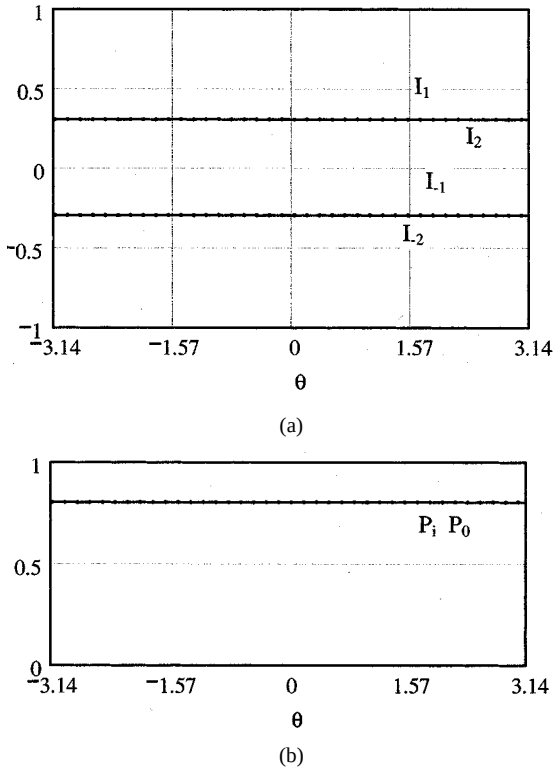


Fig. 11. (a) Average input currents and (b) total input and output power waveforms using reciprocity-transposition modulation at a modulation index of 0.53 and power factor of 1 for a four-level converter.

V. Simulation Results

A detailed circuit model of the diode-clamped four-level converter was simulated using commercial power conversion circuit simulation software (PSIM) [26]. The model was used to implement the modulation algorithm presented here as well as the conventional modulation algorithm using multiple carrier waveforms. The switching frequency was chosen to be 1 kHz in order to better illustrate the switching features of the waveforms in traces.

A. Conventional Multiple-Carrier Modulator

Fig. 12 shows the traces of phase voltage (a–c) using a multiple carrier modulator for a modulation index of 53% at unity power factor. In Fig. 12(d) and (e), the Fourier spectra of the dc-bus node currents computed using discrete Fourier transform (DFT) are shown. In addition to the switching frequency harmonics that occur at the sidebands of multiples of the switching frequency, a dominant amount of low-frequency harmonics is readily apparent from the Fourier spectrum. Furthermore, the larger dc current drawn from the inner nodes is also evident from the spectrum.

B. Reciprocity-Transposition-Based Modulator

Fig. 13 shows similar traces of phase voltage (a–c) using a reciprocity-transposition modulator for a modulation index of 53% at unity power factor. In Fig. 13(d) and (e), the Fourier spectra of the dc-bus currents are shown. The absence of low-frequency harmonics and equal value of dc components of the dc-bus currents are readily apparent from the Fourier spectra.

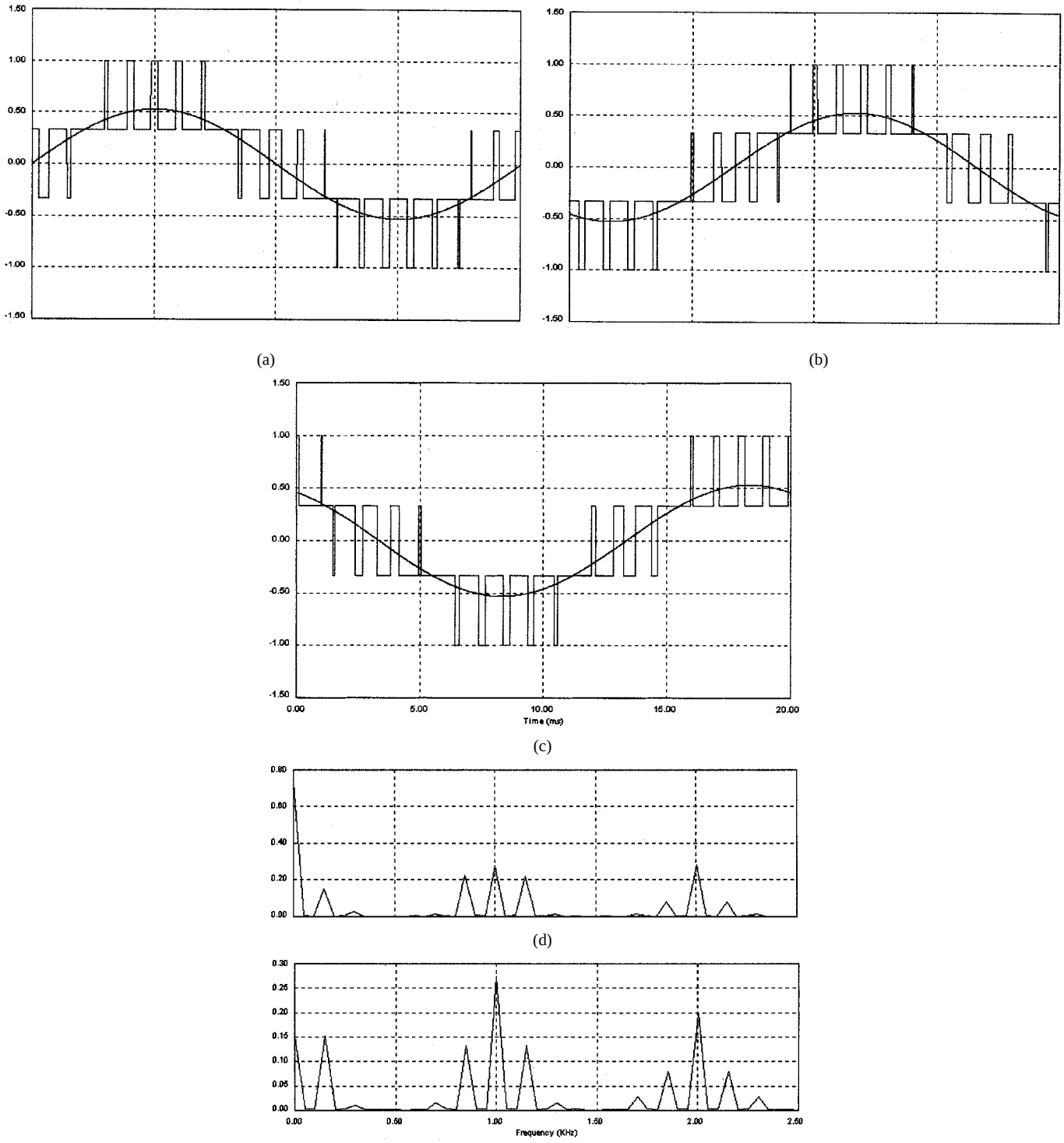


Fig. 12. (a)–(c) Simulation waveforms using multiple carrier modulation. (d) Three-phase output voltages, Fourier spectrum of inner node input current. (e) Fourier spectrum of outer node input current. Modulation index of 0. 53 and power factor of 1.

The dominant harmonics occur at the sidebands of multiples of the switching frequency. The simulation results thus confirm the modeling approach and the analytical results that have been presented.

The output voltage waveforms shown in Figs. 12(a)–(c) and 13(a)–(c) also indicate certain disadvantages of the proposed approach: 1) there are a higher number of switching events; 2) there are large phase voltage variations; and 3) there are large common-mode voltage variations in the output voltage. These issues will have to be carefully weighed against the advantages offered by the proposed approach in a given application.

VI. Conclusions

This paper has presented the application of reciprocity transposition as a systematic technique for studying the effect of

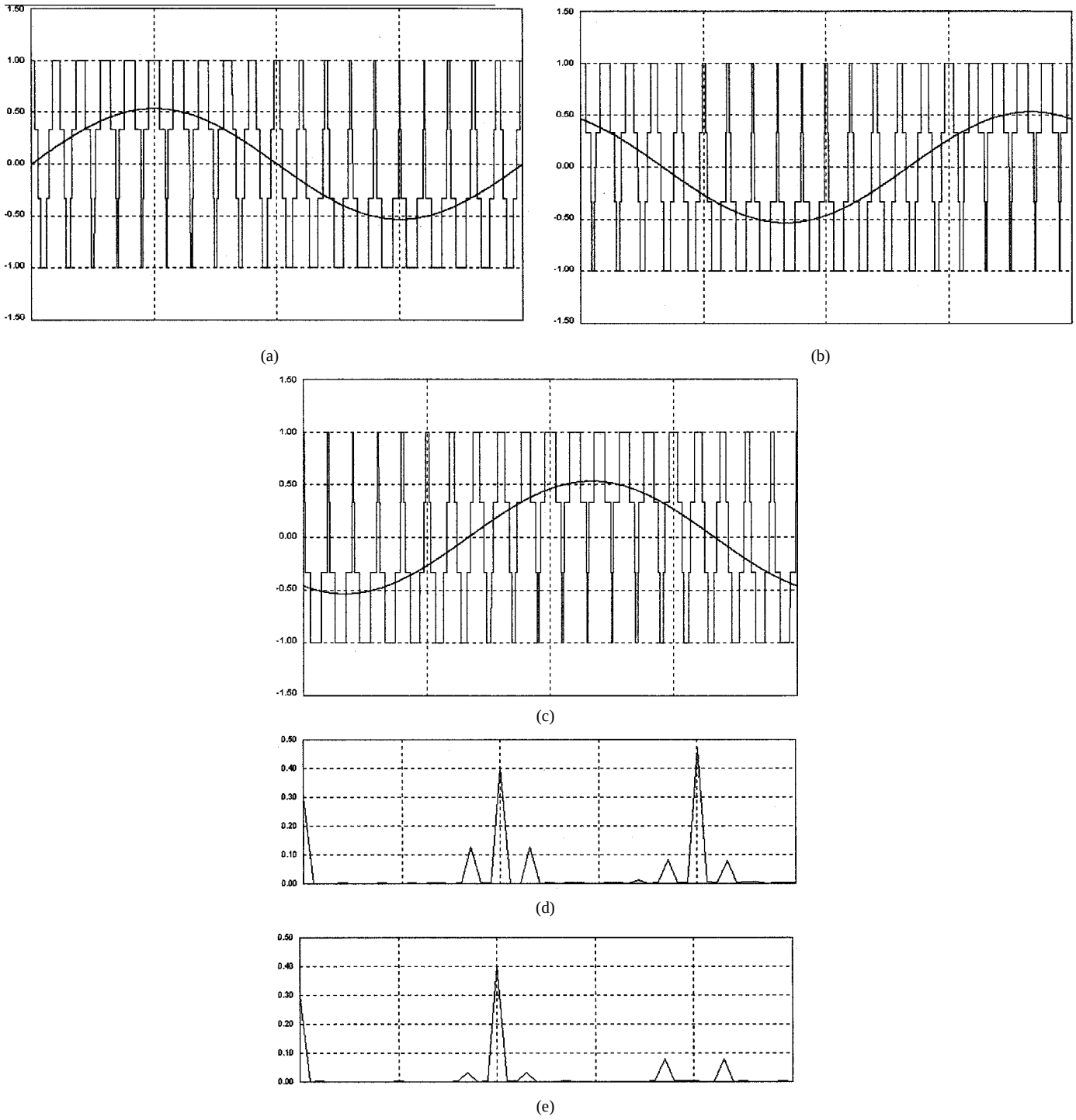


Fig. 13. (a)–(c) Simulation waveforms using reciprocity-transpsition-based modulation. (d) Fourier spectrum of inner node input current. (e) Fourier spectrum of outer node input current. Modulation index $= 0.53$ and power factor $= 1$.

modulation strategy on the current injection at the dc-bus terminals of a multilevel converter. Generally, most modulation strategies for multilevel converters have focused on the output voltage synthesis exclusively. The concomitant dc current injection results in large low-frequency variation in the stack voltages and often need corrective controllers to be incorporated. A simple but efficient technique to evaluate steady state current injection into the nodes of the dc-bus stack was presented here. The technique can be used for sizing the capacitors and incorporate appropriate power sources that feed into the different nodes of the dc-bus stack to maintain power balance. Although reciprocity transposition was presented for a carrier based modulation strategy, it can be extended to evaluate the performance of the system under any desired modulation strategy, once the modulation functions are determined.

A modulation strategy was proposed in the paper that eliminates low-frequency ripple current injection into the nodes of the dc bus stack under balanced operating conditions. The average currents drawn from each of the nodes of the dc-bus stack are constant and may be made equal. The currents are predeter-

mined by the choice of the modulation function and, hence, can be used for sizing energy replenishing power sources connected to the dc-bus stack. Moreover, the share of the current drawn from each of the nodes can be varied and, hence, can be used as a control handle to raise or lower any particular node voltage of the dc-bus stack. The strategy is equally applicable to converters with an even and an odd number of levels.

Analytical results from the application of the proposed technique to example converters with four and five levels have been presented. The results were verified using computer simulations on a four-level converter.

Reciprocity transposition as an analytical and modeling tool for study of multilevel converters has not been explored extensively with switching power converters. This paper has attempted to apply this principle in the field of multilevel converters and better manage input power flow. It is expected the application of this valuable tool will lead to further developments and yield even better modulation techniques.

REFERENCES

[1] N. P. Schibli, T. Nguyen, and A. C. Rufer, "A three-phase multilevel converter for high-power induction motors," *IEEE Trans. Power Electron.*, vol. 13, pp. 978–986, Sept. 1998.

[2] Y. Chen, B. Mwinyiwiwa, Z. Wolanski, and O. Boon-Teck, "Regulating and equalizing DC capacitance voltages in multilevel STATCOM," *IEEE Trans. Power Delivery*, vol. 12, pp. 901–907, Apr. 1997.

[3] J. S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1995, pp. 2348–2356.

[4] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A nonconventional power converter for plasma stabilization," in *Proc. IEEE PESC'88*, 1988, pp. 122–129.

[5] R. H. Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Conf. Rec. IEEE-IAS Annu. Meeting*, vol. 4, 1999, pp. 2662–2669.

[6] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel inverters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1999, pp. 1186–1192.

[7] P. Hammond, "A new approach to enhance power quality for medium voltage drives," in *Proc. IEEE-IAS PCIC Tech. Conf.*, 1995, pp. 231–235.

[8] M. D. Manjrekar, "Topologies, analysis, controls and generalization in H-Bridge multilevel power conversion," Ph.D. dissertation, Dept. Elect. Comput. Eng., Univ. Wisconsin, Madison, 1999.

[9] G. Sinha and T. A. Lipo, "A four level rectifier-inverter system for drive applications," in *Conf. Rec. IEEE-IAS Annu. Meeting*, vol. 2, 1996, pp. 980–987.

[10] Q. Jiang and T. A. Lipo, "Switching angles and DC link voltages optimization for multilevel cascade inverters," in *Proc. IEEE PEDES'98*, 1998, pp. 56–61.

[11] S. K. Biswas and B. Basak, "Stepped wave synthesis from preprogrammed PWM inverters with a common DC-DC converter supply," in *Proc. IEEE PEDES'96*, 1996, pp. 161–167.

[12] S. Sirisukprasert, J.-S. Lai, and T.-H. Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, vol. 4, 2000, pp. 2094–2099.

[13] G. Carrara, S. Gardella, M. Marchesconi, R. Salutari, and G. Schiutto, "A new multilevel PWM method: A theoretical analysis," in *Proc. IEEE PESC'90*, 1990, pp. 363–371.

[14] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," in *Proc. IEEE PESC'98*, vol. 1, 1998, pp. 172–178.

[15] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Applicat.*, vol. 37, pp. 637–641, Mar./Apr. 2001.

[16] T. Ishida, K. Matsuse, K. Sasagawa, and L. Huang, "Fundamental characteristics of a five-level double converter for induction motor drive," in *Conf. Rec. IEEE-IAS Annu. Meeting*, vol. 4, 2000, pp. 2189–2196.

[17] M. Manjrekar and G. Venkataramanan, "Advanced topologies and modulation strategies for multilevel inverters," in *Proc. IEEE PESC'96*, vol. 2, Baveno, Italy, 1996, pp. 1013–1018.

[18] L. M. Tolbert, F. Zheng Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 36–44, Jan./Feb. 1999.

[19] ——, "A multilevel converter-based universal power conditioner," *IEEE Trans. Ind. Applicat.*, vol. 36, pp. 596–603, Mar./Apr. 2000.

[20] J. Rodriguez, L. Moran, A. Gonzalez, and C. Silva, "High voltage multilevel converter with regeneration capability," in *Proc. IEEE PESC'99*, vol. 2, 1999, pp. 1077–1082.

[21] Y. Chen, B. Mwinyiwiwa, Z. Wolanski, and O. Boon-Teck, "Unified power flow controller (UPFC) based on chopper stabilized diode-clamped multilevel converters," *IEEE Trans. Power Electron.*, vol. 15, pp. 258–267, Mar. 2000.

[22] Y. Chen and O. Boon-Teck, "STATCOM based on multimodules of multilevel converters under multiple regulation feedback control," *IEEE Trans. Power Electron.*, vol. 14, pp. 959–965, Sept. 1999.

[23] F. Zheng Peng, J.-S. Lai, J. McKeever, and J. VanCoevering, "A multilevel voltage-source converter system with balanced DC voltages," in *Proc. IEEE PESC'95*, vol. 2, 1995, pp. 1144–1150.

[24] F. Zheng Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Applicat.*, vol. 37, pp. 611–618, Mar./Apr. 2001.

[25] M. Venturini and A. Alesina, "The generalized transformer: A new bidirectional sinusoidal waveform frequency converter with continuously adjustable input power factor," in *Proc. IEEE PESC'80*, 1980, pp. 242–252.

[26] *PSIM Users Manual, Version 5.0*, Powersim, Inc., Noth Andover, MA, 2001.

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