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Reconfigurable Multi-Band Quadrature $\Sigma\Delta$ Modulators

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***Abstract*—A new design methodology for reconfigurable quadrature band-pass $\Sigma\Delta$ modulator is proposed. The methodology uses architectures, which locks various range of IF frequencies to the sampling frequency for lower order quadrature modulators. A gereralized integrator based architecture is developed from the delay architectures. The method is presented with derivation of the base circuitry and with this base circuitry stringent performance can be satisfied by extending the work to cascading lower order quadrature modulators with possible image reduction techniques.**

***Index Terms*—$\Sigma\Delta$, quadrature modulators, High-pass, Reconfigurablity, Complex, ADC, Low-pass, Band-pass,cascade, MASH.**

I. Introduction

The trend in the modern receivers is to move the analog to digital converter (ADC) as close as possible to the antenna. As the wireless communication systems migrate to support multi band and multi standard radios, the requirements of ADC's are very demanding and challenging. Ideally by placing the ADC close to the antenna, functions such as filtering, band selection and frequency translation are performed in the digital domain, which increases the flexibility of the receiver. The architecture is known as software defined radio (SDR) [1], where entire RF signals directly converted into digital data. Since the down conversion and demodulation are implemented in digital domain these architectures provide complete reconfigurability and programmability, but the feasibility of the architecture may not be possible for hand held applications as the requirements of ADCs could be above few GHz with resolution over 10 bits and power consumption within few mWs.

To meet the anticipated requirements imposed by emerging standards, RF is translated down to a low intermediate frequency (IF) or to baseband before being digitized and processed. These architectures known as Zero-IF or Low-IF architectures provides little amount of reconfigurability [2]. The bandwidth and linearity requirements of ADCs are reasonable but difficult to satisfy next generation standards.

$\Sigma\Delta$ modulators [3], [4] are good candidates for the implementation of ADCs for wireless receiver applications since robustness of the architecture towards circuit imperfections without significant performance degradation. Better spectrum efficiency can obtained from quadrature band-pass $\Sigma\Delta$ modulator as they consume lower power than a pair of real band-pass modulators.

The generalized quadrature receiver architecture is as shown in Fig.1. Unlike a real band-pass $\Sigma\Delta$ modulators, the zeros

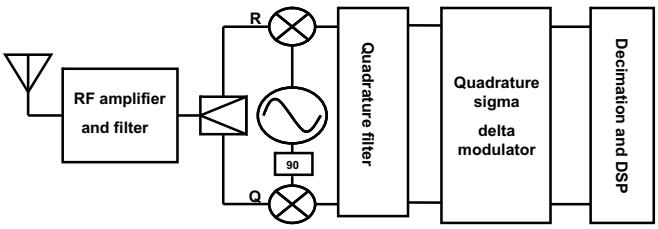

Fig. 1. Generalized quadrature receiver architecture.

of quadrature noise transfer function (NTF) are need not be complex conjugate. Zeros can be distributed around the intermediate frequency $f_S/2$. Thus, it provides twice the noise shaping with respect to real band-pass $\Sigma\Delta$ modulator [5]. On the contrary quadrature architectures are vulnerable to path mismatches between I and Q paths. As a result quantization noise in the image band is folded into signal band thus degrading the performance. The possible solution would be place one of the zeros of quadrature NTF at image location [5].

This paper presents an architectural solution for reconfigurablity in quadrature $\Sigma\Delta$ modulator without loosing performance. The modulator operates at multi modes ranging from low-pass to high-pass. Higher bandwidth can be obtained from cascading lower reconfigurable architecture.

II. Four Second Order Architectures

Many Quadratrue architectures use the integrators as basic blocks [6], [7] that are actually delays in loop configuration. Before studying possible block diagrams let us consider one of the possible NTFs [8] with aggressive noise shaping zeros on the unity circle at the positions $e^{j\phi_i}$, $i = 1, n$. The *NTF* is

$$NTF = \prod_{1}^{n}\left[1 - \frac{e^{j\phi_i}}{z}\right] = 1 + \frac{a_1}{z} + \ldots + \frac{e^{j\sum_i^n \phi_i}}{z^n} \quad (1)$$

Depending on the zero position the last term which has modulus one and phase that is the addition of the phase of all the zeros. The method developed in this paper limits the zero positioning to situations for which $\sum_i^n \phi_i = 0, \pi/2, \pi, 3\pi/2$ or correspondingly the last coefficient of (1) is $1, j, -1$ or $-j$. The reason for this choice is that the first and the last term can be implemented with minimal number of hardware. It is possible to design the NTF architectures ending with fractional coefficients but this would require additonal hardware without enhancement in the performance.

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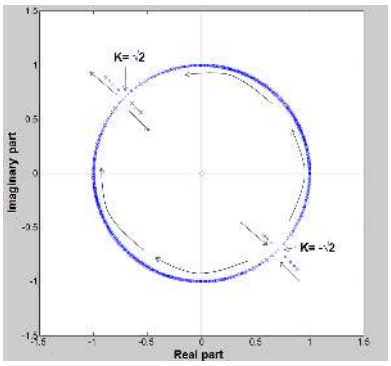

Fig. 2. Root locus of the complex zeros as k varied from $k = -1.45$ to $k = 1.45$.

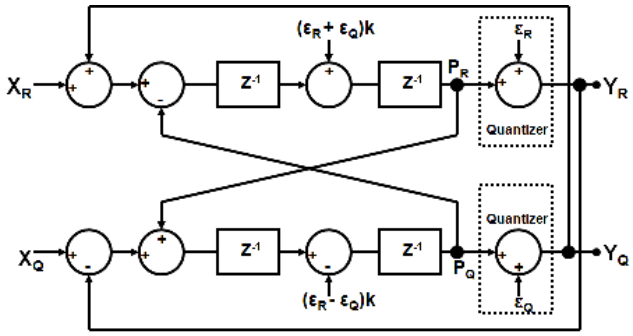

Fig. 3. Second order quadrature band-pass $\Sigma\Delta$ architecture for *NTF* = $1 + z^{-1}k(1-j) - jz^{-2}$ with IF= $3f_N/4$.

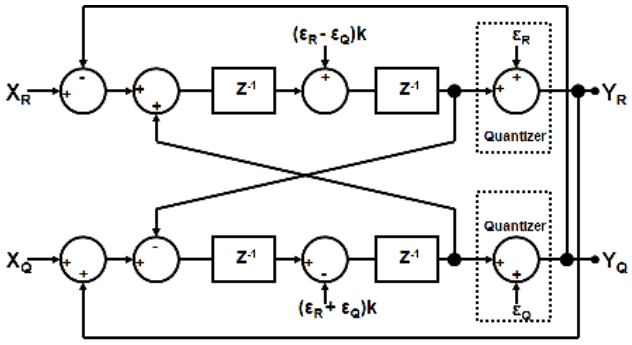

Fig. 4. Second order quadrature band-pass $\Sigma\Delta$ architecture for *NTF* = $1 - z^{-1}k(1+j) + jz^{-2}$ with IF= $f_N/4$.

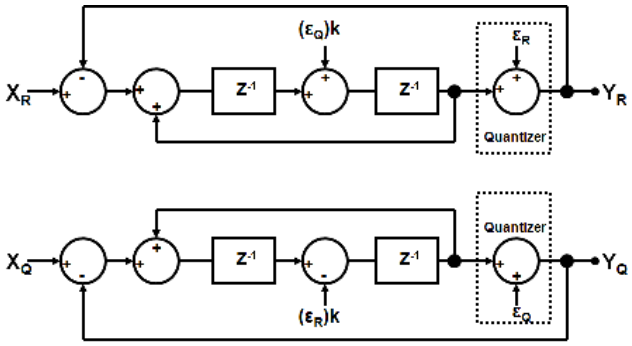

Fig. 5. Second order quadrature band-pass $\Sigma\Delta$ architecture for *NTF* = $1 + z^{-1}k(j) - z^{-2}$ with IF= $f_N/2$.

This work utilizes $n = 2$ and delay elements "z^{-2}" are sufficent for implementation and basic building block with complex transfer function $z^{-1}/(1 \pm jz^{-2})$ can be achieved. The design method discussed in [8] gives rise to the basic modulator used here in this cascade scheme. It is shown that a simple two delay scheme realizes two terms of the expected *NTF*; therefore, it is necessary to realize the inner term of the equation (1). In-order to design a modulator whose *NTF* has two zeros, one must have $\phi_1 + \phi_2 = 3\pi/2$. For such a case

$$\begin{aligned} NTF1 &= 1 - (e^{j\phi_1} + e^{j\phi_2})z^{-1} - jz^{-2}. \\ &= 1 - \alpha z^{-1} - jz^{-2}. \end{aligned} \quad (2)$$

where α is a complex number whose modulus must be less than $\sqrt{2}$. The missing middle term of the NTF is $-\alpha z^{-1}$. If the phases of the zeros are symmetrical with respect to $3\pi/4$ ($\phi_{1,2} = 3\pi/4 \pm \delta$), then

$$\alpha = -(1+j)k, \quad (k < \sqrt{2}) \quad (3)$$

Notice that if $k = 1$, then $z_1 = 1$ and $z_2 = -j$. For $k = \sqrt{2}$ and $k = -\sqrt{2}$ the zeros are coincident in second and fourth quadrant respectively. Indeed, figure 2 shows the root locus of the NTF as the parameter k varied. For $k < 1$ the zeros are in the fourth quadrant. By controlling k notch bandwidth can be changed but notch frequency is firmly defined.

The implementation of the missing term requires one delay and two quantization noise components, one from the real path, the other from the quadrature path. The architectural implementation of the targeted NTF is as shown in figure. 3, while the addition of the two quantization errors amplified by k are injected into the intermediate point with appropriate signs.

The accuracy of the result depends on the network used for the implementation of the middle terms of the NTF, however, an error on k causes a shift of the zeros proportional to the sensitivity of $\phi_{1,2}$ to k. If the zeros are apart enough the sensitivity is not very high and the effect of mismatches causes a negligible variation of the *SNR*. The same is true for error

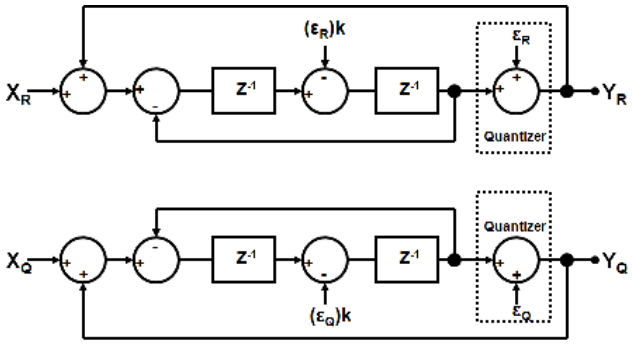

Fig. 6. Second order quadrature band-pass $\Sigma\Delta$ architecture for *NTF* = $1 - z^{-1}k + z^{-2}$ with IF located at zero.

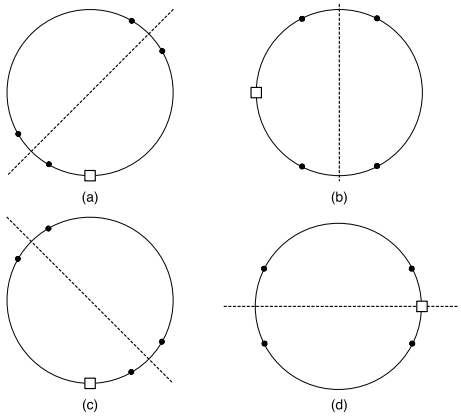

Fig. 7. Possible NTF Zero distribution: a)IF at $f_N/4$ or $5f_N/4$. b) IF at $\pm f_N/2$. c)IF at $3f_N/4$ or $7f_N/4$ d)IF at zero or $f_N/2$.

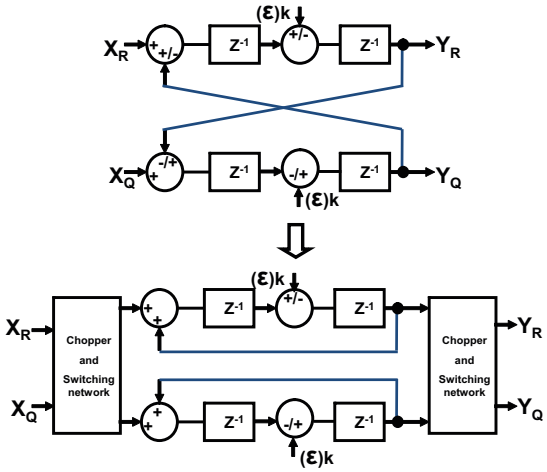

Fig. 9. Conversion step for reconfigurable architecture

affecting the addition of quantization errors.

The method described above for obtaining two complex zeros in the *NTF* can be extended to other second order schemes. If the location of receiver IF is around $f_N/4$ then the possible NTF would be

$$NTF2 = 1 - z^{-1}k(1+j) + jz^{-2}. \quad (4)$$

A similar technique can be used to generate $k(1+j)$ coefficient. The implemented architecture for above NTF is as shown in figure 4. If the location of receiver IF is around $f_N/2$ then the possible NTF would be

$$NTF3 = 1 + z^{-1}k(j) - z^{-2}. \quad (5)$$

Above NTF can implemented with self feedback and middle term coefficient $(-j)k$ can be generated by cross coupling of the quantization noise with appropriate gain. The implemented architecture for above NTF is as shown in figure 5. If the location of receiver IF is around $zero$ or f_N then the possible NTF would be

$$NTF4 = 1 - z^{-1}k + z^{-2}. \quad (6)$$

Above NTF can implemented with self feedback and middle term coefficient k can be generated by self coupling of the quantization noise with appropriate gain. The implemented architecture, which can used in image reduction technique for receiver application is as shown in figure 6.

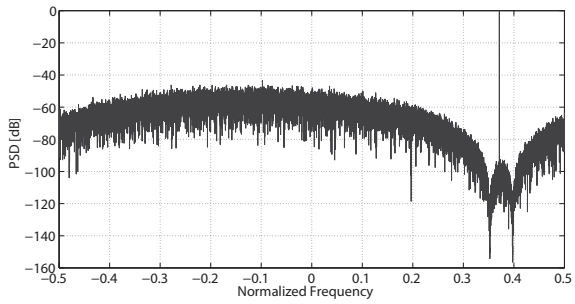

Fig. 8. PSD of the $3f_N/4$-IF second order quadrature band-pass modulator for k=1.36 using the architecture shown in figure.3.

The above study lead to four different biquad schemes with pair of zeros at symmetrical positions with respect to points on the unity circle with phase $n\pi/4$, $(n = 1, 8)$ as shown in figure 7. The value and sign of coefficient k determines the phase distance of zeros from the symmetry point. All the schemes have the same basic configuration. What differ is the connections of the inner and outer feedback and the value of multiplier k. Therefore, a generic second order cell should be capable to realize any of the four scheme shown in figures 3, 4, 5 and 6. The control of the interconnections just needs two bit. Two binary weighted arrays of capacitors control the value of k and interconnections determine the sign.

Extensive behavioral simulations of the proposed $\Sigma\Delta$ modulators are carried out with MATLAB/Simulink using a specifically developed toolbox which models the non-idealities of the basic building blocks [9], allowing us to plot the Power Spectral Density [PSD]. As an example figure 8 shows the PSD of the architecture with IF located at $3f_N/4$. It possible to satisfy a wide range of IF requirement ($n\pi/4$, $(n = 1, 8)$ IF) for receiver applications with other combinational architecture.

III. Reconfigurable Architecture

In the previous section we introduced four possible delay based quadrature $\Sigma\Delta$ modulators whose NTF coefficient ends with $1, j, -1$ or $-j$. It is worth note that the coefficients used in the previous design vary from 1 to 2 and these dynamic coefficients are reasonable to implement in switched capacitor architectures. Desirable solution for a reconfigurable architecture is to achieve all the results using a single architecture. It is observed in the literature [5] integrator solution that provides better results than delay based architecture for a quadrature modulator. The basic idea is to retain same integrators and flash ADC for all possible architectures thus providing greater flexibility and programmability.

Consider upper part of figure 9, which forms the inner part of the quadrature modulator shown in figures 3 and 4. Now if we use choppers and multiplexers at input and output of the block as shown in bottom part of figure 9, such that output response should be same then two architectures are equivalent. The power consumption of the digital part is negligible compared to the flexibility. Architecture shown in figures 5 and 6 are already in the form of integrators except the sign, which are handled easily by digital section. Similar scheme is implemented (not shown) for injection of quantization error with appropriate scaling. By reversing the capacitor signs of the coefficient can be changed. The complete architecture of the integrator based reconfigurable architecture is as shown in figure 10, which requires additional few more switches.

For many applications the noise shaping granted by a second order complex modulator cannot be enough. For such needs it is necessary to implement more zeros, one of them possibly located on the image position in order to reduce mismatch affect. The request is satisfied by the cascade of second order cells. Generic reconfigurable second order scheme of figure 10 is used to obtain wider bandwidth and higher stability [10]. The constrains on the addition of the two zero phases can be a partial design limit. However, the large number of design choices is such that the majority of requests can be properly satisfied.

Consider a four zero NTF made by cascading two second order reconfigurable cells. Zeros can be distributed similar to the schemes used in (c) of figure 7 for each of the two cells. Indeed this will result in wider bandwith but in case of mismatch, quantization error in the image band will be injected into the signal band, thus creating a degraded perfromance. The possible solution would be to place one of zeros in the image band to suppress the noise leakage. Alternatively using scheme shown in (d) of figure 7 for one the cell, it is possible to achieve spectrum as shown in figure 11. This example confirm the flexibility part of reconfigurable architectures. The inside figure shows the location of four zeros, three are around $\pi/4$ and the fourth is at the image position.

IV. Conclusion

In this work, it has been shown that synthesis of second order quadrature band-pass $\Sigma\Delta$ modulators can be performed at IF frequencies dc, $f_N/4$, $f_N/2$, $3f_N/4$ and f_N where IF frequencies locks with sampling frequency. It has been also

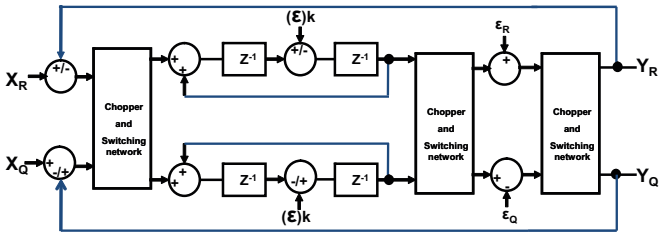

Fig. 10. Reconfigurable 2nd order quadrature modulator

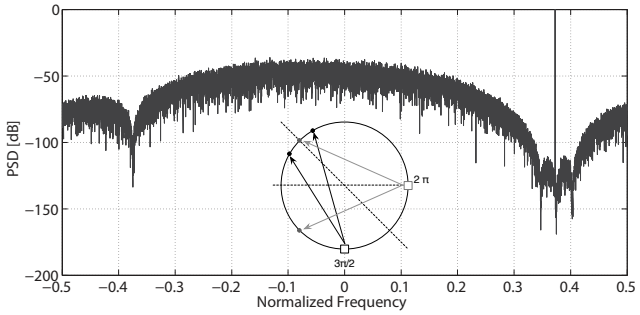

Fig. 11. Spectrum and zero distribution of the reconfigurable 2-2 MASH architecture with provision for mismatch reduction.

shown that desired *NTF* can generated by injecting suitable quantization errors. A single reconfigurable quadrature $\Sigma\Delta$ architecture which performs at all the above mentioned center frequency presented. Higher bandwidth requirements are satisfied by cascading lower order architecture with possible image reduction method.

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