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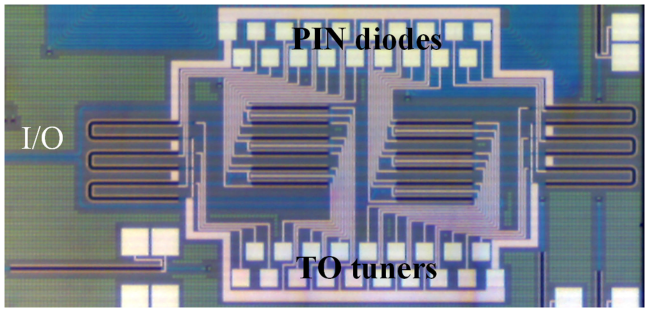

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Reconfigurable Silicon Photonic Processor Based on SCOW Resonant Structures

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Abstract: Reconfigurable photonic processors, which can be programmed to perform multiple photonic processing tasks by using the same hardware platform, own the advantages of higher flexibility and more cost-effectiveness compared with application-specific photonic integration circuits (ASPICs). In this paper, we present a novel programmable photonic processor based on two-dimensional meshes of self-coupled optical waveguide (SCOW) resonant structures. The proposed processor can be configured for realizing various basic optical components, as well as cascaded and coupled components. As a proof-of-principle, we experimentally demonstrate the concept with a 3×1 SCOW-based processor on the silicon platform, including tunable couplers, variable optical attenuators, and phase shifters. We implement eight different configurations using the chip, including ring resonators, Mach-Zehnder interferometers, Fabry-Perot resonators, and composite structures built of these basic components. These results demonstrate that the proposed processor can be a promising candidate for multi-functional photonic processors.

Index Terms: Silicon nanophotonics, waveguide devices, tunable filters.

1. Introduction

Photonic integrated circuits (PICs) have attracted increasing interest as photonic processing functions and systems tend to be more sophisticated. A wide variety of emerging applications, such as high-throughput communication systems [1]–[3], microwave photonics [4]–[6], optical computing [7], quantum optics [8], [9], and optical ranging [10], [11], require considerably more complex optical circuits with a number of interconnected optical components. Photonic integration provides the potential for extensive reduction of size, weight, and power (SWaP). In particular, silicon photonics has drawn significant attention from both academia and industry, due to the advantages of complementary-metal-oxide-semiconductor (CMOS) compatible processing, high refractive index contrast, and relatively low active tuning power [2], [7], [8]–[10]. Lots of silicon-based optical components and PICs have been demonstrated with high performance and large integration density. However, researchers have mainly focused on the design and optimization of the so-called

application-specific photonic integrated circuits (ASPICs), where a particular chip implementation is targeted at a single or a few specific functions. This approach usually requires high-cost and long-term hardware development. It is not an effective solution when the market of a specific application is relatively small but the required functions for different applications are rather versatile, such as in microwave photonics, biophotonics, and quantum optics. Alternatively, general photonic processors, inspired by the concept of Field Programmable Gate Arrays (FPGAs) in the electrical domain, can be reconfigured to perform multiple tasks by using the same hardware configuration [12]–[14]. Recently, with the rapid development of photonic integration technologies, researchers are paying more attention to the universal photonic processors due to the merits of structural flexibility and cost-effectiveness compared with ASPICs.

Generally, programmable photonic processors can be formed by many identical two-dimensional elements arranged in particular mesh networks. By configuring the states of tunable waveguide couplers and phase shifters in the elements, the light routing path is changed to a specific configuration, generating certain functions, such as optical filtering and unitary transforming. Several good programmable photonic processors have been proposed and demonstrated with square [15], hexagonal [16], or triangular [17] mesh networks. These processors show versatile functionalities in microwave photonics [18]–[20] and unitary transformation [21], [22]. The method and algorithm for setting up mesh networks composed of non-ideal components have also been proposed by D. Miller [23]–[25].

In this paper, we present a novel architecture for multi-functional photonic processors with self-coupled optical waveguide (SCOW) resonant structures as the basic elements. This architecture has the advantages of high scalability and versatile configurations, which can be programmed to perform plenty of functions like delay lines, ring resonators, Fabry-Perot (FP) resonators, and so on. Especially, as light propagates both in the forward and the backward directions in the SCOW structures, the processors are more convenient in building optical components with standing-wave features, like FP resonators. In the demonstration, we also insert silicon PIN diode based variable optical attenuators (VOAs) in the processors, which is advantageous to further extend the functionalities.

2. Device Structure and Principle

Fig. 1(a) shows the schematic of a silicon SCOW resonator, which is formed by a single meandering waveguide self-coupled to form directional couplers (DCs) at the input and output ports [26], [27]. Both clockwise (CW) and counter-clockwise (CCW) resonance modes are excited in the SCOW resonator. Therefore, a single-stage SCOW resonator can have versatile spectral responses from both transmission and reflection sides, depending on the coupling coefficients of these two DCs.

Moreover, we can easily extend the SCOW structures in a two-dimensional array. Fig. 1(b) shows an example of a two-dimensional mesh composed of N $\times$ M directly-connected SCOW structures. We name the SCOW in the n^{th} row and the m^{th} column as S_{nm}. In the vertical direction, the output waveguide of the upper SCOW is also the input waveguide of the subsequent SCOW, which makes the two contiguous SCOWs to share two DCs. In the lateral direction, the two adjacent SCOWs are placed closely to form an additional DC. Such N $\times$ M SCOWs have diverse spectral responses.

As the SCOW resonator is formed by a passive waveguide, its spectrum is fixed once it is fabricated. To realize a reconfigurable SCOW resonator, we replace the passive couplers with tunable couplers (TCs) based on 2 $\times$ 2 Mach-Zehnder interferometers (MZIs) [28], [29]. As shown in Fig. 1(c), when the phases of the two MZI arms are $\theta + \phi$ and $-\theta + \phi$ ($0 < \theta < \pi/2$), respectively, the MZI is implemented as an arbitrary coupler with the coupling coefficient determined by θ. When the two MZI arms have a common phase ϕ ($\theta = 0$), light from the input port is fully transmitted to the cross port with a field transmission of $i\exp(i\phi)$, which is referred to as cross-state. In the case where the phase difference of two arms is equal to π ($\theta = \pi/2$), the MZI is changed to the bar-state with a field transmission of $i\exp(i\phi)$. For these two specific states, the MZI is implemented as two parallel or crossed waveguides with their phases tuned by ϕ. Due to its high flexibility, the MZI-based TCs enrich the configurations of the SCOW structure.

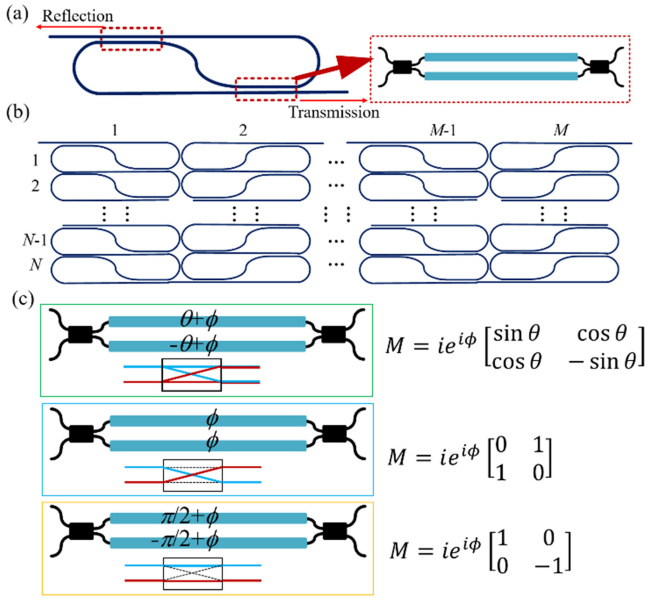

Fig. 1. (a) Schematic of a SCOW resonator as the basic unit. The inset shows an MZI based tunable coupler. (b) An array of N × M SCOW resonators placed in a two-dimensional mesh. (c) Three typical states of the MZI coupler with different phases applied to the two arms.

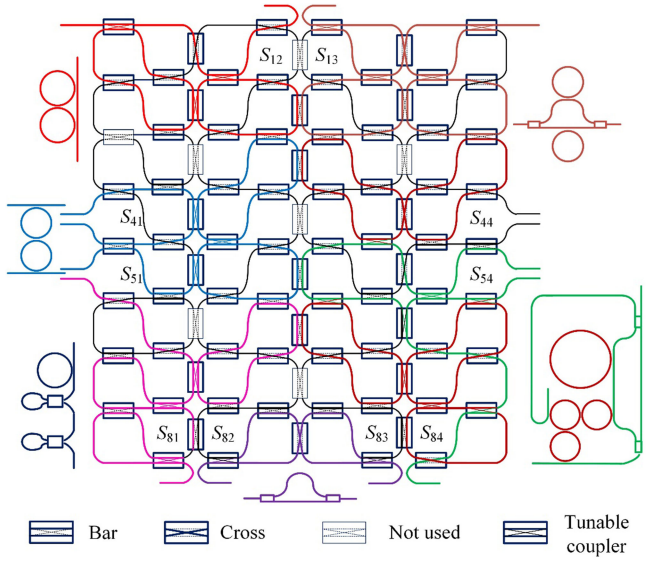

Fig. 2. Schematic of an 8 × 4 programmable photonic processor based on SCOW elements. The processor is configured to various optical components simultaneously, like ring resonators, MZIs, FP cavities and the combinations of these basic components.

With the reconfigurable SCOWs as the basic elements, we can build N × M photonic processors. Fig. 2 shows the schematic of an 8 × 4 reconfigurable photonic processor. All the SCOWs are arranged in the same way as in Fig. 1(b), except that all DCs are replaced by MZI-based TCs. Such multi-functional photonic processors can be easily extended to a larger scale, which is very important to perform multiple complex optical processing tasks. For an N × M photonic processor, there are totally 3*MN*-*N* TCs. We can break some of the connecting waveguides at the edges of

TABLE 1
Cavity Length or Arm Length Difference of Varies Photonic Processor Architectures, n ∈ N {0, 1, 2, . . . } for FP Cavities and Asymmetric MZIs, n ∈ N {1, 2, 3, . . . } for Ring Resonators, Where n Represents the Number of TCs

	Square	Triangular	Hexagonal	SCOW
Ring resonators	4 *n*	3 *n*	{6,10+2n}	6 *n*
FP cavities	/	/	14+*n*	6+3 *n*
Asymmetric MZIs	4 *n*	3 *n*	2 *n*	6 *n*

the processor to form multiple input and output ports, depending on the applications. As shown in Fig. 2, the connection waveguides in S_{41}, S_{51}, S_{44}, and S_{54}, and between S_{12} and S_{13}, S_{81} and S_{82}, and S_{83} and S_{84} are broken to offer extra input and output ports.

By setting the TCs to different states, the light propagation path is reconfigured accordingly, resulting in various basic building blocks for optical circuits. With these basic optical components, we can realize various complex functions. Fig. 2 illustrates some exemplary components built from the processor, including parallel and serially cascaded ring resonators, an FP resonator connected with a ring resonator, an asymmetric MZI, a dual-ring coupled MZI, or even a more complex device shown in the right-bottom corner of Fig. 2. These structures can be used as finite impulse response (FIR) and infinite impulse response (IIR) filters, which are the key devices in both optical and microwave signal processing [15], [20]. To further increase the reconfiguration of the photonic processor and also improve the device performance, we can also integrate amplifiers and variable optical attenuators (VOAs) in the processor [14], [30].

The spectral tuning resolution step qualifies the discretization limits of the architecture when configured to various optical components, like ring resonators, FP resonators, and asymmetric MZI. It is defined as the minimum step in TCs by which the cavity lengths or the arm length differences can be increased/decreased [17]. Here, we compare our SCOW architecture with other mesh networks as shown in Table 1. We can see that the resolution steps of the SCOW processors are both 6 for ring resonators and asymmetric MZIs, which are higher than the other state-of-the-art architectures. Sagnac-loop reflectors are the key elements in building FP resonators. However, square and triangular mesh networks cannot construct Sagnac-loop reflectors. In Hexagonal meshes, each reflector requires 7 TCs, and the cavities length is $14 + n$ with a resolution step of 1. The SCOW processors are more convenient to implement single-stage or cascaded FP resonators, as they only need a minimum of 4 TCs to build a Sagnac-loop reflector. The resolution step is 3 for SCOW processors.

3. Implementation and Results

3.1 Device Implementation

To experimentally verify the concept of the proposed multifunctional photonic processor, we realize a 3×1 SCOW photonic processor on the SOI platform. Fig. 3(a) shows the schematic of the designed programmable processor. It consists of three stages of SCOW structures, where each two contiguous SCOW resonators share two MZIs. For the three-stage processor, there are totally six TCs, which are named as TCi ($i = 1, 2 \ldots, 6$). To further expand the configurations, we also insert a phase shifter (PS) and a variable optical attenuator (VOA) between two adjacent TCs. By reconfiguring the light routing paths through TCs, PSs, and VOAs, the structure can be programmed to offer various optical functions, allowing for versatile applications.

The chip was fabricated on a 200 mm SOI wafer with a 220 nm top silicon layer and a 2 μm buried oxide layer. The waveguide is based on a silicon rib waveguide with a waveguide width of 500 nm, and a slab layer thickness of 90 nm. The chip was designed for transverse-electric (TE) polarization. The PSs are based on the silicon thermo-optic (TO) effect with integrated TiN micro-heaters, while

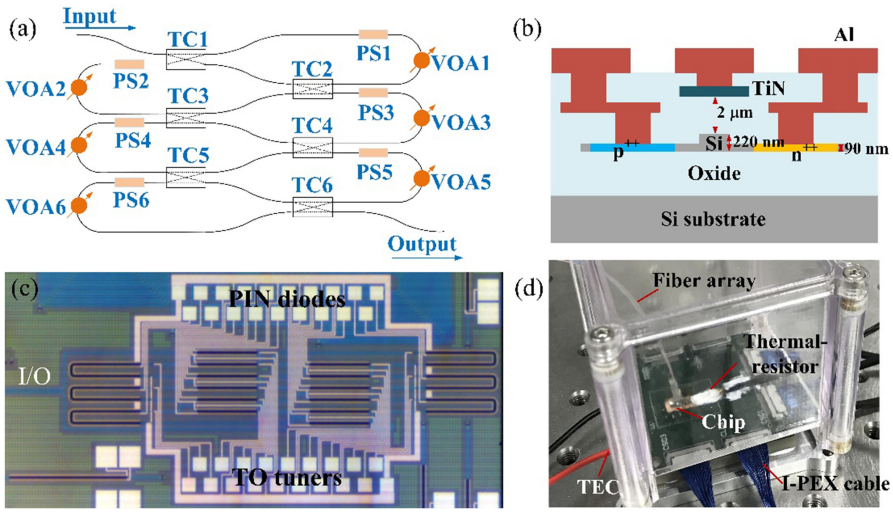

Fig. 3. (a) Schematic of the 3 × 1 SCOW-based photonic processor. (b) Cross-sectional view of the active waveguide. (c) Microscope image of the fabricated.

the VOAs are based on the free carrier absorption (FCA) effect after turning on PIN diodes. The PS and VOA are integrated into the same waveguide, which we refer to as active waveguide, as illustrated in Fig. 3(b). The length of the PS/VOA is ∼1 mm. The MZI-based TCs are made of two 2 × 2 multimode interferometers (MMIs) and two 400 μm-long active waveguides. To be mentioned, only TO-based PS in the TCs are tuned in the demonstration. The length and the width of the MMI are 30.5 μm and 5 μm, respectively. In order to reduce the propagation loss of the device, the width of the waveguide is expanded to 2 μm in the long straight waveguide through a linear taper.

The fabrication was done using a CMOS compatible process. Fig. 3(c) shows the microscope image of the fabricated chip. The footprint of the chip is 1.5 × 3.8 mm^2, including all electrode pads and input/output grating couplers. We packaged the fabricated chip before the characterization of the device performance. The chip was attached to a copper sub-mount as a heat sink. A printed circuit board (PCB) was used to connect with on-chip electrical pads. A 4-channel fiber array was coupled with the on-chip non-uniform grating couplers and firmly attached to chip using refractive index-matched UV-curable adhesive. The coupling loss is ∼5 dB/facet after package. To stabilize the temperature during the experiments, a thermistor was put aside the chip for temperature monitoring, and a thermo-electric cooler (TEC) was placed underneath the copper sub-mount to cool/heat the chip. The packaged chip was put in a plastic box with an aluminum substrate and a transparent lid as illustrated in Fig. 3(d).

3.2 Basic Elements Characterization

We first present the measurements of the basic elements. As illustrated in Fig. 4(a), we designed a test device with six cascaded 2 × 2 MMI couplers to characterize the insertion loss of the 3-dB coupler. Fig. 4(b) shows the measured transmission spectra of the device from both input ports. The insertion loss can be extracted from the linear fitting of the optical transmission as a function of the number of MMI couplers. The extracted slope from 1530 nm to 1590 nm is shown in Fig. 4(c). Therefore, the insertion loss of the MMI coupler is lower than 0.4 dB at the wavelength range of 1540 nm to 1580 nm. We also tested the PIN diode with a length of 1 mm as shown in Figs. 4(d)–(f), which is used as a VOA. The current increases rapidly when the applied voltage is larger than the threshold voltage of 0.7 V. Meanwhile, the optical transmission decreases with the injected free carriers. The attenuation of the VOA reaches ∼45 dB at the voltage of 2.0 V, which is large enough to eliminate leaked light in the processor. Loss variation from 1530 nm to 1590 nm is less than

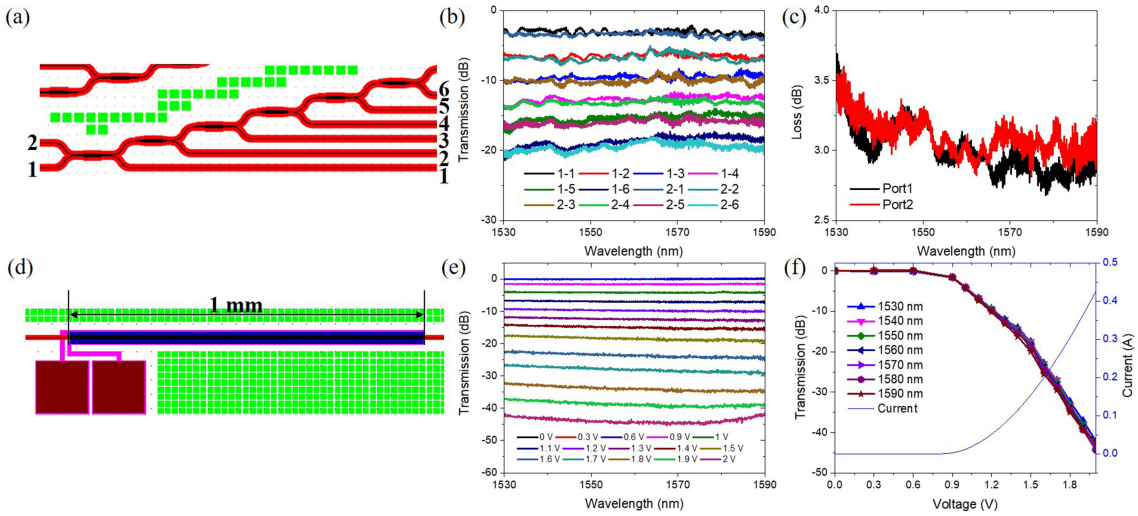

Fig. 4. (a) Mask layout of cascaded 2 × 2 MMI couplers. (b) Measured spectra of the cascaded MMI couplers. (c) Extracted splitting loss as a function of wavelength. (d) Mask layout of a PIN diode with a length of 1 mm. (e) Measured spectra of the PIN diode with various applied voltages. (f) Extracted transmission at several fixed wavelengths and measured current as a function of applied voltages.

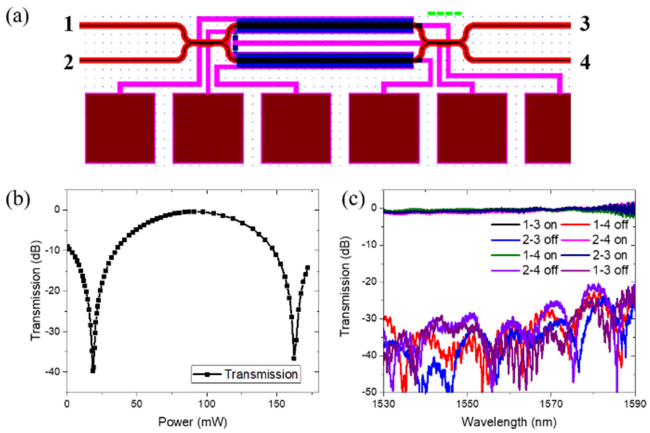

Fig. 5. (a) Mask layout of a 2 × 2 MZI. (b) Measured transmission at the 1550 nm wavelength as a function of the applied power to the upper phase shifter. (c) Measured transmission spectra of the MZI at the bar and the cross states.

3 dB. To be mentioned, as the absorption loss is proportional to the injected current, the power consumption is quite high for large attenuation. It also generates a large amount of heat, limiting the scalability of the processor.

A single MZI with the same design parameters was placed in the same chip for performance testing, with the mask layout shown in Fig. 5(a). Although both TiN micro-heaters and PIN diodes were integrated into the two MZI arms, we only turned on the TiN micro-heaters, which were exactly the same as those in the fabricated SCOW processor. The resistance of the 400-μm-long thermo-optic (TO) phase shifter is $\sim$2.44 KΩ. Fig. 5(b) shows the measured transmission of path 1–4 at the wavelength of 1550 nm with various applied powers to the upper phase shifter. We can see that the extinction ratio is larger than 40 dB. The power consumption is $\sim$72 mW/π, which is more than twice our previous results [2]. That is because we use a two-metal-layer design in this work, some of the generated heat is transferred to the metal electrical lines of the PIN diodes near the

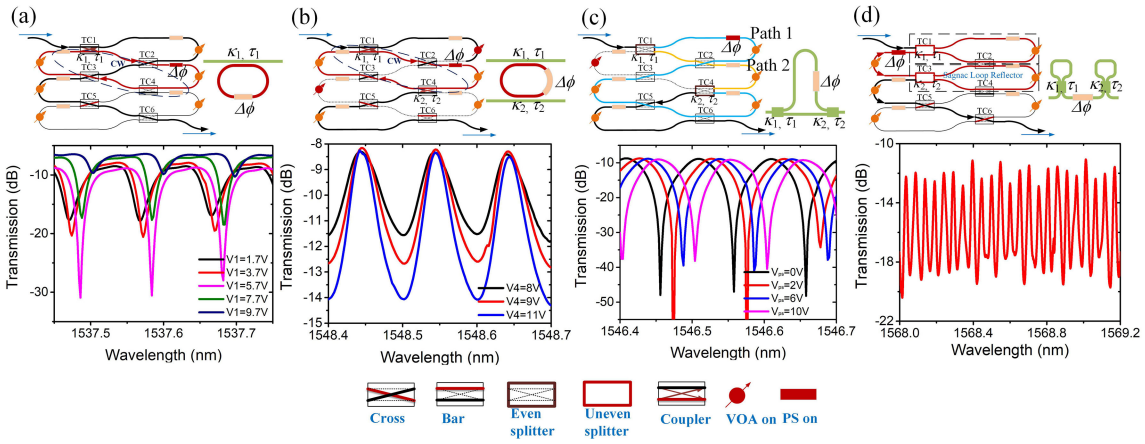

Fig. 6. Configurations and experimental results of the processor as: (a) an all-pass ring resonator, (b) an add-drop ring resonator, (c) an asymmetric MZI, and (d) a single FP cavity.

heaters. Fig. 5(c) shows the measured transmission spectra of MZI at the bar and the cross states, respectively. The extinction ratio is ∼30 dB from 1550 nm to 1570 nm, which implies the 2 × 2 MMI couplers have a near 3-dB power splitting ratio. It is higher than 20 dB in the measured wavelength range. Such a high extinction ratio is beneficial for the processor, as VOAs are not necessarily turned on to suppress the leaked light from the undesired path.

3.3 Chip Implementation and Results

We calibrated the initial states of all TCs before implementing the chip to a specific function. The chip is a one-input and one-output device and there is no internal test port. Therefore, it is necessary to find the exact bar or cross state of all TCs with the assistance of VOAs. With certain VOAs turned on, it is possible to get one light path going from input to output without any feedback coupling. In this way, we can reach the bar or cross state of each TC by monitoring the output optical power. In our calibration, we first turn on VOA1, VOA2, VOA4, and VOA5. Therefore, there is only one light path between the input and output ports without any feedback, where it passes TC1, TC2, TC4, TC5, and TC6. We then adjust the states of the four TCs and record the applied voltages one by one by tuning the output power to the maximum or the minimum. The last one coupler, TC3, can also be tuned to the bar and cross states by the same procedure but with VOA2, VOA3, VOA5, and VOA6 turned on. After the calibration, we turned off all VOAs and measured the transmission spectrum. It presents almost an identical spectrum with no significant ripples compared with the one when the VOAs are on, which means that the TCs have a relatively high extinction ratio (larger than 30 dB). It is advantageous for low power operation because VOAs are not necessary to suppress the leaked light from the TCs when at the bar or cross states.

A ring resonator is one of the most popular and fundamental optical components for optical filtering, time delay, and phase shift, etc. In Fig. 6(a), the chip is configured to an all-pass ring resonator, where the ring is formed by an internal single CW loop as illustrated by the gray dashed line. All TCs from TC1 to TC 6 are in the coupling, cross, cross, bar, cross, cross states, respectively. By changing the applied voltage on TC1, the coupling coefficient of the ring is tuned. Thus, the ring is tuned from under-coupling to over-coupling, as shown by the measured results in Fig. 6(a). The free-spectral-range (FSR) of the ring resonance is ∼12.5 GHz and the 3-dB optical bandwidth of the near critically-coupled ring resonance is ∼3.5 GHz. We find that the resonance line-shapes are slightly asymmetrical, which are caused by the undesired-coupling of TC3. Then, VOA1 and VOA4 are turned on to attenuate light from the through port, and TC4 is reconfigured to a coupler. Thus, the chip is implemented to an add-drop ring resonator, as shown in Fig. 6(b). The spectra show the

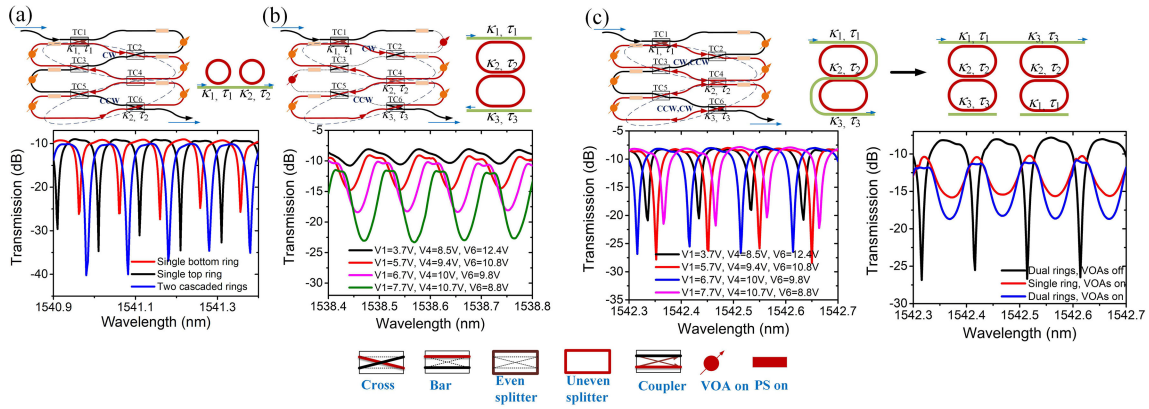

Fig. 7. Configurations and experimental results of the processor as: (a) two cascaded all-pass ring resonators, (b) two directly-coupled ring resonators, (c) a fourth-order ring resonator filter, and (d) a single ring-coupled MZI.

measured drop passband changing with the voltage on one arm of TC4 while keeping TC1 fixed. The on-off ratio increases with the voltage V4 and the central wavelength is also slightly red-shifted.

Other than ring resonators, the chip can also be implemented to an asymmetric MZI, which is basically recognized as an FIR filter. Fig. 6(c) shows the implementation of the processor where TC1 and TC4 are configured to even splitters. TC2, TC3, TC5, and TC6 are configured as cross, cross, cross, and bar, respectively. The two interfering paths in the MZI are illustrated by the blue and orange lines. VOA2 is turned on to attenuate light coupled back to TC1. The measured spectra also have an FSR of 12.5 GHz. The filter has a high extinction ratio of more than 30 dB, and the central wavelength is red-shifted by ~6.2 GHz upon thermal tuning of PS1. The SCOW-based processor is also reconfigured to a single FP cavity. Two Sagnac loop reflectors are formed by configuring TC1 and TC3 as uneven splitters, as illustrated by the gray dashed rectangles in Fig. 6(d). The measured transmission shows a comb filtering spectrum with an FSR of ~6.2 GHz.

Besides the above four basic configurations, the fabricated chip also allows for more complex configurations, consisting of more than one basic structure. Fig. 7(a) shows the implementation of two cascaded all-pass ring resonators. In that case, TC1 and TC6 are configured as couplers, and TC4 is configured to the bar-state. Thus, a second CCW resonance loop is established and coupled with the bus waveguide. The red and black traces in the bottom panel of Fig. 7(a) are the measured transmission spectra when only one ring is turned on, while the blue trace shows the transmission spectrum of the second-order all-pass filter. The 3-dB optical bandwidth is expanded from 3.15 to 4.45 GHz. Subsequently, by configuring TC4 to a coupler and turning on VOA1 and VOA4, the processor becomes two directly-coupled ring resonators, as shown in Fig. 7(b). The output transmission spectrum of the coupled ring can be tuned by the coupling coefficients of TC1, TC4, and TC6. Here, we gradually change the applied voltages on these three TCs to tune the filter passband shape. The spectra show a flat-top response with varied bandwidth. However, the insertion loss and the extinction ratio also change with the passband width.

Besides these ordinary cascaded or coupled ring resonators, the chip can also be configured to unconventional ring-based structures, as shown in Fig. 7(c) as an example. Compared with the previous configuration, we turn off VOA1 and VOA4. Therefore, the bus waveguide couples with both of the rings, and excites both CW and CCW modes in these two rings. Meanwhile, the two rings are also coupled with each other. Such a kind of structure is difficult to implement in planar optical waveguide circuits, as it induces several waveguide crossings. Actually, the structure can be recognized as two cascaded CROWs, or a fourth-order ring resonator filter as shown in the upper-right of Fig. 7(c). As these two CROWs share two rings, the resonances are self-aligned, which are more convenient in practical usage. The bottom-left of Fig. 7(c) shows the measured spectrum with

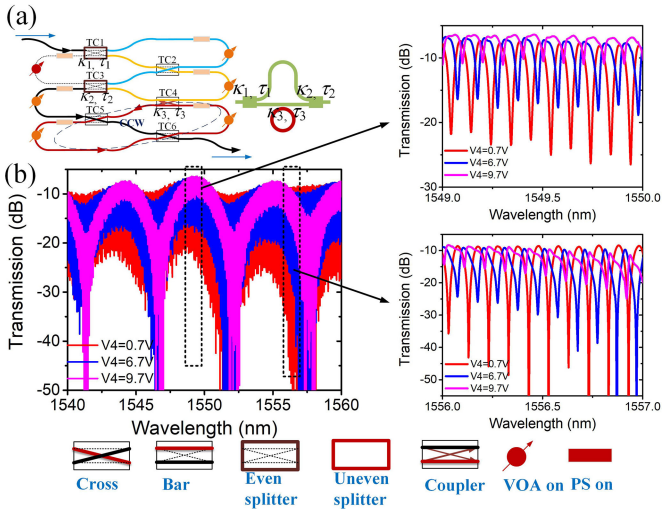

Fig. 8. (a) Configurations and (b) experimental results of the processor as a single ring-coupled MZI.

various voltages on TC1, TC4, and TC6. The 3-dB optical bandwidth is tuned from 3.21 GHz to 2.93 GHz, which is smaller than the second-order ring resonators in Fig. 7(a). The extinction ratio changes from 20 dB to 15 dB, which can be further optimized. We also plot the measured spectra of three different configurations in the bottom-right of Fig. 7(c). The applied voltages to the couplers are the same. These results also prove that integrating VOAs in the SCOW processor can enrich the functionality of the chip.

We also realize a single ring-coupled MZI with the proposed processor, as illustrated in Fig. 8. Here, TC1 and TC3 are configured to uneven splitters, and VOA2 is turned on to attenuate feedback light from TC3. A CCW ring (red-solid line) is coupled to one arm of the MZI (yellow-solid line) with TC4. The left-corner of Fig. 8 shows the measured transmission spectra in the 20 nm wavelength range with various voltages applied on TC4. They exhibit a large periodic envelope with an FSR of $\sim$5 nm, which is decided by length difference between the MZI arms. The magnified spectra in a 1-nm wavelength range present the details. They show a smaller FSR of 12.5 GHz, which equals that of the ring resonator. We can also observe that the output spectra exhibit an asymmetrical Fano-resonance line-shape varying with the coupling coefficients. Such a Fano-resonance has potential applications in optical switching and ultra-wideband signal generation.

It should be noted that we only present a small portion of all possible configurations. For all the implementations, both the spectral shape and the central wavelength can be tuned with these active basic elements. By cascading more stages of SCOW resonators in both lateral and vertical directions, we can obtain a larger quantity of configurations with more complicated functions. Thus, the SCOW-based processor can be used as a powerful chip to satisfy versatile photonic signal processing tasks.

4. Discussion

The proposed multi-functional M $\times$ N SCOW processors can be potentially used in microwave photonic signal processing, like true-time delay and filtering. However, the functionality of the programmable processor is directly proportional to the scalability of the cascaded SCOWs. The main limitations of SCOW-based processors are insertion loss and power consumption of the elements. The insertion loss comes from the 2 $\times$ 2 3-dB couplers, the active waveguides, and the connecting waveguides. Typically, the transmission loss of silicon-based waveguides is around 1$\sim$3 dB/cm, which is mainly contributed by the scattering loss of the rough waveguide sidewalls. It can be improved to less than 0.5 dB/cm using advanced fabrication processes or waveguide dimension

optimization [31], [32]. Active waveguides can have almost the same loss as the passive waveguides as long as the heavily-doped regions of the PIN diodes are separated far enough from the waveguide edges. In our implementation, MMIs are used as 2×2 couplers and the insertion loss is $\sim$0.4 dB. That is the largest loss contribution for the SCOW element. Thus, rings or other resonators constructed by the SCOW elements have a relatively low Q-factor. Besides, it is very challenging to lower the insertion loss below 0.2 dB even for a DC-based TC [19]. In a SCOW element, we can have a maximum of 6 TCs and light can propagate through the TCs 8 times. Therefore, ten SCOW elements will suffer 16 dB transmission loss from TCs. One potential solution is to use on-chip optical amplifiers to compensate for the loss [14]. Recently, both heterogeneous and monolithic integrations of III-V and Si materials are rapidly developing with improved performances.

The second limitation is power consumption. Silicon TO effect is frequently used for active phase tuning due to the high TO coefficient of 1.86 $\times$ 10-4/K and no extra loss induced during tuning. In our device, the thermal tuning power efficiency is around 72 mW/π, which is more than twice of our previous results, due to the heat leakage from the double metal layers [2]. For a 10×10 SCOW processor, there are 290 TCs in total, and the power consumption is almost 20.9 W. If VOAs and optical amplifiers are also integrated into the processor, the consumed power will be much higher. The high power also causes a thermal crosstalk issue in such a small chip area, which limits the scalability of the photonic processor. The TO tuning power can be drastically reduced to 1.2 mW/π by undercutting the silicon substrate but at the sacrifice of the tuning speed [33]. Silicon hybrid integration with phase change materials (e.g., $Ge_2Sb_2Te_5$) also offers a promising solution, due to the large non-volatile change of the refractive index upon phase transition [34]. The self-holding nature of the materials can greatly reduce the power consumption of the processor as no power is required to hold the TC states. The VOAs in our chip also consume considerable power as we use the free-carrier injection method to attenuate light. One way to reduce the power is to replace the VOAs with III-V based SOAs. The power consumption for optical attenuation with the reverse-biased SOA is sub mW [11]. Besides, the SOAs can also work in the forward bias regime for optical amplification

Besides these two main limitations, chip size, temperature sensitivity, and crosstalk of the TCs also limit the scalability of the reconfigurable processor. To extend the scale, we need to reduce the size of the SCOW structure and also fabricate it with a larger wafer size. The SOI platform has the advantages of a small waveguide bending radius of several microns due to the high index contrast of $\sim$2. The size of SOI wafers is much larger than that of III-V wafers. Therefore, silicon photonics is a very promising technology for the multi-functional processor. Temperature sensitivity is one major disadvantage of silicon-based photonic devices. We could integrate on-chip temperature sensors or on-chip power monitors in the chip to actively control and stabilize the processor working state, at the expense of system complexity. The crosstalk of the TCs is also important to the scalability of the processor, as the accumulated noise from the leaked nodes greatly degrades the system performance. In the paper, the TCs have crosstalk of -30 dB, which still slightly influences the output spectral shape as shown in Fig. 6(a). Thus, for a larger-scale processor, the crosstalk of the TCs should be better with -40 dB. In some cases, VOAs can be used to attenuate leaked noise and improve the performance of the processors.

For all the photonic processing tasks, a suitable optical source is indispensable. Various functions usually require different kinds of optical sources, like continuous-wave light, pulsed light, supercontinuum light, and single-photon source, etc. The operation wavelength may be different from the commonly used 1550 nm for different applications. Moreover, it is difficult to integrate light sources on the silicon chip. Therefore, we prefer to use an external optical source. We also notice the recent development in on-chip silicon light-emitting diodes (LEDs) [35], [36]. The wide spectrum of silicon LEDs could be a proper light source for applications like bio-sensing.

5. Conclusion

In conclusion, we have proposed a multi-functional photonic processor based on a SCOW-resonator structure. With the unique feature of both forward and backward transmission in the SCOW structure,

the photonic processor can be programmed to implement various basic optical components. The processor is easy to expand in both vertical and lateral directions for versatile photonic processing in applications like microwave photonics and quantum computing. Besides, the integration of extra VOAs in the processors can further extend the functionality and also improve the performance. We have experimentally demonstrated a three-stage SCOW resonator on the SOI platform to prove the reconfigurable ability of the processor. By tuning TCs, PSs, and VOAs, we realized eight different configurations using the chip, representing only a small portion of all possible configurations. These results open the way for a new class of programmable silicon photonic processors that utilize self-coupled waveguide to increase the flexibility and extend the functionality.

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